Fully Integrated PMIC Optimized for Automotive EMB Systems with Wheel Speed Sensor Interface

FEATURES AND BENEFITS

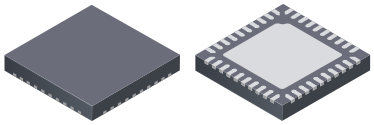
- ASIL-Compliant: ASIL D safety element out-of-context (SEooC) developed in accordance with ISO 26262, when used as specified in the safety manual
  ISO 26262 ASIL Compliant
- AEC-Q100 Grade 0 qualified
- VIN input range; 3.2 to 36 V operating, 40 V maximum
- Integrated wheel speed sensor interface compatible with 2-level, 3-level AK protocol, and 3-level high-resolution AK protocol
- Fully integrated, 2.2 MHz synchronous buck-boost pre-regulator (VREG: 5.8 V)
- Five internal linear regulators with fold back short-circuit protection:
  - VUC, 600 mA, 3.3/5 V LDO regulator for MCU
  - VLDOA, 200 mA, 5/3.3 V LDO regulator, normally used to supply the CAN transceivers
  - VLDOB, 200 mA, 5/3.3 V LDO regulator
  - VLDOC, 50 mA, 5 V 1% accuracy LDO regulator, normally used as MCU ADC reference

Continued on next page...

APPLICATIONS

- Electrical mechanical braking (EMB) module

PACKAGE



40-pin 6 mm × 6 mm QFN
(suffix EV)

Not to scale

DESCRIPTION

The A81415 is a power management IC that is optimized for electromechanical braking (EMB) applications. The A81415 integrates a buck boost pre-regulator, five LDOs, one channel wheel-speed sensor interface, and many safety features. The pre-regulator uses a fully integrated 2.2 MHz buck-boost topology to efficiently convert automotive battery voltages into a tightly regulated intermediate voltage complete with control, diagnostics, and protections.

The output of the pre-regulator supplies the five linear regulators and the wheel speed interface. The linear regulators can supply power for microprocessors, sensors, and CAN transceivers.

The wheel speed sensor interface is available to supply and measure the sensor current to provide the sensor data to the MCU through SPI and/or the digital output pin (WSIO).

Two automotive-battery-rated enable inputs are available on the A81415. An additional logic-level enable is also available for control via an MCU.

Diagnostic outputs from the A81415 include power-on reset (RESETn) and two safety outputs (POE1 and POE2). The microprocessor can read fault registers through SPI.

Dual bandgaps, one for regulation and one for fault checking, improve safety coverage and fault detection.

The A81415 also contains three types of watchdog timers: pulse width watchdog (PWWD), window watchdog (WWD), and Q&A watchdog (QAWD). The watchdog timers can be put into various operating states via secure SPI commands.

The A81415 is supplied in a low profile 40-pin QFN package with exposed power pad and wettable flanks.

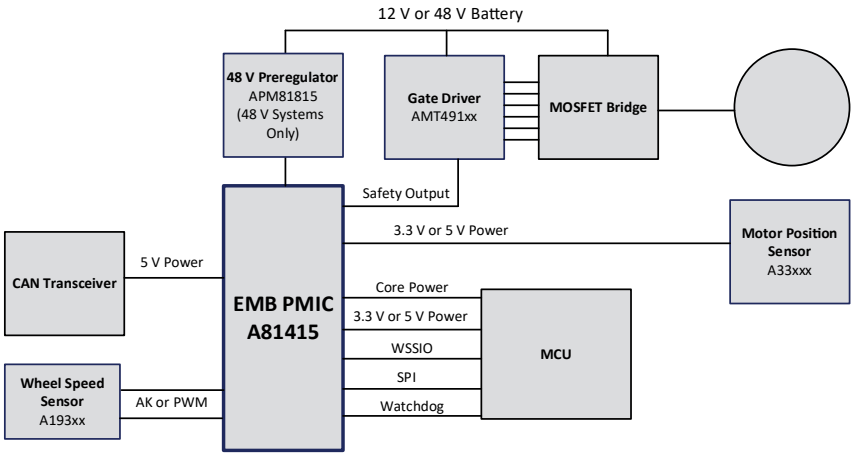


Figure 1: A81415 Simplified Application Diagram

FEATURES AND BENEFITS (continued)

- VLDOP, 50 mA, 5/3.3 V or VLDOC tracking LDO regulator with short-to battery protection for remote sensors
- Pulse-width watchdog (PWWD), window watchdog (WWD), and Q&A watchdog (QAWD)
- Voltage monitor (VCORMON) to verify MCU core voltage provided by an external DC-DC regulator
- Control and diagnostic reporting through secure SPI
- Two high-voltage enable inputs (ENBAT and ENCOM)
- Frequency dithering and controlled slew rate to mitigate EMI
- Over/undervoltage and current protections for all output rails
- Short-to-battery protections on all I/O
- Thermal warning and shutdown protection

SELECTION GUIDE [1]

Part Number	VLDOA Output Voltage (V)	VLDOB Output Voltage (V)	VCOREMON	Package and Leadframe	Packing
A81415KEVGTR-1	5	5	Enabled	6 mm × 6 mm, 40-pin QFN with thermal pad and wettable flank, 100% matte tin leadframe plating	Tape and reel, 1500 pieces per 7-inch reel
A81415KEVGTR-2	5	3.3	Enabled		
A81415KEVGTR-3	3.3	3.3	Enabled		
A81415KEVGTR-4	5	5	Disabled		

[1] Not all combination of programmable options are available preprogrammed From Allegro. For details, contact Allegro.

ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
VIN, VINP, WSIS Voltage	V_{VINx}, V_{WSIS}		−0.3 to 40	V
VREG, VUCIN Voltage	V_{VREG}, V_{VUCIN}		−0.3 to 20	V
ENBAT, ENCOM Voltage	V_{ENBAT}, V_{ENCOM}		−0.3 to 40	V
ENBAT, ENCOM Current	I_{ENBAT}, I_{ENCOM}		±75	mA
VUCSEL Voltage	V_{VUCSEL}		−0.3 to 20	V
LX1 Voltage	V_{LX1}		−0.3 to V_{VIN} + 0.3	V
		t < 250 ns	−1.5	V
LX2 Voltage	V_{LX1}		−0.3 to V_{VREG} + 0.3	V
		t < 250 ns	−1.5	V
CP1 Voltage	V_{CP1}		– 0.3 to V_{VIN} + 0.3	V
CP2 Voltage	$_{VCP2}$		V_{VREG} – 0.3 to 20	V
VCP Voltage	V_{VCP}		V_{VREG} – 0.6 to 20	V
BOOT1 Voltage	V_{BOOT1}		– 0.3 to V_{LX1} + 7	V
BOOT2 Voltage	V_{BOOT2}		– 0.3 to V_{LX2} + 7	V
VLDOP Voltage	V_{VLDOP}		−1 to 40	V
WSIH, WSIL Voltage	V_{WSIH}, V_{WSIL}		−18 to 40	V
PGND, GND Voltage	V_{PGND}, V_{GND}		−0.3 to 0.3	V
All other pins			−0.3 to 7	V
Junction Temperature Range	T_J		−40 to 175	°C
Storage Temperature Range	T_{stg}		−40 to 150	°C

[1] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ALLEGRO microsystems

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ESD CHARACTERISTICS

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ESD HBM Robustness	$V_{ESD(HBM)}$	ESD susceptibility to GND on all pins	–2	–	2	kV
ESD CDM Robustness	$V_{ESD(CDM)}$	ESD susceptibility to GND on all pins	–500	–	500	V
	$V_{ESD(CDM,CORNER)}$	ESD susceptibility to GND on corner pins	–750	–	750	V
WSS IF Powered System Level ESD	$V_{ESD(PWR,CNT)}$	WSIH, WSIL @ –18 V and 40 V; Powered device, contact discharge, 150 pF / 2 kΩ	–	–	8	kV
WSS IF Unpowered System Level ESD	$V_{ESD(UNPWR,CNT)}$	WSIH, WSIL @ –18 V and 40 V; Unpowered device, contact discharge, 150 pF / 2 kΩ	–	–	6	kV
	$V_{ESD(UNPWR,AIR)}$	WSIH, WSIL @ –18 V and 40 V; Unpowered device, air discharge, 150 pF / 2 kΩ	–	–	6	kV

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [1]	Value	Unit
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	QFN, 40-pin package, 4-layer PCB based on JEDEC standard	27	°C/W

[1] Additional thermal information are available on the Allegro website.

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PACKAGE OUTLINE DRAWING
(Preliminary)

For Reference Only – Not for Tooling Use

Dimensions in millimeters
NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown

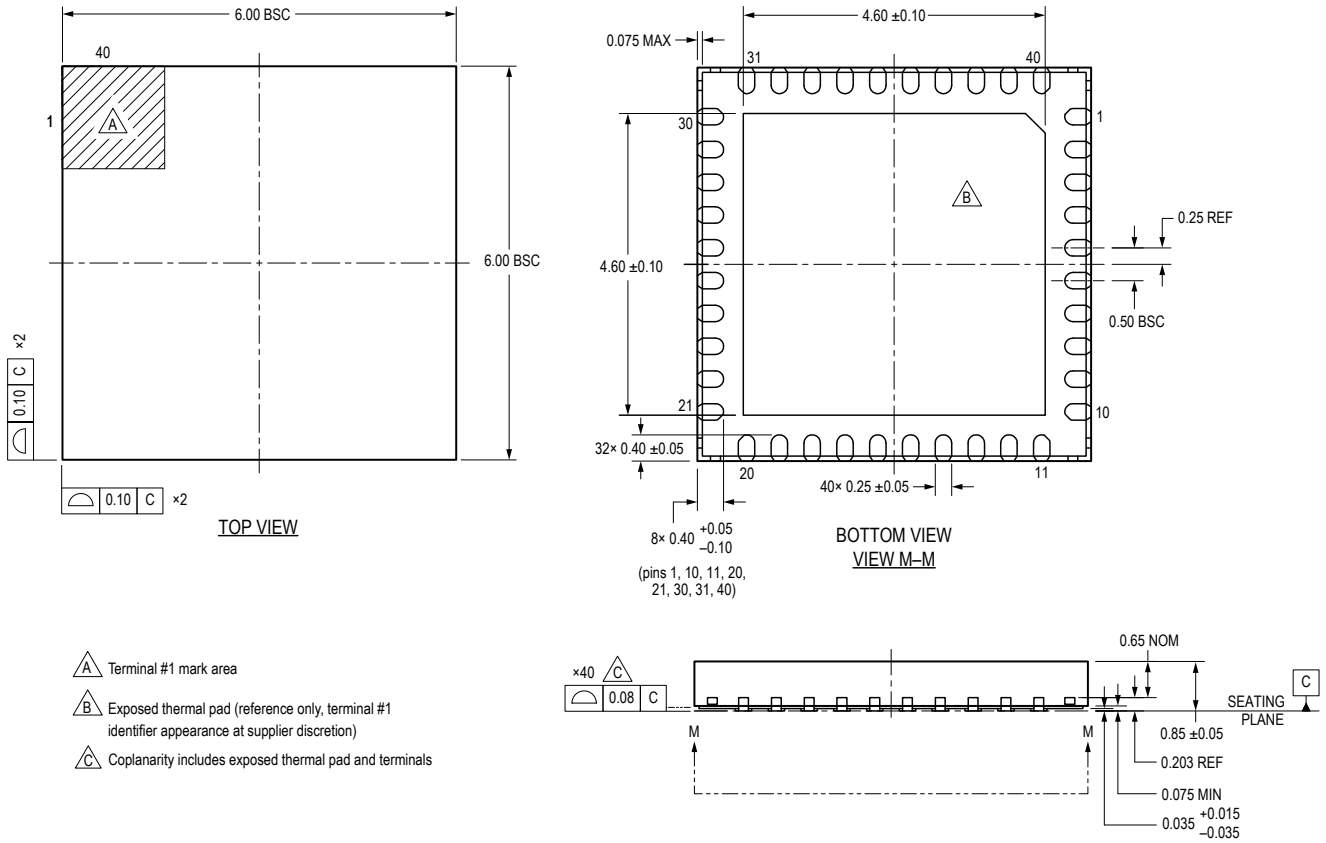

Figure 2: 6 mm × 6 mm, 40-pin QFN with exposed power pad and wettable flank (suffix EV)

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REVISION HISTORY

Number	Date	Description
–	June 25, 2026	Advance information release to web

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