Fully Integrated PMIC Optimized for Automotive EMB Systems with Wheel Speed Sensor Interface

FEATURES AND BENEFITS

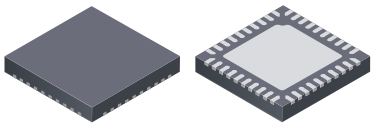
- ASIL Compliant: ASIL D safety element out-of-context developed per ISO 26262
- AEC-Q100 Grade 0 qualified
- VIN input range; 3.2 to 36 V operating, 40 V maximum
- Integrated wheel speed sensor interface compatible with 2-level, 3-level AK protocol, and 3-level high-resolution AK protocol
- Fully integrated, 2.2 MHz synchronous buck-boost pre-regulator (VREG: 5.8 V)
- Five internal linear regulators with fold back short-circuit protection:
  - VUC, 600 mA, 3.3/5 V LDO regulator for MCU
  - VLDOA, 200 mA, 5/3.3 V LDO regulator, normally used to supply the CAN transceivers
  - VLDOB, 200 mA, 5/3.3 V LDO regulator
  - VLDOC, 50 mA, 5 V 1% accuracy LDO regulator, normally used as MCU ADC reference

Continued on next page...

APPLICATIONS

- Electrical mechanical braking (EMB) module

PACKAGE



40-pin 6 mm × 6 mm QFN
(suffix EV)

Not to scale

DESCRIPTION

The A81415 is a power management IC that is optimized for electromechanical braking (EMB) applications. The A81415 integrates a buck boost pre-regulator, five LDOs, one channel wheel-speed sensor interface, and many safety features. The pre-regulator uses a fully integrated 2.2 MHz buck-boost topology to efficiently convert automotive battery voltages into a tightly regulated intermediate voltage complete with control, diagnostics, and protections.

The output of the pre-regulator supplies the five linear regulators and the wheel speed interface. The linear regulators can supply power for microprocessors, sensors, and CAN transceivers.

The wheel speed sensor interface is available to supply and measure the sensor current to provide the sensor data to the MCU through SPI and/or the digital output pin (WSIO).

Two automotive-battery-rated enable inputs are available on the A81415. An additional logic-level enable is also available for control via an MCU.

Diagnostic outputs from the A81415 include power-on reset (RESETn) and two safety outputs (POE1 and POE2). The microprocessor can read fault registers through SPI.

Dual bandgaps, one for regulation and one for fault checking, improve safety coverage and fault detection.

The A81415 also contains three types of watchdog timers: pulse width watchdog (PWWD), window watchdog (WWD), and Q&A watchdog (QAWD). The watchdog timers can be put into various operating states via secure SPI commands.

The A81415 is supplied in a low profile 40-pin QFN package with exposed power pad and wettable flanks.

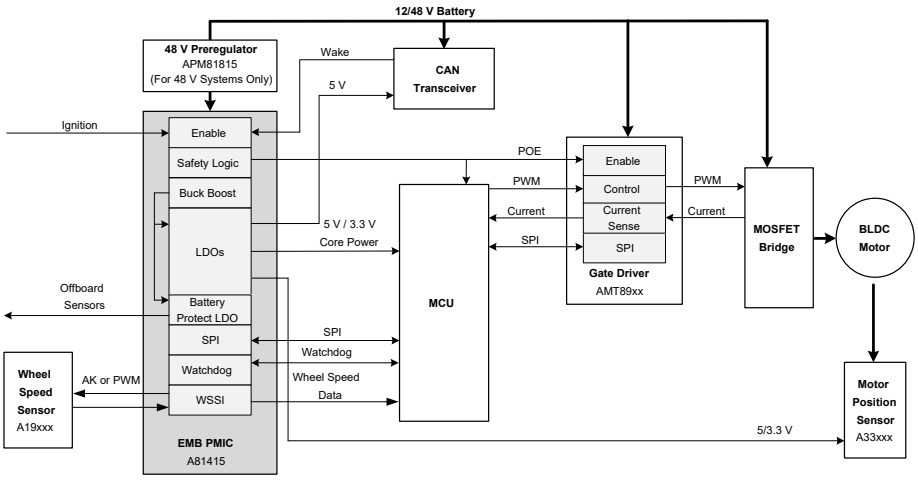


Figure 1: A81415 Simplified Application Diagram

FEATURES AND BENEFITS (continued)

- ◦ VLDOP, 50 mA, 5/3.3 V or VLDOC tracking LDO regulator with short-to battery protection for remote sensors
- Pulse-width watchdog (PWWD), window watchdog (WWD), and Q&A watchdog (QAWD)
- Voltage monitor (VCORMON) to verify MCU core voltage provided by an external DC-DC regulator
- Control and diagnostic reporting through secure SPI
- Two high-voltage enable inputs (ENBAT and ENCOM)
- Frequency dithering and controlled slew rate to mitigate EMI
- Over/undervoltage and current protections for all output rails
- Short-to-battery protections on all I/O
- Thermal warning and shutdown protection

SELECTION GUIDE [1]

Part Number	VLDOA Output Voltage (V)	VLDOB Output Voltage (V)	VCORMON	Package and Leadframe	Packing
A81415KEVGTR-1	5	5	Enabled	6 mm × 6 mm, 40-pin QFN with thermal pad and wettable flank, 100% matte tin leadframe plating	Tape and reel, 1500 pieces per 7-inch reel
A81415KEVGTR-2	5	3.3	Enabled		
A81415KEVGTR-3	3.3	3.3	Enabled		
A81415KEVGTR-4	5	5	Disabled		

[1] Not all combinations of programmable options are available preprogrammed From Allegro. For details, contact Allegro.

ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
VIN, VINP, WSIS Voltage	V_{VINx}, V_{WSIS}		−0.3 to 40	V
VREG, VUCIN Voltage	V_{VREG}, V_{VUCIN}		−0.3 to 20	V
ENBAT, ENCOM Voltage	V_{ENBAT}, V_{ENCOM}		−0.3 to 40	V
ENBAT, ENCOM Current	I_{ENBAT}, I_{ENCOM}		±75	mA
VUCSEL Voltage	V_{VUCSEL}		−0.3 to 20	V
LX1 Voltage	V_{LX1}		−0.3 to V_{VIN} + 0.3	V
		t < 250 ns	−1.5	V
LX2 Voltage	V_{LX1}		−0.3 to V_{VREG} + 0.3	V
		t < 250 ns	−1.5	V
CP1 Voltage	V_{CP1}		–0.3 to V_{VIN} + 0.3	V
CP2 Voltage	$_{VCP2}$		V_{VREG} – 0.3 to 20	V
VCP Voltage	V_{VCP}		V_{VREG} – 0.6 to 20	V
BOOT1 Voltage	V_{BOOT1}		–0.3 to V_{LX1} + 7	V
BOOT2 Voltage	V_{BOOT2}		–0.3 to V_{LX2} + 7	V
VLDOP Voltage	V_{VLDOP}		−1 to 40	V
WSIH, WSIL Voltage	V_{WSIH}, V_{WSIL}		−18 to 40	V
PGND, GND Voltage	V_{PGND}, V_{GND}		−0.3 to 0.3	V
All other pins			−0.3 to 7	V
Junction Temperature Range	T_J		−40 to 175	°C
Storage Temperature Range	T_{stg}		−40 to 150	°C

[1] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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ESD CHARACTERISTICS

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ESD HBM Robustness	$V_{ESD(HBM)}$	ESD susceptibility to GND on all pins	–2	–	2	kV
ESD CDM Robustness	$V_{ESD(CDM)}$	ESD susceptibility to GND on all pins	–500	–	500	V
	$V_{ESD(CDM,CORNER)}$	ESD susceptibility to GND on corner pins	–750	–	750	V
WSS IF Powered System Level ESD	$V_{ESD(PWR,CNT)}$	WSIH, WSIL @ –18 V and 40 V; Powered device, contact discharge, 150 pF / 2 kΩ	–	–	8	kV
WSS IF Unpowered System Level ESD	$V_{ESD(UNPWR,CNT)}$	WSIH, WSIL @ –18 V and 40 V; Unpowered device, contact discharge, 150 pF / 2 kΩ	–	–	6	kV
	$V_{ESD(UNPWR,AIR)}$	WSIH, WSIL @ –18 V and 40 V; Unpowered device, air discharge, 150 pF / 2 kΩ	–	–	6	kV

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [1]	Value	Unit
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	QFN, 40-pin package, 4-layer PCB based on JEDEC standard	27	°C/W

[1] Additional thermal information are available on the Allegro website.

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FUNCTIONAL BLOCK DIAGRAM

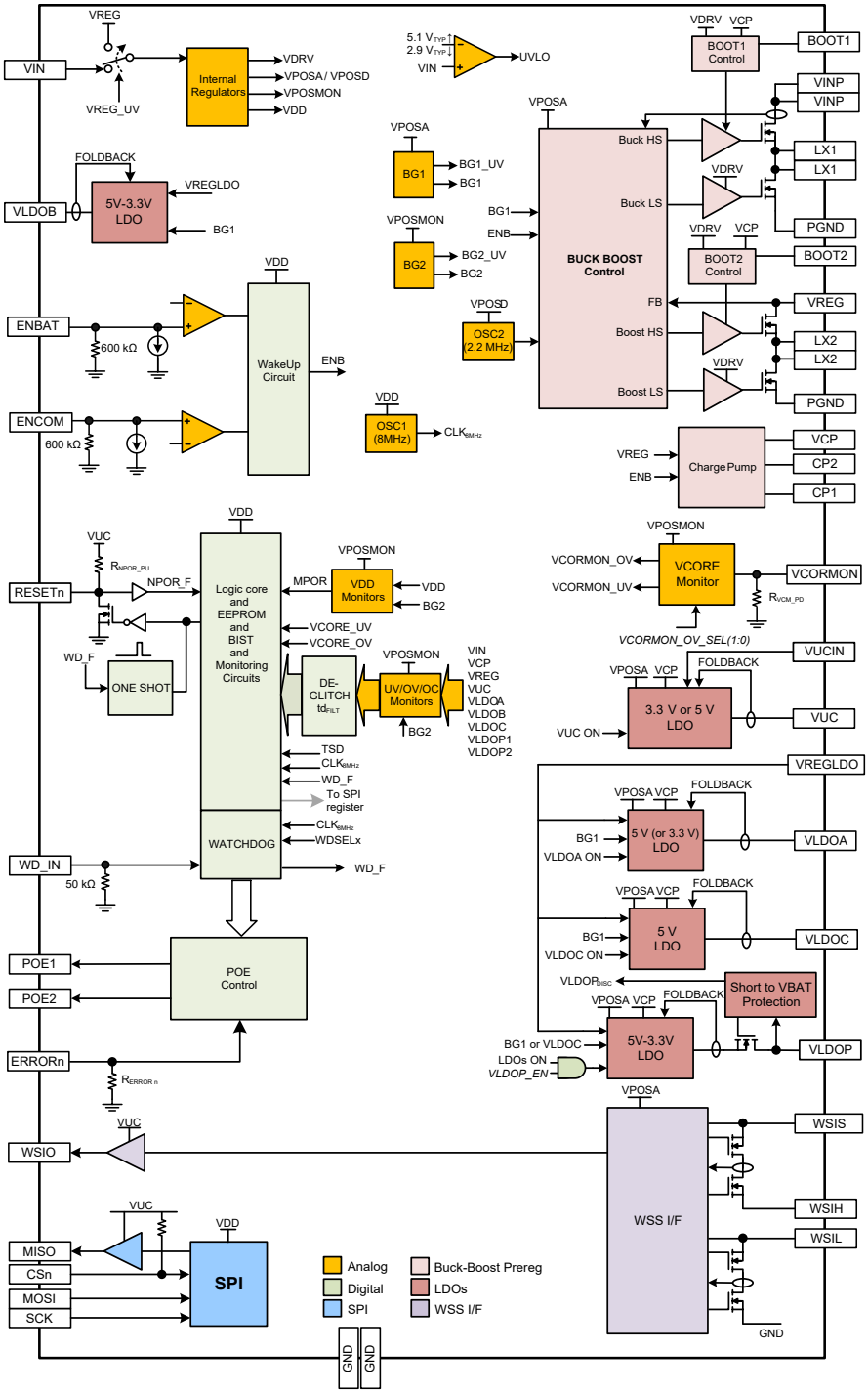

Figure 2: Functional Block Diagram

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APPLICATION SCHEMATIC

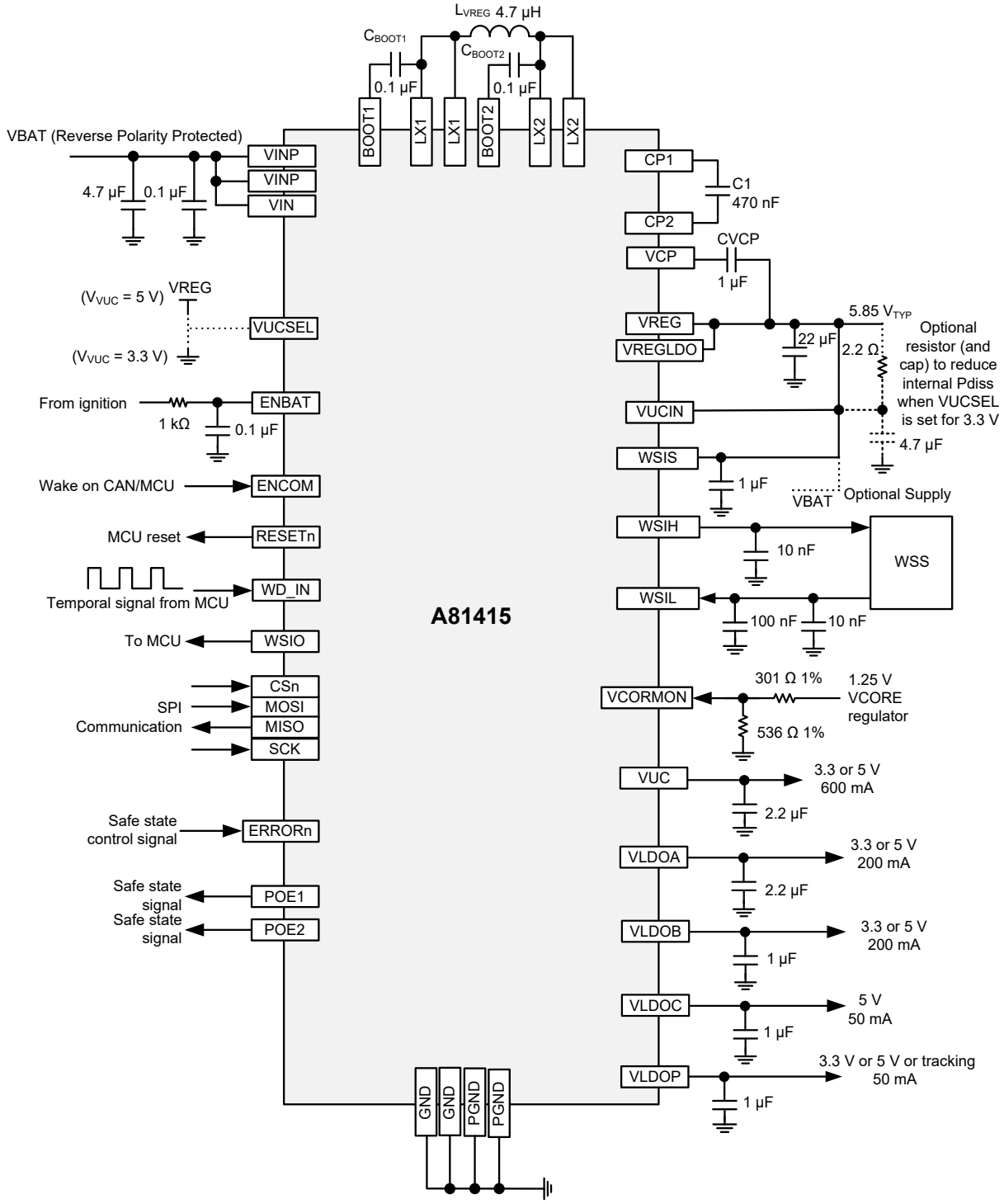

Figure 3: Application Schematic

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PINOUT DIAGRAM AND TERMINAL LIST

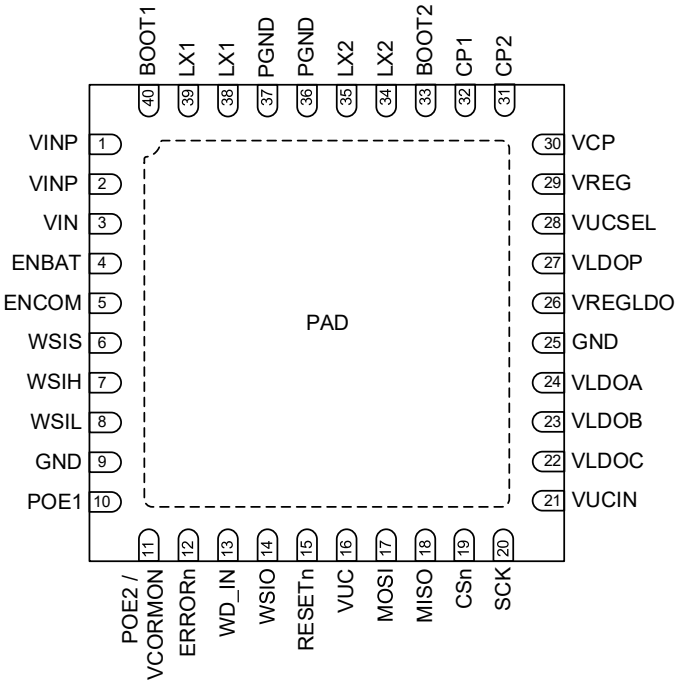

Figure 4: EV Package Pinout
40-Pin QFN with wettable flank

Table 1: Terminal List Table

Number	Name	Function
1, 2	VINP	Input voltage pin for buck drain connection. Connect high frequency capacitors between this pin and the PGND.
3	VIN	Control circuits input voltage pin.
4	ENBAT	Ignition enable input from the key/switch via a series resistor.
5	ENCOM	High-level enable for wake by CAN/ETHERNET or any other wakeup signal.
6	WSIS	Wheel speed sensor interface supply.
7	WSIH	Wheel speed sensor feed connection.
8	WSIL	Wheel speed sensor return connection.
9	GND	Signal ground.
10	POE1	Power-on enable 1 / Safety output 1, forced low during safety state.
11	POE2 / VCORMON	Power-on enable 2 / Safety output 2, forced low during safety state or external regulator MCU core voltage monitor input. Connect this pin via a resistor divider to the output of the external regulator used to supply the MCU core rail.
12	ERRORn	Active-low input or toggling signal that can be used to drive POEx low. If not used, short this pin to VUC or leave it open and mask it by SPI configuration.
13	WD_IN	Watchdog input signal from the MCU.
14	WSIO	Wheel speed sensor interface digital output.

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Table 1: Terminal List Table (continued)

Number	Name	Function
15	RESETn	Active-low VUC fault detection output (default functionality). Using SPI programming, a watchdog (WD) fault and/or VLDOA out of regulation can be added to the RESETn logic. Alternatively, this pin will function as an input so the MCU can generate a self-reset.
16	VUC	3.3 V or 5 V LDO output for a microcontroller. Voltage selected using the VUCSEL pin.
17	MOSI	SPI data input from the microcontroller (master output, slave input).
18	MISO	SPI data output to the microcontroller (master input, slave output).
19	CSn	SPI chip select input from the microcontroller, active low.
20	SCK	SPI clock input from the microcontroller.
21	VUCIN	Input to VUC regulator. Connect to VREG through optional external power resistor to reduce IC power dissipation.
22	VLDOC	5 V LDO output with 1% accuracy. Designed to power the ADC of the MCU.
23	VLDOB	5 V general purpose LDO output.
24	VLDOA	5 V (or 3.3 V factory trim option); designed to power one or two CAN transceivers.
25	GND	Signal ground.
26	VREGLDO	Voltage input to the VLDOA, VLDOC, VLDOP, and VLDOB regulators.
27	VLDOP	5V or 3.3V short to battery protected regulator, output enabled and selected through SPI
28	VUCSEL	VUC output voltage selection pin. Connect to VREG for 5 V output, connect to GND or leave it open for 3.3 V output. Status is latched at the end of VREG startup.
29	VREG	Voltage feedback to the pre-regulator control loop and input to the onboard LDOs and charge pump. Connect high frequency capacitors between this pin and PGND pin.
30	VCP	Charge pump reservoir capacitor connection, for LDO bias and high-side MOSFETs.
31	CP2	Charge pump flying capacitor connection, terminal 2.
32	CP1	Charge pump flying capacitor connection, terminal 1.
33	BOOT2	Boot capacitor for the boost regulator.
34, 35	LX2	Boost switching node.
36, 37	PGND	Power ground for boost low-side switch and its driver.
38, 39	LX1	Buck switching node.
40	BOOT1	Boot capacitor for the buck regulator.
–	PAD	Exposed thermal pad.

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ELECTRICAL CHARACTERISTICS: Valid at 3.2 V ≤ V_{VIN} ≤ 36 V, –40°C ≤ T_J ≤ 150°C, V_{ENCOM} or V_{ENBAT} high, unless otherwise specified. For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL						
Operating Input Voltage [1]	V_{VIN}	After V_{VIN} > $V_{VIN(START,MAX)}$ and VREG in regulation	3.2	13.5	36	V
Functional Input Voltage [1]	$V_{VIN(TRAN)}$	t < 1 second	2.6	–	40	V
VIN Supply Quiescent Current	I_Q	V_{VIN} = 13.5 V, V_{VREG} = 6 V (no PWM)	–	20	–	mA
VIN Supply Sleep Current	$I_{Q(OFF)}$	V_{VIN} = 13.5 V, VENB = Low [2], T_J = 40°C [1], off state	–	–	10	µA
VIN UVLO Start Voltage	$V_{VIN(START)}$	V_{VIN} rising and ENB = 1 [2]	4.9	5.1	5.3	V
VIN UVLO Stop Voltage	$V_{VIN(STOP)}$	V_{VIN} falling and ENB = 1 [2]	2.65	2.8	3.05	V
VIN UVLO Hysteresis	$V_{VIN(HYS)}$	$V_{VIN(START)}$ – $V_{VIN(STOP)}$	1	2.3	–	V
VIN UVLO Detection Delay [1]	$t_{d(UVLO)}$		7	10	13	µs
VIN Overvoltage Rising Threshold	$V_{VIN(OV,H)}$	V_{VIN} rising	37	38.5	40	V
VIN Overvoltage Falling Threshold	$V_{VIN(OV,L)}$	V_{VIN} falling	36	37.5	39	V
VIN Overvoltage Hysteresis	$V_{VIN(OV,HYS)}$	$V_{VIN(OV,H)}$ – $V_{VIN(OV,L)}$	–	1.0	–	V
VIN Overvoltage Detection Delay [1]	$t_{d(OV)}$		10	–	40	µs
VIN Input Ceramic Capacitance Range [1]	C_{VIN}		2.3	4.7	–	µF
	ESR_{C1VIN}		–	–	20	mΩ
Internal Clock Frequency	f_{CLOCK}		–5%	16	+5%	MHz
Internal Bandgap Voltages	V_{BG1}, V_{BG2}		–1%	1.204	+1%	V
ENABLE INPUTS: ENBAT AND ENCOM						
ENBAT Upper Threshold	$V_{ENBAT(H)}$	V_{ENBAT} rising	2.7	3.1	3.5	V
ENBAT Lower Threshold	$V_{ENBAT(L)}$	V_{ENBAT} falling	2.2	2.6	2.9	V
ENBAT Hysteresis	$V_{ENBAT(HYS)}$	$V_{ENBAT(H)}$ – $V_{ENBAT(L)}$	–	500	–	mV
ENBAT Bias Current	I_{ENBAT}	V_{ENBAT} = 40 V	–	20	50	µA
ENBAT Pulldown Resistance	R_{ENABLE}	When V_{ENBAT} < 1.2 V	–	600	–	kΩ
ENBAT Delay Time [1]	$t_{d(ENBAT)}$	Rising and falling, time from ENBAT to ENB [2]	1	1.25	1.6	ms
ENCOM Input High Voltage	$V_{ENCOM(H)}$		–	2	–	V
ENCOM Input Low Voltage	$V_{ENCOM(L)}$		–	0.8	–	V
ENCOM Hysteresis	$V_{ENBAT(HYS)}$	$V_{ENCOM(H)}$ – $V_{ENCOM(L)}$	–	250	–	mV
ENCOM Pulldown Resistance	R_{ENCOM}	When V_{ENCOM} < 1.2 V	150	600	–	kΩ
ENCOM Delay Time [1]	$t_{d(ENCOM)}$	Rising and falling, time from ENCOM to ENB [2]	0.10	0.23	0.35	ms

[1] Ensured by design and characterization, not production tested.
[2] ENB is internal startup/shutdown signal.

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Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
VREG BUCK-BOOST							
VREG Output Voltage [1]	V_{VREG}	0.1 A < I_{VREG} ≤ 1.25 A		5.7	5.85	6	V
VREG Output Inductance	L_{VREG}			–	4.7	–	µH
	DCR_{VREG}			–	–	80	mΩ
VREG Output Capacitor	C_{VREG}			10	22	–	µF
	ESR_{CVREG}			–	–	50	mΩ
Boot Capacitor	C_{BOOT1}, C_{BOOT2}			50	100	130	nF
	ESR_{CBOOT}			–	–	20	mΩ
Switching Frequency	$f_{sw(VREG)}$	Dithering off, V_{VIN} falling and V_{VIN} ≤ 18 V		2.0	2.2	2.4	MHz
		Dithering off, V_{VIN} rising and V_{VIN} ≥ 19 V		1.0	1.1	1.2	MHz
Frequency Dithering	$\Delta f_{sw(VREG)}$	As a percent of $f_{sw(VREG)}$		–10	–	+10	%
LX1 Rising Slew Rate [1]	$SR_{LX1(RISE)}$	V_{VIN} = 13.5 V, 10% to 90%, I_{VREG} = 1 A	BUCK_HS_SLEW = 00	–	2.2	–	V/ns
			BUCK_HS_SLEW = 01 (default)	–	1.4	–	V/ns
			BUCK_HS_SLEW = 10	–	0.75	–	V/ns
			BUCK_HS_SLEW = 11	–	3.6	–	V/ns
LX1 Falling Slew Rate [1]	$SR_{LX(RISE\_SLOW)}$	V_{VIN} = 13.5 V, 10% to 90%, I_{VREG} = 1 A		1.5	3	4.5	V/ns
LX2 Rising Slew Rate [1]	$SR_{LX(FALL)}$	V_{VIN} = 3.2 V, 90% to 10%, I_{VREG} = 1 A		1.5	3	4.5	V/ns
LX2 Falling Slew Rate [1]	$SR_{LX(FALL\_SLOW)}$	V_{VIN} = 3.2 V, 90% to 10%, I_{VREG} = 1 A		1.5	3	4.5	V/ns
Buck HS MOSFET On Resistance	$R_{DS(ON,BUCK,HS)}$	T_J = 150°C		–	–	150	mΩ
Buck LS MOSFET On Resistance	$R_{DS(ON,BUCK,LS)}$	T_J = 150°C		–	–	210	mΩ
Boost LS MOSFET On Resistance	$R_{DS(ON,BST,LS)}$	T_J = 150°C		–	–	210	mΩ
Boost HS MOSFET On Resistance	$R_{DS(ON,BST,HS)}$	T_J = 150°C		–	–	150	mΩ
Soft Start Ramp Time [1]	$t_{SS(VREG)}$			400	600	800	µs
SS PWM Frequency Foldback	$f_{PWM(SS,FFB)}$	V_{VREG} < 1.46 V typical		–	$f_{sw(VREG)}$ / 4	–	MHz
		1.46 V ≤ V_{VREG} < 2.92 V typical		–	$f_{sw(VREG)}$ / 2	–	MHz
		V_{VREG} ≥ 2.92 V typical		–	$f_{sw(VREG)}$	–	MHz
Hiccup Recovery Time [1]	$t_{HIC(REC)}$			–	5	–	ms
Hiccup OCP PWM Counts [1]	$t_{HIC(OCP)}$	V_{VREG} < 1.46 V_{TYP}		–	32	–	PWM cycles
		V_{VIN} ≤ 18 V, V_{VREG} > 1.46 V_{TYP}		120	–	–	PWM cycles
Normal Power Load Mode Pulse-by-Pulse Current Limit	$I_{LIM(ton,min)}$	V_{VIN} < 5.75 V, HIGH_POWER = 0 (default)		2.4	2.85	3.3	A
		V_{VIN} > 6.25 V, HIGH_POWER = 0 (default)		1.85	2.175	2.5	A
High Power Load Mode Pulse-by-Pulse Current Limit	$I_{LIM(ton,min)}$	V_{VIN} < 5.75 V, HIGH_POWER = 1		3.4	3.9	4.4	A
		V_{VIN} > 6.25 V, HIGH_POWER = 1		2.1	2.45	2.75	A
LX Short-Circuit Current Limit	$I_{LIM(LX)}$	Hiccup mode activated after 2nd detection		5.3	7.1	–	A
LX Short-Circuit Current Detection Delay [1]	$t_{d(Ilim,LX)}$			–	4	–	PWM cycles

[1] Ensured by design and characterization, not production tested.
[2] ENB is internal startup/shutdown signal.

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VREG BUCK-BOOST (continued)						
VREG Overvoltage Threshold	$V_{VREG(OV,H)}$	V_{VREG} rising, LX PWM will be disabled	6.45	6.65	6.85	V
	$V_{VREG(OV,L)}$	V_{VREG} falling, LX PWM will be enabled	–	6.25	–	V
VREG Overvoltage Hysteresis	$V_{VREG(OV,HYS)}$	$V_{VREG(OV,H)} – V_{VREG(OV,L)}$	–	100	–	mV
VREG OV Detection Delay [1]	$t_{d(VREG,OV)}$		20	25	30	µs
VREG Undervoltage Thresholds	$V_{VREG(UV,H)}$	V_{VREG} rising	5.1	5.3	5.5	V
	$V_{VREG(UV,L)}$	V_{VREG} falling	–	5.2	–	V
VREG Undervoltage Hysteresis	$V_{VREG(UV,HYS)}$	$V_{VREG(UV,H)} – V_{VREG(UV,L)}$	–	100	–	mV
VREG UV Detection Delay [1]	$t_{d(VREG,UV)}$		20	25	30	µs
BOOTx Undervoltage Thresholds	$V_{BOOT(UV,H)}$		2.5	–	3.3	V
	$V_{BOOT(UV,L)}$		2	–	2.6	V
BOOTx Overvoltage Thresholds	$V_{BOOT(OV,H)}$		5.5	–	6.5	V
	$V_{BOOT(OV,L)}$		5	–	5.9	V
BOOTx UV Detection Delay [1]	$t_{d(BOOT,UV)}$		–	18	–	PWM cycles
BOOTx OV Detection Delay [1]	$t_{d(BOOT,OV)}$		–	6	–	PWM cycles
CHARGE PUMP						
CP Output Voltage	V_{VCP}	$V_{VCP} – V_{VREG}$, I_{VCP} ≥ –4 mA	4.1	4.7	6	V
CP Flying Capacitor [1]	C_{PUMP}		200	470	620	nF
	ESR_{CPUMP}		–	–	20	mΩ
VCP Output Capacitor [1]	C_{VCP}		0.5	1	1.3	µF
	ESR_{VCP}		–	–	20	mΩ
VCP Switching Frequency	f_{CPx}		59.37	62.5	65.63	kHz
VCP Startup Time [1]	$t_{VCP(START)}$	$V_{REG} = V_{VREG(UV,H)}$, high to $V_{CP} = V_{VCP(UV,H)}$, C_{VCP} = 1 µF	–	–	2.5	ms
VCP Undervoltage Thresholds	$V_{VCP(UV,H)}$	V_{VCP} rising	2.78	3.1	3.26	V
	$V_{VCP(UV,L)}$	V_{VCP} falling	–	2.7	–	V
VCP Undervoltage Hysteresis	$V_{VCP(UV,HYS)}$	$V_{VCP(UV,H)} – V_{VCP(UV,L)}$	200	400	800	mV
VCP Overvoltage Thresholds	$V_{VCP(OV,H)}$	$V_{VCP} – V_{VREG}$, V_{VREG} = 5.85 V	6	7	8	V
	$V_{VCP(OV,L)}$	V_{VCP} falling	–	6.81	–	V
VCP Overvoltage Hysteresis	$V_{VCP(OV,HYS)}$	$V_{VCP(OV,H)} – V_{VCP(OV,L)}$	40	190	340	mV
VCP UV Detection Delay [1]	$t_{d(VCP,UV)}$		20	25	30	µs
VCP OV Detection Delay [1]	$t_{d(VCP,OV)}$		20	25	30	µs

[1] Ensured by design and characterization, not production tested.

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ELECTRICAL CHARACTERISTICS (continued): Valid at 3.2 V ≤ V_{VIN} ≤ 36 V, –40°C ≤ T_J ≤ 150°C, V_{ENCOM} or V_{ENBAT} high, unless otherwise specified. For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
THERMAL SENSOR AND PROTECTION							
Thermal Warning Threshold [1]	T_{WARN}	T_J rising		150	160	170	°C
Thermal Shutdown Threshold [1]	T_{TSD}	T_J rising		175	190	–	°C
Thermal Warning/Shutdown Hysteresis [1]	T_{HYS}			–	15	–	°C
Thermal Warning Detection Delay [1]	$t_{d(TWARN)}$			–	12	–	µs
Thermal Shutdown Detection Deglitch Filter On Rising Edge [1]	$t_{d(TSD)}$	T_J rising		–	12	–	µs
Thermal Shutdown Detection Deglitch Filter On Falling Edge [1]	$t_{d(TSD)}$	T_J falling		1.9	2.1	2.3	ms
LDO LINEAR REGULATORS							
VUC Output Voltage	V_{VUC}	0 mA ≤ I_{VUC} ≤ 600 mA	5V	4.9	5.0	5.1	V
			3V3	3.23	3.30	3.37	V
VUCIN Input Capacitance Range [1]	C_{VUCIN}			2.3	4.7	–	µF
	ESR_{CVUCIN}			–	–	20	mΩ
VUC Output Capacitance Range [1]	C_{VUC}			1.0	–	50	µF
	ESR_{CVUC}			–	–	20	mΩ
VLDOA Output Voltage	V_{VLDOA}	0 mA ≤ I_{VLDOA} ≤ 200 mA	5V	4.9	5.0	5.1	V
		0 mA ≤ I_{VLDOA} ≤ 200 mA A81415XXX-1	3V3	3.23	3.30	3.37	V
VLDOA Output Capacitance Range [1]	C_{VLDOA}			1.0	2.2	15	µF
	ESR_{CVLDOA}			–	–	20	mΩ
VLDOB Output Voltage	V_{VLDOB}	0 mA < I_{VLDOB} ≤ 200 mA	5V	4.9	5.0	5.1	V
		0 mA ≤ I_{VLDOB} ≤ 200 mA	3V3	3.23	3.30	3.37	V
VLDOB Output Capacitance Range [1]	C_{VLDOB}			1.0	2.2	15	µF
	ESR_{CVLDOB}			–	–	20	mΩ
VLDOC Output Voltage	V_{VLDOC}	0 mA ≤ I_{VLDOC} ≤ 50 mA		4.95	5.0	5.05	V
VLDOC Output Capacitance Range [1]	C_{VLDOC}			0.5	1.0	8	µF
	ESR_{CVLDOC}			–	–	20	mΩ
VLDOP Output Voltage	V_{VLDOP}	0 mA < I_{VLDOP} ≤ 50 mA	5V	4.9	5.0	5.1	V
			3V3	3.23	3.30	3.37	V
			VLDOC Tracking	–10	–	10	mV
VLDOP Output Capacitance Range [1]	C_{VLDOP}			0.5	1.0	8	µF
	ESR_{CVLDOP}			–	–	20	mΩ
VUC, VLDOA, VLDOB, VLDOC, and VLDOP Turn-Off Pull-Down Current	$I_{OFF(PD,LDO)}$	V_{VLDOx} = 5 V		10	20	30	mA

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Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
VUC OVERCURRENT PROTECTION							
VUC Current Limit	$I_{VUC(LIM)}$			–700	–900	–1100	mA
VUC Foldback Current	$I_{VUC(FBK)}$	V_{VUC} = 0 V		–60	–120	–220	mA
VUC Overcurrent Detection	$I_{VUC(OC)}$			–650	–790	–930	mA
VLDOA OVERCURRENT PROTECTION							
VLDOA Current Limit	$I_{VLDOA(LIM)}$			–240	–300	–360	mA
VLDOA Foldback Current	$I_{VLDOA(FBK)}$	V_{VLDOA} = 0 V		–20	–40	–60	mA
VLDOA Overcurrent Detection	$I_{VLDOA(OC)}$			–220	–280	–340	mA
VLDOB OVERCURRENT PROTECTION							
VLDOB Current Limit	$I_{VLDOB(LIM)}$			–240	–300	–360	mA
VLDOB Foldback Current	$I_{VLDOB(FBK)}$	V_{VLDOB} = 0 V		–20	–40	–60	mA
VLDOB Overcurrent Detection	$I_{VLDOB(OC)}$			–220	–280	–340	mA
VLDOC OVERCURRENT PROTECTION							
VLDOC Current Limit	$I_{VLDOC(LIM)}$			–64	-75	–86	mA
VLDOC Foldback Current	$I_{VLDOC(FBK)}$	V_{VLDOC} = 0 V		–5	–10	–15	mA
VLDOC Overcurrent Detection	$I_{VLDOC(OC)}$			–56	–66	–76	mA
VLDOP OVERCURRENT PROTECTION							
VLDOP Current Limit	$I_{VLDOP(LIM)}$			–64	–75	-86	mA
VLDOP Foldback Current	$I_{VLDOP(FBK)}$	V_{VLDOP} = 0 V		–5	–10	–15	mA
VLDOP Overcurrent Detection	$I_{VLDOP(OC)}$			–56	–66	–76	mA
VUC, VLDOA, VLDOC, VLDOP STARTUP TIMING							
VUC Startup Time [1]	$t_{VUC(START)}$	CVUC = 2.2 µF ± 20% and no current load	5 V_{OUT}	–	0.15	1.0	ms
			3.3 V_{OUT}	–	0.13	0.65	ms
VLDOA Startup Time [1]	$t_{VLDOA(START)}$	C_{VLDOA} = 2.2 µF ± 20% and no current load		–	0.15	1.0	ms
VLDOB Startup Time [1]	$t_{VLDOB(START)}$	C_{VLDOB} = 2.2 µF ± 20% and no current load		–	0.15	1.0	ms
VLDOC Startup Time [1]	$t_{VLDOC(START)}$	C_{VLDOC} = 2.2 µF ± 20% and no current load		–	0.15	1.0	ms
VLDOP Startup Time [1]	$t_{VLDOP(START)}$	C_{VLDOPx} = 2.2 µF ± 20% and no current load		–	0.15	1.0	ms
VUC, VLDOA, VLDOC, VLDOP SHUTDOWN DELAY (Z = A, C)							
VUC Shutdown Delay Time	$t_{VUC(OFF,DLY)}$			10	–	–	µs
VLDOx Shutdown Delay Time	$t_{VLDOx(OFF,DLY)}$			10	–	–	µs
VLDOP Shutdown Delay Time	$t_{VLDOP(OFF,DLY)}$			10	–	–	µs

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VCOR MONITOR (VCORMON)						
VCORMON Undervoltage Threshold	$V_{VCORMON(UV)}$	$V_{VCORMON}$ falling	716	728	740	mV
VCORMON Undervoltage Hysteresis	$V_{VCORMON(UV,HYS)}$		5	10	15	mV
VCORMON Overvoltage Threshold	$V_{VCORMON(OV,0)}$	$V_{VCORMON}$ rising, VCORMON_OV_SEL = 00	860	874	888	mV
	$V_{VCORMON(OV,1)}$	$V_{VCORMON}$ rising, VCORMON_OV_SEL = 01	879.5	894	908.5	mV
	$V_{VCORMON(OV,2)}$	$V_{VCORMON}$ rising, VCORMON_OV_SEL = 10	899.3	914	928.7	mV
	$V_{VCORMON(OV,3)}$	$V_{VCORMON}$ rising, VCORMON_OV_SEL = 11	919	934	949	mV
VCORMON Overvoltage Hysteresis	$V_{VCORMON(OV,HYS)}$		5	10	15	mV
VCORMON Undervoltage Deglitch [1]	$t_{d(VCORMON,UV)}$	VCORMON_UV_FILT = 0	20	25	30	µs
		VCORMON_UV_FILT = 1	60	75	90	µs
VCORMON Overvoltage Deglitch [1]	$t_{d(VCORMON,OV)}$	VCORMON_OV_FILT = 0	20	25	30	µs
		VCORMON_OV_FILT = 1	60	75	90	µs
VCORMON Pull-Down Resistance	$R_{VCM(PD)}$		224	320	416	kΩ
LDO ENABLES AND MONITORS						
VUC VOLTAGE SELECT (VUCSEL)						
VUCSEL Input High Voltage	$V_{VUCSEL(H)}$	V_{VUC} = 5 V	2.0	–	–	V
VUCSEL Input Low Voltage	$V_{VUCSEL(L)}$	V_{VUC} = 3.3V	–	–	0.8	V
VUCSEL Pull-Down Resistor	$R_{VUCSEL(PD)}$		–	50	–	kΩ
VUC, VLDOA, VLDOB, VLDOC, VLDOP UNDERVOLTAGE DETECTION THRESHOLDS						
VUC 5V Undervoltage Thresholds	$V_{VUC(UV,H)}$	V_{VUC} rising	–	4.63	–	V
	$V_{VUC(UV,L)}$	V_{VUC} falling	4.5	4.6	4.7	V
VLDOA, VLDOB, VLDOC, and VLDOP 5V Undervoltage Thresholds	$V_{V5(UV,H)}$	V_{VLDOx} rising	–	4.855	–	V
	$V_{V5(UV,L)}$	V_{VLDOx} falling	4.75	4.825	4.9	V
VUC, VLDOA, VLDOB, VLDOC, and VLDOP 5V Undervoltage Hysteresis	$V_{V5(UV,HYS)}$	$V_{V5(UV,H)} – V_{V5(UV,L)}$	–	30	–	mV
VUC, VLDOA, VLDOB, and VLDOP 3V3 Undervoltage Thresholds	$V_{3V3(UV,H)}$	V_{3V3} rising	–	3.09	–	V
	$V_{3V3(UV,L)}$	V_{3V3} falling	3.00	3.07	3.135	V
VUC, VLDOA, VLDOB, and VLDOP 3V3 Undervoltage Hysteresis	$V_{3V3(UV,HYS)}$	$V_{3V3(UV,H)} – V_{3V3(UV,L)}$	–	20	–	mV
VUC, VLDOx Short Undervoltage Detection Delay [1]	$t_{d(Vx,UV)}$	LDO_UV_FILT = 0	20	25	30	µs
VUC, VLDOx Long Undervoltage Detection Delay [1]	$t_{d(Vx,UV)}$	LDO_UV_FILT = 1	60	75	90	µs
VLDOA and VLDOP UV Startup Filter Time [1]	$t_{Vx(UV,START)}$			2		ms

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VUC, VLDOA, VLDOB, VLDOC, VLDOP OVERVOLTAGE DETECTION THRESHOLDS						
VUC, VLDOA, VLDOB, and VLDOP 5V Overvoltage Thresholds	$V_{V5(OV,H)}$	5 V LDO output voltage rising	5.25	5.375	5.5	V
	$V_{V5(OV,L)}$	5 V LDO output voltage falling	–	5.345	–	V
VUC, VLDOA, VLDOB, and VLDOP 5V Overvoltage Hysteresis	$V_{V5(OV,HYS)}$	$V_{V5(OV,H)} – V_{V5(OV,L)}$	–	30	–	mV
VLDOC 5V Overvoltage Thresholds	$V_{VLDOC5(OV,H)}$	5 V VLDOC LDO output voltage rising	5.15	5.2	5.25	V
	$V_{VLDOC5(OV,L)}$	5 V VLDOC LDO output voltage falling	–	5.17	–	V
VLDOC 5V Overvoltage Hysteresis	$V_{VLDOC5(OV,HYS)}$	$V_{VLDOC5(OV,H)} – V_{VLDOC5(OV,L)}$	–	30	–	mV
VUC, VLDOA, VLDOB, and VLDOP 3V3 Overvoltage Thresholds	$V_{3V3(OV,H)}$	3.3 V LDO output voltage rising	3.465	3.53	3.6	V
	$V_{3V3(OV,L)}$	3.3 V LDO output voltage falling	–	3.51	–	V
VUC, VLDOA, VLDOB, and VLDOP 3V3 Overvoltage Hysteresis	$V_{3V3(OV,HYS)}$	$V_{3V3(OV,H)} – V_{3V3(OV,L)}$	–	20	–	mV
VUC, VLDOx Overvoltage Detection Delay [1]	$t_{d(Vx,OV)}$	LDO_OV_FILT = 0	20	25	30	µs
		LDO_OV_FILT = 1	60	75	90	µs
VUC Absolute Maximum Rating Overvoltage Thresholds	$V_{VUC(AMR,OV,H)}$	VUC voltage rising	6	6.3	6.6	V
	$V_{VUC(AMR,OV,L)}$	VUC voltage falling	–	6.15	–	V
VUC Absolute Maximum Rating Over Voltage Hysteresis	$V_{VUC(AMR,OV,HYS)}$		90	150	210	mV
VUC AMR Overvoltage Detection Delay [1]	$t_{d(VUC,AMR,OV)}$		–	5	–	µs
RESETn OUTPUT						
RESETn Turn-On Delay	$t_{d(RESETn,ON)}$	Time from VUC_UV, VLDOC_UV, VLDOB_UV, and VCORMON_UV to the RESETn pin high	1.6	2	2.4	ms
RESETn Output Low Voltage	$V_{RESETn(L)}$	I_{RESETn} = 4 mA	–	150	400	mV
		V_{VIN} = 5.5 V, I_{RESETn} = 2 mA	–	–	200	mV
RESETn Internal Pull-Up	$R_{PU(RESETn)}$	Pull up to VUC	7	10	13	kΩ
RESETn Leakage Current	$I_{LKG(RESETn)}$	$V_{RESETn} = V_{VUC}$	–	–	2	µA
RESETn One-Shot Low Time After Watchdog Fault	$t_{WD(FAULT)}$	Enabled via SPI using the RESETn_KEY	1.6	2	2.4	ms
RESETn One-Shot Low Time After MCU Self Reset	$t_{MIN(RESETn,LOW)}$	Enabled via SPI using the RESETn_KEY	1.6	2	2.4	ms
RESETn LDO Fault De-Assertion Time	$t_{d(RESETn)}$	Enabled via SPI using the RESETn_KEY	1.6	2	2.4	ms
RESETn Unlatch Time [1]	$t_{RESETn(UNLATCH)}$		4.65	5	5.35	seconds

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Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
WATCHDOG, POEx, ERRORn, BIST							
WD_IN Input High Voltage	$V_{WDIN(H)}$	V_{WDIN} rising		2.0	–	–	V
WD_IN Input Low Voltage	$V_{WDIN(L)}$	V_{WDIN} falling		–	–	0.8	V
WD_IN Pull-Down Resistance	$R_{WDIN(PD)}$			30	50	70	kΩ
Watchdog Configuration Timeout [1]	$t_{CONFIG(TO)}$	Can be bypassed by setting WD_SEL bits		240	270	300	ms
POEx Output Voltage	$V_{POE(L)}$	POE is tripped, I_{POE} = 4 mA		–	150	400	mV
POEx Internal Pull-Up	$R_{POE(PU)}$	Pull up to VUC		7	10	13	kΩ
POEx Leakage Current	$I_{LKG(POE)}$	V_{POE} = V_{VUC}		–	–	2	µA
ERRORn Input High Voltage	$V_{ERRORn(H)}$			2.0	–	–	V
ERRORn Input Low Voltage	$V_{ERRORn(L)}$			–	–	0.4	V
ERRORn Pull-Down Resistance	$R_{ERRORn(PD)}$			38.5	55	71.5	kΩ
ERRORn to POE Delay	$t_{d(ERRORn)}$	ERRORn_SEL = 0		–	6	9	µs
ERRORn Valid Frequency	$f_{ERR(OK)}$	Considering 50% duty cycle on ERRORn, ERRORn_SEL = 1		–	30	–	kHz
ERRORn Detection Time Low Frequency	$t_{D(ERR,LF)}$	ERRORn_SEL = 1		50.1	–	99.9	µs
ERRORn Detection Time High Frequency	$t_{D(ERR,HF)}$	ERRORn_SEL=1		5.2	–	11.1	µs
ERRORn Activation Time-out	$t_{ERR(TO)}$	Time from RESETn release, ERRORn_SEL = 1		8.5	10.5	12.5	ms
ERRORn SPI Activation Timeout	$t_{ERR(SPI,TO)}$	Time from ERRORn_DIS = 0 to ERRORn monitoring start, ERRORn_SEL = 1		50.1	–	110	µs
ERRORn Recovery Time	$t_{ERR(REC)}$	ERRORn_REC = 1, ERRORn_REC_SEL = 1		8.5	10.5	12.5	ms
Logic BIST Duration [1]	t_{LBIST}			–	–	30	ms
Analog BIST Duration [1]	t_{ABIST}			–	–	0.2	ms
WHEEL SPEED SENSOR INTERFACE							
Operational Input Supply Range [1]	V_{WSIS}			5.3	–	36	V
WSIS Undervoltage Rising Threshold	$V_{WSIS(UV,H)}$	V_{WSIS} rising		5.35	5.5	5.65	V
WSIS Undervoltage Falling Threshold	$V_{WSIS(UV,L)}$	V_{WSIS} falling		5.3	5.45	5.6	V
WSIS Undervoltage Hysteresis	$V_{WSIS(UV,HYS)}$	$V_{WSIS(UV,H)}$ – $V_{WSIS(UV,L)}$		–	50	–	mV
WSIS Undervoltage Detection Delay [1]	$t_{D(WSIS,UV)}$			20	25	30	µs
WSI Output Differential Voltage	$V_{WSI(DIFF)}$	$V_{WSI(H)}$ – $V_{WSI(L)}$, V_{WSIS} ≥ 5.3 V, I_{sensor} = 33.6 mA		4.5	–	15	V
High-Side and Low-Side Switches Total Resistance	$R_{WSI(TOT)}$	$R_{WSI(H)}$ + $R_{WSI(L)}$		5	–	23.8	Ω
High-Side Switch Leakage	$I_{LEAK(WSIH)}$	Device off, –18 V < V_{WSIH} < 40 V	–40°C ≤ T_J ≤ 60°C	–2	–	2	µA
			–40°C ≤ T_J ≤ 175°C	–50	–	100	µA
Low-Side Switch Leakage	$I_{LEAK(WSIL)}$	Device off, –18 V < V_{WSIL} < 40 V	–40°C ≤ T_J ≤ 60°C	–2	–	2	µA
			–40°C ≤ T_J ≤ 175°C	–50	–	100	µA

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
WHEEL SPEED SENSOR INTERFACE (continued)						
High-Side Switch Current Limitation	$I_{LIM(WSIH)}$	High-side switch enabled and V_{WSIH} = 0 V	60	–	100	mA
High-Side Overcurrent Threshold	$I_{OC(WSIH)}$		54	–	–	mA
High-Side Overcurrent Deglitch Filter [1]	$t_{D(IOC,WSIH)}$		88	–	121	µs
High-Side Short-To-Battery Threshold	$V_{STB(WSIH)}$	V_{WSIH} – V_{WSIS}	–	250	–	mV
High-Side Short-To-Battery Deglitch Filter [1]	$t_{d(STB,WSIH)}$		9	–	13	us
Low-Side Switch Current Limitation	$I_{LIM(WSSL)}$	Low-side switch enabled and V_{WSIL} = 40 V	60	–	100	mA
Low-Side Overcurrent Threshold	$I_{OC(WSIL)}$		54	–		mA
Low-Side Overcurrent Deglitch Filter [1]	$t_{d(IOC,WSIL)}$		88	–	121	µs
Low-Side Short-To-Ground Pull-Up Current	$I_{STG(WSIL)}$	V_{WSIL} = 0 V	35	47.5	70	µA
Low-Side Short-To-Ground Detection Voltage	$V_{STG(WSIL)}$	WSIL_EN = 0	2.25	2.5	2.75	V
Low-Side Short-To-Ground Deglitch Time [1]	$t_{d(STG,WSIL)}$	C_{WSIL} < 180 nF	15	–	26	ms
Low-Side Negative Ground Voltage Threshold	$V_{REVG(WSIL)}$		–	–0.5	–	V
Low-Side Negative Ground Deglitch Time [1]	$t_{d(REVG,WSIL)}$		9	–	13	µs
Open Condition Current Threshold	$I_{OPEN(a)}$	WSI_OC_TH = 0	3.9	–	5.8	mA
	$I_{OPEN(b)}$	WSI_OC_TH = 1	2.3	–	4.9	mA
Low Current Threshold	$I_{TH1(LH)}$	Rising edge; offset not considered	–	–	11.76	mA
	$I_{TH1(HL)}$	Falling edge; offset not considered	8.4	–	–	mA
	$I_{TH1(HYS)}$	Hysteresis	1.49	–	–	mA
High Current Threshold	$I_{TH2(LH)}$	Rising edge; offset not considered	–	–	22.4	mA
	$I_{TH2(HL)}$	Falling edge; offset not considered	17.0	–	–	mA
	$I_{TH2(HYS)}$	Hysteresis	1.27	–	–	mA
WSS Resistive Short Value	R_{RWSS}	Minimum resistive short value to be compensated during short to battery	2	–	–	kΩ
		Minimum resistive short value to be compensated from V_{WSIL} = 0 V	2	–	–	kΩ
WSI Current Threshold Filter [1]	$t_{d(ITH,a)}$	WSI_TD_SEL = 00	–	0	–	µs
	$t_{d(ITH,b)}$	WSI_TD_SEL = 01 (default)	13.3	15	15.8	µs
	$t_{d(ITH,c)}$	WSI_TD_SEL = 10	26.6	29	31.5	µs
	$t_{d(ITH,d)}$	WSI_TD_SEL = 11	53.2	58	63	µs
WSIO Propagation Delay [1]	$t_{dly(WSIO,a)}$	WSI_TD_SEL = 00	1.12	–	2.43	µs
	$t_{dly(WSIO,b)}$	WSI_TD_SEL = 01 (default)	15.4	–	18.15	µs
	$t_{dly(WSIO,c)}$	WSI_TD_SEL = 10	28.6	–	32.8	µs
	$t_{dly(WSIO,d)}$	WSI_TD_SEL = 11	56.2	–	63.3	µs

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
WHEEL SPEED SENSOR INTERFACE (continued)						
WSI Thermal Warning Threshold [1]	$T_{WARN(WSI)}$		150	160	170	°C
WSI Thermal Warning Deglitch Filter [1]	$t_{d(TWARN,WSI)}$		88	–	121	µs
WSI Thermal Protection Threshold [1]	$T_{TSD,WSI}$		175	–	–	°C
WSI Thermal Protection Deglitch Filter [1]	$t_{d(TSD,WSI)}$		88	–	121	µs
WSIH Output ESD Capacitor [1]	$C_{ESD(WSIH)}$		–35%	10	+25%	nF
WSIL Output ESD Capacitor [1]	$C_{ESD(WSIL)}$		–35%	10	+25%	nF
WSIL Output Capacitor [1]	C_{WSIL}		–35%	100	+25%	nF
WSIO Output Low Voltage	$V_{OL(WSIO)}$	I_{OL} = 1 mA	–	–	0.4	V
WSIO Output High Voltage	$V_{OH(WSIO)}$	I_{OH} = –1 mA	0.8 × V_{VUC}	–	–	V
WSIO PWM On-Time Measurement Resolution	$t_{WSI(PWM,ON)}$		4.6	–	5.4	µs
WSIO PWM On-Time Counter Saturation [1]	$t_{WSI(PWM,SAT)}$		–	–	511 × $t_{WSI(PWM,ON)}$	µs
WSIO Standstill Pulse Low Threshold [1]	$t_{WSI(SS,LOW)}$		1.007 (219 × $t_{WSI(PWM,ON)}$	–	1.188 (219 × $t_{WSI(PWM,ON)}$	ms
WSIO Standstill Pulse High Threshold [1]	$t_{WSI(SS,HIGH)}$		1.693 (219 × $t_{WSI(PWM,ON)}$	–	1.993 (219 × $t_{WSI(PWM,ON)}$	ms
WSIO Edge Counter [1]	$N_{WSI(EDGE)}$		–	–	63	–
3-Level Mode 3: WSIO Output Initial Pulse Minimum Time [1]	$t_{p(min)}$	$t_{d(ITH)}$ = 15 µs, including jitter	28.8	–	36.4	µs
3-Level Mode 3: WSIO Output Initial Pulse Maximum Time [1]	$t_{p(max)}$	$t_{d(ITH)}$ = 15 µs, including jitter	66.1	–	77.6	µs
3-Level Mode 3: WSIO Output Initial Pulse Overrun Time [1]	$t_{p(over)}$	$t_{d(ITH)}$ = 15 µs, including jitter	102	–	118	µs
3-Level Hr Mode 4/5: WSIO Output Standard Speed Pulse Width [1]	$t_{WSIO(SP)}$		235	–	269	µs
3-Level Hr Mode 4/5: WSIO Output Interpolated Speed Pulse Width [1]	$t_{WSIO(ISP)}$		326	–	370	µs
3-Level Hr Mode 4: WSIO Output Standstill Speed Pulse Width [1]	$t_{WSIO(SSP)}$		425	–	479	µs
SERIAL INTERFACE						
Input Low Voltage (CSn, MOSI, SCK)	V_{IL}		–	–	0.8	V
Input High Voltage (CSn, MOSI, SCK)	V_{IH}		2.0	–	–	V
Input Hysteresis (CSn, MOSI, SCK)	V_{ihys}		–	250	–	mV
MOSI Input Internal Pull-Down	$R_{MOSI(PD)}$		30	50	70	kΩ
SCK Input Internal Pull-Down	$R_{SCK(PD)}$		30	50	70	kΩ
CSn Input Internal Pull-Up	$R_{WD\_IN(PU)}$	Pull up to VUC	30	50	70	kΩ

[1] Ensured by design and characterization, not production tested.

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ELECTRICAL CHARACTERISTICS (continued): Valid at 3.2 V ≤ V_{VIN} ≤ 36 V, –40°C ≤ T_J ≤ 150°C, V_{ENCOM} or V_{ENBAT} high, unless otherwise specified. For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), positive current is defined as going into the node or pin (sinking).

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SERIAL INTERFACE (continued)						
MISO Output Low Voltage	V_{OL}	I_{OL} = 1 mA [1]	–	–	0.4	V
MISO Output High Voltage	V_{OH}	I_{OH} = –1 mA [1]	0.8 × V_{VUC}	–	–	V
SPI Clock Frequency	f_{SCK}	MISO pins, C_L = 20 pF	0.1	–	10	MHz
SPI Frame Rate [1]	t_{SPI}		2.94	–	294	kHz
Clock High Time [1]	$t_{SCK(H)}$	A in Figure 1	40	–	–	ns
Clock Low Time [1]	$t_{SCK(L)}$	B in Figure 1	40	–	–	ns
Chip Select Lead Time [1]	$t_{CS(LD)}$	C in Figure 1	30	–	–	ns
Chip Select Lag Time [1]	$t_{CS(LG)}$	D in Figure 1	30	–	–	ns
Chip Select High Time [1]	$t_{CS(H)}$	E in Figure 1	400	–	–	ns
Data Out (MISO) Enable Time [1]	$t_{MISO(EN)}$	F in Figure 1	–	–	40	ns
Data Out (MISO) Disable Time [1]	$t_{MISO(D)}$	G in Figure 1	–	–	30	ns
Data Out (MISO) Valid Time from SCK Falling [1]	$t_{MISO(V)}$	H in Figure 1	–	–	40	ns
Data Out (MISO) Hold Time from SCK Falling [1]	$t_{MISO(H)}$	J in Figure 1	5	–	–	ns
Data In (MOSI) Set-Up Time to SCK Rising [1]	$t_{MOSI(SU)}$	K in Figure 1	15	–	–	ns
Data In (MOSI) Hold Time from SCK Rising [1]	$t_{MOSI(H)}$	L in Figure 1	10	–	–	ns

[1] Ensured by design and characterization, not production tested.

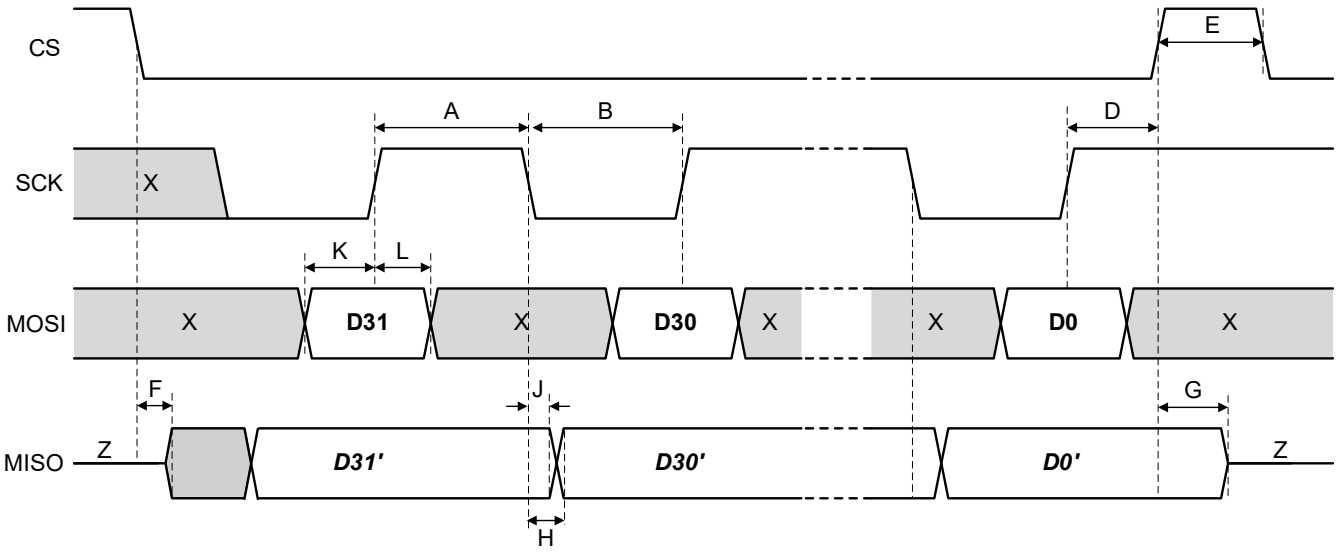

Figure 5: Serial Interface Timing for Write and Read Cycles.
MISO activity assumes the Chip_ID from the previous frame was correct.

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TIMING DIAGRAMS

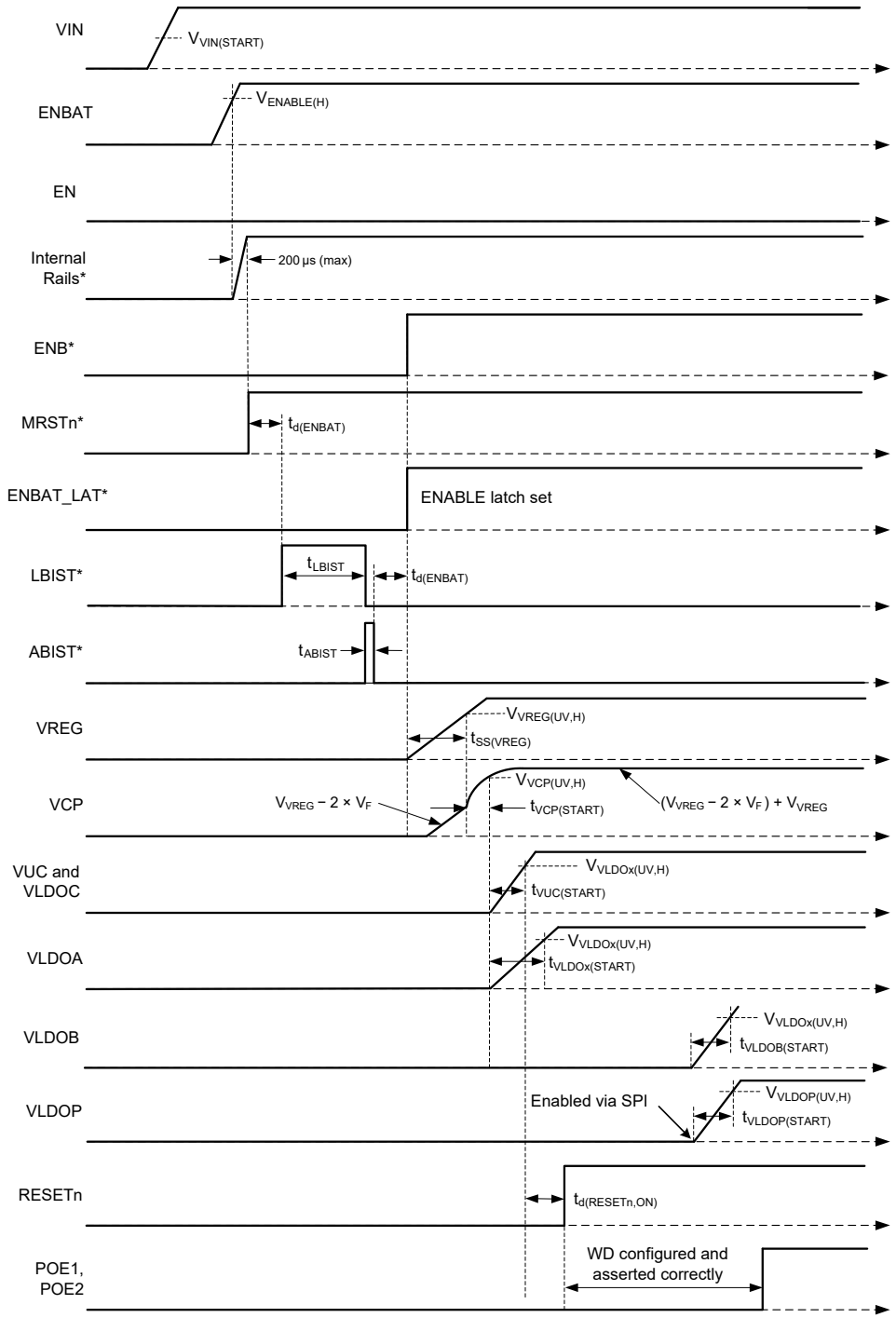

Figure 6: Startup by ENBAT Timing Diagram
* = internal signal

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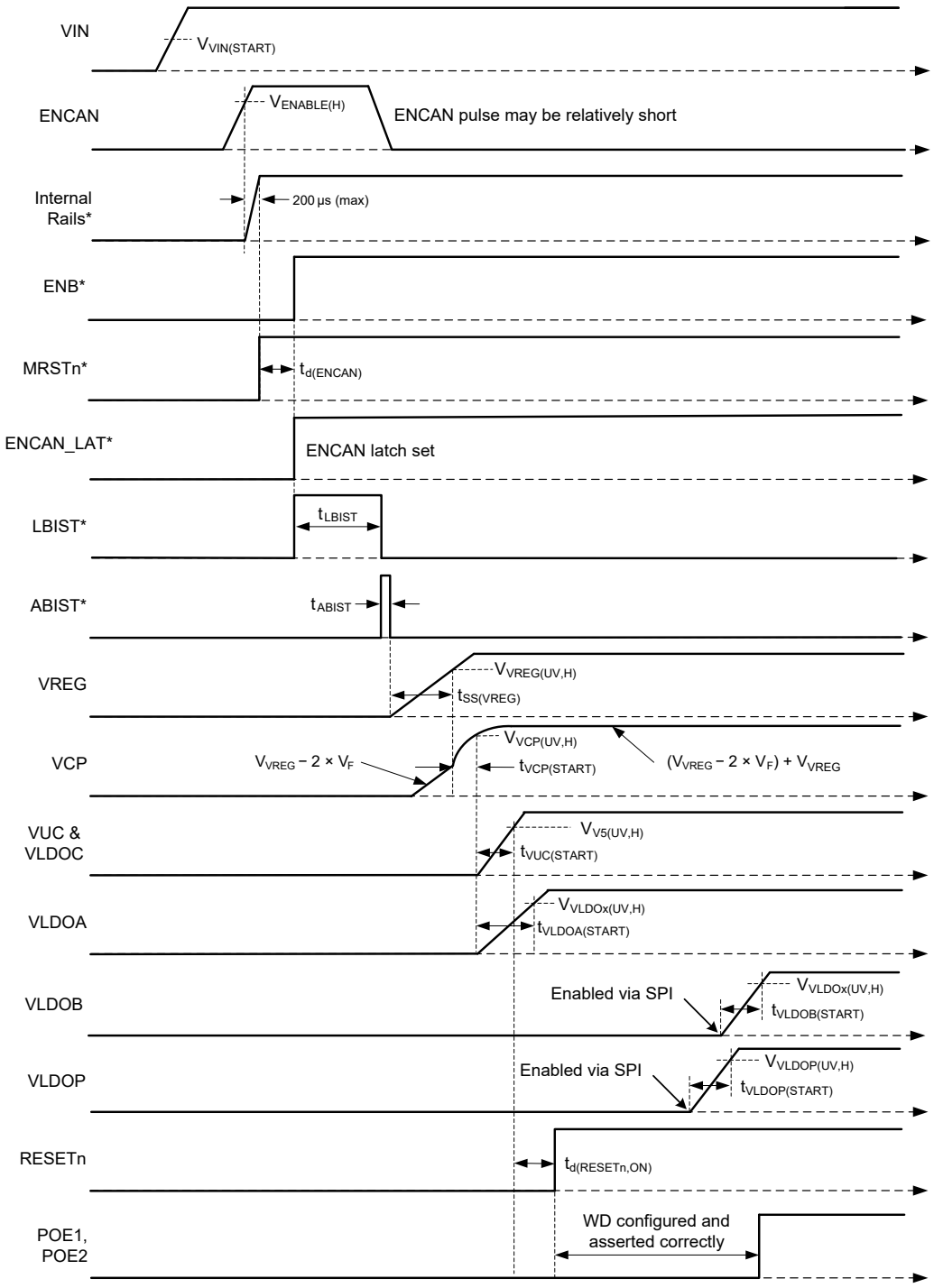

Figure 7: Startup by ENCOM Timing Diagram (ENxyz_LAT disabled)
* = internal signal

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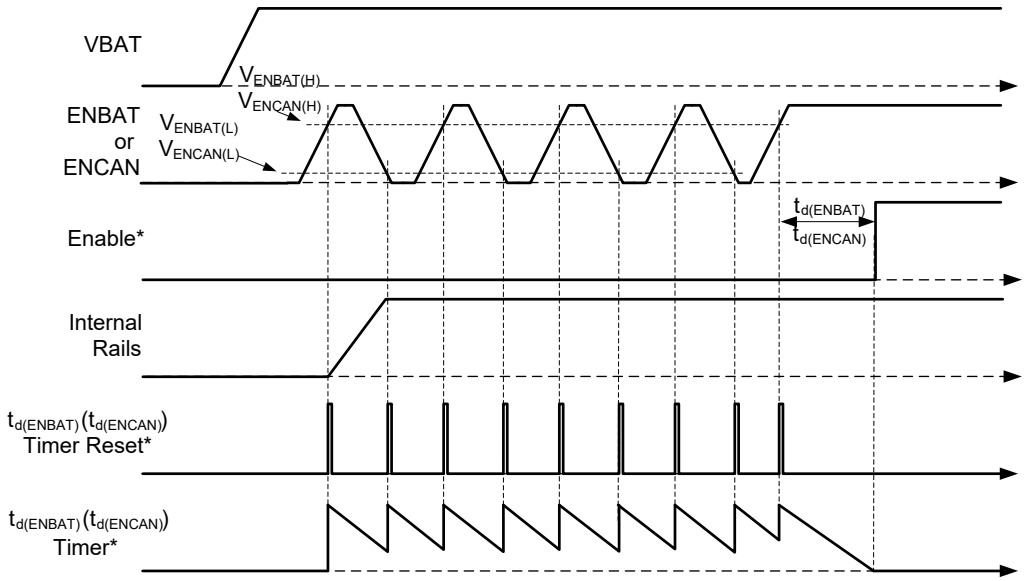

Figure 8: Startup with oscillating ENBAT (ENCOM) Signal.
* = internal signal

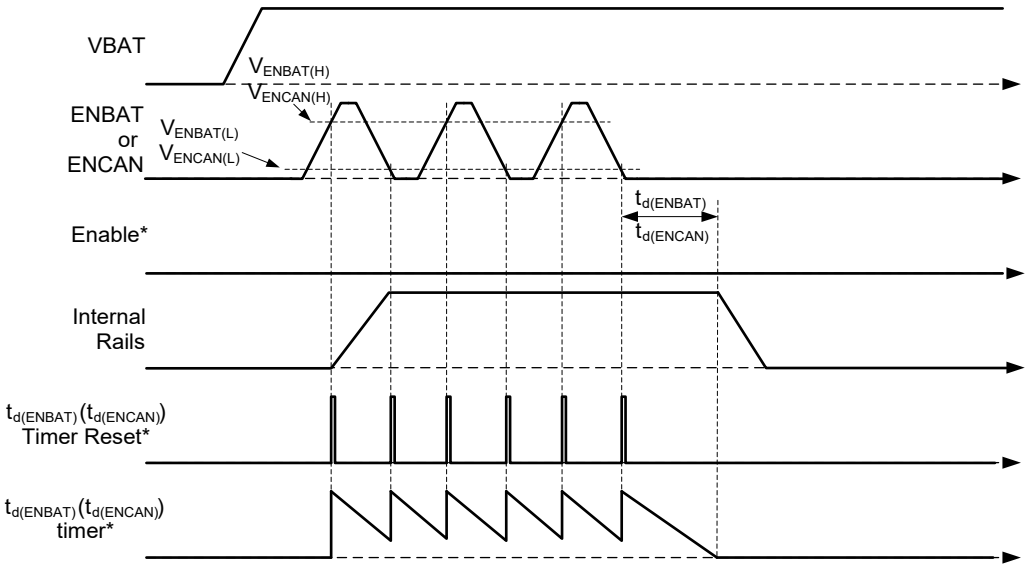

Figure 9: No start up with oscillating ENBAT (ENCOM) Signal.
* = internal signal

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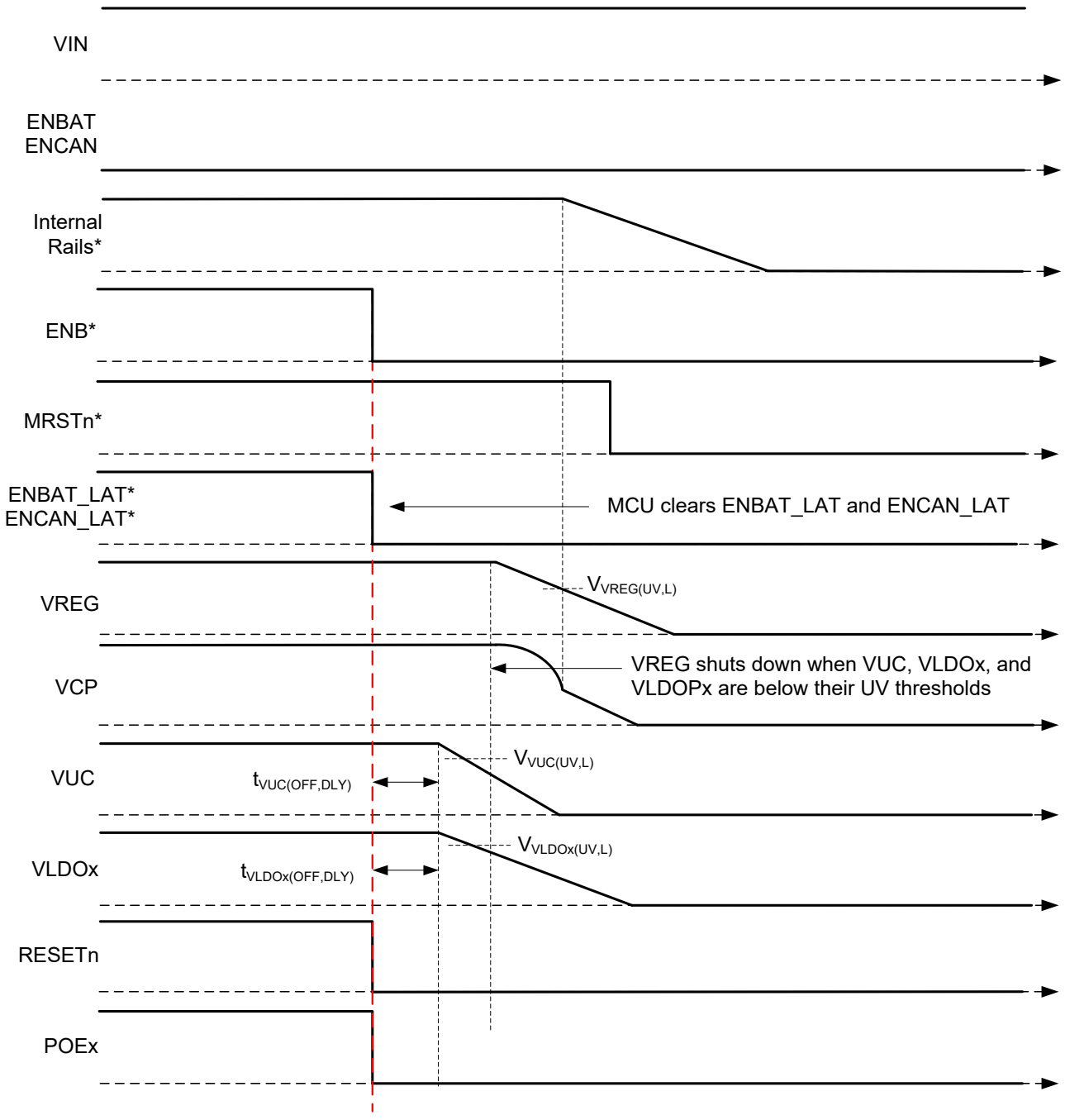

Figure 10: Shutdown Timing Diagram.
The time for an output to decay to zero, $t_{x(FALL)}$, varies for each output and depends on load and output capacitance.
* = internal signal

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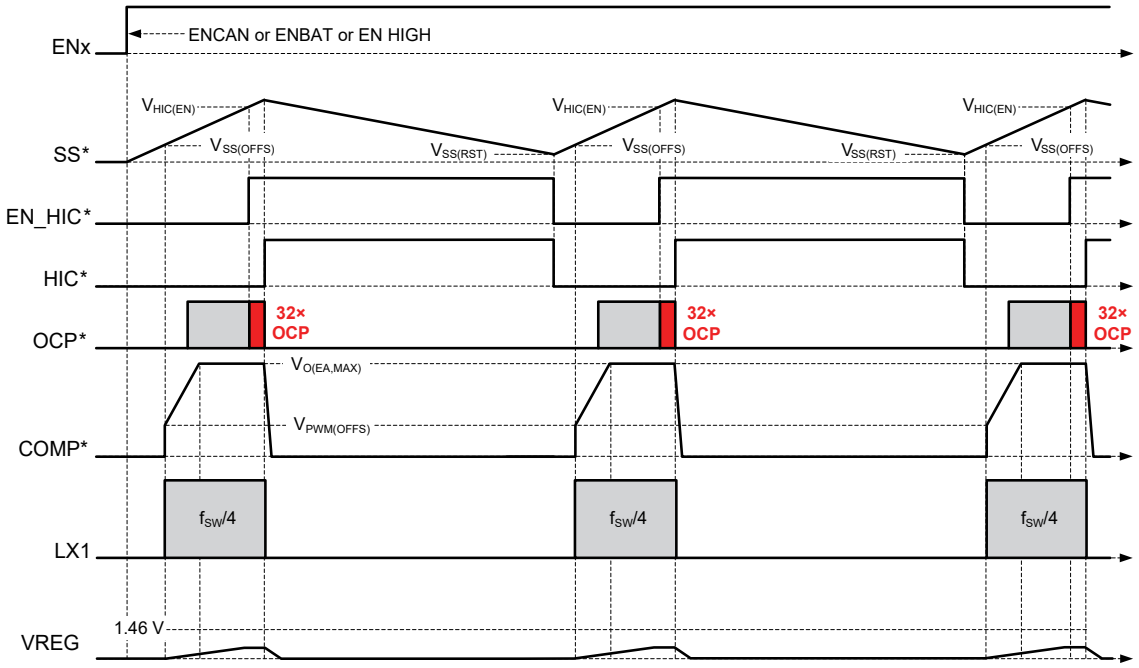

Figure 11: Hiccup Mode Operation with VREG Shorted to GND (R_{LOAD} < 50 mΩ)
* = internal signal or threshold

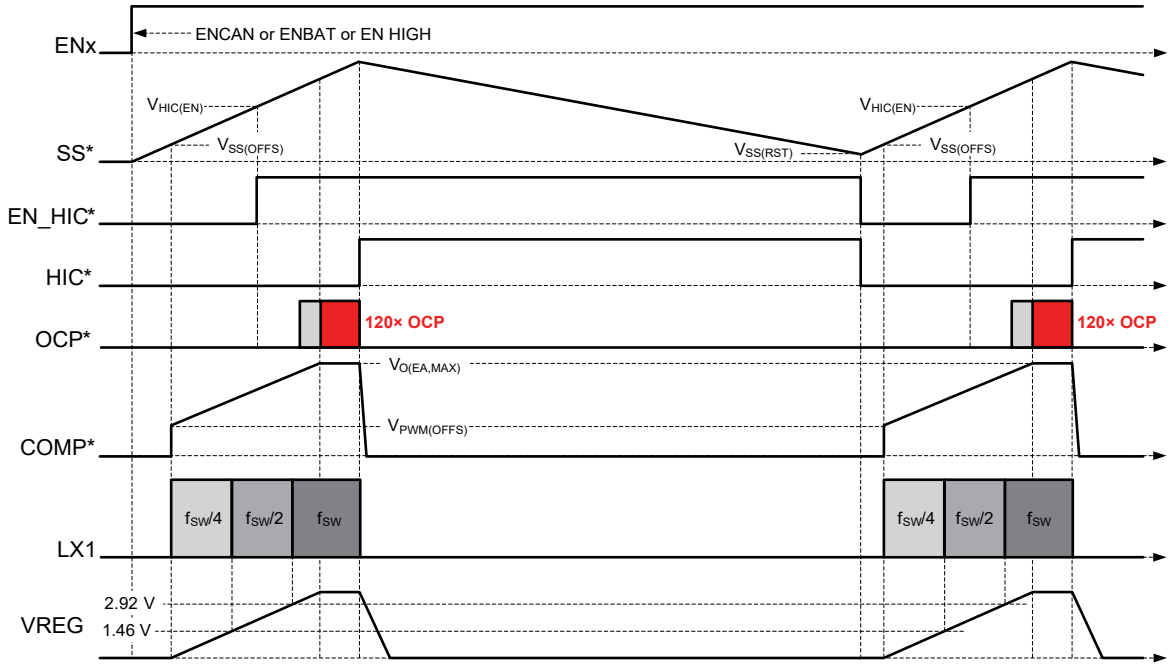

Figure 12: Hiccup Mode Operation with VREG Overloaded (R_{LOAD} ≈ 0.5 Ω)
* = internal signal or threshold

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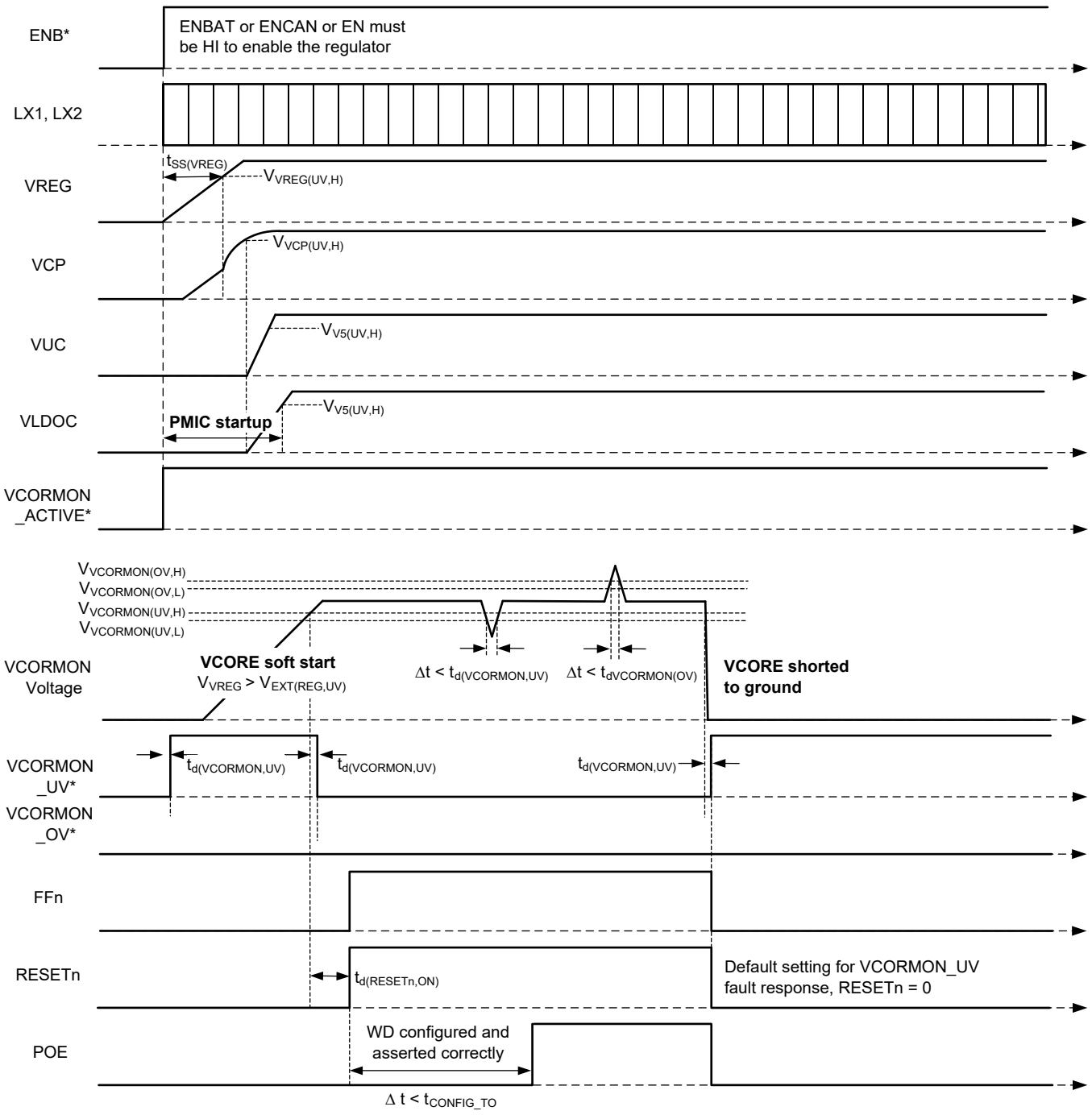

Figure 13: VCORMON Startup (Powered by VREG), and Short-to-Ground (UV+STG) Operation.
* = internal signal
The external VCORE regulator is powered by VREG (or VUC).
External regulator begins soft start when its input voltage (VREG or VUC) is above its UV threshold.

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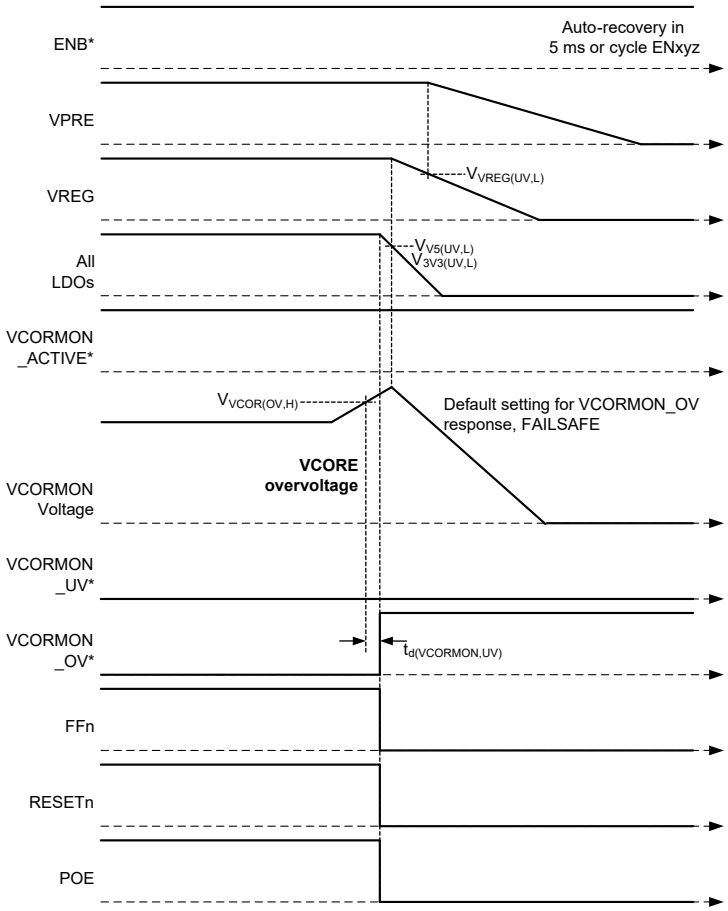

Figure 14: VCORMON overvoltage (OV) operation
*** = internal signal**

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FAULT MODES OPERATION

Table 2: Fault Modes Operation [1][2][3][4]

Fault	Description or SPI Configuration	VCP	VREG	WSI	VUC	VLDOA	VLDOB	VLDOC	VLDOP	SPI FF	RESETn	POE	SPI	WD	Reset (Recovery) Method
$V_{VIN} < V_{IN(STOP)}$ and $V_{DD} < V_{DD(UV)}$	Device in power off; MRSTn = 0 (Reset IC)	Off	Off	Off	Off	Off	Off	Off	Off	Init. Low	Init. Low	Init. Low	Off	Off	Increase VIN
$V_{VIN} < V_{IN(STOP)}$ and $V_{DD} > V_{DD(UV)}$		Off	Off	Off	Off	Off	Off	Off	Off	Init. Low	Low	Low	On, no comms	Off	
VCP Undervoltage		UV	–	–	Off	Off	Off	Off	Off	High	– [4]	– [4]	On, no comms	– [4]	Remove UV factor
VREG Undervoltage	If $V_{VIN} > V_{VIN(START)}$	Off	UV	Off	Off	Off	Off	Off	Off	High	– [4]	– [4]	On, no comms	– [4]	Remove UV factor
VUC Undervoltage		–	–	–	UV	–	–	–	–	High	Low	Low	On, no comms	Off	Remove UV factor
VLDOC Undervoltage	FAULT_KEY: VLDOC_UV does not affect RESETn	–	–	–	–	–	–	UV	–	High	–	–	–	–	Remove UV factor
	FAULT_KEY (default setting): VLDOC_UV affects RESETn	–	–	–	–	–	–	UV	–	High	Low	Low	–	Off	Remove UV factor
VLDOB Undervoltage	FAULT_KEY: VLDOB_UV does not affect RESETn	–	–	–	–	–	UV	–	–	High	–	–	–	–	Remove UV factor
	FAULT_KEY (default setting): VLDOB_UV affects RESETn	–	–	–	–	–	UV	–	–	High	Low	Low	–	Off	Remove UV factor
VCORMON Undervoltage	FAULT_KEY: VCORMON_UV does not affect RESETn	–	–	–	–	–	–	–	–	High	–	Low	–	–	Remove UV factor
	FAULT_KEY (default setting): VCORMON_UV affects RESETn	–	–	–	–	–	–	–	–	High	Low	Low	–	Off	Remove UV factor
VLDOA Undervoltage		–	–	–	–	UV	–	–	–	High	–	–	–	–	Remove UV factor
VLDOP Undervoltage		–	–	–	–	–	–	–	UV	High	–	–	–	–	Remove UV factor
BOOT1 Undervoltage		Off	Off	Off	Off	Off	Off	Off	Off	High	– [4]	– [4]	On, no comms	– [4]	Remove UV factor
BOOT2 Undervoltage	Hiccup mode	Off	Off	Off	Off	Off	Off	Off	Off	High	– [4]	– [4]	On, no comms	Off	Remove UV factor
VIN Overvoltage	FAULT_KEY (default setting): VIN_OV results in FAILSAFE	Off	Off	Off	Off	Off	Off	Off	Off	High	Low	Low	On, no comms	Off	Remove OV factor
	FAULT_KEY: Inform the MCU of VIN OV	–	–	–	–	–	–	–	–	High	–	–	–	–	Remove OV factor
VCP Overvoltage	Charge pump in pulse skipping mode	OV	–	–	–	–	–	–	–	High	–	–	–	–	Remove OV factor
VREG Overvoltage	VREG results in FAILSAFE	Off	Off	Off	Off	Off	Off	Off	Off	High	Low	Low	On, no comms	Off	Remove OV factor
VUC Overvoltage	FAULT_KEY (default setting): VUC_OV results in FAILSAFE	Off	Off	Off	Off	Off	Off	Off	Off	High	Low	Low	On, no comms	Off	Remove OV factor
	FAULT_KEY: VUC_OV results in reset of MCU	–	–	–	OV	–	–	–	–	High	Low	Low	–	Off	Remove OV factor
VUC_AMR_OV	Inform the MCU via FF bit, and set VUC_AMR_F bit high; when VUC transition is faster than $t_{d(Vx,OV)}$	–	–	–	OV	–	–	–	–	High	–	Low	–	Off	Remove OV factor
VLDOA Overvoltage	FAULT_KEY (default setting): VLDOA_OV results in FAILSAFE	Off	Off	Off	Off	Off	Off	Off	Off	High	Low	Low	On, no comms	–	Remove OV factor
	FAULT_KEY: VLDOA_OV forces FF high	–	–	–	–	OV	–	–	–	High	–	–	–	–	Remove OV factor

[1] "–" = no effect; output pin or function is not directly affected by the fault.
[2] "On, no comms" = the SPI circuits are powered up but cannot communicate because the MISO pin needs VUC to function.
[3] "Latch Off" = PWM switching and all LDOs are turned off via a latch. To reset the latch, cycle VIN or toggle ENx.
[4] "–" = no direct effect, but subsequent faults, such as VUC (MCU shutdown) or WD fault sets this pin low

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Table 2: Fault Modes Operation (continued)

Fault	Description or SPI Configuration		VCP	VREG	WSI	VUC	VLDOA	VLDOB	VLDOC	VLDOP	SPI FF	RESETn	POE	SPI	WD	Reset (Recovery) Method
VLDOB Overvoltage	FAULT_KEY (default setting): VLDOB_OV results in FAILSAFE		Off	Off	Off	Off	Off	Off	Off	Off	High	Low	Low	On, no comms	–	Remove OV factor
	FAULT_KEY: VLDOB_OV results in reset of MCU		–	–	–	–	–	OV	–	–	High	–	–	–	–	Remove OV factor
VLDOC Overvoltage	FAULT_KEY (default setting): VLDOC_OV results in FAILSAFE		Off	Off	Off	Off	Off	Off	Off	Off	High	Low	Low	On, no comms	Off	Remove OV factor
	FAULT_KEY: VLDOC_OV results in reset of MCU		–	–	–	–	–	–	OV	–	High	Low	Low	–	Off	Remove OV factor
VCORMON Overvoltage	FAULT_KEY (default setting): VCORMON_OV results in FAILSAFE if VCORMON_EN = 1		Off	Off	Off	Off	Off	Off	Off	Off	High	Low	Low	On, no comms	Off	Remove OV factor
	FAULT_KEY: VCORMON_OV results in RESET of MCU if VCORMON_EN = 1		–	–	–	–	–	–	–	–	High	Low	Low	–	Off	Remove OV factor
VLDOP Overvoltage			–	–	–	–	–	–	–	OV	High	–	–	–	–	Remove OV factor
BOOT1 Overvoltage	Latch Off		Off	Off	Off	Off	Off	Off	Off	Off	Init. Low	– [4]	– [4]	On, no comms	– [4]	Toggle enable pin
BOOT2 Overvoltage	Latch Off		Off	Off	Off	Off	Off	Off	Off	Off	Init. Low	– [4]	– [4]	On, no comms	– [4]	Toggle enable pin
VREG Short-to-Ground	VREG in Hiccup mode		Off	OC	Off	Off	Off	Off	Off	Off	High	– [4]	– [4]	On, no comms	– [4]	Remove short-to-ground factor
VUC Overcurrent	VUC OC threshold		–	–	–	OC	–	–	–	–	High	–	–	–	–	Remove short-to-ground factor
VLDOA Overcurrent	VLDOA OC threshold		–	–	–	–	OC	–	–	–	High	–	–	–	–	Remove short-to-ground factor
VLDOB Overcurrent	VLDOB OC threshold		–	–	–	–	–	OC	–	–	High	–	–	–	–	Remove short-to-ground factor
VLDOC Overcurrent	VLDOC OC threshold		–	–	–	–	–	–	OC	–	High	–	–	–	–	Remove short-to-ground factor
VLDOP Overcurrent	VLDOP OC threshold		–	–	–	–	–	–	–	OC	High	–	–	–	–	Remove short-to-ground factor
LX1 Short-to-Ground	$V_{VIN} > V_{VIN(START)}$: Hiccup mode after 4× $f_{SW(VREG)}$		Off	LX1 STG	Off	Off	Off	Off	Off	Off	High	– [4]	– [4]	On, no comms	– [4]	Remove short-to-ground factor
	$V_{VIN} < V_{VIN(START)}$		Off	Off	Off	Off	Off	Off	Off	Off	High	– [4]	– [4]	On, no comms	– [4]	Remove short-to-ground factor
LX2 Short-to-Ground	$V_{VIN} > V_{VIN(START)}$: Hiccup mode after 4× $f_{SW(VREG)}$		Off	LX2 STG	Off	Off	Off	Off	Off	Off	High	– [4]	– [4]	On, no comms	– [4]	Remove short-to-ground factor
	$V_{VIN} < V_{VIN(START)}$		Off	Off	Off	Off	Off	Off	Off	Off	High	– [4]	– [4]	On, no comms	– [4]	Remove short-to-ground factor
VCP Short-to-Ground	VCP high current and fusing, no LDO drive		UV	–	–	Off	Off	Off	Off	Off	–	– [4]	– [4]	On, no comms	– [4]	Replace the IC
Watchdog Fault	FAULT_KEY (default setting): WD_FAULT does NOT affect RESETn	WSI_WD_CONFIG = 0	–	–	–	–	–	–	–	–	High	–	Low	–	Off	Input proper WD feedback
		WSI_WD_CONFIG = 1	–	–	Off	–	–	–	–	–	High	–	Low	–	Off	Input proper WD feedback
	FAULT_KEY: WD_FAULT affects RESETn	WSI_WD_CONFIG = 0	–	–	–	–	–	–	–	–	High	–	Low	–	Off	Input proper WD feedback
		WSI_WD_CONFIG = 1	–	–	Off	–	–	–	–	–	High	Low 2 ms	Low	–	Off	Input proper WD feedback

[1] "–" = no effect; output pin or function is not directly affected by the fault.
[2] "On, no comms" = the SPI circuits are powered up but cannot communicate because the MISO pin needs VUC to function.
[3] "Latch Off" = PWM switching and all LDOs are turned off via a latch. To reset the latch, cycle VIN or toggle ENx.
[4] "–" = no direct effect, but subsequent faults, such as VUC (MCU shutdown) or WD fault sets this pin low

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Table 2: Fault Modes Operation (continued)

Fault	Description or SPI Configuration	VCP	VREG	WSI	VUC	VLDOA	VLDOB	VLDOC	VLDOP	SPI FF	RESETn	POE	SPI	WD	Reset (Recovery) Method
ERRORn Fault	Active low mode (ERRORN_SEL = 0)	–	–	–	–	–	–	–	–	–	–	Low	–	–	Input proper ERRORn signal
	Toggling mode (ERRORN_SEL = 1) with ERRORN_REC_SEL = 0	–	–	–	–	–	–	–	–	–	–	Low	–	–	Input proper ERRORn signal
	Toggling mode (ERRORN_SEL = 1) with ERRORN_REC_SEL = 1	–	–	–	–	–	–	–	–	High	–	Low	–	–	Input proper ERRORn signal
ABIST Fault	Set POE low, MCU reads	–	–	–	–	–	–	–	–	High	–	Low	–	–	Restart/Replace the IC
LBIST Fault	Inform the MCU and set POE low	–	–	–	–	–	–	–	–	High	–	Low	–	–	Restart/Replace the IC
EEPROM Fault	Inform the MCU and set POE low	–	–	–	–	–	–	–	–	High	–	Low	–	–	Restart/Replace the IC
Internal Logic Error	Inform the MCU and set POE low	–	–	–	–	–	–	–	–	High	–	Low	–	–	Replace the IC
SE Fault	Inform the MCU	–	–	–	–	–	–	–	–	High	–	–	–	–	Replace the IC
SPI CSn Timeout	Inform the MCU	–	–	–	–	–	–	–	–	High	–	–	–	–	Restore communications with device
POEx/RESETn Stuck Low/High	Inform the MCU	–	–	–	–	–	–	–	–	High	–	–	–	–	Remove external fault or replace the IC
Master Clock Stuck High or Low	Shutdown	Off	Off	Off	Off	Off	Off	Off	Off	Init. Low	Low	Low	Off	Off	Replace the IC
PWM Clock Stuck High or Low	VREG shutdown	– [4]	Off	– [4]	– [4]	– [4]	– [4]	– [4]	– [4]	High	– [4]	Low	On, no comms	– [4]	Replace the IC
One Clock Out of Range	If the clock is beyond ±15% the nominal value, inform the MCU	–	–	–	–	–	–	–	–	High	–	Low	–	–	Replace the IC
L_{VREG} Missing	VREG cannot start	Off	UV	Off	Off	Off	Off	Off	Off	High	– [4]	– [4]	On, no comms	– [4]	Replace missing component
C_{PUMP} Missing	VCP_UV, no LDO bias	UV	–	–	Off	Off	Off	Off	Off	High	– [4]	– [4]	On, no comms	– [4]	Replace missing component
C_{VCP} Missing	VCP_UV, no LDO bias	UV	–	–	Off	Off	Off	Off	Off	High	– [4]	– [4]	On, no comms	– [4]	Replace missing component
L_{VREG} Shorted	LX1 fault, Hiccup mode after 2× $f_{SW(VREG)}$	Off	LX1 STG	Off	Off	Off	Off	Off	Off	High	– [4]	– [4]	On, no comms	– [4]	Remove short circuit and toggle VIN or ENx
C_{PUMP} Shorted	VCP_UV, no LDO bias	UV	–	–	Off	Off	Off	Off	Off	High	– [4]	– [4]	On, no comms	– [4]	Remove short circuit. Replace the IC.
C_{VCP} Shorted	VCP_UV, no LDO bias	UV	–	–	Off	Off	Off	Off	Off	High	– [4]	– [4]	On, no comms	– [4]	Remove short circuit. Replace the IC.
Thermal Warning	Inform the MCU	–	–	–	–	–	–	–	–	High	–	–	–	–	IC cool down
Thermal Shutdown (TSD)	Stop PWM	Off	Off	Off	Off	Off	Off	Off	Off	High	– [4]	Low	On, no comms	– [4]	IC cool down

[1] "–" = no effect; output pin or function is not directly affected by the fault.
[2] "On, no comms" = the SPI circuits are powered up but cannot communicate because the MISO pin needs VUC to function.
[3] "Latch Off" = PWM switching and all LDOs are turned off via a latch. To reset the latch, cycle VIN or toggle ENx.
[4] "–" = no direct effect, but subsequent faults, such as VUC (MCU shutdown) or WD fault sets this pin low

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Table 3: WSS IF Fault

Fault	Description or SPI Configuration	WSIL_SWITCH	WSIH_SWITCH	SPI FF	RESETn	POEx	SPI	WD	Reset (Recovery) Method
WSIS_UV		Off	Off	High	–	–	–	–	
WSIL_STG_F		(Off)	Off	High	–	–	–	–	Detection available when WSIL is disabled. Remove STG factor, clear the SPI flag, and set both WSIH_EN and WSIL_EN SPI bits.
WSIH_OVC_F	Forward current limitation active	–	Off	High	–	–	–	–	Remove the STG factor, clear the SPI flag, and set WSIH_EN SPI bits.
WSIL_OVC_F	Forward current limitation active	Off	Off	High	–	–	–	–	Remove the STB factor, clear the SPI flag, and set both WSIH_EN and WSIL_EN SPI bits.
WSIH_REVERSE_BAT_F	Reverse current blocked	–	Off	High	–	–	–	–	Check WSIS connection and set WSIL_EN SPI bits.
WSIL_REVERSE_GND_F	Reverse current blocked, internal pullup activated	Off	Off	High	–	–	–	–	Remove STG factor clear the SPI flag, and set both WSIH_EN and WSIL_EN SPI bits.
WSI_EXCESSIVE_OFFSET_F		–	–	High	–	–	–	–	
WSI_OPEN_CUR_F		–	–	High	–	–	–	–	
WSI_ITH2_GZ / ITH2_EXCEED_F		–	–	High	–	–	–	–	
WSI_ITH1_GZ_F		–	–	High	–	–	–	–	
VDA_ERR_F		–	–	High	–	–	–	–	
WSI_TWARN_F		–	–	High	–	–	–	–	
WSI_TSD_F		Off	Off	High	–	–	–	–	IC cool down, clear the SPI flag, and set both WSIH_EN and WSIL_EN SPI bits.

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FUNCTIONAL DESCRIPTION

Overview

The A81415 is a power management IC designed for safety-critical applications. It contains one switching regulator, five linear post-regulators, and one wheel speed sensor interface.

The A81415 pre-regulator uses a synchronous buck-boost converter topology. This pre-regulator generates a fixed 5.7 V (VREG) and can deliver up to 1.25 A to power the internal post-regulators and external ICs. The post regulators generate the various voltage levels for the end system.

Power Up and Power Down

The A81415 is powered up as soon as one of the enable pin (ENx) is high and the VIN voltage is above the UVLO upper threshold. Power-up sequence is shown in Figure 6. If during the power-up sequence none of the enable pins stay high for a time longer than their deglitch filter time, the device is switched off immediately.

If the enable deglitch filter time is exceeded, the enable is latched and the device is not powered down when any of the ENx pin are forced low.

During normal operation, if the MCU forces the RESETn pin low for more than $t_{RESETn(UNLATCH)}$ or a watchdog fault lasts more than $t_{RESETn(UNLATCH)}$, the latch on ENx pins is removed.

The power-down sequence starts when all the ENx pins are low and the MCU sends the SPI command to clear the enable signals latches.

During any states, the device is powered down as soon as the VIN UVLO lower threshold is detected.

Pre-Regulator (VREG)

The pre-regulator incorporates four internal switches. An external inductor and output capacitors are required to complete the buck-boost converter.

The pre-regulator provides many protection and diagnostic functions.

- Pulse-by-pulse and hiccup mode current limit
- Undervoltage and overvoltage detection and reporting
- Shorted switch node to ground protection
- High voltage rating for load dump

The switching frequency is fixed at 2.2 MHz typical and it is decreased to 1.1 MHz (typical) if V_{VIN} is increased above 19 V, while it is changed back to 2.2 MHz as soon as V_{VIN} is decreased below 18 V on VIN.

Internal Bias Supply (VDRV, VPOSA, VPOSMON, VDD)

The internal bias supplies are generated by internal linear regulators. These supplies are the first rails to start up as soon as the VIN and one ENx pin are high and during power-up they are supplied directly from VIN. Most of the internal control circuitry are powered by these supplies. The bias supplies include some unique features to ensure safe operation of the A81415. These features include:

- VIN input undervoltage lockout
- Overvoltage and undervoltage detection
- Dual input operation: VIN or VREG, for low-battery voltage operation

Crossover Switches

The A81415 incorporates the crossover switch feature, which changes the input supply of internal regulators from VIN to VREG and vice versa.

Once the VREG pre-regulator is in regulation ($V_{VREG} > V_{VREG(UV,H)}$), the crossover switch changes the input supply from VIN to VREG pre-regulator output. If for any reason, V_{VREG} goes lower than $V_{VREG(UV,L)}$, the input supply is switched back to VIN.

BOOT Circuits (BOOT1, BOOT2)

Two boot circuits provide the voltage necessary to drive the two high-side N-channel MOSFETs in the pre-regulator. Each boot circuit requires an external 0.1 µF capacitor to ensure correct operation.

Charge Pump (VCP)

The A81415 incorporates a charge pump circuit, VCP. This circuit provides bias voltage for the linear post regulators.

Two external capacitors are required for charge pump operation. The charge pump is only active when VREG is above its UV threshold.

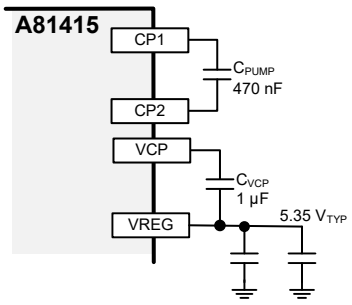

Figure 15: Charge Pump Connections

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During the first cycle of the charge pump, the flying capacitors, C_{PUMP}, is charged from VREG. During the second cycle, the voltage on the flying capacitor charges a reservoir capacitor, C_{VCP}. The charge pump incorporates some safety features:

- Undervoltage and overvoltage detection and reporting
- Overcurrent safe mode protection

Bandgaps (BG1, BG2)

Dual bandgaps are implemented within the A81415. One bandgap is dedicated to the voltage regulation loops within each of the regulators, VCP, VREG and the five post regulators. The second is dedicated to the undervoltage and overvoltage monitoring functions of all the regulators. This improves safety coverage and fault reporting from the A81415.

Should the regulation bandgap fail, then the output voltages is out of specification and the monitoring bandgap reports the fault.

If the monitoring bandgap fails, the output voltages remain in regulation, but the monitoring circuits report the outputs as out of specification and trip the fault flag.

The bandgap circuits include two smaller, secondary bandgaps that are used to monitor the undervoltage state of the main bandgaps.

Enable I/O (ENCOM, ENBAT)

Two enable input pins are available on the A81415. The two enable pins ENBAT and ENCOM are battery-level rated and can be connected to the ignition switch through a low-pass filter.

As soon as at least one of these pins is forced high, the internal regulators are activated and the power-up sequence is initiated. If the ENBAT pin is high at end of the $t_{d(ENBAT)}$ filter time, after the internal ABIST/LBIST, the ENBAT_LAT signal is latched to 1 automatically, while the ENCOM_LAT is latched to 1 automatically if ENCOM is high at the end of the $t_{d(ENCOM)}$ filter time. Once the power-up sequence is completed and the MCU reset has been released (RESETn high), the MCU can decide to latch to 1 or clear the latch of the ENBAT_LAT and/or ENCOM_LAT signals by SPI command. In this way the MCU is able to control when the power-down sequence must be started independently on the ENCOM and ENBAT signal status.

Table 4: Truth Table for Enable Inputs

ENCOM	ENBAT	ENCOM_LAT	ENBAT_LAT	ENB
0	0	0	0	0
1	x	x	x	1
x	1	x	x	1
x	x	1	x	1
x	x	x	1	1

Linear Regulators

The A81415 has five linear regulators: one (VUC) that provides 3.3 V or 5 V based on VUCSEL pin, one fixed at 5 V (or 3.3 V factory option, VLDOA), one programmed at 5 V that can be disabled via SPI (VLDOB), one fixed at 5 V (VLDOC), and one short-to-battery protected regulators (VLDOP) programmed (5 V or 3.3 V or VLDOC tracking) and enabled via SPI.

The pre-regulator supplies 5.7 V (VREG) to the linear regulators, which reduces power dissipation and temperature.

A separate input to the VUC regulator (VUCIN) is provided to allow the use of an external voltage dropping resistor. This helps reduce power dissipation in the A81415 when VUC is set to 3.3 V. The suggested value for this external resistor is 1.7 V / $I_{VUC(max)}$, where $I_{VUC(max)}$ is the maximum current load on VUC.

VUCSEL is monitored and latched at the end of VREG power-up. This pin also includes an internal pulldown resistor. If pin is open, the VUC voltage will be set to 3.3 V. If the pin opens while operating, the VUC voltage will be unaffected. The VUCSEL pin also has one redundant and identical input buffer to assure the right selection of the VUC voltage. The output signals of the two buffers are compared right before latching the value. If the two output buffer values match, then the VUCSEL value is latched; otherwise, VUC and VLDOA are not enabled. If the two output signals no longer match after the latch, only SPI bit (VUCSEL_F) is set, so LDOs are not turned off.

All linear regulators provide the following protection features:

- Current limit with foldback
- Overcurrent detection and reporting
- Undervoltage and overvoltage detection and reporting

Fault Detection and Reporting (RESETn, POE1, POE2)

There is extensive fault detection within the A81415; most have been discussed previously. There is one fault reporting mechanism used by the A81415 through serial communications interface (SPI).

Three hardwire pins are used for fault reporting. The first pin, RESETn (open drain with internal pull-up, active low), reports on the status of the VUC and VLDOC outputs. By default, this signal transitions low only if VUC is out of regulation (UV or OV), or VLDOC is too high (OV), or VCORE is too high (OV) or VREG is too high (OV). However, options are available via SPI configuration to:

- Respond to a Watchdog Fault by setting RESETn low for 2 ms to reset the MCU

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- Indicate if VLDOC is too low (UV)
- Report if VIN is too high (OV)
- Indicate if VCORMON is too low (UV)
- Indicate if VLDOB is too low (UV)

These additional reporting options are selectable through SPI using the RESETn_KEY or mask bits. See registering mapping for details. Figure 16 shows the logic setup for the RESETn signal.

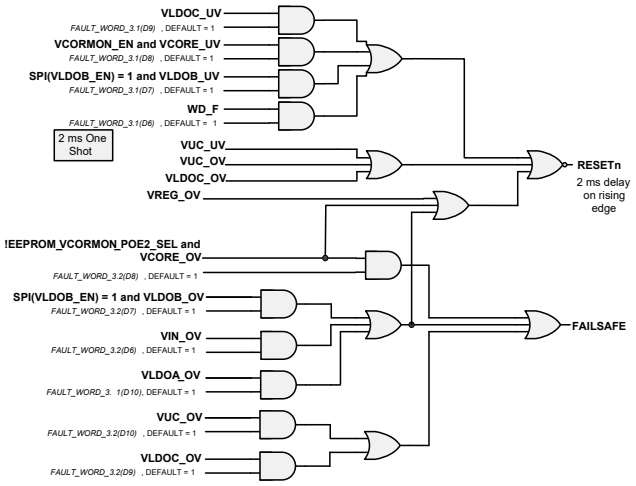

Figure 16: RESETn and Failsafe Generation Logic

The other two fault flag pins are power-on enable pins, POE1 and POE2, and are safe-state flags. These report faults are seen on the watchdog circuits or ERRORn pin. These faults signal a bad processor. The POEx pins should be used to put the system in a safe state. These pins are an open-drain output, with internal pull-up resistor. The A81415 continuously monitors the state of these pins and compares it to the demanded states.

The ERRORn input allows the user to feed other safe state signals into the A81415 and set POEx low. If ERRORn is not used, it shall be connected to VUC and disabled via ERRORn_DIS SPI bit.

The ERRORn input can be configured to accept a level-state signal setting the ERRORN_SEL SPI bit to 0. In this case, POEx is pulled low when ERRORn signal transitions low, and is released when it transitions high.

Alternatively, ERRORn can be configured to accept a frequency signal setting ERRORn_SEL SPI bit to 1. In this case, the MCU shall constantly provide a square wave signal with a frequency in the 10 to 45 kHz range to the ERRORn pin. If the frequency of the received signal is higher or lower than the accepted frequency range, internal ERRORn state is qualified low and POEx outputs are pulled low. An ERRORn recovery time can be configured to mask a frequency fault for 10 ms before pulling low POEx outputs. Figure 17 illustrates the POEx response to a LF and HF fault in the toggling ERRORn signal (a and b), and behavior of the recovery time with a LF fault (c and d).

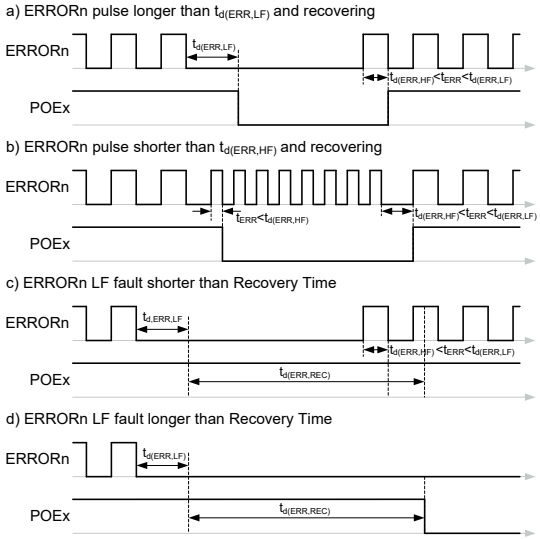

Figure 17: POEx response to toggling ERRORn signal

The POEx outputs are continuously controlled, and if the output does not match the control signal, the POE1_ERR and POE2_ERR faults are triggered.

The whole safety control logic is implemented in an isolated portion of the die to minimize the impact of a chip damage on the safety outputs. Every logic signal interacting with the safety block is protected from a short-to-VBAT fault; moreover, every supply line is internally clamped.

The complete logic that controls the POEx signals when ERRORN_SEL = 0 is reported in Figure 18.

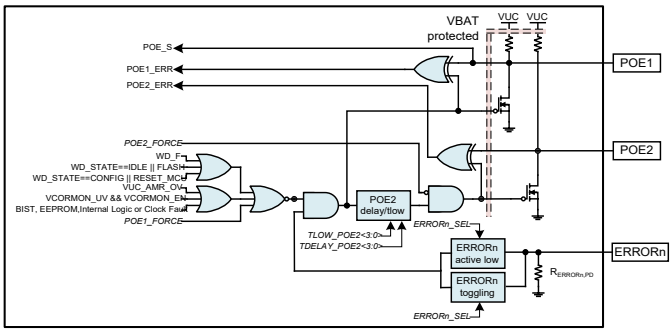

Figure 18: POEx Control Logic Diagram

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POE2 can be configured to go down after a configurable delay $t_{d(POE2)}$; it can also be configured to automatically toggle up after a configurable delay $t_{low(POE2)}$ from the previous falling edge, as showed in Figure 19.

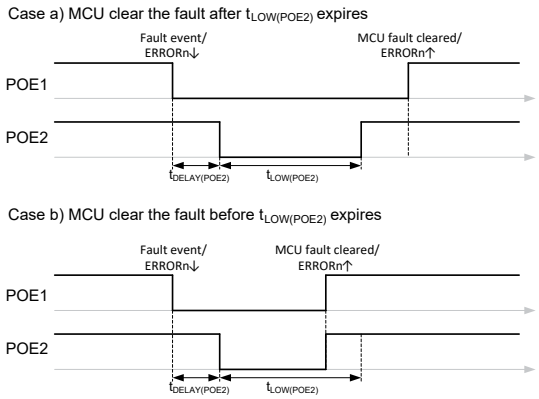

Figure 19: POEx Timing Diagram

Built-In Self Tests

The A81415 includes an analog (ABIST) and a logic (LBIST) built-in self-tests which are performed only during the startup sequence. The ABIST verifies the operation of the undervoltage and overvoltage monitor circuits for the main outputs and the overtemperature shutdown circuitry. It also includes self-testing of the RESETn and POE fault generation circuits. The LBIST performs on the chip logic, state machine and registers, including the watchdog circuits.

At startup, LBIST is performed after the ENBAT or ENCOM filtered signal is high (after $t_{d(ENBAT)}$ or $t_{d(ENCOM)}$). Once LBIST is completed, the ABIST is performed. After the completion of the ABIST, the VREG and the LDOs start.

The MCU must read the verification register and clear any faults. Also, the MCU can verify if BIST passed by reading the relevant bits in the verification registers.

In the event the self-test fails, the A81415 reports the failure through SPI.

Undervoltage Detect Self-Test

The undervoltage (UV) detection circuits are verified during startup of the A81415. A voltage that is lower than the undervoltage threshold is applied to each UV comparator; this should cause the corresponding undervoltage bit in the diagnostic register to change state: 0→1, indicating a fault. If a diagnostic UV register bit does not change state, the corresponding verify result bit is latched high. So, when testing is complete, if any bits in the verify result registers are high, then verification has failed. The following UV comparators are tested: VREG, VUC, VLDOA, VLDOB, VLDOP, and VCP.

Overvoltage Detect Self-Test

The overvoltage (OV) detection circuits are verified during startup of the A81415.

A voltage that is higher than the overvoltage threshold is applied to each OV comparator; this should cause the corresponding overvoltage bit in the diagnostic register to change state: 0→1, indicating a fault. If a diagnostic OV register bit does not change state, the corresponding verify result register bit is latched high. So, when testing is complete, if any bits in the verify result registers are high then verification has failed. The following OV comparators are tested: VREG, VUC, VLDOA, VLDOB, VLDOP, VIN, and VCP.

Overtemperature Shutdown Self-Test

The overtemperature shutdown (TSD) detector is verified during startup of the A81415.

A voltage that is higher than the overvoltage threshold is applied to the TSD comparator; this should cause the overtemperature bit in the diagnostic register to change state: 0→1, indicating a fault. If the TSD register bit does not change state, the TSD verify result register bit is latched high. So, when testing is complete, if the TSD bit in the verify result registers is high, then verification has failed.

Power-On Enable (POE) Self-Test

The A81415 incorporates continuous self-testing of the power-on enable (POEx) outputs. It compares the status of the POEx pin (POE_S) with the internal expected status. If they differ for any reason, the FF SPI bit is set high and POE_ERR in the status register is set high.

Core Voltage Monitor (VCORMON)

The A81415 integrates a pin intended for analog monitoring of the MCU core voltage (VCORMON). The VCORMON function is enabled by default for selected part numbers (via EEPROM bit) and cannot be enabled or disabled via SPI.

During device operation, the MCU core voltage is constantly monitored for OV/UV faults. While the UV threshold is fixed, the OV threshold can be programmed via SPI using the configuration register 1 field VCORMON_OV_SEL.

A VCORMON_UV fault triggers the pull-down of the POE1 outputs; an additional SPI configuration using the FAULT_KEYs configures the device to pull-down, and the RESETn output in response to the UV fault (Figure 13).

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A VCORMON_OV fault always triggers the pull-down of the RESETn pin; an additional SPI configuration using the FAULT_KEYs configures the device to enter FAILSAFE state in case of OV fault (Figure 14). Both additional UV/OV fault responses configurable via SPI FAULT_KEYs are active by default to guarantee complete voltage monitoring functionality from startup.

The selected part numbers with disabled VCORMON functionality do not react in any way to a VCORMON UV/OV fault, and the pin act as a second power-on enable (POE2).

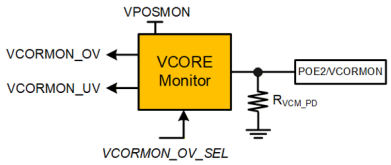

Figure 20

MCU Self-Reset

The MCU can self-reset in different ways, via externally pulling low the RESETn pin (see section Power Up and Power Down) or via MCU fault key, with word3 = 011xxxxx.

If the MCU pulls the RESETn pin low, then:

- The RESETN_MCU latched bit is set high.
- The enable unlatch timer, $t_{RESETn(UNLATCH)}$, starts.
- The WD state machines move to RESETn_LOW state where it waits for $t_{RESETn(UNLATCH)}$ and release of the RESETn pin.

If $t_{RESETN(UNLATCH)}$ expires and the MCU has released the RESETn pin, the WD state machine moves to CONFIG state.

The MCU must clear the RESETn_MCU bit because it controls POE during the CONFIG state.

WD configuration is not affected unless it was changed via SPI. WD configuration is latched again when the WD state machine leaves the CONFIG state.

If MCU sets the dedicated fault key, then:

- The RESETN_REQ latched bit is set high.
- The one-shot timer, $t_{MIN(RESETn\_LOW)}$, starts and RESETn pin is forced low by the A81415.
- The WD state machines moves to the RESETn_LOW state where it waits for $t_{RESETn(UNLATCH)}$ and release of RESETn pin.

If $t_{MIN(RESETN\_LOW)}$ expires, the WD state machine moves to CONFIG state.

The MCU must clear the RESETn_REQ bit because it controls POEx during CONFIG state.

WD configuration is not affected unless it was changed via SPI. WD configuration is latched again when the WD state machine leaves the CONFIG state.

Output Pin Checker

The device monitors the voltage directly on the RESETn, POE1, POE2, and WSIO pins in order to check if the pin status matches the internal signal value. If there is a mismatch between pin and internal signal, due to external or internal fault, then the corresponding SPI flag is set (DIAGNOSTIC_2 register 0x06 bit 12:15).

Watchdog

The A81415 contains three different watchdogs. The selection and configuration of each watchdog is done through SPI. After a watchdog is selected and running, it cannot be reconfigured without going through a secure SPI procedure. The watchdog circuits are updated/latched when the state machine leaves configuration mode. After leaving the CONFIG state, modifications to the watchdog registers do not take effect unless a CONFIG or RESTART command is issued.

The three types of watchdogs are:

- Pulse width watchdog (PWWD)
- Window watchdog (WWD)
- Q&A watchdog (QAWD) (default)

The Q&A watchdog is the default watchdog. It will automatically start with default settings if the following conditions are met:

- RESETn transitions high, and
- No watchdog is selected: WD_SEL(2:0) = [0,0,0], and
- The $t_{CONFIG(TO)}$ configuration timer expires.
  - The configuration timer can be forced to expire by selecting a watchdog, including QAWD, with the WD_SEL(2:0) bits.

The watchdog can be restarted by the microcontroller by sending either a RESTART or CONFIG command via the three-word WD_KEYs.

In case of a watchdog fault, POE is set low and the respective bit (WWD_F, QAWD_F or PWWD_F) in diagnostic register is latched high.

By default, a watchdog fault does not affect RESETn. However, at any time, the microcontroller can configure the device by SPI to force RESETn low after a watchdog fault. This is accomplished by writing three secure words to the SPI RESETn_KEY register. In this case, a watchdog fault sets RESETn low for $t_{WD(FAULT)}$ (2 ms) to reset/restore the microcontroller.

When RESETn goes high after the toggle cycle, the $t_{CONFIG(WD)}$ timer starts. The MCU can reconfigure and select WD type by

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writing to WD_SEL(2:0) to ensure proper synchronization, especially of Q&A Watchdog. If WD_SEL(2:0) is not written and $t_{CONFIG(WD)}$ expires, then the WD configuration is latched when the state machine leaves the configuration mode.

Logic Built-In Self-Test (LBIST)

The logic for the watchdogs, fault reporting, registers, the EEPROM interface, and the SPI interface are verified with a logic built-in self-test (LBIST). A 26-bit linear feedback shift register (LFSR) exercises internal scan chains for 16 milliseconds and a 26-bit multi-input signature register (MISR) compresses the results into a 26-bit signature. A logic error is detected if the calculated signature does not match the expected value.

While LBIST is active, inputs are ignored and outputs are frozen. For example, the A81415 does not respond to SPI transactions and faults are not recorded. When LBIST completes, the logic is reset and the shadow registers are again loaded from the on-chip EEPROM memory.

Pulse-Width Window Watchdog (PWWD)

The pulse width watchdog circuit monitors an external clock applied to the WD_IN pin. This clock should be generated by the primary microcontroller or DSP. The pulse-width window watchdog (PWWD) measures the time between two clock edges, either rising or falling. So the watchdog effectively measures both the high and low pulse widths, as shown in Figure 21. By default, the nominal WD_IN pulse width (PWWD_PW) is set to 1 ms, but can be modified to 0.5, 1.5, or 2 ms via SPI.

If an incorrect pulse width is detected, the watchdog increments its fault counter by 10 (default). If a correct pulse width is detected, the watchdog decrements its fault counter by 2 (default). If the watchdog fault counter exceeds 160 (default), then the POE pin transitions low. Operation of the PWWD is shown in Figure 21 and Figure 22. The increment value (PWWD_INC), decrement value (PWWD_DEC), and maximum fault count (PWWD_MAX) all have alternate values that can be accessed via SPI.

The watchdog default values are loaded when:

- The internal rails transitions low (i.e., VIN is removed, or ENCOM and ENBAT are both low), or
- the bandgap, BG1, transitions low.

Clock pulses from the microcontroller must be applied to WD_IN pin before the watchdog is selected (via WD_SEL) or restarted (via the three-word WD_KEY command). The PWWD error counter can be preloaded to a value set by PWWD_POE_DLY (default of 2). Preloading the error counter forces the microcontroller to send valid pulses before POE transitions high, effectively prequalifying the performance of the microcontroller. Figure 21 and Figure 22 demonstrate prequalification with PWWD_POE_DLY set to a value of 10, which requires 5 valid clock pulses (–2 counts per valid clock pulse) before POE transitions high.

After moving into NORMAL operation, if no clock edges are detected at WD_IN for PWWD_EDGE_TO, the POE pin transitions low. By default, PWWD_EDGE_TO is 5 ms, but can be modified to 2.5, 10, or 15 ms via SPI. The edge timeout condition is shown as (1) in Figure 22.

While in the NORMAL state, if clock activity at WD_IN terminates for at least PWWD_ACT_TO, the POE pin transitions low. By default, PWWD_ACT_TO is 16 ms, but can be modified to 8, 24, or 32 ms via SPI. The loss of clock activity condition is shown as (2) in Figure 22.

The pulse widths generated by a microcontroller or DSP depend on many factors and have some pulse-to-pulse variation. The A81415 accommodates pulse width variations by allowing the designer to select a window of allowable variations. By default, the window tolerance (PWWD_WIN_TOL) is set to ±13%, but can be modified to ±8, ±18, and ±23 percent via SPI.

The watchdog performs its calculations based on an internally generated clock. The internal clock typically has an accuracy of ±2.5% at 25°C but may vary as much as ±5% due to IC process shifts and temperature variations. Variations in the watchdog clock result in a shift of the OK Region (i.e., the expected pulse width) at WD_IN.

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PULSE-WIDTH WINDOW WATCHDOG (PWWD) TIMING DIAGRAMS

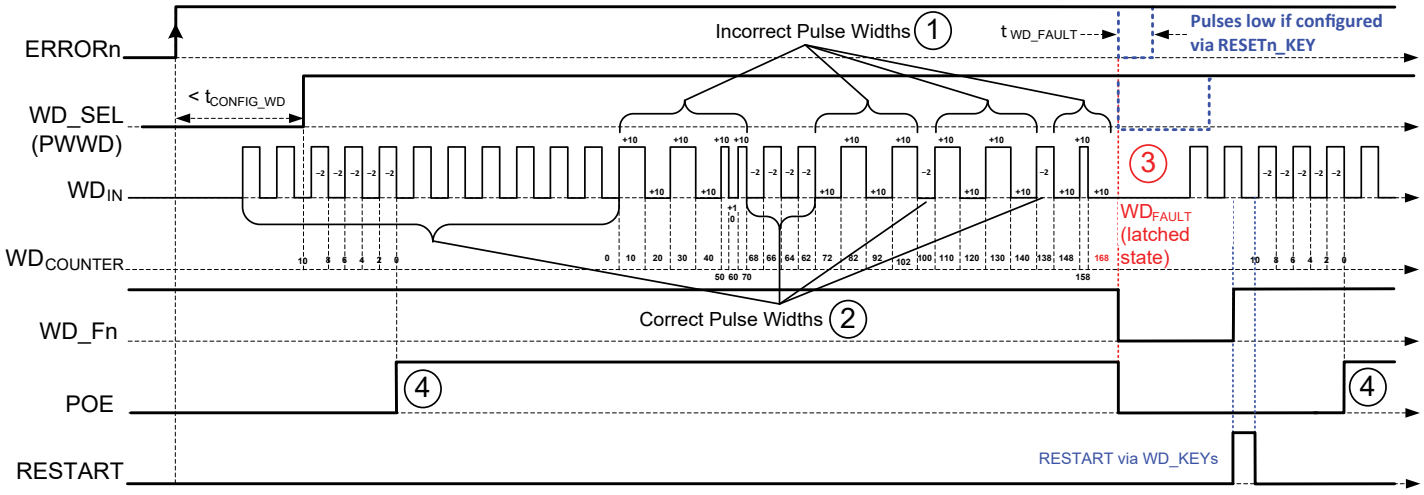

Figure 21: Watchdog (WD) operation with both correct and incorrect pulse widths

1. Incorrect pulse widths increment the WD counter by 10.
2. Correct pulse widths decrement the WD counter by 2.
3. A WD fault occurs if the total fault count exceeds 160.
4. PWWD_POE_DLY is set to 10. So, 5 valid pulse widths (10 ÷ 2 counts per valid pulse) are required before POE transitions high.

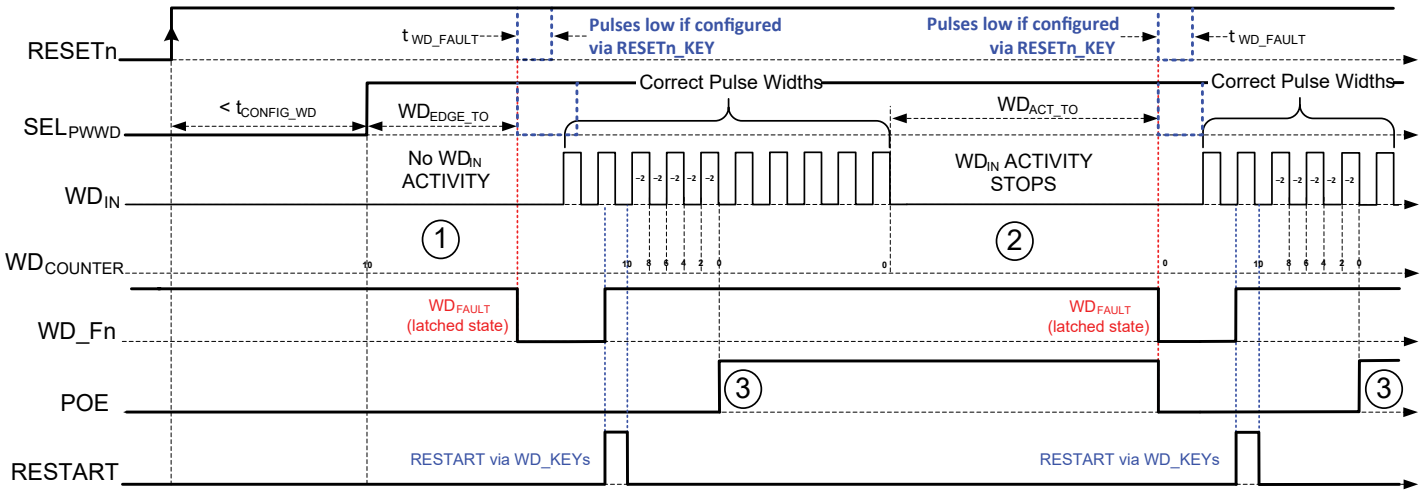

Figure 22: Watchdog operation with faults

1. No WD_IN activity for $t_{WDEDGE(TO)}$.
2. WD_IN activity stops.
3. PWWD_POE_DLY is set to 10. So, 5 valid pulse widths (10 ÷ 2 counts per valid pulse) are required before POE transitions high.

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Window Watchdog (WWD)

The window watchdog monitors the time between rising edges of an external clock applied to the WD_IN pin. This clock should be generated by the microcontroller or DSP. The time between rising edges (i.e., the frequency) of the clock must fall within an acceptable window, or a watchdog fault is generated. In general, valid watchdog clocks must be present at WD_IN for at least $t_{WD(SLOW)}$ before POE will transition high.

After RESETn transitions high, the processor must:

- Program the configuration registers WWD_TIMER(3:0) to select and initiate valid WD pulses on the WD_IN pin and,
- Select the WWD by setting WD_SEL(2:0) = [010] or [011].

Both these tasks must be completed before $t_{CONFIG(WD)}$ expires.

Initiate valid WD pulses on the WD_IN pin. It is strongly recommended that the processor produce valid clock pulses at WD_IN prior to selecting the watchdog or issuing the RESTART command.

A window watchdog fault occurs if the time between rising clock edges is either too short (a fast fault) or too long (a slow fault). If a WD fault occurs, then the POE signal is driven low. The WWD_F bit in diagnostic register is latched high. RESETn toggles for 2 ms if selected.

Valid watchdog clocks should be present at WD_IN pin for at least $t_{WD(SLOW)}$ before POE is allowed to transition high. This prequalifies correct operation of the microcontroller before enabling the gate driver (via POE). At least 1 complete clock cycle must occur during the prequalification time ($t_{WD(SLOW)}$). For prequalification, the maximum WD_IN clock frequency ($f_{WD\_IN(MAX)}$) and the selected value of WWD_TIMER(3:0) must satisfy the following equation.

Equation 1:

$$t_{WWD(SLOW)} > \frac{1.5}{f_{WD_{IN}(MAX)}}$$

Minimum and maximum values of the $t_{WWD(SLOW)}$ and $t_{WWD(FAST)}$ parameters depends on the tolerance of the internal clock frequency ($f_{CLOCK(TOL)}$). Starting from this value in %, the tolerance of $t_{WWD(SLOW)}$ and $t_{WWD(FAST)}$ can be calculated by the following equations.

Equation 2:

$$t_{WWD\_X(TOL)}\Big|_{max} = \frac{100}{100 - f_{CLOCK(TOL)}} - 1$$

Equation 3:

$$t_{WWD\_X(TOL)}\Big|_{min} = \frac{100}{100 + f_{CLOCK(TOL)}} - 1$$

Typical watchdog operation with both FAST and SLOW fault events, along with recommended RESTART conditions, are shown in Figure 23 and Figure 24.

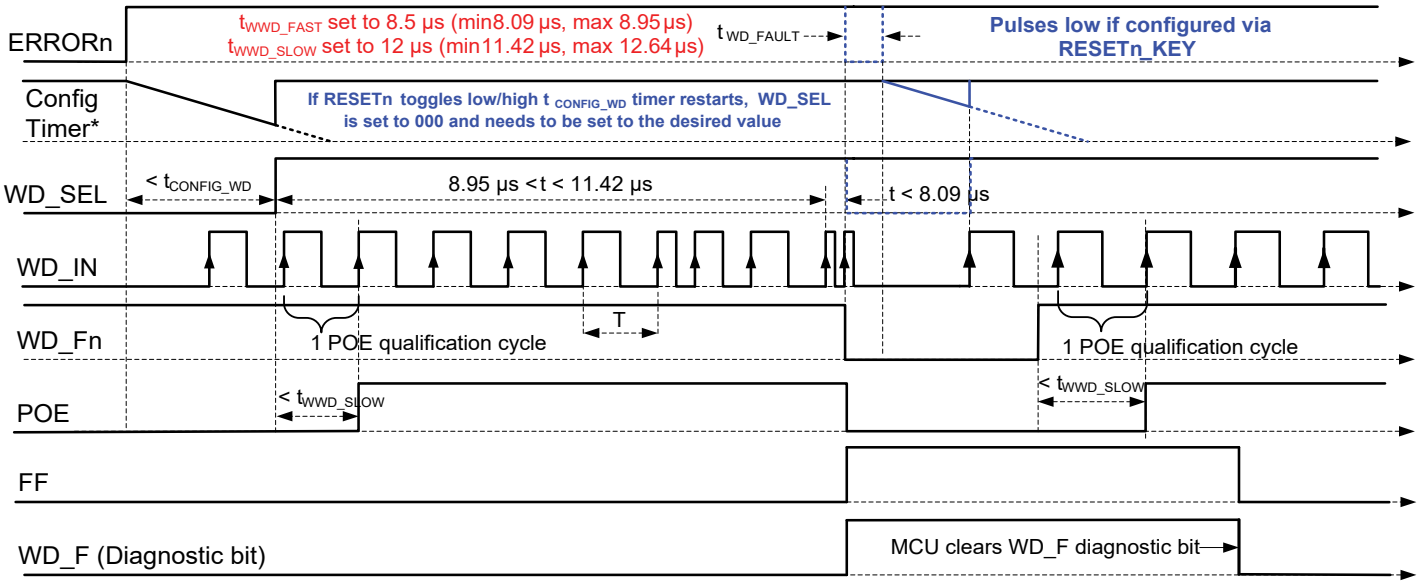

Figure 23: Window Watchdog (WWD) Operation

A watchdog fault occurs when the WD_IN period (T) is too short. * Signal is internal to A81415.

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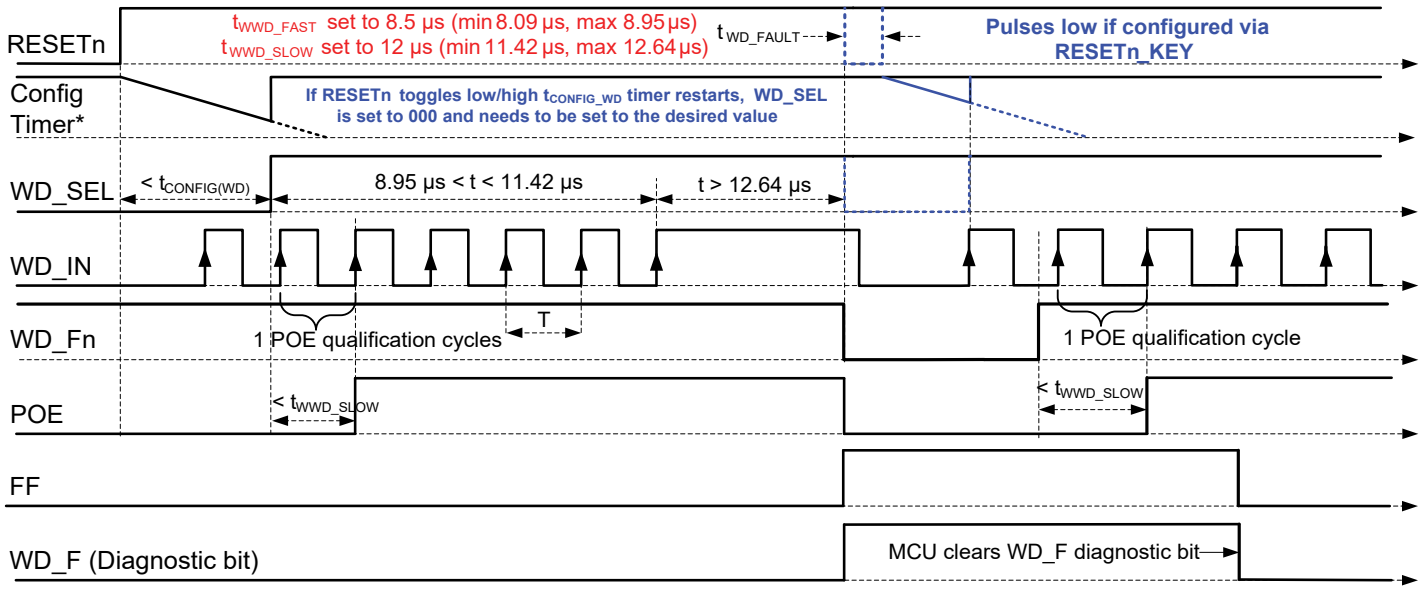

Figure 24: Window Watchdog (WWD) Operation

A watchdog fault occurs when the WD_IN period (T) is too long. * Signal is internal to A81415.

Q&A Watchdog (QAWD)

The question-and-answer watchdog (QAWD) requires the MCU to read a 6-bit word from a register within the A81415. The MCU must then generate four answer words based on the word read. If the QAWD_TIMERS bit is 0, all four answer words must be written in the correct sequence within one timed window; if QAWD_TIMERS bit is set to 1, the first two words must be written within the first timed window, then the third and the fourth in the second timed window.

The QAWD has parameters that must be configured before it is activated. QAWD_TIMERS defines whether the answers must be submitted in one or two time windows. QAWD_RETRY[2:0] defines the maximum number of retries the microcontroller is allowed to retry the question-and-answer sequence before a watchdog fault is declared. QAWD_TIMER1_ MIN1[3:0], QAWD_TIMER1_ MAX1[3:0], QAWD_TIMER2_ MIN[3:0], and QAWD_ TIMER2_MAX[3:0] configure the timed windows.

After configuration is complete, the watchdog is activated via writing WD_SEL[2:0], the A81415 generates the 6-bit random word QAWD_RAND[5:0], and the first internal timer starts. The microcontroller must start its own timer to synchronize with A81415, read the challenge word, and compute the answer to be submitted within the configured timed windows. Upon receipt of the last answer words, a new question-and-answer watchdog session starts. The MCU should synchronize its timers with the writing of the answer words.

The microcontroller should use a 6-bit linear feedback shift register (LFSR) to generate the next four 6-bit words in the sequence. The random word received from the A81415 is used to seed the LFSR.

The following example is illustrated in Figure 25. The MCU reads the question (seed) from the A81415 register; here, the seed is 0b101001. The MCU implements an LFSR with polynomial $x^5 + x^4 + 1$. The MCU seeds its LFSR with this word. The MCU clocks the LFSR and computes the LSB as the XOR between bit4 and bit5 of the seed, which returns 0b010011, answer word 1. The MCU again clocks the LFSR and computes the LSB as the XOR between bit4 and bit5 of the answer word 1 to return 0b100111, answer word 2. Two further clocks cycles give 0b001111 (answer word 3) and 0b011110 (answer word 4).

The MCU puts answer word 1 and answer word 2 in a 32-bit SPI frame; answer word 1 uses bits [D11:D6] and answer word 2 uses [D21:D16]. The MCU writes this frame to the A81415 configuration register 4. The A81415 determines if the answers received are correct and if they arrived within the timer window. The MCU repeats the process with answer word 3 using bits [D11:D6] and answer word 4 using [D21:D16].

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If QAWD_TIMERS is cleared, single-window mode is selected, and the microcontroller must wait for the first time limit to elapse (QAWD_TIMER1_MIN) before writing the first two 6-bit word answers (word 1 and word 2), followed by the second two 6-bit word answers (word 3 and word 4) using two SPI frames. The four answers must be submitted before the first maximum time limit elapses (QAWD_TIMER1_MAX) with margin.

If QAWD_TIMERS is set, two-window mode is selected, and the microcontroller must wait for the first time limit to elapse (QAWD_TIMER1_MIN) before writing the first two 6-bit word answers (word 1 and word 2). These answers must be submitted before the first maximum time limit elapses (QAWD_TIMER1_ MAX) with margin. After the second minimum time limit elapsed (QAWD_TIMER2_MIN), the microcontroller must write the second two 6-bit word answers (word 3 and word 4). These answers must be submitted before the second maximum time limit elapses (QAWD_TIMER2_MAX) with margin.

When the second answers are received, or the maximum time limit is elapsed, a new question-and-answer cycle starts by resetting the timers and generating a new random question word.

If a successful watchdog session is completed, the retry counter increments by 1. The maximum increments are limited by the content of the QAWD_RETRY[2:0] configuration register

The microcontroller is allowed to retry the question-and-answer sequence QAWD_ RETRY [2:0] times before a watchdog fault is declared. A question-and-answer watchdog fault occurs only after the retry counter reaches zero, as shown in Figure 28. During a question-and-answer watchdog session, the retry counter is decremented by 1 if one or more of the following occur:

- An answer is received before the respective minimum time limit expires (QAWD_TIMER1_MIN or QAWD_TIMER2_ MIN).
- An answer is not received before the respective maximum time limit expires (QAWD_TIMER1_MAX or QAWD_ TIMER2_ MAX).
- An incorrect answer is received from the microcontroller.

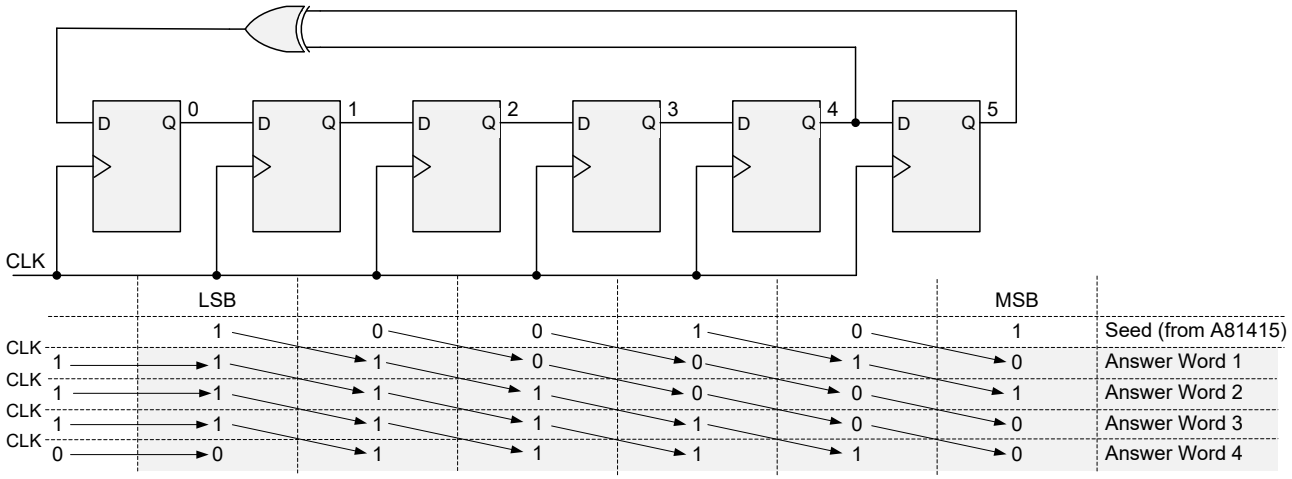

Figure 25: 6-Bit Q&A Linear Feedback Shift Register using Polynomial $x^5 + x^4 + 1$

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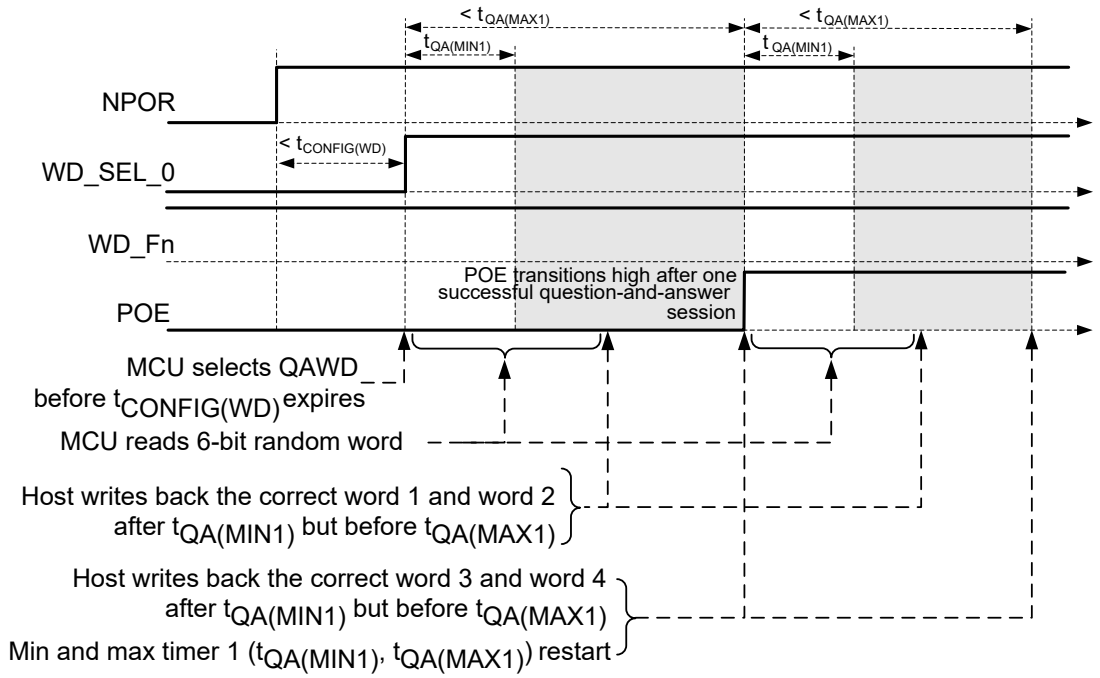

Figure 26: Q&A Watchdog Selection, Operation, and Successful Session SPI (QAWD_TIMERS) = 0

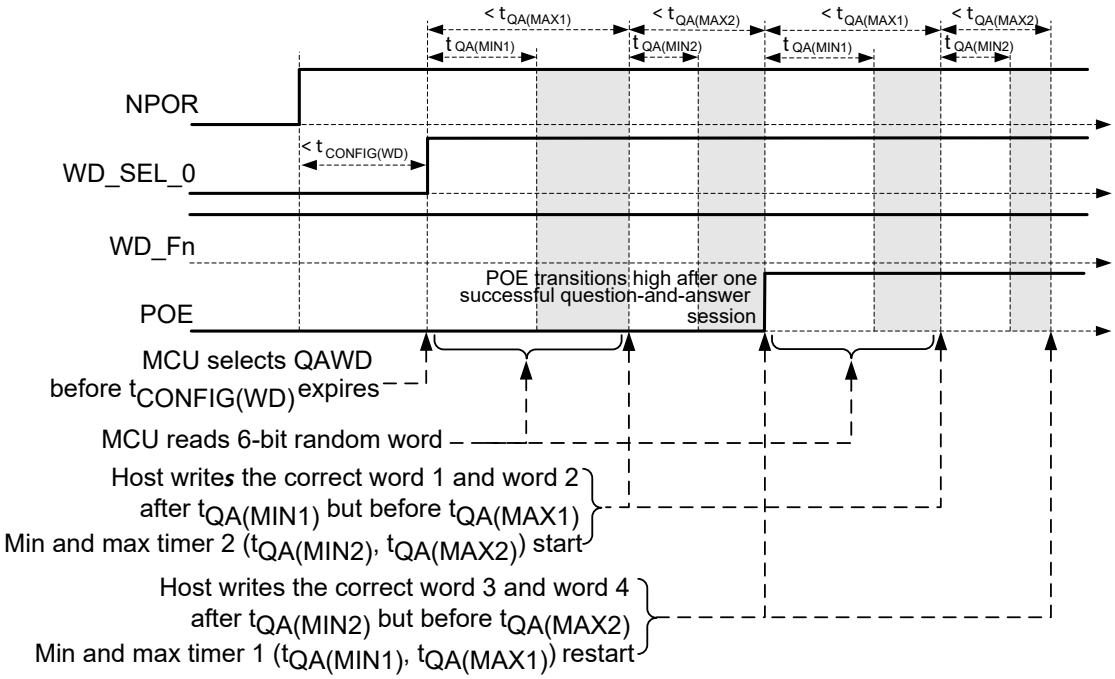

Figure 27: Q&A Watchdog Selection, Operation and Successful Session SPI (QAWD_TIMERS) = 1

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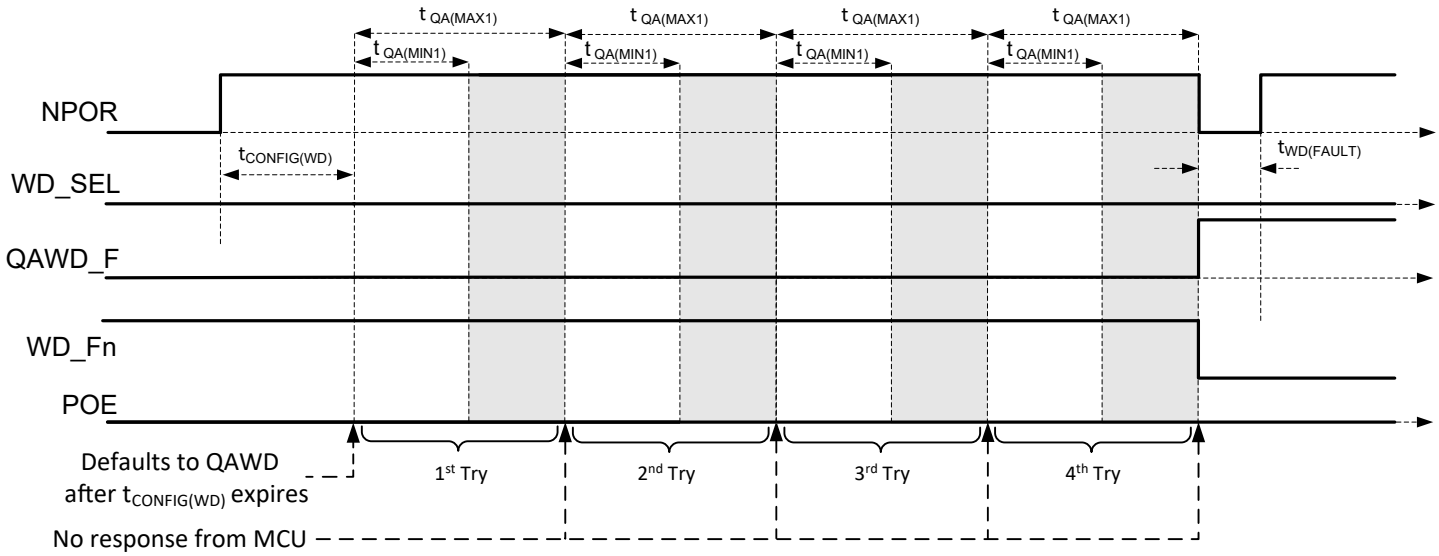

Figure 28: Watchdog Fault Behavior When WD Selection Is Not Performed By MCU

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WATCHDOG FLOW CHARTS

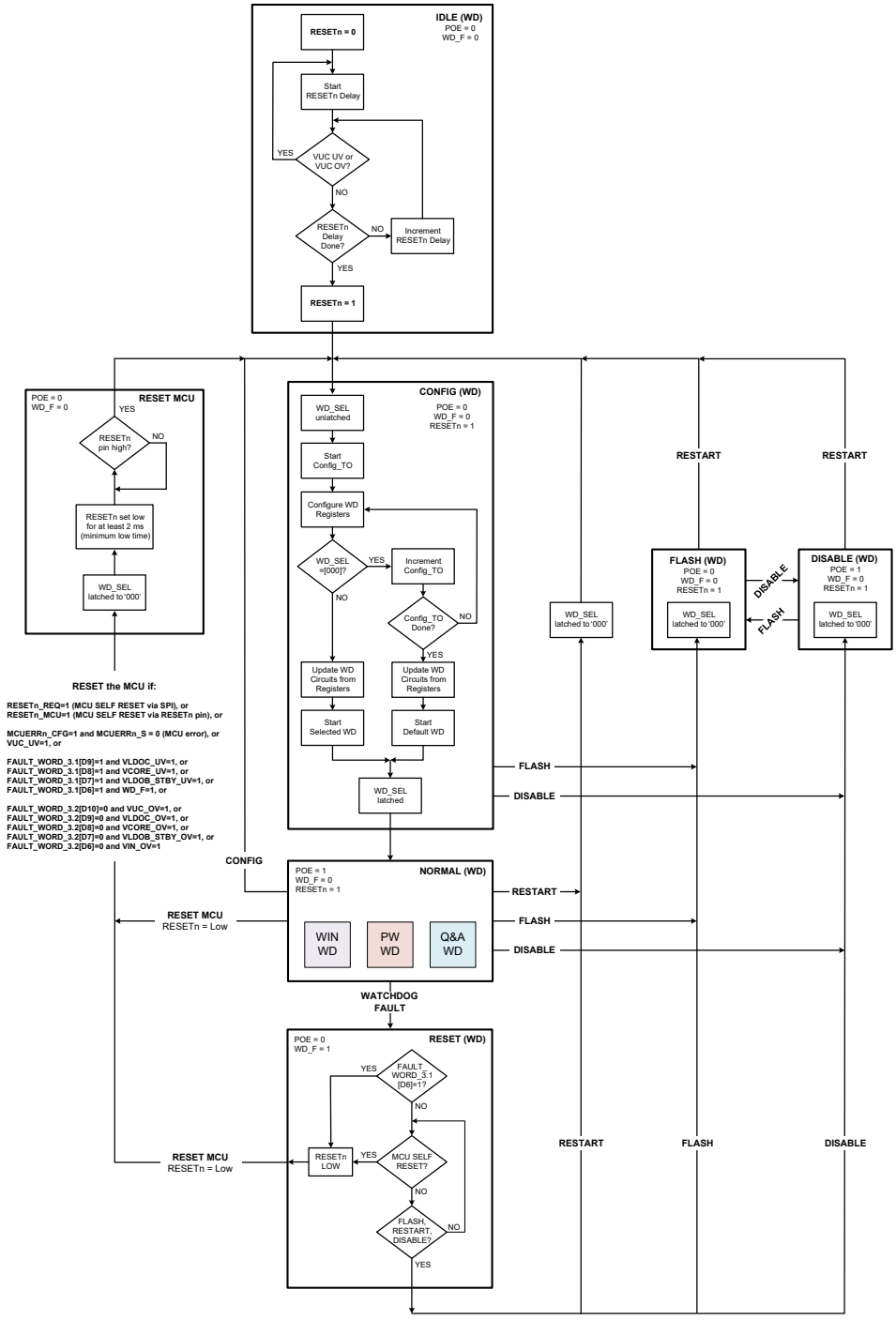

Figure 29: State Diagram of Watchdog Operation

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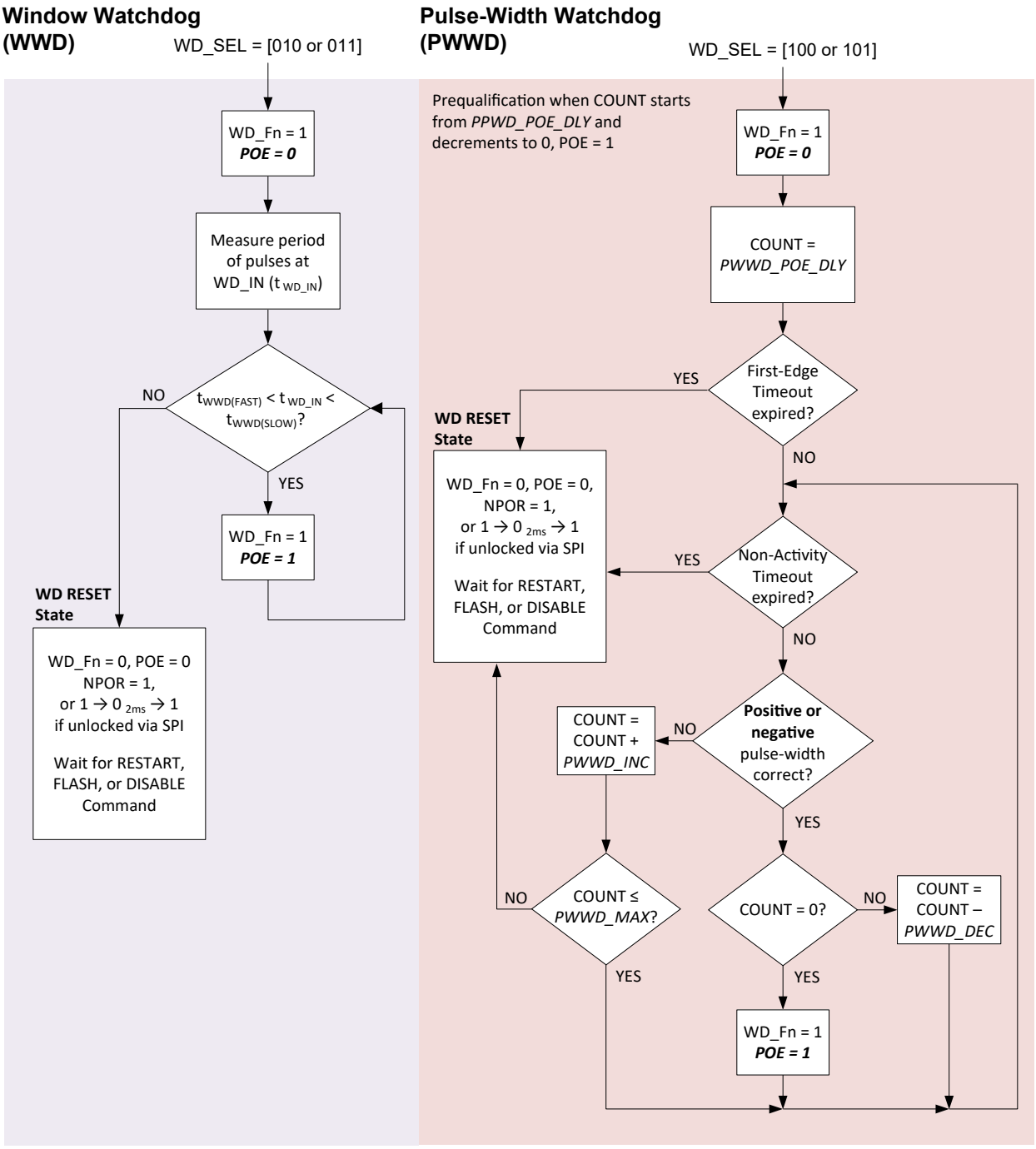

Figure 30: WWD and PWWD Flow Charts

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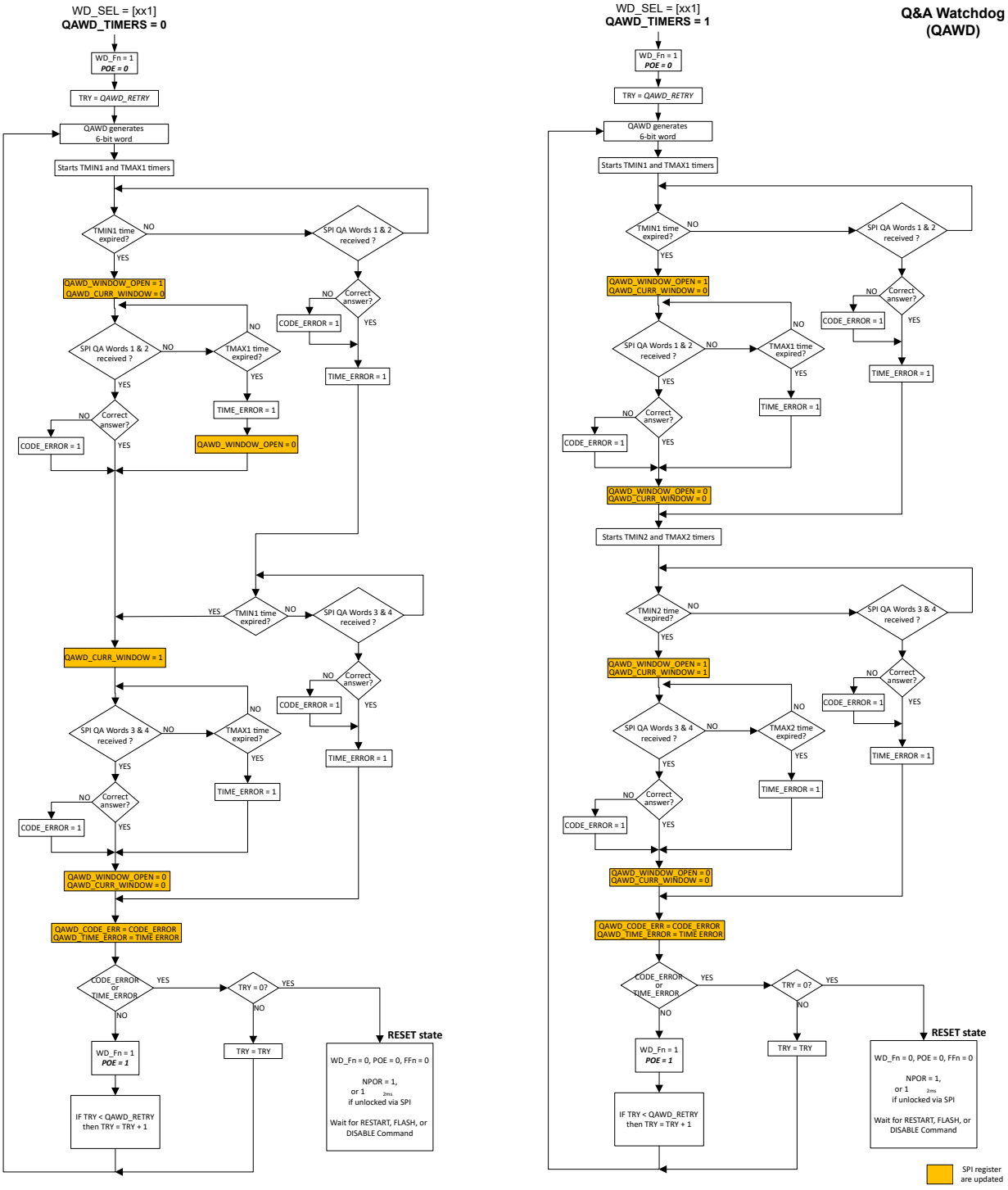

Figure 31: QAWD Flow Charts

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WSS Interface

The A81415 includes one wheel speed channel interface with high-side and low-side switches fully protected against short to battery or short to ground. The interface provides the voltage supply to the sensor and at the same time it measures the current absorbed through the low-side path by the integrated current sense. The current signal is then translated into the voltage domain by the signal processing block and decoded based on the protocol configured by SPI.

The interface can receive and decode the following wheel speed sensor types:

- Standard 2-level (7 mA / 14 mA)
- 2-level PWM with one rising edge per tooth
- 2-level PWM with two rising edges per tooth
- 3-level standard resolution AK protocol (7 mA / 14 mA / 28 mA)
- 3-level high resolution AK protocol with 14 mA / 28 mA interpolated pulse

Once decoded the sensor data is provided either through SPI bus and/or digital output pin (WSIO).

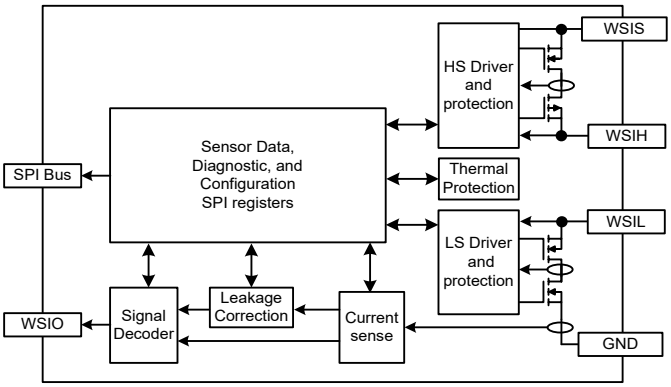

Figure 32: WSS Interface Block Diagram

Signal Processing

The signal processing includes two main current thresholds, I_{TH1} and I_{TH2}, to distinguish between the two levels 7 mA / 14 mA and between the two levels 14 mA / 28 mA. Both thresholds have hysteresis and deglitch filters to remove signal noise and avoid output glitches.

The circuit is also capable of detecting a signal within the zone between hysteresis thresholds: I_{TH1-} and I_{TH1+}, I_{TH2-} and I_{TH2+}.

The interface also integrates an offset compensation algorithm able to automatically compensate for a resistive short on WSS bus, if the short resistance is higher than 2 kΩ. The algorithm can decode the right data within two speed pulse edges. The amount of leakage current/offset compensated by the interface algorithm is available and updated in real-time in the SPI WSI_OFFSET_COMP bits.

If the short resistance value is too low to properly decode the data, then the SPI warning flag is set.

The interface also includes an additional configurable lower-threshold I_{OC} to detect an open-circuit condition. The open-circuit detection remains operational even if the high-side switch channel is turned off or disabled and it is not affected by the offset compensation. In this way, the MCU can switch off the high-side switch and verify that the open circuit detection of the channel is activated. The MCU is responsible for monitoring the high-side switch-state feedback and distinguishing a high-side switch-off condition (either commanded, or due to an overcurrent disable) from a true open circuit. Because current sensing is not possible with the low-side switch off, open-circuit detection is masked while the low-side switch is off.

The wheel speed interface filter time $t_{d(ITH\_x)}$, can be configured using two bits of the WSI_CONFIG register, and defines the filter applied on every current level transition.

Decoder configuration modes

The interface integrates five configuration modes to address each wheel speed sensor type:

MODE 1

The WSIO output signal is generated with the same frequency, duty cycle, and polarity as the sensor current signal, with a small shift due to the filter time and the IC internal delay.

The A81415 also provides the current signal on time value (from above I_{TH1+} to below I_{TH1-}) through the pulse width SPI field (WSI_PW). In case the on-time value is within the standstill pulse minimum and maximum threshold values, the standstill SPI bit is set; otherwise, it is cleared.

As long as the WSS interface remains active, the WSS data SPI register is updated either on the falling edge of the current signal or if the on-time counter saturates.

When new WSS data is decoded and updated in the SPI register, the device also sets the SPI NEWDATA bit. This bit is latched and cleared on read, in this way the MCU can understand if there is new data (NEWDATA = 1) or if the data has been already read (NEWDATA = 0).

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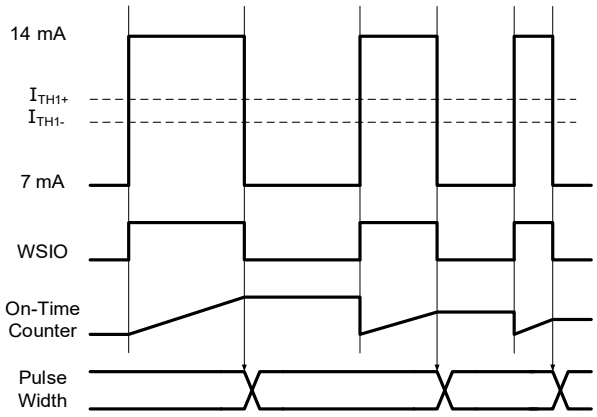

Figure 33: 2-Level Sensor with Mode 1 Decoder

MODE 2

In mode 2 configuration, the WSIO output signal only toggles each current signal rising edge. In this way, the WSIO output signal is half the frequency of the current signal and approximately 50% of duty cycle.

The device also provides the total number of both WSIO rising and falling edges. The value is available in the SPI register bits (WSI_EDGE_COUNT) and the counter is reset every time the user sets the WSI_SYNC SPI bit.

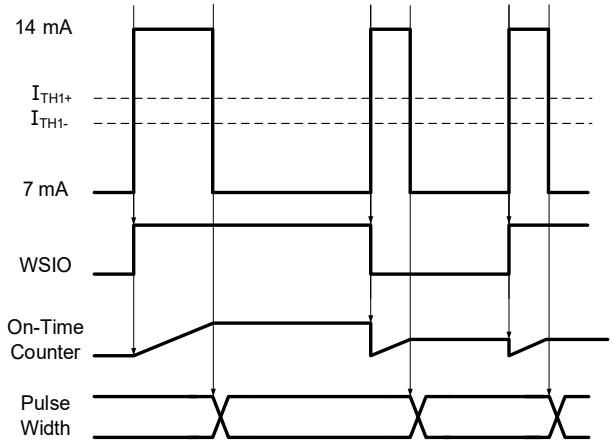

Figure 34: 2-Level PWM Sensor with Mode 2

In case of standstill pulse, the WSIO output does not toggle on the next current signal rising edge. In this way, the multiple concurrent standstill pulses are filtered; however, the WSIO signal toggles again only at the rising edge of the second speed pulse. The standstill SPI flag toggles up only after the first standstill pulse is concluded and toggles down only after the first good pulse is concluded. However, the pulse width register catches this as indicated in Figure 35.

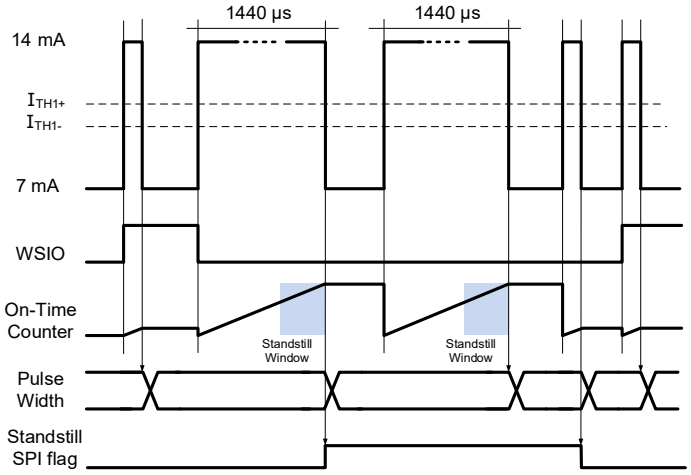

Figure 35: 2-Level PWM sensor with Standstill pulse and Mode 2

MODE 3

In mode 3 configuration, the device is capable of decoding AK protocol. This is a three-level protocol where speed (first pulse at 7 to 28 mA levels) is followed by nine Manchester-encoded VDA data bits (7 to 14 mA levels). These VDA data bits are reported in the SPI register field VDA_DATA together with the number of decoded bits VDA_BIT_COUNT.

In case the device receives more than nine bits, the VDA data stores only the first 9 bits received, while the VDA bit counter stops after 15 bits.

In order to properly decode the VDA data bits, the device measures the width of the initial speed pulse (t_p) of each transmitted frame and uses that value as a time base for the Manchester decoder. In case the measured t_p is longer than $t_{p(max)}$ or shorter than $t_{p(min)}$, the WSI_TP_OUT_RANGE SPI bit is set.

The t_p measurement is aborted in case of:

- Sensor current remains above I_{TH2} for a time longer than t_p overrun threshold.
- Sensor current remains between I_{TH1} and I_{TH2} (for example, in case of replacement pulse) for a time longer than t_p overrun threshold ($t_{p(over)}$)

If the t_p measurement is aborted, the device decodes the subsequent VDA bits anyway, even if the data is invalid.

The filter time $t_{d(ITHx)}$ is applied also on the t_p measurement, thus the width of the speed pulse shall be longer than the filter time selected.

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All the VDA data, VDA bit counter, standstill, t_p out of range, and I_{TH1} threshold SPI fields are updated at same time together with the data read bit (NEW DATA) upon the completion of sensor transmission.

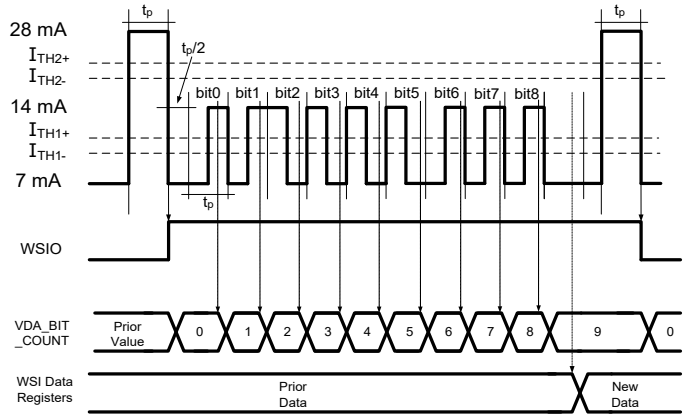

Figure 36: 3-Level Sensor AK Protocol with Mode 3

The first bit (bit0) transmitted by the sensor is the LSB of the VDA data SPI register bit, and the ninth sensor bit (parity bit) is the MSB. The device does not perform the parity bit check, but in case the first bit (bit0) is high, then the VDA Error SPI bit is set and latched as soon as the VDA data SPI bits are updated.

In order to allow the MCU to detect the VDA error, the VDA error SPI bit latch can be cleared only by the SPI write command.

In case the VDA bits are truncated because of higher wheel speed, the device reports and count the valid VDA bits while the truncated ones are reported as zero in the VDA_DATA bits.

The device is compatible with sensor suppress bit stumps.

In mode 3, the WSIO triggers every falling edge of a valid speed pulse (28 mA). It does not toggle when a standstill pulse (14 mA) is detected.

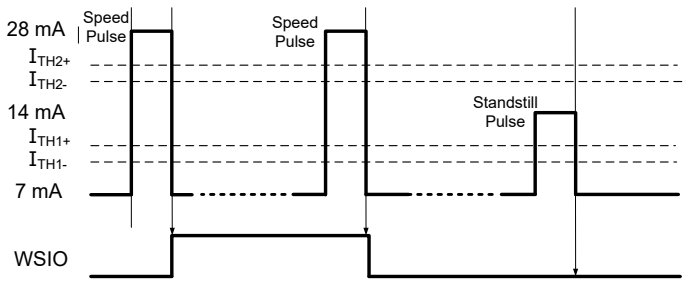

Figure 37: Standstill Pulse with Mode 3

MODE 4

Mode 4 is specifically for high-resolution speed sensors with 14 mA interpolated pulse:

- Falling edge of any speed/interpolated/standstill pulses (28 mA) triggers WSIO rising edge.
- WSIO falling edge/pulse width is defined based on the current level of the first pulse and on the VDA bit2 value:
  - If standard speed pulse, the second current threshold is triggered, then the WSIO pulse width is $t_{WSIO(SP)}$.
  - If interpolated or standstill pulse, the second current threshold is not triggered, then the WSIO pulse width is either $t_{WSIO(ISP)}$ or $t_{WSIO(SSP)}$ and depends on VDA bit2 value and on the config register field WSI_MODE_CONFIG.
  - If interpolated or standstill pulse, and bit2 is not present, the WSIO pulse width is $t_{WSIO(SSP)}$ and the standstill flag bit asserts high.

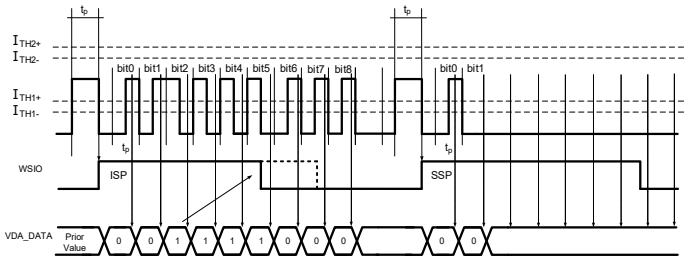

Figure 38: Mode 4 Speed Replacement Pulse without Bit2

- MCU measures the period between each rising edge and the pulse width to recognize pulse type (speed, interpolated, or standstill).

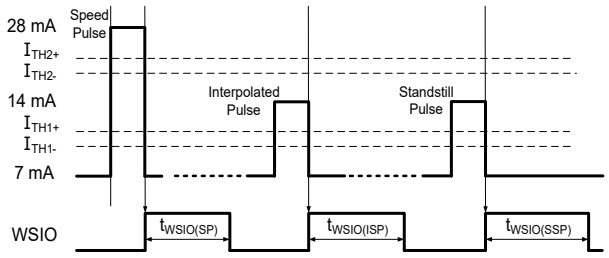

Figure 39: 3-Level High Resolution Sensor 14 mA Interpolated Pulse with Mode 4

At higher speed, the WSIO falling edge triggers as soon as a new speed pulse is received (28 mA rising edge).

In this way, the WSIO rising edge on a valid speed pulse is correctly generated.

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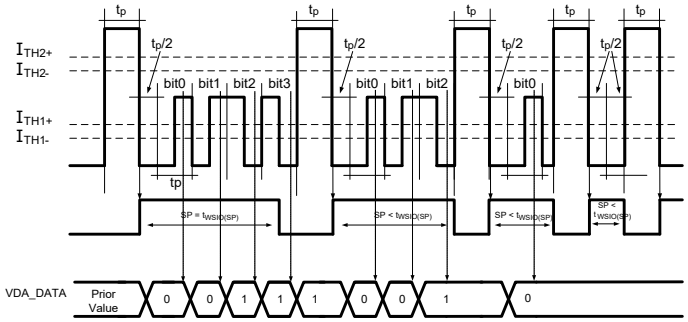

Figure 40: WSIO Length Reduction at High Speed

MODE 5

Mode 5 is similar to mode 4 but is specifically for high-resolution speed sensors with 28 mA interpolated pulse:

- Falling edge of any speed/interpolated pulses (28 mA) triggers WSIO rising edge
- WSIO falling edge/pulse width is defined based on the VDA bit2 value:
  - If standard speed or interpolated pulse, and the second current threshold is triggered, then WSIO pulse width is either $t_{WSIO(SP)}$ or $t_{WSIO(ISP)}$, and it depends on VDA bit2 value and on the config register field WSI_MODE_CONFIG.
  - If standard speed or interpolated pulse, and bit2 is not present, the WSIO pulse width is $t_{WSIO(SP)}$.
- Standstill pulse (14 mA) is filtered, so WSIO does not toggle.

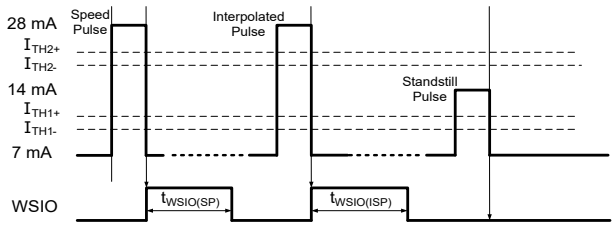

Figure 41: 3-Level High-Resolution Sensor 14 mA Interpolated Pulse with Mode 5

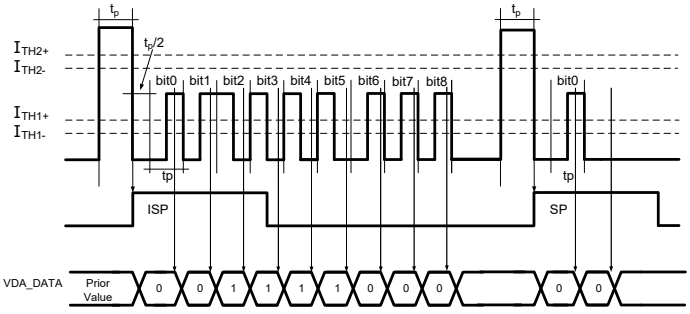

Figure 42: Mode 5 Standard Speed Pulse without Bit2

At higher speed, where VDA bit #2 is no longer available, as in Figure 39, the WSIO falling edge triggers as soon as a new speed pulse is received (28 mA rising edge).

In this way, the WSIO rising edge on a valid speed pulse is correctly generated.

Wheel Speed Interface Test Mode

The device provides the capability to activate a dedicated test-mode through SPI bit. Once activated the test mode, the WSIO output can be forced high or low by SPI bit.

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SERIAL COMMUNICATION INTERFACE

The A81415 provides the user with a full-duplex, four-wire, synchronous serial interface. It is compatible with the Serial Peripheral Interface (SPI) standard using mode 3 (CPOL = 1, CPHA = 1). The SPI interface uses an out-of-frame communications protocol, meaning the logical response of the slave is within the next frame of the master, as shown in the Figure 43. The serial interface timing requirements are specified in the electrical characteristics table and illustrated in the Serial Interface Timing diagram, Figure 5.

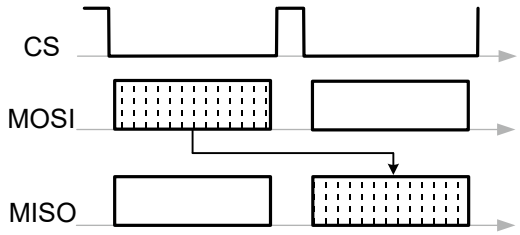

Figure 43: Out-of-Frame SPI Communication

Each 32-bit frame has a read/write bit, WR (bit 30). This bit must be set to 1 to write the subsequent bits into the selected register. If WR is set to 0 (a read), then the data bits (21 to 6) are ignored. The state of the WR bit also determines the data output on MISO. If WR is set to 1 then general diagnostic information is output. If WR is set to 0 then the contents of the register selected by the address bits is output.

MOSI

The master-output slave-input (MOSI; data input from the master). A 32-bit word sent/received MSB first. When CSN is low, data from the master is received on this pin. The slave reads/latches the data on the rising edge of SCK. The master advances to the next bit on the falling edge of SCK.

MISO

The master-input slave-output (MISO; data output from the slave, or A81415). A 32-bit word is sent/received MSB first. This pin is high impedance when CSN is high or when the Chip_ID (bit 22 from the previous frame) was incorrect. When CSN is low, data from the slave is sent on this pin. The master reads/latches the data on the rising edge of SCK. The slave advances to the next bit on the falling edge of SCK.

SCK

The serial clock (SCK; input) from the master. There must be 32 rising clock edges per frame. During each clock cycle, a full duplex data transmission occurs. The master sends a bit on the MOSI line and the slave reads it, while the slave sends a bit on the MISO line and the master reads it. This sequence is maintained even when only one-directional data transfer is intended. Data changes state on the falling edge of SCK and is latched on the rising edge of SCK. SCK must be set high before CSN transitions.

CS

The chip select (CS; input) from the master. When CSN is high, MISO is high impedance, and activity on MOSI and SCK is ignored. This allows multiple SPI slaves to have common MISO, SCK, and MOSI connections. However, each slave must have a dedicated CSN signal. CSN is brought low to initiate a serial transfer. When 32 data bits have been clocked into the shift register, CSN must be taken high to latch the data into the selected register. When this occurs, the internal control circuits act on the new data.

If CSN transitions high and there are fewer than 32 rising edges on SCK, the write will be cancelled, and no data will be written to the registers. Similarly, if there are more than 32 rising edges on SCK while CSN is low, the write will be cancelled, and no data will be written. In both cases, the SE (serial error) and FF (Fault Flag) bits will be set high.

The device also integrates a timeout that checks the inactivity on SPI CSN pin. This additional checker can enabled/disabled using the SPI bit CSN_TO_EN. If CSN pin is inactive for longer than the timeout threshold (configured by SPI CSN_TO_THR) latched bit is set and puts MISO to Hi-Z until the bit is cleared.

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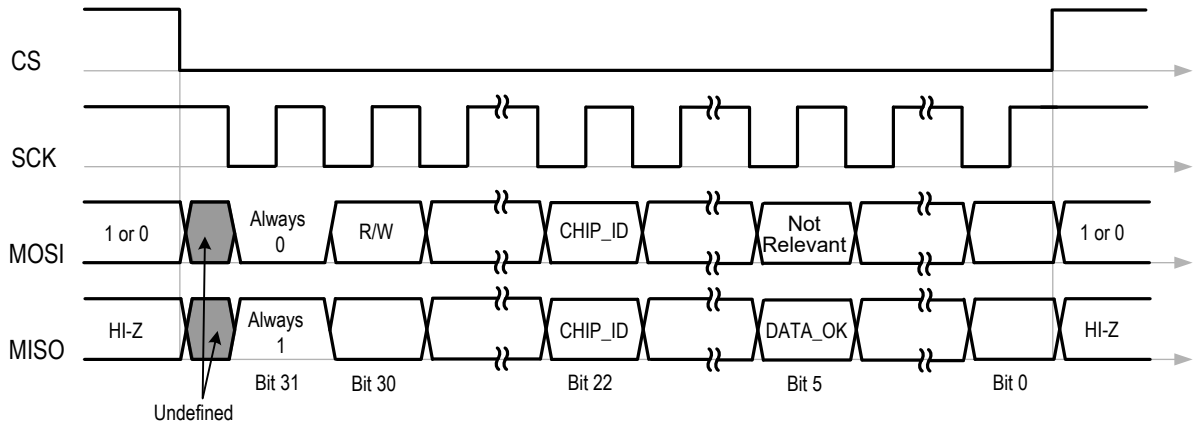

Data changes on the falling edge of SCK. Data latches on the rising edge of SCK.

Figure 44: Example SPI Communications.

SPI FRAME DEFINITIONS

1. Request register ID is the address of the host command, from the previous SPI message.
2. When the A81411 shares SPI with a second device, the CHIP_ID bit, bit [22] in both the MISO and MOSI frames, ensures that the A81415 only accepts commands intended for it. The CHIP_ID for the A81415 is internally fixed at 0. The CHIP_ID for the second device on SPI should be internally fixed at 1.
3. MOSI and MISO frames include a 5-bit CRC calculated from bits [30] through [5].
   A. Because the MSB is static, it does not need to be included in the CRC calculation; rather, it can be checked at the host-side or device-side independently.
   B. The polynomial of 0x12 ($x^5 + x^2 + 1$) is used with a start value of 11111b and a target of 00000b.
   C. All single-bit and dual-bit errors are covered.
   D. Hamming distance of 3 is achieved.
   E. Every four consecutive bit errors.
   F. Line stuck low or high is detected.
   G. If a CRC error occurs, the SE and FF bits are set to 1, and the FFn pin is pulled low.
4. MISO frame includes a 5-bit request register ID [30:26].
5. MISO frame includes a 3-bit frame counter [25:23]. It is a simple modulo-8 (0 → 1 → 2 → … → 7 → 0 → …) counter value that increments at every SPI message.
6. SPI integrity is checked via writes and reads of 2-bit patterns to the read-back register.

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HOST COMMANDS

- Bit [31] is static, fixed at 0.
- Bit [30] indicates a write or a read: 1 = Write, 0 = Read.
- For a read command, the data bits are considered not relevant (NR).

Write Command from Host to MOSI Pin

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	5-bit address					NR			16-bit data																NR	5-bit CRC				

Read Command from Host to MOSI Pin

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	5-bit address					NR			16-bit data																	5-bit CRC				

DEVICE RESPONSES

- Bit [31] is static, fixed at 1.
- Bit [22], Fault Flag bit; it is the OR of all the faults in the diagnostic registers:
  - 1 = there is a fault
  - 0 = there is no fault
- Bit [5], DATA_OK, indicates if the 16-bit data is valid:
  - 1 = Valid data, errors not detected.
  - 0 = Typical response after detection of a MOSI write or an error (i.e., SE or CRC); general status bits are sent.

Pattern at MISO Pin After MOSI Read Where 16-Bit Data Is Valid (Errors Not Detected)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	Request Register ID					Frame Counter			FF	16-bit data																1	5-bit CRC				

Pattern at MISO Pin After MOSI Write, or Pattern at MISO Pin After MOSI Read Where Error Is Detected

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	Request Register ID					Frame Counter			FF	Status Register 0																0	5-bit CRC				

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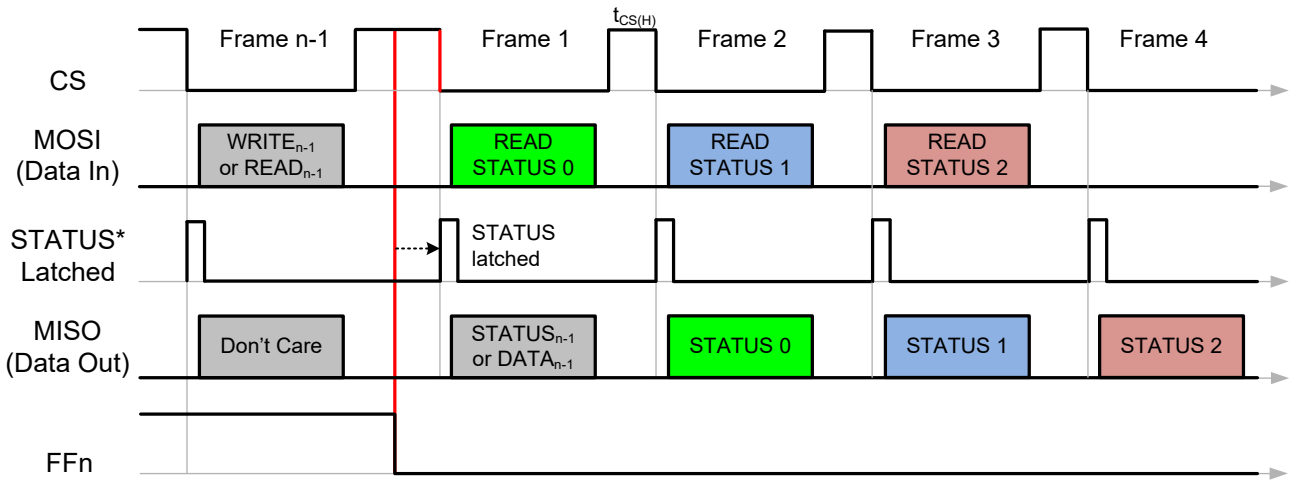
STATUS UPDATES AND SPI PROCEDURE IF FF→0

The SPI diagnostic status bits of the A81415 are updated at the end of each SPI frame (i.e., when CSN transitions high). This is shown by the STATUS Latched signal in Figure 45.

If the FF signal transitions low, it is up to the MCU to perform diagnostics on the A81415; this can be done by a simple write to the read-back register (or any other, the read-back is the safest as it does not change any functionality) to get the device response on write.

NOTE: The A81415 uses out-of-frame communication so the actual response is available on the next frame.

The other option is to perform a read of the status/diagnostic registers.



*** The "STATUS Latched" signal is internal to the IC.**

Figure 45: Recommended SPI Operations after SPI bit FF→1. (Figure to be updated)

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Register Mapping

STATUS REGISTERS

The A81415 provides three status registers. These registers are read only. They provide real-time status of various functions within the A81415.

These registers report on the status of the four system rails: VUC, VLDOA, VLDOP, and VLDOP2.

They also report on internal rail status, which include VREG and the charge pump, VCP.

The general fault flag (FF), watchdog fault flag (WD_F), and watchdog state (WD_STATE) are found in these status registers.

Fault signals RESETn and POE pins are monitored and reported if they do not match the internally generated signal.

At startup, the undervoltage faults are masked.

CONFIGURATION REGISTERS

Six registers in the A81415 are used for configuration. Four of these registers are dedicated to the watchdog parameters.

The watchdog registers can only be configured in the CONFIG state. This occurs after the A81415 is first enabled or the watchdog receives a secure SPI restart command.

The watchdog configuration register allows the user to:

1. Select the type of watchdog via WD_SEL(2:0). The default watchdog is the question-and-answer watchdog (QAWD).
2. Set the Q&A watchdog (QAWD) timer allowed number of retries.
3. Read the 6-bit random word.
4. Write the QAWD answers.
5. Set the pulse width watchdog parameters and timers.

Two other configuration registers allow the user to:

1. Disable the PWM dither feature.
2. Modify the response to a watchdog fault.
3. Mask thermal shutdown.
4. Disable/enable the 5V/3V3 rails, VLDOB, VLDOP.

By default, VLDOP is off, but can be enabled via SPI. If an LDO is disabled, its output will decay to 0 V. Normally, this causes an UV fault to occur. However, the fault flag (both FF bit) does not register a fault as this condition is expected and internally masked. Both the UV and OV faults are masked when any LDO is disabled. This allows the system to disable one of the LDOs and still maintain interrupt functionality to the microcontroller via the fault flag bit (FF). Also, if an LDO is disabled/off, the corresponding SPI diagnostic status bits (VLDOB_F or VLDOP_F) indicate a failure has not occurred.

WATCHDOG MODE KEY REGISTER

At times, it may be necessary to reflash or restart the processor. To do this, the user should put the watchdog into flash mode. This is done by writing a sequence of key words to the WD_CMD_KEY register. If the correct word sequence is not received, then the sequence must restart. While in flash mode, the A81415 sets RESETn high and POE low.

Once flash is complete, the processor must send the restart sequence of keywords for the watchdog to exit flash mode. If VIN has not been removed, the watchdog restarts with the new configuration.

RESETN INPUT KEY AND CONFIGURATION

The RESETn input key allows the user to modify which faults generate a RESETn. It also allows the MCU to toggle RESETn for 2 ms. Any changes to this register require three specific words in the correct order to be written.

VERIFY RESULT REGISTERS

At power-up, the A81415 performs a self-test of the UV and OV detection circuits. This test should cause their diagnostic registers to toggle state. If any diagnostic register does not change state, the corresponding verify result register latches high and SPI FF bit is set high.

Upon completion of power-up, the system microcontroller may be interrupted by the SPI FF bit. At that time, the microcontroller should examine the verify result registers to determine which self-test failed. If a register contains a 1, the microcontroller should make note about the failure and decide how to proceed.

Lastly, the microcontroller should write a 1 to the failed register bits (RW1C) to clear it and regain functionality of FF.

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REGISTER MAP

Table 5: Register Map

HEX	DEC	Register Name	Type	D21 / D13	D20 / D12	D19 / D11	D18 / D10	D17 / D9	D16 / D8	D15 / D7	D14 / D6
0x00	0	STATUS_0	RO	VMON_F	SE_S	WD_F	POE_S	RESETn_S	TSD_F_S	EEPROM_F	VUCSEL_F
				POE2_ERR	POE1_ERR	RESETn_ERR	TSD_WARN	ENCOM_S	ENBAT_S	ENCOM_LAT_S	ENBAT_LAT_S
0x01	1	STATUS_1	RO	VREG_F	OVUV_F	WSI_F	VCP_F	RESETn_VLDOC_UV	RESETn_VCORE_UV	RESETn_VLDOB_UV	RESETn_WD_F
				BIST_F	VUCSEL_S	FAILSAFE_VLDOA_OV	FAILSAFE_VUC_OV	FAILSAFE_VLDOC_OV	FAILSAFE_VCORE_OV	FAILSAFE_VLDOB_OV	FAILSAFE_VIN_OV
0x02	2	STATUS_2	RO	PWWD_CNT(7:0)							
				QAWD_RETRY_CNT(2:0)			WD_STATE(2:0)			QAWD_WINDOW_OPEN	QAWD_CURR_WINDOW
0x03	3	STATUS_3 [1]	RO	QAWD_WIN_TIMER(7:0)							
				QAWD_TIME_ERR	QAWD_CODE_ERR	QAWD_RAND(5:0)					
0x04	4	DIAGNOSTIC_0	RW1C	VREG_OV	VREG_UV	VUC_OV	VUC_UV	VLDOA_OV	VLDOA_UV	VLDOB_OV	VLDOB_UV
				VLDOP_OV	VLDOP_UV	VLDOC_OV	VLDOC_UV	VCP_OV	VCP_UV	VCORMON_OV	VCORMON_UV
0x05	5	DIAGNOSTIC_1	RW1C	VUC_OC	VLDOA_OC	VLDOB_OC	VLDOP_OC	VLDOC_OC	VREG_OC	–	–
				TSD_F	VIN_OV	TWARN_F	VUC_AMR_OV	BOOT1_UV	BOOT2_UV	LX1_STG	LX2_STG
0x06	6	DIAGNOSTIC_2	RW1C	SE	PWM_F	CLK_OOR	WWD_F	QAWD_F	PWWD_F	POE1_FAIL	POE2_FAIL
				RESETn_FAIL	–	RESETn_F	RESETn_REQ	RESETn_MCU	RESETn_PWR	ERRORn_TOG_F	SPI_CSN_TO
0x07	7	WD and FAULT INPUTS KEYS	WO	WD_KEY(7:0)							
				FAULT_KEY(7:0)							
0x08	8	CONFIG_0	RW	LDO_UV_FILT	LDO_OV_FILT	VLDOB_EN	VLDOP_OUT	VLDOP_TRK	VLDOP_EN	POE2_FORCE	POE1_FORCE
				TLOW_POE2(3:0)				TDELAY_POE2(3:0)			
0x09	9	CONFIG_1	RW	VCORMON_OV_SEL(1:0)		VCORMON_OV_FILT	VCORMON_UV_FILT	HIGH_POWER	BUCK_HS_SLEW(1:0)		DITH_DIS
				ENCOM_LAT(3:0)				ENBAT_LAT(3:0)			
0x0A	10	CONFIG_2: ERRORn and WD [1]	RW	ERRORn_DIS	ERRORn_SEL	ERRORn_REC_SEL	–	QAWD_TIMERS	QAWD_RETRY(2:0)		
				WD_SEL(2:0)			–	WWD_TIMER(3:0)			
0x0B	11	CONFIG_3: WD [1]	RW	QAWD_TIMER1_MAX(3:0)				QAWD_TIMER1_MIN(3:0)			
				QAWD_TIMER2_MAX(3:0)				QAWD_TIMER2_MIN(3:0)			
0x0C	12	CONFIG_4: WD (1)	RW	QAWD_ANS_2_4(5:0)						–	–
				–	WSI_SYNC	QAWD_ANS_1_3(5:0)					
0x0D	13	CONFIG_5: WD (1)	RW	PWWD_EDGE_TO(1:0)		PWWD_ACT_TO(1:0)		PWWD_WIN_TOL(1:0)		PWWD_PW(1:0)	
				PWWD_DEC(1:0)		PWWD_INC(1:0)		PWWD_MAX(1:0)		PWWD_POE_DLY(1:0)	
0x0E	14	CONFIG_6	RW	ABIST_ON	–	–	–	–	SPI_CSN_TO_EN	SPI_CSN_TO_THR(9:8)	
				SPI_CSN_TO_THR(7:0)							
0x0F	15	READ-BACK	RW	READ-BACK(15:8)							
				READ-BACK(7:0)							
0x10	16	VERIFY_RESULT_0	RW1C	VUC_OV_FAIL	VLDOA_OV_FAIL	VLDOB_OV_FAIL	VLDOP_OV_FAIL	VLDOC_OV_FAIL	VREG_OV_FAIL	VCP_OV_FAIL	VIN_OV_FAIL
				VUC_UV_FAIL	VLDOA_UV_FAIL	VLDOB_UV_FAIL	VLDOP_UV_FAIL	VLDOC_UV_FAIL	VREG_UV_FAIL	VCP_UV_FAIL	TSD_BIST_FAIL
0x11	17	VERIFY_RESULT_1	RW1C	ABIST_FAIL	LBIST_FAIL	INT_LOGIC_ERR	VUC_AMR_OV_FAIL	WSIS_UV_FAIL	WSTSD_FAIL	VCORMON_OV_FAIL	VCORMON_UV_FAIL
				–	–	–	–	–	–	–	–
0x1C	28	WSI_CONFIG	RW	WSI_TM_EN	WSI_FORCE	WSI_OFFSET_COMP_BYP	-	WSI_OC_TH	-	WSI_TD_SEL [1:0]	
				-	WSI_MODE_CONFIG [2:0]			WSI_WD_CONFIG	WSI_SYNC	WSIL_EN	WSIH_EN
0x1D	29	WSI_FAULT	RW1C	WSIL_EN_S	WSIH_EN_S	WSIO_FAIL	WSIS_UV	WSI_TWARN[ML1.1] [MG1.2]	WSI_TSD	WSIL_STG_F	WSIH_OVC_F
				WSIL_OVC_F	WSIH_REVERSE_BAT_F	WSIL_REVERSE_GND_F	WSI_EXCESSIVE_OFFSET_F	WSI_OPEN_CUR_F	WSI_ITH2_GZ_ITH2_EXCEED_F	WSI_ITH1_GZ_F	VDA_ERR_F
0x1E	30	WSI_DATA_1	RO	WSI_EDGE_COUNT [5:0]						-	WSI_OFFSET_COMP [8]
				WSI_OFFSET_COMP [7:0]							
0x1F	31	WSI_DATA_2	RO	WSI_TP_OUT_RANGE	VDA_BIT_COUNT [3:0]				WSI_PW / VDA_DATA [8:6]		
				WSI_PW / VDA_DATA [5:0]						WSI_STANDSTILL	NEWDATA

[1] With the exception of QAWD_RAND, the watchdog (WD) registers only take effect after the state machine exits the CONFIG mode.

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0x00: Status Register 0

Address: 00000b; Type: Read Only (RO)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	VMON_F	SE_S	WD_F	POE_S	RESETn_S	TSD_F_S	EEPROM_F	VUCSEL_F
Data Bit/ Name	D13	D12	D11	D10	D9	D8	D7	D6
	POE2_ERR	POE1_ERR	RESETn_ERR	TSD_WARN	ENCOM_S	ENBAT_S	ENCOM_LAT_S	ENBAT_LAT_S

VMON_F [D21]

Monitor supply fault (UV/OV not communicated):

- 0: Fault not detected
- 1: Fault detected (default)

SE_S [D20]

Serial communications error:

- 0: Error not detected (default)
- 1: Error detected—Less than or more than 32 rising SCK edges occurred in a frame, or there is a CRC error

WD_F [D19]

Watchdog fault status:

- 0: Fault not detected or watchdog is disabled (default)
- 1: Fault detected

POE_S [D18]

Power-on enable internal logic status:

- 0: POE is low (default)
- 1: POE is high

RESETn_S [D17]

Power-on reset internal logic status:

- 0: RESETn is low (default)
- 1: RESETn is high

TSD_F_S [D16]

Thermal shutdown status:

- 0: Temperature is OK (default)
- 1: Overtemperature event

EEPROM_F [D15]

EEPROM error:

- 0: Fault not detected (default)
- 1: Fault detected

VUCSEL_F [D14]

VUCSEL is terminated incorrectly:

- 0: Fault not detected (default)
- 1: Fault detected

POE2_ERR [D13]

Power-on enable (POE2) error. POE2 output pin does not match the demand of the A81415:

- 0: Fault not detected (default)
- 1: Fault detected

POE1_ERR [D12]

Power-on enable (POE1) error. POE1 output pin does not match the demand of the A81415:

- 0: Fault not detected (default)
- 1: Fault detected

RESETn_ERR [D11]

RESETn error. RESETn output pin does not match the demand of the A81415:

- 0: Fault not detected (default)
- 1: Fault detected

TSD_WARN [D10]

Thermal warning:

- 0: Temperature is less than 155°C (default)
- 1: Temperature exceeds 155°C

ENCOM_S [D9]

Status of the COM enable input pin (ENCOM):

- 0: ENCOM is low (default)
- 1: ENCOM is high

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ENBAT_S [D8]

Status of the high-voltage enable input pin (ENBAT):

- 0: ENBAT is low (default)
- 1: ENBAT is high

ENCOM_LAT_S [D7]

Status of the internal SPI COM enable (ENCOM_LAT):

- 0: ENCOM_LAT is low (default)
- 1: ENCOM_LAT is high

ENBAT_LAT_S [D6]

Status of the internal high-voltage enable (ENBAT_LAT):

- 0: ENBAT_LAT is low (default)
- 1: ENBAT_LAT is high

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0x01: Status Register 1

Address: 00001b; Type: Read Only (RO)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	VREG_F	OVUV_F	WSI_F	VCP_F	RESETn_ VLDOC_UV	RESETn_ VCORE_UV	RESETn_ VLDOB_UV	RESETn_WD_F
Data Bit/ Name	D13	D12	D11	D10	D9	D8	D7	D6
	BIST_F	VUCSEL_S	FAILSAFE_ VLDOA_OV	FAILSAFE_ VUC_OV	FAILSAFE_ VLDOC_OV	FAILSAFE_ VCORE_OV	FAILSAFE_ VLDOB_OV	FAILSAFE_VIN_OV

VREG_F [D21]

Indicates if the voltage at the preregulator output pin is within regulation:

- 0: Fault not detected (default)
- 1: Fault detected

OVUV_F [D20]

OR of all undervoltage and overvoltage faults of VUC, VLDOA, VLDOB, VLDOP, VLDOC, and VCORMON regulators:

- 0: Fault not detected (default)
- 1: Fault detected

WSI_F [D19]

OR of all WSI faults:

- 0: Fault not detected (default)
- 1: Fault detected

VCP_F [D18]

Indicates if the voltage at the VCP pin is within regulation:

- 0: Fault not detected (default)
- 1: Fault detected

RESETn_VLDOC_UV [D17]

Reports status on RESETn configuration register:

- 0: VLDOC UV fault is excluded from RESETn generation (default)
- 1: VLDOC UV fault is included in RESETn generation

RESETn_VCORE_UV [D16]

Reports status on RESETn configuration register:

- 0: VCORE UV fault is excluded from RESETn generation (default)
- 1: VCORE UV fault is included in RESETn generation

RESETn_VLDOB_UV [D15]

Reports status on RESETn configuration register:

- 0: VLDOB UV fault is excluded from RESETn generation (default)
- 1: VLDOB UV fault is included in RESETn generation

RESETn_WD_F [D14]

Reports status on RESETn configuration register:

- 0: WD_F fault is excluded from RESETn generation (default)
- 1: WD_F fault is included in RESETn generation

BIST_F [D13]

LBIST or ABIST failure:

- 0: LBIST and ABIST report that a fault is not detected (default)
- 1: LBIST or ABIST report that a fault is detected

VUCSEL_S [D12]

Indicates the voltage setting for VUC:

- 0: VUC is set to 3.3 V
- 1: VUC is set to 5 V

FAILSAFE_VLDOA_OV [D11]

Reports status on FAILSAFE config register:

- 0: VLDOA OV fault is excluded from FAILSAFE generation (default)
- 1: VLDOA OV fault is included in FAILSAFE generation

FAILSAFE_ VUC_OV [D10]

Reports status on FAILSAFE config register:

- 0: VUC OV fault is excluded from FAILSAFE generation (default)
- 1: VUC OV fault is included in FAILSAFE generation

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FAILSAFE_VLDOC_OV [D9]

Reports status on FAILSAFE config register:

- 0: VLDOC OV fault is excluded from FAILSAFE generation (default)
- 1: VLDOC OV fault is included in FAILSAFE generation

FAILSAFE_VCORE_OV [D8]

Reports status on FAILSAFE config register:

- 0: VCORE OV fault is excluded from FAILSAFE generation (default)
- 1: VCORE OV fault is included in FAILSAFE generation

FAILSAFE_VLDOB_OV [D7]

Reports status on FAILSAFE config register:

- 0: VLDOB OV fault is excluded from FAILSAFE generation (default)
- 1: VLDOB OV fault is included in FAILSAFE generation

FAILSAFE_VIN_OV [D6]

Reports status on FAILSAFE config register:

- 0: VIN OV fault is excluded from FAILSAFE generation (default)
- 1: VIN OV fault is included in FAILSAFE generation

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0x02: Status Register 2

Address: 00010b; Type: Read Only (RO)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	PWWD_CNT [7:0]							
Data Bit/ Name	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**
	QAWD_RETRY_CNT [2:0]			WD_STATE [2:0]			QAWD_ WINDOW_OPEN	QAWD_CURR_ WINDOW

PWWD_CNT [D21:D14]

Indicates the value of the error counter of the pulse-width watchdog:

- 00000000 = 0, starting value
- …
- 10100000 = 160, default maximum value
- …
- 11011100 = 220, alternate maximum value selectable via SPI

QAWD_RETRY_CNT [D13:D11]

Question-and-answer watchdog remaining retries:

- 000 = 0 retries remaining
- 001 = 1 retry remaining
- 010 = 2 retries remaining
- 011 = 3 retries remaining
- 100 = 4 retries remaining
- 101 = 5 retries remaining
- 110 = 6 retries remaining
- 111 = 7 retries remaining

WD_STATE [D10:D8]

Watchdog state:

WD_STATE [D10]	WD_STATE [D11]	WD_STATE [D8]	Watchdog State
0	0	0	Idle
0	0	1	Config
0	1	0	Reset
0	1	1	Normal
1	0	0	Flash
1	0	1	Disable
1	1	0	Reserved/Future Use
1	1	1	Reserved/Future Use

QAWD_WINDOW_OPEN [D7]

When the minimum time elapses and the maximum time is counting, the content is 1:

- 0: Question-and-answer window excluding zone
- 1: Question-and-answer window valid zone

QAWD_CURR_WINDOW [D6]

Reports which answer window is currently active, valid only:

- 0: QAWD is waiting for answer words 1 and 2
- 1: QAWD waits for answer words 3 and 4

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0x03: Status Register 3 (QAWD)

Address: 00011b; Type: Read Only (RO)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	QAWD_WIN_TIMER							
Data Bit/ Name	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**
	QAWD_TIME_ ERR	QAWD_ CODE_ERR	QAWD_RAND [5:0]					

QAWD_WIN_TIMER [D21:D14]

The 8 MSBs of the QAWD window 8-bit counter, resolution = 128 µs.

QAWD_TIME_ERR [D13]

At least one timing error occurred in the last question-and-answer cycle.

QAWD_CODE_ERR [D12]

At least one data error occurred in last question-and-answer cycle

QAWD_RAND [D11:D6]

Randomly generated 6-bit word for the question-and-answer watchdog.

To generate the answer words, these bits must be read (questioned) from the microcontroller during the typical mode of operation.

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0x04: Diagnostic Register 0

Address: 00100b; Type: Read, or Write 1 to Clear (RW1C); Faults are not latched until RESETn ceases to release.

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	VREG_OV	VREG_UV	VUC_OV	VUC_UV	VLDOA_OV	VLDOA_UV	VLDOB_OV	VLDOB_UV
Data Bit/ Name	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**
	VLDOP_OV	VLDOP_UV	VLDOC_OV	VLDOC_UV	VCP_OV	VCP_UV	VCORMON_OV	VCORMON_UV

VREG_OV [D21]

Indicates if an overvoltage occurs at the preregulator output:

- 0: Fault not detected (default)
- 1: Fault detected

VREG_UV [D20]

Indicates if an undervoltage occurs at the preregulator output:

- 0: Fault not detected (default)
- 1: Fault detected

VUC_OV [D19]

Indicates if an overvoltage occurs at the VUC LDO output:

- 0: Fault not detected (default)
- 1: Fault detected

VUC_UV [D18]

Indicates if an undervoltage occurs at the VUC LDO output:

- 0: Fault not detected (default)
- 1: Fault detected

VLDOA_OV [D17]

Indicates if an overvoltage occurs at the VLDOA LDO output:

- 0: Fault not detected (default)
- 1: Fault detected

VLDOA_UV [D16]

Indicates if an undervoltage occurs at the VLDOA LDO output:

- 0: Fault not detected (default)
- 1: Fault detected

VLDOB_OV [D15]

Indicates if an overvoltage occurs at the VLDOB LDO output:

- 0: Fault not detected (default)
- 1: Fault detected

VLDOB_UV [D14]

Indicates if an undervoltage occurs at the VLDOB LDO output:

- 0: Fault not detected (default)
- 1: Fault detected

VLDOP_OV [D13]

Indicates if an overvoltage occurs at the VLDOP LDO output:

- 0: Fault not detected (default)
- 1: Fault detected

VLDOP_UV [D12]

Indicates if an undervoltage occurs at the VLDOP LDO output:

- 0: Fault not detected (default)
- 1: Fault detected

VLDOC_OV [D11]

Indicates if an overvoltage occurs at the VLDOC LDO output:

- 0: Fault not detected (default)
- 1: Fault detected

VLDOC_UV [D10]

Indicates if an undervoltage occurs at the VLDOC LDO output:

- 0: Fault not detected (default)
- 1: Fault detected

VCP_OV [D9]

Indicates if an overvoltage occurs at the VCP pin:

- 0: Fault not detected (default)
- 1: Fault detected

VCP_UV [D8]

Indicates if an undervoltage occurs at the VCP pin:

- 0: Fault not detected (default)
- 1: Fault detected

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VCORMON_OV [D7]

Indicates if an overvoltage occurs at the VCORMON pin:

- 0: Fault not detected (default)
- 1: Fault detected

VCORMON_UV [D6]

Indicates if an undervoltage occurs at the VCORMON pin:

- 0: Fault not detected (default)
- 1: Fault detected

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0x05: Diagnostic Register 1

Address: 00101b; Type: Read, or Write 1 to Clear (RW1C); Faults are not latched until RESETn is released.

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	VUC_OC	VLDOA_OC	VLDOB_OC	VLDOP_OC	VLDOC_OC	VREG_OC	UNUSED	UNUSED
Data Bit/ Name	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**
	TSD_F	VIN_OV	TWARN_F	VUC_AMR_OV	BOOT1_UV	BOOT2_UV	LX1_STG	LX2_STG

VUC_OC [D21]

Indicates if the VUC regulator undergoes an overcurrent condition:

- 0: In the time since the register was last cleared, an overcurrent event did not occur (default)
- 1: An overcurrent event occurred

VLDOA_OC [D20]

Indicates if the VLDOA regulator undergoes an overcurrent condition:

- 0: In the time since the register was last cleared, an overcurrent event did not occur (default)
- 1: An overcurrent event occurred

VLDOB_OC [D19]

Indicates if the VLDOB regulator undergoes an overcurrent condition:

- 0: In the time since the register was last cleared, an overcurrent event did not occur (default)
- 1: An overcurrent event occurred

VLDOP_OC [D18]

Indicates if the VLDOP regulator undergoes an overcurrent condition:

- 0: In the time since the register was last cleared, an overcurrent event did not occur (default)
- 1: An overcurrent event occurred

VLDOC_OC [D17]

Indicates if the VLDOC regulator undergoes an overcurrent condition:

- 0: In the time since the register was last cleared, an overcurrent event did not occur (default)
- 1: An overcurrent event occurred

VREG_OC [D16]

Indicates if a VREG overcurrent occurs:

- 0: Fault not detected (default)
- 1: Fault detected

UNUSED[D15:D14]

Unused

TSD_F [D13]

Indicates if a thermal fault occurs:

- 0: Fault not detected (default)
- 1: Fault detected

VIN_OV [D12]

Indicates if an overvoltage occurs at the VIN pin:

- 0: Fault not detected (default)

1: Fault detected

TWARN_F [D11]

Indicates if a temperature warning is flagged to the MCU:

- 0: Fault not detected (default)
- 1: Fault detected

VUC_AMR_OV [D10]

Indicates if an absolute maximum rate overvoltage occurs at the VUC LDO output:

- 0: Fault not detected (default)
- 1: Fault detected

BOOT1_UV [D9]

Indicates if the buck boot is undervoltage:

- 0: Fault not detected (default)
- 1: Fault detected

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BOOT2_UV [D8]

Indicates if the boost boot is undervoltage:

- 0: Fault not detected (default)
- 1: Fault detected

LX1_STG [D7]

Indicates if LX1 is shorted to ground:

- 0: Fault not detected (default)
- 1: Fault detected

LX2_STG [D6]

Indicates if LX2 is shorted to ground:

- 0: Fault not detected (default)
- 1: Fault detected

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0x06: Diagnostic Register 2

Address: 00110b; Type: Read, or Write 1 to Clear (RW1C); Faults are not latched until RESETn is not released.

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	SE	PWM_F	CLK_OOR	WWD_F	QAWD_F	PWWD_F	POE1_FAIL	POE2_FAIL
Data Bit/ Name	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**
	RESETn_FAIL	UNUSED	RESETn_F	RESETn_REQ	RESETn_MCU	RESETn_PWR	ERRORn_TOG_F	SPI_CSN_TO

SE [D21]

Indicates if there is a serial communications error:

- 0: Error not detected (default)
- 1: Fault detected—There were less than or more than 32 rising SCK edges in a frame, or a CRC error occurred

PWM_F [D20]

Indicates if there is a PWM oscillator fault:

- 0: Fault not detected (default)
- 1: Stuck fault detected

CLK_OOR [D19]

Indicates if there is a main and/or PWM oscillator fault:

- 0: Fault not detected (default)
- 1: Out-of-range fault detected

WWD_F [D18]

Indicates if there is a window watchdog fault:

- 0: Fault not detected (default)
- 1: Fault detected

QAWD_F [D17]

Indicates if there is a question-and-answer watchdog fault:

- 0: Fault not detected (default)
- 1: Fault detected

PWWD_F [D16]

Indicates if there is a pulse-width watchdog fault:

- 0: Fault not detected (default)
- 1: Fault detected

POE1_FAIL [D15]

Indicates if there is a POE1 output pin fault:

- 0: Fault not detected (default)
- 1: Fault detected—The POE1 output pin does not match the demand from the A81415

POE2_FAIL [D14]

Indicates if there is a POE2 output pin fault:

- 0: Fault not detected (default)
- 1: Fault detected—The POE2 output pin does not match the demand from the A81415

RESETn_FAIL [D13]

The value of the RESETn output is 0, even if the A81415 demands the value to be 1:

- 0: Fault not detected (default)
- 1: Fault detected

UNUSED [D12]

Unused

RESETn_F [D11]

Indicates if the A81415 resets the MCU because of an internal fault:

- 0: Reset did not occur (default)
- 1: MCU reset by a fault; refer to the RESETn key configuration

RESETn_REQ [D10]

Indicates if the MCU requests a reset by SPI command:

- 0: Request not received (default)
- 1: MCU reset itself by RESETn input key (RESETn_VAL = 0)

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RESETn_MCU [D9]

Indicates if MCU self-reset occurs by pulling the RESETn pin low. The value of the RESETn output is 0, even if the A81415 demands the value to be 1:

- 0: Reset did not occur (default)
- 1: MCU pulled the RESETn pin low, which triggered a self-reset sequence

RESETn_PWR [D8]

Indicates if the A81415 resets the MCU because of an internal reset:

- 0: RESETn_PWR bit is cleared by the MCU via SPI
- 1: MCU reset is caused by powerup (default)

ERRORn_TOG_F [D7]

Indicates if there is an ERRORn toggling fault:

- 0: Fault not detected (default)
- 1: Fault detected

SPI_CSN_TO [D6]

SPI CSN timeout

- 0: Timeout not reached (default)
- 1: Timeout occurred

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0x07: WD and FAULT Input Keys

Address: 00111b; Type: Write Only (WO)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	WD_KEY [7:0]							
Data Bit/ Name	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**
	FAULT_KEY [7:0]							

WD_KEY [D21:D14]

Watchdog mode key. To enable flash mode or to restart the watchdog, three 8-bit words (WORD1 – WORD3) must be sent in the correct order. If an incorrect word is received, the register resets and the first word must be resent. The third 8-bit word (WORD3) is the command to force the watchdog to transition from state to state.

		WD_KEY [D21]	WD_KEY [D20]	WD_KEY [D19]	WD_KEY [D18]	WD_KEY [D17]	WD_KEY [D16]	WD_KEY [D15]	WD_KEY [D14]
WORD1 (Key)		1	1	0	1	0	0	1	1
WORD2 (Key)		0	0	1	1	0	0	1	1
WORD3 (Command)	**Flash**	1	1	0	0	1	1	0	0
	Configuration	1	1	0	0	1	1	0	1
	Restart	1	1	0	0	1	1	1	0
	Disable	1	1	0	0	1	1	1	1

FAULT_KEY [D13:D6]

FAULT key. To unlock the FAULT configuration register, two 8-bit words (WORD1, WORD2) must be sent in the correct order. If an incorrect word is received, the register resets and the first word must be resent. A third 8-bit word (WORD3) can modify the REST and FAILSAFE response to each fault shown; it also allows the MCU to command a self-reset by toggling RESETn low for 2 ms. If the A81415 experiences a master power-on reset (MPOR), it transitions back to the default state.

	FAULT_KEY[D13:D6]								Description
	[D13]	[D12]	[D11]	[D10]	[D9]	[D8]	[D7]	[D6]	
WORD1	1	1	0	1	0	1	0	0	Required key #1
WORD2	0	0	1	0	1	0	1	1	Required key #2
WORD3:0	0	1	1	X	X	X	X	X	MCU SELF RESET via SPI; RESETn low for 2 ms
WORD3:1	1	1	1	VLDOA_OV	VLDOC_UV	VCORE_UV	VLDOB_UV	WD_F	Reset the MCU
				0: RESETn=1, POE=1	0: RESETn=1, POE=1	0: RESETn=1, POE=1	0: RESETn=1, POE=1	0: RESETn=1, POE=0 (default)	
				1: FAILSAFE (default)	1: RESETn=0, POE=0 (default)	1: RESETn=0, POE=0 (default)	1: RESETn=0, POE=0 (default)	1: RESETn=0, POE=0	
WORD3:2	1	0	0	VUC_OV	VLDOC_OV	VCORE_OV	VLDOB_OV	VIN_OV	Failsafe
				0: RESETn=0, POE=0	0: RESETn=0, POE=0	0: RESETn=0, POE=0	0: RESETn=1, POE=1	0: RESETn=1, POE=1	
				1: FAILSAFE (default)	1: FAILSAFE (default)	1: FAILSAFE (default)	1: FAILSAFE (default)	1: FAILSAFE (default)	

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0x08: Configuration Register 0

Address: 01000b; Type: Read or Write (RW)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	LDO_UV_FILT	LDO_OV_FILT	VLDOB_EN	VLDOP_OUT	VLDOP_TRK	VLDOP_EN	POE2_FORCE	POE1_FORCE
Data Bit/ Name	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**
	TLOW_POE2 (3 :0)				TDELAY_POE2(3 :0)			

LDO_UV_FILT [D21]

Controls VUC, VLDOA, VLDOB, VLDOP, and VLDOC regulators undervoltage filter time setting.

- 0: Short undervoltage detection delay (default)
- 1: Long undervoltage detection delay

LDO_OV_FILT [D20]

Controls VUC, VLDOA, VLDOB, VLDOP, and VLDOC regulators overvoltage filter time setting.

- 0: Short overvoltage detection delay (default)
- 1: Long overvoltage detection delay

VLDOB_EN [D19]

Controls the on and off states of the VLDOB linear regulator:

- 0: Disabled or off
- 1: Enabled or on (default)

VLDOP_OUT [D18]

Controls VLDOP regulator output voltage setting:

- 0: Output is set to 3.3 V (default)
- 1: Output is set to 5.0 V

VLDOP_TRK [D17]

Commands VLDOP to track VLDOC:

- 0: No tracking (default)
- 1: Tracking enabled, VLDOP2 will track VLDOC

VLDOP_EN [D16]

Controls the on and off states of the VLDOP linear regulator:

- 0: Disabled or off (default)
- 1: Enabled or on

POE2_FORCE [D15]

POE2 force bit:

- 0: No effect on POE control when 0 (default)
- 1: Force POE low when 1

POE1_FORCE [D14]

POE1 force bit:

- 0: No effect on POE control when 0 (default)
- 1: Force POE1 (and POE2 with t_{delay}/t_{low}) low when 1

TLOW_POE2 [D13:D10]

POE2 low time selection.

- 0000 = 0 ms
- 0001 = 1 ms
- 0010 = 2 ms
- 0011 = 4 ms
- 0100 = 6 ms
- 0101 = 8 ms
- 0110 = 10 ms
- 0111 = 12 ms
- 1000 = 15 ms
- 1001 = 18 ms
- 1010 = 20 ms
- 1011 = 30 ms
- 1100 = 50 ms
- 1101 = 70 ms
- 1110 = 80 ms
- 1111 = Infinite (default) only MCU command can toggle up the POE2

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TDELAY_POE2 [D9:D6]

POE2 delay time selection.

- 0000 = 0 ms (default)
- 0001 = 1 ms
- 0010 = 2 ms
- 0011 = 4 ms
- 0100 = 6 ms
- 0101 = 8 ms
- 0110 = 10 ms
- 0111 = 12 ms
- 1000 = 15 ms
- 1001 = 18 ms
- 1010 = 20 ms
- 1011 = 30 ms
- 1100 = 50 ms
- 1101 = 70 ms
- 1110 = 80 ms
- 1111 = 100 ms

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0x09: Configuration Register 1

Address: 01001b; Type: Read or Write (RW)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	VCORMON_OV_SEL(1:0)		VCORMON_ OV_FILT	VCORMON_ UV_FILT	HIGH_POWER	BUCK_HS_SLEW(1:0)		DITH_DIS
Data Bit/ Name	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**
	ENCOM_LAT(3:0)				ENBAT_LAT(3:0)			

VCORMON_OV_SEL [D21:D20]

Controls VCORMON overvoltage threshold setting.

- 00: 874 mV_{TYP}
- 01: 894 mV_{TYP}
- 10: 91 mV_{TYP}
- 11: 934 mV_{TYP} (default)

VCORMON_OV_FILT [D19]

Controls filter time for VCORMON overvoltage monitoring:

- 0: Short overvoltage detection delay (default)
- 1: Long overvoltage detection delay

VCORMON_UV_FILT [D18]

Controls filter time for VCORMON undervoltage monitoring:

- 0: Short undervoltage detection delay (default)
- 1: Long undervoltage detection delay

HIGH_POWER [D17]

Controls current limit selection:

- 0: Normal power load mode
- 1: High power load mode

BUCK_HS_SLEW [D16:15]

Controls slew rate of high-side in buck mode:

- 00: Medium-fast slew rate
- 01: Medium-slow slew rate (default)
- 10: Slower slew rate
- 11: Fastest slew rate

DITHER_DIS [D14]

Controls the status of the PWM frequency dithering:

- 0: Dithering is enabled (default)
- 1: Dithering is disabled

ENCOM_LAT [D13:D10]

ENCOM latch reset word:

- 0000: Writing 0x0 to these bits clears the ENCOM latch. Reading 0x0 means the latch output was not set by ENCOM pin or has been cleared by the MCU via SPI.ENCOM latch ENCOM_LAT output is low (default).
- 0001 to 0100: Previous state
- 0101: Writing 0x5 to these bits sets the ENCOM latch. Reading 0x5 means the latch has been set via the ENCOM pin or set by the MCU via SPI. If ENCOM latch signal (ENCOM_ LAT) is set to 1 and ENCOM pin is 0 the A81415 is kept on.
- 0110 to 1111: Previous state

ENBAT_LAT [D9:D6]

ENBAT latch reset word:

- 0000: ENBAT latch Writing 0x0 to these bits clears the ENBAT latch. Reading 0x0 means the latch output was not set by the ENBAT pin or has been cleared by the MCU via SPI. ENBAT_LAT output is low (default).
- 0001 to 1001: Previous state
- 1010: ENBAT latch signal (ENBAT_LAT) is set to 1. If ENBAT pin is 0 MCU keeps A81415 on. Writing 0xA to these bits sets the ENBAT latch. Reading 0xA means the latch has been set via the ENBAT pin (a factory trim option), or set by the MCU via SPI.
- 1011 to 1111: Previous state

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0x0A: Configuration Register 2 (ERRORn and WD)

Address: 01010b; Type: Read or Write (RW)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	ERRORn_DIS	ERRORn_SEL	ERRORn_REC_SEL	UNUSED	QAWD_TIMERS	QAWD_RETRY [2:0]		
Data Bit/ Name	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**
	WD_SEL [2:0]			UNUSED	WWD_TIMER [3:0]			

ERRORn_DIS [D21]

Controls the status of ERRORn:

- 0: ERRORn functionality is enabled (default)
- 1: ERRORn functionality is disabled

ERRORn_SEL [D20]

Controls ERRORn operative mode selection:

- 0: ERRORn active low functionality
- 1: ERRORn toggling signal (default)

ERRORn_REC_SEL [D19]

Controls ERRORn recovery timeout selection:

- 0: 0 ms (default)
- 1: 10 ms

UNUSED [D18]

Unused

QAWD_TIMERS [D17]

Selects the number of windows for the question-and-answer watchdog:

- 0: One window selected, programmed using QAWD timer 1 (default)
- 1: Two windows selected

QAWD_RETRY [D16:D14]

Acceptable number of retries:

QAWD_RETRY			Acceptable Number of Retries
[D16]	[D15]	[D14]	
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3 (default)
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

WD_SEL [D13:D11]

Type of active watchdog:

WD_SEL			Type of Active Watchdog
[D13]	[D12]	[D11]	
0	0	0	None; default, after $t_{CONFIG(WD)}$
0	0	1	Question-and-answer watchdog (QAWD)
0	1	0	Window watchdog (WWD)
0	1	1	Question-and-answer watchdog and window watchdog
1	0	0	Pulse-width watchdog
1	0	1	Question-and-answer watchdog and pulse-width watchdog
1	1	x	None; default to QAWD after $t_{CONFIG(WD)}$

UNUSED [D10]

Unused

WWD_TIMER [D9:D6]

Watchdog timers:

WWD_TIMER				$t_{WWD(FAST)}$	$t_{WWD(SLOW)}$
[D9]	[D8]	[D7]	[D6]		
0	0	0	0	0.5 ms	4 ms
0	0	0	1	1 ms	8 ms
0	0	1	0	2 ms	16 ms
0	0	1	1	4 ms	32 ms
0	1	0	0	6 ms	42 ms
0	1	0	1	8 ms	64 ms
0	1	1	0	10 ms	80 ms
0	1	1	1	12.5 ms	100 ms
1	0	0	0	4.25 µs	6.00 µs
1	0	0	1	8.50 µs (default)	12 µs (default)
1	0	1	0	17 µs	24 µs
1	0	1	1	34 µs	48 µs

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0x0B: Configuration Register 3 (QAWD_TIMER)

Address: 01011b; Type: Read or Write (RW)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	QAWD_TIMER1_MAX [3:0]				QAWD_TIMER1_MIN [3:0]			
Data Bit/ Name	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**
	QAWD_TIMER2_MAX [3:0]				QAWD_TIMER2_MIN [3:0]			

QAWD_TIMER1_MAX [D21:D18]

Maximum timeout:

QAWD_TIMER1_MAX				MAX_ TIMEOUT $t_{QA(MAX2)}$ (ms)
[D21]	[D20]	[D19]	[D18]	
0	0	0	0	1
0	0	0	1	1.5
0	0	1	0	2
0	0	1	1	2.5 (default)
0	1	0	0	2.75
0	1	0	1	3
0	1	1	0	3.25
0	1	1	1	3.5
1	0	0	0	3.75
1	0	0	1	4
1	0	1	0	4.25
1	0	1	1	4.5
1	1	0	0	8
1	1	0	1	16
1	1	1	0	24
1	1	1	1	32

For invalid configurations, the question-and-answer watchdog function cannot be guaranteed. Invalid configurations include:

- QAWD_TIMER1_MIN [3:0] ≥ QAWD_TIMER1_MAX [3:0]
- QAWD_TIMER2_MIN [3:0] ≥ QAWD_TIMER2_MAX [3:0].

QAWD_TIMER1_MIN [D17:D14]

Minimum timeout:

QAWD_TIMER1_MIN				MIN_ TIMEOUT $t_{QA(MIN1)}$ (ms)
[D17]	[D16]	[D15]	[D14]	
0	0	0	0	0.5
0	0	0	1	1
0	0	1	0	1.5 (default)
0	0	1	1	2
0	1	0	0	2.25
0	1	0	1	2.5
0	1	1	0	2.75
0	1	1	1	3
1	0	0	0	3.25
1	0	0	1	3.5
1	0	1	0	3.75
1	0	1	1	4
1	1	0	0	5
1	1	0	1	8
1	1	1	0	12
1	1	1	1	16

For invalid configurations, the question-and-answer watchdog function cannot be guaranteed. Invalid configurations include:

- QAWD_TIMER1_MIN [3:0] ≥ QAWD_TIMER1_MAX [3:0]
- QAWD_TIMER2_MIN [3:0] ≥ QAWD_TIMER2_MAX [3:0].

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QAWD_TIMER2_MAX [D13:D10]

Maximum timeout:

QAWD_TIMER2_MAX				MAX_ TIMEOUT $t_{QA(MAX2)}$ (ms)
[D13]	[D12]	[D11]	[D10]	
0	0	0	0	1
0	0	0	1	1.5
0	0	1	0	2
0	0	1	1	2.5
0	1	0	0	2.75
0	1	0	1	3
0	1	1	0	3.25
0	1	1	1	3.5
1	0	0	0	3.75 (default)
1	0	0	1	4
1	0	1	0	4.25
1	0	1	1	4.5
1	1	0	0	8
1	1	0	1	16
1	1	1	0	24
1	1	1	1	32

For invalid configurations, the question-and-answer watchdog function cannot be guaranteed. Invalid configurations include:

- QAWD_TIMER1_MIN [3:0] ≥ QAWD_TIMER1_MAX [3:0]
- QAWD_TIMER2_MIN [3:0] ≥ QAWD_TIMER2_MAX [3:0].

QAWD_TIMER2_MIN [D9:D6]

Minimum timeout:

QAWD_TIMER2_MIN				MIN_ TIMEOUT $t_{QA(MIN1)}$ (ms)
[D9]	[D8]	[D7]	[D6]	
0	0	0	0	0.5
0	0	0	1	1
0	0	1	0	1.5
0	0	1	1	2
0	1	0	0	2.25
0	1	0	1	2.5
0	1	1	0	2.75
0	1	1	1	3
1	0	0	0	3.25 (default)
1	0	0	1	3.5
1	0	1	0	3.75
1	0	1	1	4
1	1	0	0	5
1	1	0	1	8
1	1	1	0	12
1	1	1	1	16

For invalid configurations, the question-and-answer watchdog function cannot be guaranteed. Invalid configurations include:

- QAWD_TIMER1_MIN [3:0] ≥ QAWD_TIMER1_MAX [3:0]
- QAWD_TIMER2_MIN [3:0] ≥ QAWD_TIMER2_MAX [3:0].

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0x0C: Configuration Register 4 (QAWD_ANS)

Address: 01100b; Type: Read or Write (RW)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	QAWD_ANS_2_4 [5:0]						UNUSED	
Data Bit/ Name	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**
	UNUSED	WSI_SYNC	QAWD_ANS_1_3 [5:0]					

QAWD_ANS_2_4 [D21:D16]

MCU writes question-and-answer watchdog answer word 2 and word 4 here.

UNUSED [D15:D13]

Unused.

WSI_SYNC [D12]

SYNC event start bit:

- 0: Device sets this bit to 0 every time the MCU set this to 1 (default)
- 1: Write 1 to set a new SYNC event

QAWD_ANS_1_3 [D11:D6]

MCU writes question-and-answer watchdog answer word 1 and word 3 here.

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0x0D: Configuration Register 5 (PWWD)

Address: 01101b; Type: Read or Write (RW)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	PWWD_EDGE_TO [1:0]		PWWD_ACT_TO [1:0]		PWWD_WIN_TOL [1:0]		PWWD_PW [1:0]	
Data Bit/ Name	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**
	PWWD_DEC [1:0]		PWWD_INC [1:0]		PWWD_MAX [1:0]		PWWD_POE_DLY [1:0]	

PWWD_EDGE_TO [D21:D20]

First-edge timeout:

PWWD_EDGE_TO [D21]	PWWD_EDGE_TO [D20]	First-Edge Timeout (ms)
0	0	2.5
0	1	5 (default)
1	0	10
1	1	15

PWWD_ACT_TO [D19:D18]

Nonactivity timeout:

PWWD_ACT_TO [D19]	PWWD_ACT_TO [D18]	Nonactivity Timeout (ms)
0	0	8
0	1	16 (default)
1	0	24
1	1	32

PWWD_WIN_TOL [D17:D16]

Window tolerance:

PWWD_WIN_TOL [D17]	PWWD_WIN_TOL [D16]	Window Tolerance (%)
0	0	±8
0	1	±13 (default)
1	0	±18
1	1	±23

PWWD_PW [D15:D14]

Pulse width:

PWWD_PW [D15]	PWWD_PW [D14]	Pulse Width (ms)
0	0	0.5
0	1	1 (default)
1	0	1.5
1	1	2

PWWD_DEC [D13:D12]

Decrement amount:

PWWD_DEC [D13]	PWWD_DEC [D12]	Decrement Amount (counts)
0	0	1
0	1	2 (default)
1	0	3
1	1	4

PWWD_INC [D11:D10]

Increment amount:

PWWD_INC [D11]	PWWD_INC [D10]	Increment Amount (counts)
0	0	5
0	1	10 (default)
1	0	20
1	1	30

PWWD_MAX [D9:D8]

Maximum fault counter value:

PWWD_MAX [D9]	PWWD_MAX [D8]	Maximum Fault Counter Value
0	0	80
0	1	120
1	0	160 (default)
1	1	220

PWWD_POE_DLY [D7:D6]

Sets the value preloaded into the PWWD error counter. This value is used to prequalify the WD_IN clock before POE is allowed to transition high:

PWWD_POE_DLY [D7]	PWWD_POE_DLY [D6]	Value
0	0	2 (default)
0	1	4
1	0	10
1	1	16

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0x0E: Configuration Register 6 (ABIST and SPI_CSN_TO)

Address: 01110b; Type: Read or Write (RW)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	ABIST_ON	UNUSED	UNUSED	UNUSED	UNUSED	SPI_CSN_TO_EN	SPI_CSN_TO_THR [9:8]	
Data Bit/ Name	D13	D12	D11	D10	D9	D8	D7	D6
	SPI_CSN_TO_THR [7:0]							

ABIST_ON [D21]

Runs internal analog self-test:

- 0: ABIST only runs at startup (default)
- 1: ABIST runs on this command; cleared when ABIST is complete

UNUSED [D20:17]

Unused.

SPI_CSN_TO_EN [D16]

CSN timeout enable:

- 0: Disabled
- 1: Enabled (default)

SPI_CSN_TO_THR [D15:D6]

CSN timeout threshold

- 0x000 to 0x3FF: 10-bit threshold compared with CSN timeout counter. If the counter reaches the threshold, SPI_CSN_TO is asserted. The CSN timeout counter is incremented each 1 ms, and it is asynchronous to SPI; thus, if the CSN timeout threshold is set to 1, the actual timeout fault bit is set to a value between 0 and 1 ms. The default value is 0x12C (this means the timeout occurs between 299 ms and 300 ms).

0x0F: Read-Back Register

Address: 01111b; Type: Read or Write (RW)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	Read-Back[15:8]							
Data Bit/ Name	D13	D12	D11	D10	D9	D8	D7	D6
	Read-Back[7:0]							

Read-Back [D21:D6]

The host microcontroller can implement a loopback test with this register. The host should write a specific pattern (value) to this register, read it back, and compare the two results. The host should use at least two different write patterns to be certain there are no stuck bits.

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0x10: Verify Result Register 0

Address: 10000b; Type: Read, or Write 1 to Clear (RW1C)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	VUC_OV_FAIL	VLDOA_OV_FAIL	VLDOB_OV_FAIL	VLDOP_OV_FAIL	VLDOC_OV_FAIL	VREG_OV_FAIL	VCP_OV_FAIL	VIN_OV_FAIL
Data Bit/ Name	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**
	VUC_UV_FAIL	VLDOA_UV_FAIL	VLDOB_UV_FAIL	VLDOP_UV_FAIL	VLDOC_UV_FAIL	VREG_UV_FAIL	VCP_UV_FAIL	TSD_BIST_FAIL

VUC_OV_FAIL [D21]

Indicates if the VUC overvoltage circuit fails its self-test:

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. POEx set low. To clear and regain POEx functionality, write the value 1.

VLDOA_OV_FAIL [D20]

Indicates if the VLDOA overvoltage circuit fails its self-test:

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. POEx set low. To clear and regain POEx functionality, write the value 1.

VLDOB_OV_FAIL [D19]

Indicates if the VLDOB overvoltage circuit fails its self-test:

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. POEx set low. To clear and regain POEx functionality, write the value 1.

VLDOP_OV_FAIL [D18]

Indicates if the VLDOP overvoltage circuit fails its self-test:

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. POEx set low. To clear and regain POEx functionality, write the value 1.

VLDOC_OV_FAIL [D17]

Indicates if the VLDOC overvoltage circuit fails its self-test:

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. POEx set low. To clear and regain POEx functionality, write the value 1.

VREG_OV_FAIL [D16]

Indicates if the VREG overvoltage circuit fails its self-test:

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. POEx set low. To clear and regain POEx functionality, write the value 1.

VCP_OV_FAIL [D15]

Indicates if the VCP overvoltage circuit fails its self-test:

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. POEx set low. To clear and regain POEx functionality, write the value 1.

VIN_OV_FAIL [D14]

Indicates if the VIN overvoltage circuit fails its self-test:

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. POEx set low. To clear and regain POEx functionality, write the value 1.

VUC_UV_FAIL [D13]

Indicates if the VUC undervoltage circuit fails its self-test:

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. POEx set low. To clear and regain POEx functionality, write the value 1.

VLDOA_UV_FAIL [D12]

Indicates if the VLDOA undervoltage circuit fails its self-test:

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. POEx set low. To clear and regain POEx functionality, write the value 1.

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VLDOB_UV_FAIL [D11]

Indicates if the VLDOB undervoltage circuit fails its self-test:

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. POEx set low. To clear and regain POEx functionality, write the value 1.

VLDOP_UV_FAIL [D10]

Indicates if the VLDOP undervoltage circuit fails its self-test:

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. POEx set low. To clear and regain POEx functionality, write the value 1.

VLDOC_UV_FAIL [D9]

Indicates if the VLDOC undervoltage circuit fails its self-test:

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. POEx set low. To clear and regain POEx functionality, write the value 1.

VREG_UV_FAIL [D8]

Indicates if the VREG undervoltage circuit fails its self-test:

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. POEx set low. To clear and regain POEx functionality, write the value 1.

VCP_UV_FAIL [D7]

Indicates if the VCP undervoltage circuit fails its self-test

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. POEx set low. To clear and regain POEx functionality, write the value 1.

TSD_BIST_FAIL [D6]

Indicates if the TSD circuit fails its self-test

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. POEx set low. To clear and regain POEx functionality, write the value 1.

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0x11: Verify Result Register 1

Address: 10001b; Type: Read, or Write 1 to Clear (RW1C)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	ABIST_FAIL	LBIST_FAIL	INT_LOGIC_ERR	VUC_AMR_OV_FAIL	WSIS_UV_FAIL	WSTSD_FAIL	VCORMON_OV_FAIL	VCORMON_UV_FAIL
Data Bit/ Name	D13	D12	D11	D10	D9	D8	D7	D6
	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED	UNUSED

ABIST_FAIL [D21]

Indicates if the A81415 fails ABIST:

- 0: ABIST passed (default value at powerup).
- 1: ABIST failed. POEx set low. To clear and regain POEx functionality, write the value 1.

LBIST_FAIL [D20]

Indicates if the A81415 failed LBIST:

- 0: LBIST passed (default value at powerup).
- 1: LBIST failed. POEx set low. To clear and regain POEx functionality, write the value 1.

INT_LOGIC_ERR [D19]

Indicates if an internal logic error occurs:

- 0: The digital logic function is OK.
- 1: An internal logic error occurred.

VUC_AMR_OV_FAIL [D18]

Indicates if the VUC AMR overvoltage circuit failed its self-test:

- 0: Self-test passed (default value at power-up).
- 1: Self-test failed. POEx set low. To clear and regain POEx functionality, write the value 1.

WSIS_UV_FAIL [D17]

Indicates if the WSIS undervoltage circuit failed its self-test:

- 0: Self-test passed (default value at power-up).
- 1: Self-test failed. POEx set low. To clear and regain POEx functionality, write the value 1.

WSTSD_FAIL [D16]

Indicates if the WSI thermal shutdown circuit failed its self-test:

- 0: Self-test passed (default value at power-up).
- 1: Self-test failed. POEx set low. To clear and regain POEx functionality, write the value 1.

VCORMON_OV_FAIL [D15]

Indicates if the VCORMON overvoltage circuit failed its self-test:

- 0: Self-test passed (default value at power-up).
- 1: Self-test failed. POEx set low. To clear and regain POEx functionality, write the value 1.

VCORMON_UV_FAIL [D14]

Indicates if the VCORMON undervoltage circuit failed its self-test:

- 0: Self-test passed (default value at power-up).
- 1: Self-test failed. POEx set low. To clear and regain POEx functionality, write the value 1.

UNUSED [D13:D6]

Unused

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0x1C: WSI Config Register

Address: 11100b; Type: Read or Write (RW)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	WSI_TM_EN	WSI_FORCE	WSI_OFFSET_ COMP_BYP	UNUSED	WSI_OC_TH	UNUSED	WSI_TD_SEL [1:0]	
Data Bit/ Name	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**
	UNUSED	WSI_MODE_CONFIG [2:0]			WSI_WD_CONFIG	WSI_SYNC	WSIL_EN	WSIH_EN

WSI_TM_EN [D21]

WSI testing mode enable:

- 0: Not enabled (default)
- 1: Enabled

WSI_FORCE [D20]

Controls forcing a logic high or low on the WSIO pin:

- 0: Forced low (default)
- 1: Forced high

WSI_OFFSET_COMP_BYP [D19]

Controls WSI offset compensation bypass:

- 0: Offset compensation is not disabled (default)
- 1: Offset compensation is disabled

UNUSED [D18]

Unused

WSI_OC_TH [D17]

Controls open condition current threshold selection:

- 0: I_{OPEN} = 4.85 mA (default)
- 1: I_{OPEN} = 3.6 mA

UNUSED [D16]

Unused

WSI_TD_SEL [D15:D14]

Controls filter time selection:

- 00: Filter time is 0 µs
- 01: Filter time is 15 µs (default)
- 10: Filter time is 29 µs
- 11: Filter time is 58 µs

UNUSED [D13]

Unused

WSI_MODE_CONFIG [D12:D10]

Controls decoding mode configuration:

- 000: Mode 1: 2-Level Pass Through
- 001: Mode 2: 2-Level Decoded
- 010-011: Mode 3: 3-Level Standard Resolution AK Protocol (default)
- 100: Mode 4: 3-Level High Resolution AK Protocol
  - VDA Data Bit 2:
  - 0 = Standstill Pulse
  - 1 = Interpolated Speed Pulse
- 101: Mode 4: 3-Level High Resolution AK Protocol
  - VDA Data Bit 2:
  - 0 = Interpolated Speed Pulse
  - 1 = Standstill Pulse
- 110: Mode 5: 3-Level High Resolution AK Protocol
  - VDA Data Bit 2:
  - 0 = Standard Speed Pulse
  - 1 = Interpolated Speed Pulse
- 111: Mode 5: 3-Level High Resolution AK Protocol
  - VDA Data Bit 2:
  - 0 = Interpolated Speed Pulse
  - 1 = Standard Speed Pulse

WSI_WD_CONFIG [D9]

Controls watchdog configuration on the wheel speed interface:

- 0: WD status has no effect on the WSI switches
- 1: WD status fault disable the WSI high and low side switches (default)

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WSI_SYNC [D8]

Controls SYNC event start bit:

- 0: Device sets this bit to 0 every time the MCU set this to 1 (default)
- 1: Write 1 to set a new SYNC event

WSIL_EN [D7]

Low-side channel enable:

- 0: Channel disabled (default)
- 1: Channel enabled

WSIH_EN [D6]

High-side channel enable:

- 0: Channel disabled (default)
- 1: Channel enabled

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0x1D: WSI Fault Register

Address: 11101b; Type: Read, or Write 1 to Clear (RO or R/W1C)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	WSIL_EN_S	WSIH_EN_S	WSIO_FAIL	WSIS_UV	WSI_TWARN	WSI_TSD	WSIL_STG_F	WSIH_OVC_F
Data Bit/ Name	D13	D12	D11	D10	D9	D8	D7	D6
	WSIL_OVC_F	WSIH_REVERSE_ BAT_F	WSIL_REVERSE_ GND_F	WSI_EXCESSIVE_ OFFSET_F	WSI_OPEN_CUR_F	WSI_ITH2_GZ_ ITH2_EXCEED_F	WSI_ITH1_GZ_F	VDA_ERR_F

WSIL_EN_S [D21]

Live status of the enable of low-side channel (read only):

- 0: Channel disable
- 1: Channel enable

WSIH_EN_S [D20]

Live status of the enable of high-side channel (read only):

- 0: Channel disable
- 1: Channel enable

WSIO_FAIL [D19]

WSIO output pin of A81415 demand mismatch fault:

- 0: Fault not detected (default)
- 1: Fault detected

WSIS_UV [D18]

Indicates WSIS undervoltage fault:

- 0: Fault not detected
- 1: Fault detected

WSI_TWARN [D17]

Indicates WSI thermal warning fault:

- 0: Fault not detected
- 1: Fault detected

WSI_TSD [D16]

Indicates WSI thermal shutdown fault:

- 0: Fault not detected
- 1: Fault detected

WSIL_STG_F [D15]

Indicates WSIL short-to-ground fault:

- 0: Fault not detected
- 1: Fault detected

WSIH_OVC_F [D14]

Indicates WSIH overcurrent fault:

- 0: Fault not detected
- 1: Fault detected

WSIL_OVC_F [D13]

Indicates WSIL overcurrent fault:

- 0: Fault not detected
- 1: Fault detected

WSIH_REVERSE_BAT_F [D12]

Indicates WSIH reverse-battery fault:

- 0: Fault not detected
- 1: Fault detected

WSIL_REVERSE_GND_F [D11]

Indicates WSIL reverse-ground fault:

- 0: Fault not detected
- 1: Fault detected

WSI_EXCESSIVE_OFFSET_F [D10]

Indicates WSI resistive short is lower than the minimum resistance:

- 0: Fault not detected
- 1: Fault detected

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WSI_OPEN_CUR_F [D9]

Indicates WSI current is lower than the open current threshold:

- 0: Fault not detected
- 1: Fault detected

WSI_ITH2_GZ_ITH2_EXCEED_F [D8]

Indicates current is in the I_{TH2} gray zone (mode 3/4/5) or exceed region for a 2-level sensor configuration (mode 1/2):

- 0: Fault not detected
- 1: Fault detected

WSI_ITH1_GZ_F [D7]

Indicates current is in the I_{TH1} gray zone:

- 0: Fault not detected
- 1: Fault detected

VDA_ERR_F [D6]

Indicates VDA data error fault:

- 0: Fault not detected
- 1: Fault detected

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0x1E: WSI Data Register 1

Address: 11110b; Type: Read Only (RO)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	WSI_EDGE_COUNT [5:0]						UNUSED	WSI_OFFSET_ COMP [8]
Data Bit/ Name	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**
	WSI_OFFSET_COMP [7:0]							

WSI_EDGE_COUNT [D21:D16]

Counter of the received edges:

- 000000: Counter is 0
- …
- 111111: Counter is 63

UNUSED [D15]

Unused

WSI_OFFSET_COMP [D14:D6]

Offset compensation value:

- 000000001: 200 µA
- …
- 011111111: 51.2 mA
- 100000000: –51.2 mA

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0x1F: WSI Data Register 2

Address: 11111b; Type: Read Only (RO)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	WSI_TP_OUT_ RANGE	VDA_BIT_COUNT [3:0]				WSI_PW / VDA_DATA [8:6]		
Data Bit/ Name	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**
	WSI_PW / VDA_DATA [5:0]						WSI_ STANDSTILL	NEWDATA

WSI_TP_OUT_RANGE [D21]

Indicates WSIL t_p out of range fault:

- 0: Fault not detected or fixed to 0 for 1/2 level mode
- 1: t_p is lower or higher than $t_{p(min)}$ or $t_{p(max)}$

VDA_BIT_COUNT [D20:D17]

VDA bit counter:

- 0000: Counter is 0
- …
- 1111: Counter is 15

WSI_PW / VDA_DATA [D16:D8]

Counter of the Pulse Width in a 2-level configuration (mode 1/2);
VDA data in AK protocol configuration (mode 3/4/5):

- 000000000:
- …
- 111111111:

WSI_STANDSTILL [D7]

Indicates standstill pulse received:

- 0: Standstill condition not detected
- 1: Standstill condition detected

NEWDATA [D6]

Indicates VDA data is ready (clear on read bit):

- 0: No new pulse width or VDA data available yet
- 1: New pulse width or VDA data ready to be read

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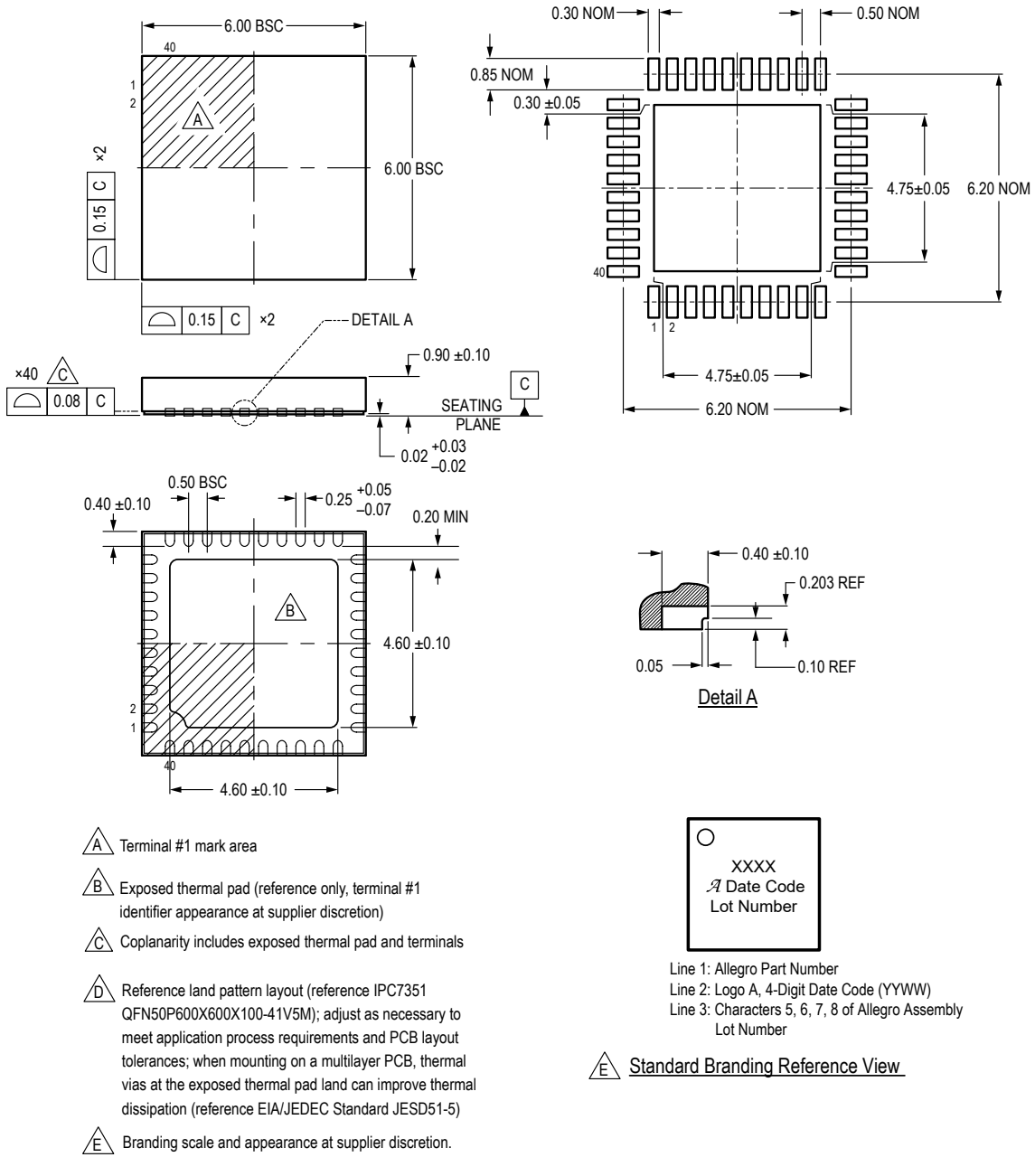
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000378, Rev. 8 and JEDEC MO-220VJJD-2)
Dimensions in millimeters
NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Coplanarity includes exposed thermal pad and terminals

D Reference land pattern layout (reference IPC7351 QFN50P600X600X100-41V5M); adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

E Branding scale and appearance at supplier discretion.

Line 1: Allegro Part Number
Line 2: Logo A, 4-Digit Date Code (YYWW)
Line 3: Characters 5, 6, 7, 8 of Allegro Assembly Lot Number

E Standard Branding Reference View

Figure 46: 6 mm × 6 mm, 40-pin QFN with exposed power pad and wettable flank (suffix EV)

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REVISION HISTORY

Number	Date	Description
–	June 25, 2026	Advance information datasheet released to web
1	September 2, 2026	Initial full datasheet released to web

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