40 V Input, 65 V Output, 160 W, Two-Channel Synchronous Boost/Buck Converter Controllers with Programmable Output and SPI

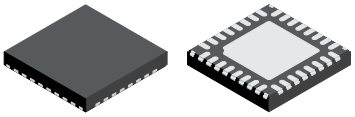
FEATURES AND BENEFITS

- ASIL-Compliant: ASIL B safety element out-of-context (SEooC) developed in accordance with ISO 26262, when used as specified in the safety manual
- Automotive AEC-Q100 Grade 0 qualified
- Two-channel synchronous boost/buck controllers or single channel buck-boost controller
- Wide VIN range: 5 to 37 V operating, 40 V transient
- Output voltage ranges:
  - Boost mode: 16 to 65 V, with 2% accuracy
  - Buck mode: 3.3 to 6 V, with 1.5% accuracy
  - Buck-boost mode: 5 to 22 V, with 2% accuracy
- SPI communication interface
- Programmable SPI features:
  - Output voltage
  - Output overvoltage, input under- and overvoltage
  - Switch peak current
  - Switching frequency
  - Dithering type and amplitude
- Fault detection and telemetry through SPI, with configurable FFn pin
- Supports stand-alone operation (no SPI bus required)
- Programable output voltage
  - 8-bit resolution in boost and buck-boost mode
  - 3.3 V, 4.5 V, 5 V, 5.5 V, and 6 V in buck mode
- Integrated fail-safe gate driver disconnects converter from battery line when short is detected
- Fixed frequency operation, 200 to 450 kHz
- Array mode supports to 2 units (4 phases) to operate in parallel:
  - Units can be synchronized
  - Coordinated fault capability

APPLICATIONS

- Automotive headlight
- Automotive taillight
- Advanced infotainment, instrument cluster
- ADAS domain controller

PACKAGE



5 mm × 5 mm, 32-pin QFN with exposed thermal pad and wettable flank (suffix ET)

Not to scale

DESCRIPTION

The A81850 is a synchronous boost/buck/buck-boost controller with programmable outputs and a SPI communication interface capable of 80 W per channel. The device integrates two half-bridge drivers able to create a dual-channel synchronous boost or buck converter or single-channel synchronous buck-boost converter.

The output voltage in buck mode can be selected through SPI between 3.3 to 6 V in 0.5V steps with a 1.5% accuracy, and can fulfill all typical buck applications scenarios. In boost or buck-boost mode, it is possible to obtain an output voltage, respectively in the range 16 to 65 V and 5 to 22 V, with a 2% accuracy using an 8-bit resolution selector.

The device can operate with SPI communication or without SPI communication in stand-alone mode.

In SPI mode, the device is highly configurable, such as output voltage selection, operating frequency, soft start ramp time, output overvoltage threshold, gate driver current and faults programmability, allowing latched and not-latched modes.

In stand-alone mode, it is possible to operate in boost, buck, or buck-boost mode with 1-channel, 2-channel, or array mode. By configuring external pins, the output voltage is selectable using an external resistor divider, and PGOOD functions as a monitor of the output voltage status.

An integrated fail-safe gate driver can control an external FET to ensure the protection of the battery line when a short is detected on the output of the controller.

The device can be used in array configuration, putting two devices in sequence. In this configuration, connecting the SYNC and SHARE pin between devices, it is possible to deliver up to 320 W without the need for an external compensation network for each channel, thus reducing the number of external components.

The device is supplied in a low-profile 32-lead, 5 mm × 5 mm, 0.5 mm pitch QFN package (suffix ET) with exposed thermal pad and wettable flank.

SPECIFICATIONS

SELECTION GUIDE

Part Number	Package	Packing
A81850KETSR	5 mm × 5 mm, 32-pin QFN with exposed thermal pad and wettable flank	6000 pieces per 13-inch reel

ABSOLUTE MAXIMUM RATINGS [1][2]

Characteristic	Symbol	Notes	Min.	Typ.	Max.	Unit
SWx	V_{SWx}		–0.3	–	75	V
SWx_tran	V_{SWx_tran}	t < 20 ns	–2	–	75	V
BOOTx, GHx	V_{BOOTx}, V_{GHx}		V_{SWx} – 0.3 [3]	–	V_{SWx} + 6.7	V
GHx_tran	V_{GHx_tran}	t < 20 ns	V_{SWx_tran} – 0.3 [3]	–	V_{SWx} + 6.7	V
VOUTx/FBx	$V_{OUTx/FBx}$		–0.3	–	75	V
VIN, EN/FFn, FSG	V_{IN}, $V_{EN/FFn}$, V_{FSG}		–0.3	–	40	V
GLx	V_{GLx}		–0.3	–	6.6	V
GLx_tran	V_{GLx_tran}	t < 20 ns	–2	–	6.6	V
CSn, SCK, MISO/PGOOD, MOSI, SYNC, VIO, COMP1, COMP2/SHARE, VDRV	V_{CSn}, V_{SCK}, $V_{MISO/PGOOD}$, V_{MOSI}, V_{SYNC}, V_{VIO}, V_{COMP1}, $V_{COMP2/SHARE}$, V_{VDRV}		–0.3	–	6.6	V
ISxP, ISxN	V_{ISxP}, V_{ISxN}		V_{SWx} – 0.6	–	V_{SWx} + 0.6	V
Operating Junction Temperature	T_J		–40	–	150	°C
Storage Temperature	T_{STG}		–55	–	150	°C

[1] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only. Functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
[2] All absolute maximum ratings shall be measured with respect to the GND pin.
[3] Minimum value is –0.3 V for $V_{SWx} \le 0$ V or $V_{SWx\_tran} \le 0$ V.

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [1]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$		38	°C/W

[1] Additional thermal information are available on the Allegro website.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table of Contents

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PINOUT DIAGRAM AND TERMINAL LIST

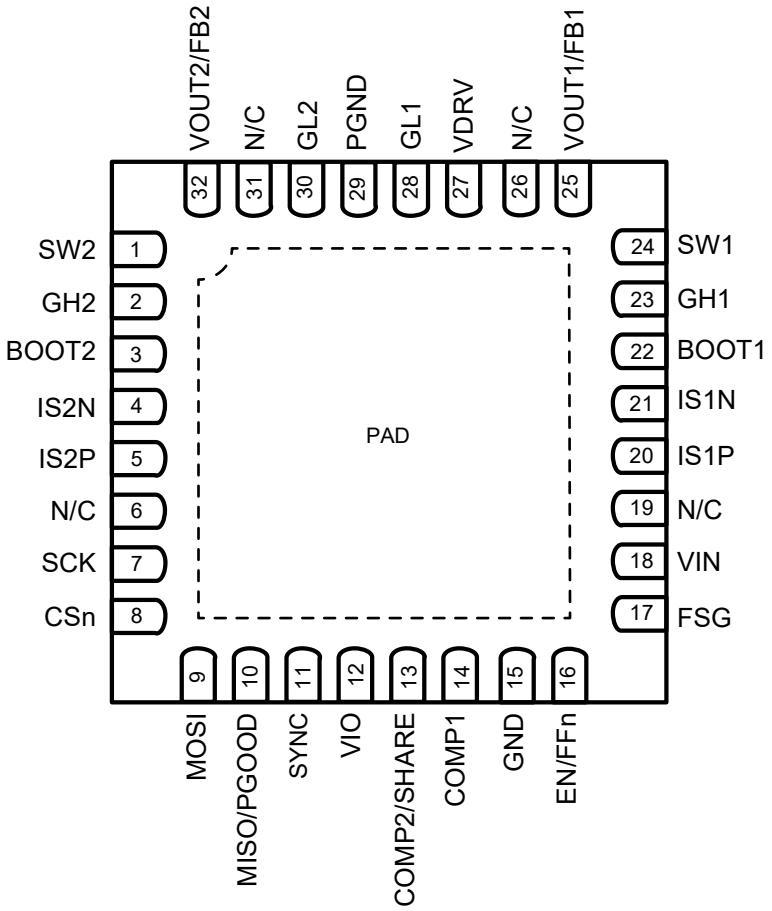


Figure 1: Package ET, 32-Pin QFN Pinout Diagram

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Terminal List Table

Number	Name	Function
1	GH1	Used to drive gate of high-side external FET
2	SW2	Connect to switching node of DC-DC regulator; connect external inductance and load as close as possible to reduce parasitic effects and EMI
3	BOOT2	High-side driver supply; connect external capacitor from BOOT2 to SW2
4	IS2N	Used as Kelvin connection for current sense shunt, negative polarity
5	IS2P	Used as Kelvin connection for current sense shunt, positive polarity
6	N/C	No connect
7	VIO	SPI interface supply
8	MISO/ PGOOD	SPI mode (MISO): Serial interface data output.
		Stand-alone mode (PGOOD): Reports fault detection and coordinates shutdown in array mode after fault event.
9	MOSI	Serial interface data input
10	SCK	Serial interface clock signal input
11	CSn	Serial interface chip select input
12	SYNC	Synchronizes two devices in array mode
13	COMP2/ SHARE	Follower: Compensation pin when not used in array mode connecting COMP2 pin to compensation rail of second channel
		Share: Ties two devices together to communicate error amplifier voltage of master to slave when used in array mode
14	COMP1	Connect to R-C network to stabilize converter
		Follower / array mode slave: connect to ground
15	GND	Ground
16	EN/FFn	EN: Connect to enable monitor; voltage greater than $V_{EN(HI)}$ shall be applied on EN pin to allow device to power up
		FFn: In SPI mode, communicates fault in device
17	VIN	Primary power supply input
18	FSG	Drives gate of external FET used for fail-safe driver function
19	N/C	No connect
20	IS1P	Used as Kelvin connection for current sense shunt, positive polarity
21	IS1N	Used as Kelvin connection for current sense shunt, negative polarity
22	BOOT1	High-side driver supply; connect external capacitor from BOOT1 to SW1
23	SW1	Connect to switching node of DC-DC regulator; connect external inductance and load as close as possible to reduce parasitic effects and EMI
24	GH1	Used to drive gate of high-side external FET
25	VOUT1/ FB1	SPI mode (VOUT1): Voltage feedback of DC-DC regulator; feedback path used as error amplifier input
		Stand-alone mode (FB1): Connect external output voltage resistor divider; feedback path used as error amplifier input
26	N/C	No connect
27	VDRV	Supply for drivers; connect to external decoupling capacitor
28	GL1	Used to drive gate of low-side external FET
29	PGND	Power ground
30	GL2	Used to drive gate of low-side external FET
31	N/C	No connect
32	VOUT2/ FB2	SPI mode (VOUT2): Voltage feedback of DC-DC regulator; feedback path used as error amplifier input
		Stand-alone mode (FB2): Connect external output voltage resistor divider; feedback path used as error amplifier input
–	PAD	Thermal pad

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

FUNCTIONAL BLOCK DIAGRAM

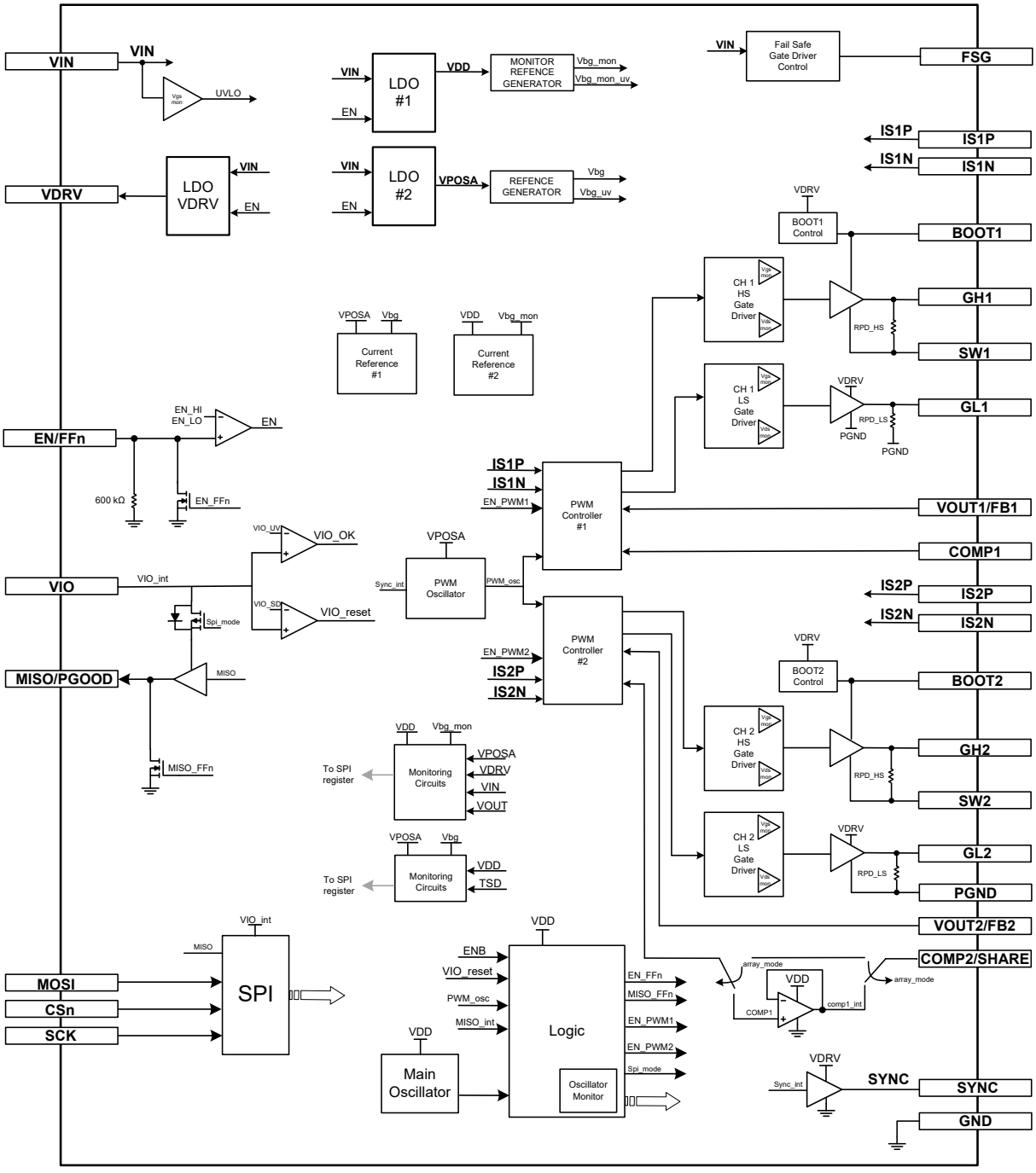


Figure 2: Functional Block Diagram

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

APPLICATION BLOCK DIAGRAMS

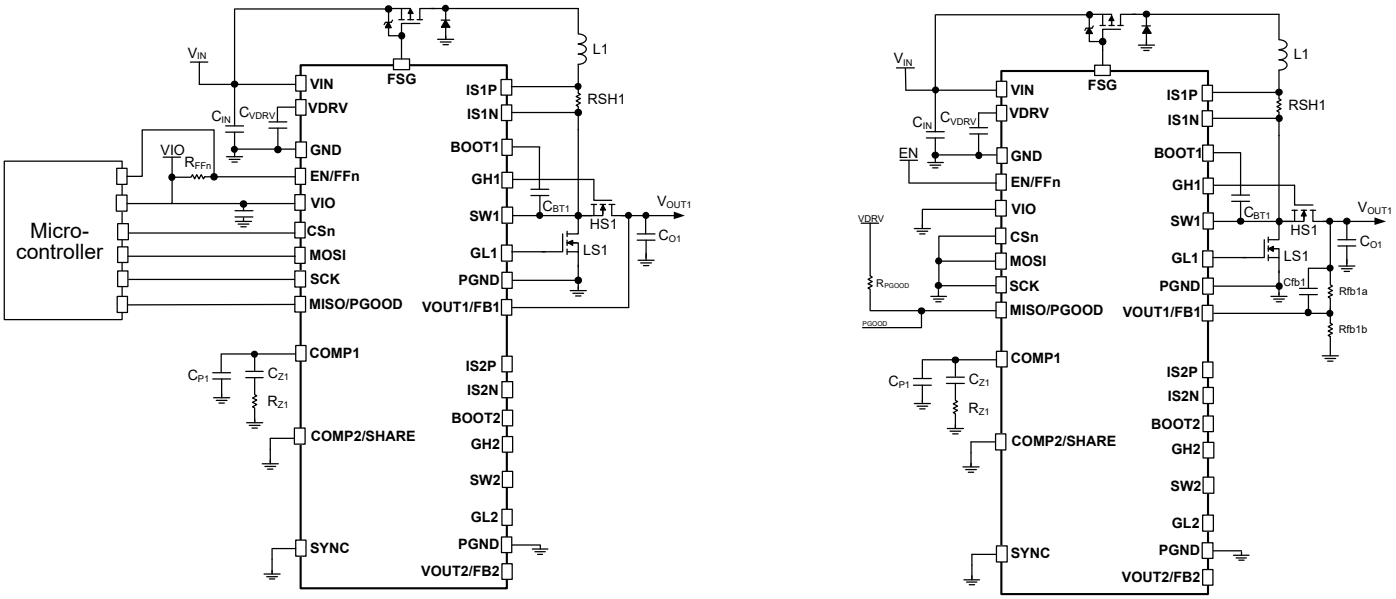


Figure 3: Boost 1 Channel SPI (left) and Standalone (right)

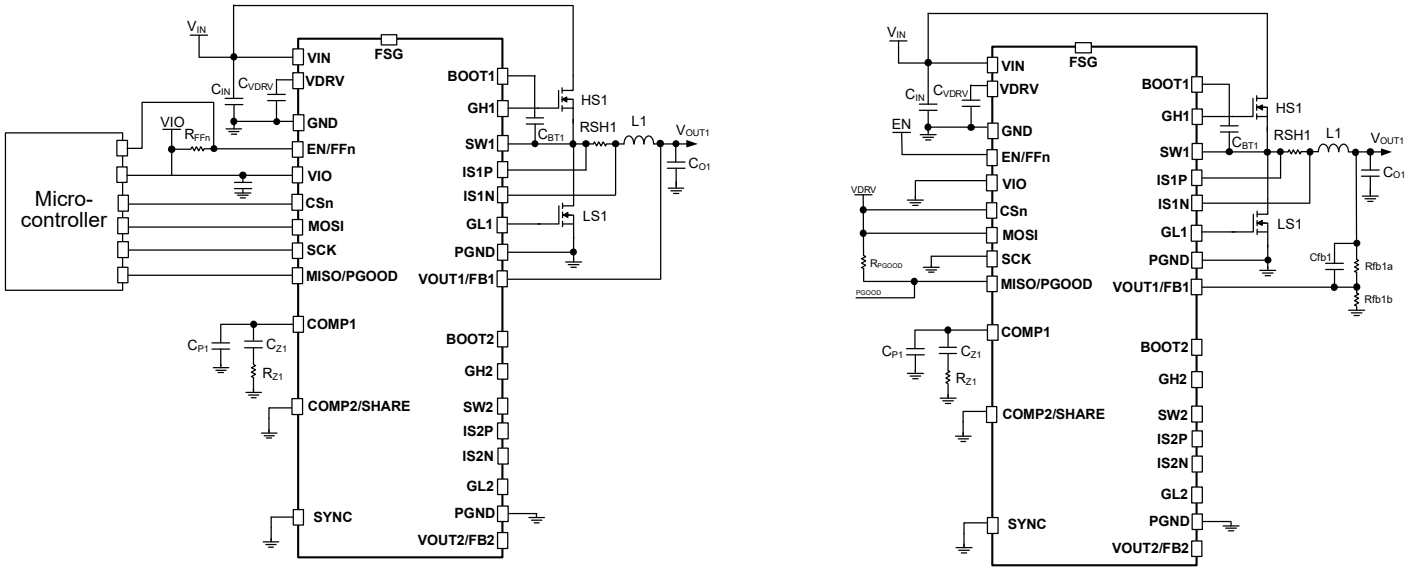


Figure 4: Buck 1 Channel SPI (left) and Standalone (right)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

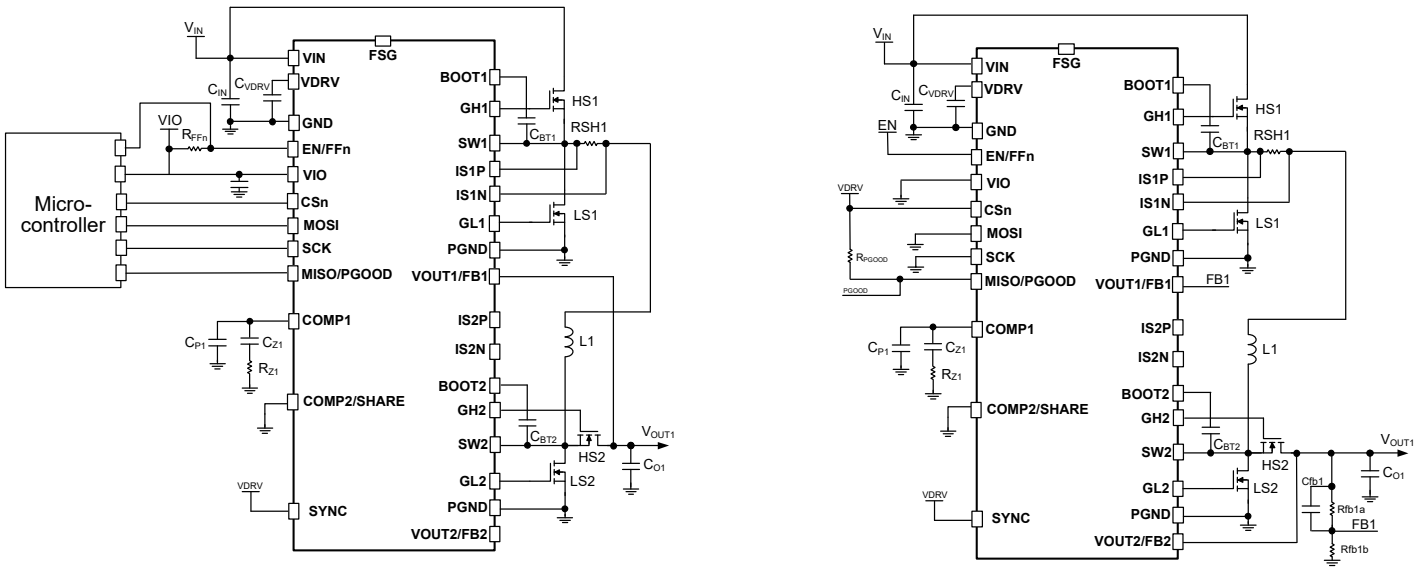


Figure 5: Buck-Boost 1 Channel SPI (left) and Standalone (right)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS: Valid at 5 V ≤ V_{IN} ≤ 37 V, –40°C ≤ T_J ≤ 150°C, V_{EN} high, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
INPUT VOLTAGE SPECIFICATIONS						
Input Voltage Range [1]	V_{IN}	V_{IN} must first rise above $V_{UVLO(ON,MAX)}$	5	–	37	V
Undervoltage Lockout Start	$V_{UVLO(ON)}$	V_{IN} rising ramp	5	5.3	5.6	V
Undervoltage Lockout Stop	$V_{UVLO(OFF)}$	V_{IN} falling ramp	4.3	4.5	4.7	V
VIN Overvoltage Rising	$V_{IN(OV,rising)}$		37	38	39	V
VIN Overvoltage Falling	$V_{IN(OV,falling)}$		36	37	38	V
VIN Overvoltage Detection Delay [1]	$t_{d(VIN,OV)}$		10	–	40	µs
INPUT SUPPLY CURRENT						
Input Current, PWM Mode	$I_{IN(STANDBY)}$	V_{IN} = 12 V, V_{EN} high, no load, no switching	–	7.5	10	mA
Input Shutdown Current	$I_{IN(SD)}$	V_{IN} = V_{SWx} = V_{OUTx} = 12 V, $V_{EN/FFn}$ = V_{IO} = 0 V, T_J = 25°C	–	–	16	µA
ENABLE						
EN High Threshold	$V_{EN(HI)}$	V_{EN} rising	1.5	1.75	2	V
EN Low Threshold	$V_{EN(LO)}$	V_{EN} falling	0.8	0.95	1.1	V
EN Pin Input Current	I_{EN}	V_{EN} = 3.3 V	–	–	11	µA
EN Deglitch Filter [1]	$t_{d(EN)}$		1	1.25	1.5	ms
EN EMI Analog Filter Time [1]	$t_{EN(deg)}$		20	30	40	µs
EN Pulldown Resistance	R_{EN}	V_{EN} = 3.3 V	300	450	600	kΩ
FFn Input High Voltage	$V_{FFn(HI)}$		0.6	0.95	1.3	V
FFn Input Hysteresis Voltage	$V_{FFn(HYS)}$		20	–	70	mV
FFn Pulldown Current	$I_{FFn(PD)}$	V_{EN} = 3.3 V	–	50	100	mA
FFn Pin Checker Filter Time [1]	$t_{FFn(filter)}$		–	–	1	ms
OUTPUT VOLTAGE RANGE						
Output Voltage Range Boost [1]	$V_{OUT(BOOST)}$	$V_{OUT(MAX)}$ / V_{IN} ≤ 8	16	–	65	V
Output Voltage Range Buck	$V_{OUT(BUCK)}$		3.3	–	6	V
Output Voltage Range Buck-Boost [1]	$V_{OUT(BUCKBOOST)}$		5	–	22	V
Boost Output Voltage Selection Accuracy	$V_{OUT(BOOST,LSB)}$	($V_{OUT(BOOST,MAX)}$ – $V_{OUT(BOOST,MIN)}$) / 255	–	192 .15	–	mV
Buck-Boost Output Voltage Selection Accuracy	$V_{OUT(BUCKBOOST,LSB)}$	($V_{OUT(BUCKBOOST,MAX)}$ – $V_{OUT(BUCKBOOST,MIN)}$) / 255	–	66.66	–	mV
Buck Output Voltage Selection A	$V_{OUT(BUCK,A)}$	VOUTx_REGVOLT_SEL[2:0] = 000	–	3.3	–	V
Buck Output Voltage Selection B	$V_{OUT(BUCK,B)}$	VOUTx_REGVOLT_SEL[2:0] = 001	–	4.5	–	V
Buck Output Voltage Selection C	$V_{OUT(BUCK,C)}$	VOUTx_REGVOLT_SEL[2:0] = 010	–	5	–	V
Buck Output Voltage Selection D	$V_{OUT(BUCK,D)}$	VOUTx_REGVOLT_SEL[2:0] = 011	–	5.5	–	V
Buck Output Voltage Selection E	$V_{OUT(BUCK,E)}$	VOUTx_REGVOLT_SEL[2:0] = 100	–	6	–	V
VOUT Leakage	$V_{OUT(LEAK)}$	V_{IN} = V_{SWx} = V_{OUTx} = 12 V , $V_{EN/FFn}$ = V_{IO} = 0 V, T_J = 25°C	–	–	1	µA
Failsafe Pre-Charge Comparator	$V_{d(OUT)}$	V_{IN} – V_{SW}, boost mode	1.95	2.2	2.45	V
Max Soft Start Slew Rate Boost	$SR_{SS(BOOST,OUT)}$	I_{load} = 0 A	–	24	–	V/ms
Max Soft Start Slew Rate Buck	$SR_{SS(BUCK,OUT)}$	I_{load} = 0 A	–	2.5	–	V/ms

[1] Ensured by design and/or characterization, not production tested.

Continued on next page...

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS: Valid at 5 V ≤ V_{IN} ≤ 37 V, –40°C ≤ T_J ≤ 150°C, V_{EN} high, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
OUTPUT VOLTAGE RANGE (continued)						
Maximum Soft Start Slew Rate Buck-Boost	$SR_{SS(BUCKBOOST,OUT)}$	I_{load} = 0 A	–	8	–	V/ms
Soft Start Ramp Time A [1]	$t_{SS(A)}$	I_{load} = 0 A, VOUTx_SS_SEL = 000	0.8	1	1.2	ms
Soft Start Ramp Time B [1]	$t_{SS(B)}$	I_{load} = 0 A, VOUTx_SS_SEL = 001	1.2	1.5	1.8	ms
Soft Start Ramp Time C [1]	$t_{SS(C)}$	I_{load} = 0 A, VOUTx_SS_SEL = 010	2.16	2.7	3.24	ms
Soft Start Ramp Time D [1]	$t_{SS(D)}$	I_{load} = 0 A, VOUTx_SS_SEL = 011 (default)	4	5	6	ms
Soft Start Ramp Time E [1]	$t_{SS(E)}$	I_{load} = 0 A, VOUTx_SS_SEL = 100	6	7.5	9	ms
Soft Start Ramp Time F [1]	$t_{SS(F)}$	I_{load} = 0 A, VOUTx_SS_SEL = 101	8	10	12	ms
Soft Start Ramp Time G [1]	$t_{SS(G)}$	I_{load} = 0 A, VOUTx_SS_SEL = 110	12	15	18	ms
Soft Start Ramp Time H [1]	$t_{SS(H)}$	I_{load} = 0 A, VOUTx_SS_SEL = 111	16	20	24	ms
OUTPUT VOLTAGE ACCURACY						
Output Voltage Accuracy Boost [1]	$V_{OUT(ACC,BOOST)}$	16 V ≤ V_{OUT} ≤ 65 V	–2	–	2	%
Output Voltage Accuracy Buck [1]	$V_{OUT(ACC,BUCK)}$	3.3 V ≤ V_{OUT} ≤ 6 V	–1.5	–	1.5	%
Output Voltage Accuracy Buck-Boost [1]	$V_{OUT(ACC, BUCKBOOST)}$	5 V ≤ V_{OUT} ≤ 22 V	–2	–	2	%
Boost Voltage Dip During Load Transient [1]	$V_{ODIP(BOOST)}$	V_{OUT} = 50 V, V_{IN} =14 V, C_{out} = 47 µF, Δi_{VOUT} / Δt: 1000 mA / 1 µs (CCM), i_{VOUT} from 100 mA to 1 A	–	–	4	%
Buck Voltage Dip During Load Transient [1]	$V_{ODIP(BUCK)}$	V_{OUT} = 4.5 V, V_{IN} = 14 V, C_{out} = 750 µF, Δi_{VOUT} / Δt: 1000 mA / 1 µs (CCM), i_{VOUT} from 100 mA to 1 A	–	–	4	%
Buck-Boost Voltage Dip During Load Transient [1]	$V_{ODIP (BUCKBOOST)}$	V_{OUT} = 18 V, V_{IN} = 14 V, C_{out} = 330 µF, Δi_{VOUT} / Δt: 1000 mA / 1 µs (CCM), i_{VOUT} from 100 mA to 1 A	–	–	4	%
Boost Voltage Overshoot During Load Transient [1]	$V_{OOVER(BOOST)}$	V_{OUT} = 50 V, V_{IN} =14 V, C_{out} = 47 µF, Δi_{VOUT} / Δt: 1000 mA / 1 µs (CCM), i_{VOUT} from 1 A to 100 mA	–	–	6	%
Buck Voltage Overshoot During Load Transient [1]	$V_{OOVER(BUCK)}$	V_{OUT} = 4.5 V, V_{IN} = 14 V, C_{out} = 750 µF, Δi_{VOUT} / Δt: 1000 mA / 1 µs (CCM), i_{VOUT} from 1 A to 100 mA	–	–	6	%
Buck-Boost Voltage Overshoot During Load Transient [1]	$V_{OOVER (BUCKBOOST)}$	V_{OUT} = 18 V, V_{IN} = 14 V, C_{out} = 330 µF, Δi_{VOUT} / Δt: 1000 mA / 1 µs (CCM), i_{VOUT} from 1 A to 100 mA	–	–	6	%
GATE DRIVER						
Low-Side V_{GS} Falling Threshold	$V_{GS(LS,FALL)}$		–	1.4	2.1	V
High-Side V_{GS} Falling Threshold	$V_{GS(HS,FALL)}$		–	2.3	3.2	V
Low-Side Resistance A	$R_{GLx(A)}$	D_DRVx_GATE_CURR_LS_SEL = 00, V_{DRV} = 6 V, $V_{GLx(PD)}$ = 1 V, $V_{GLx(PU)}$ = 5 V	3.4	7	10.6	Ω
Low-Side Resistance B	$R_{GLx(B)}$	D_DRVx_GATE_CURR_LS_SEL = 01, V_{DRV} = 6 V, $V_{GLx(PD)}$ = 1 V, $V_{GLx(PU)}$ = 5 V	1.5	3.5	5.5	Ω
Low-Side Resistance C	$R_{GLx(C)}$	D_DRVx_GATE_CURR_LS_SEL = 10, V_{DRV} = 6 V, $V_{GLx(PD)}$ = 1 V, $V_{GLx(PU)}$ = 5 V	1	2.5	3.9	Ω
Low-Side Resistance D	$R_{GLx(D)}$	D_DRVx_GATE_CURR_LS_SEL = 11, V_{DRV} = 6 V, $V_{GLx(PD)}$ = 1 V, $V_{GLx(PU)}$ = 5 V	0.7	1.9	3.1	Ω

[1] Ensured by design and/or characterization, not production tested.

Continued on next page...

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS: Valid at 5 V ≤ V_{IN} ≤ 37 V, –40°C ≤ T_J ≤ 150°C, V_{EN} high, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GATE DRIVER (continued)						
High-Side Resistance A	$R_{GHx(A)}$	D_DRVx_GATE_CURR_HS_SEL = 00, V_{DRV} = 6 V, $V_{GLx(PD)}$ = 1 V, $V_{GLx(PU)}$ = 5 V	3	5.55	8.1	Ω
High-Side Resistance B	$R_{GHx(B)}$	D_DRVx_GATE_CURR_HS_SEL = 01, V_{DRV} = 6 V, $V_{GLx(PD)}$ = 1 V, $V_{GLx(PU)}$ = 5 V	1.5	2.8	4.1	Ω
High-Side Resistance C	$R_{GHx(C)}$	D_DRVx_GATE_CURR_HS_SEL = 10 V_{DRV} = 6 V, $V_{GLx(PD)}$ = 1 V, $V_{GLx(PU)}$ = 5 V	1	2	3	Ω
High-Side Resistance D	$R_{GHx(D)}$	D_DRVx_GATE_CURR_HS_SEL = 11 V_{DRV} = 6 V, $V_{GLx(PD)}$ = 1 V, $V_{GLx(PU)}$ = 5 V	0.7	1.6	2.5	Ω
High-Side Gate Driver Pull-Down Resistance [1]	$R_{PD(HS)}$		–	700	910	kΩ
Low-Side Gate Driver Pull-Down Resistance [1]	$R_{PD(LS)}$		–	700	910	kΩ
PWM CONTROLLER						
PWM Switching Frequency A	$f_{OSC(A)}$	D_CLK_PWM_FREQ_SEL = 000	–	200	–	kHz
PWM Switching Frequency B	$f_{OSC(B)}$	D_CLK_PWM_FREQ_SEL = 001	–	250	–	kHz
PWM Switching Frequency C	$f_{OSC(C)}$	D_CLK_PWM_FREQ_SEL = 010 (default option)	–	300	–	kHz
PWM Switching Frequency D	$f_{OSC(D)}$	D_CLK_PWM_FREQ_SEL = 011	–	350	–	kHz
PWM Switching Frequency E	$f_{OSC(E)}$	D_CLK_PWM_FREQ_SEL = 100	–	400	–	kHz
PWM Switching Frequency F	$f_{OSC(F)}$	D_CLK_PWM_FREQ_SEL = 101	–	450	–	kHz
PWM Switching Frequency Accuracy	$f_{OSC(ACC)}$		–10	–	10	%
PWM Frequency Dither Range A	$f_{DITH(RNG\_A)}$	D_CLK_PWM_DITH_AMPL_SEL = 00 (default option)	–5	–	+5	% f_{OSC}
PWM Frequency Dither Range B	$f_{DITH(RNG\_B)}$	D_CLK_PWM_DITH_AMPL_SEL = 01	–	0	–	% f_{OSC}
PWM Frequency Dither Range C	$f_{DITH(RNG\_C)}$	D_CLK_PWM_DITH_AMPL_SEL = 10	–10	–	+10	% f_{OSC}
PWM Frequency Dither Range D	$f_{DITH(RNG\_D)}$	D_CLK_PWM_DITH_AMPL_SEL = 11	–15	–	+15	% f_{OSC}
PWM Dither Modulation Frequency	$f_{DITH(FREQ)}$		0	–	+1	% f_{OSC}
Gate Driver Additional Non-Overlap Time A [1]	$t_{NO(A)}$	VOUTx_DEADTIME_SEL = 00, $V_{BOOT} - V_{SW}$ = 4.5 V	7	10	13	ns
Gate Driver Additional Non-Overlap Time B [1]	$t_{NO(B)}$	VOUTx_DEADTIME_SEL = 01, $V_{BOOT} - V_{SW}$ = 4.5 V	14	20	26	ns
Gate Driver Additional Non-Overlap Time C [1]	$t_{NO(C)}$	VOUTx_DEADTIME_SEL = 10, $V_{BOOT} - V_{SW}$ = 4.5 V	28	40	52	ns
Gate Driver Additional Non-Overlap Time D [1]	$t_{NO(D)}$	VOUTx_DEADTIME_SEL = 11, $V_{BOOT} - V_{SW}$ = 4.5 V	42	60	78	ns
Gate Driver Blanking Time [1]	t_{BLANK}		150	200	250	ns
Hiccup Recovery Time [1]	$t_{hic(REC)}$		4.725	5.5	6.275	ms
Hiccup V_{OUT} OC Deglitch Filter Time	$t_{HIC(VOUT)}$		14	16	21	µs
Hiccup STG Counts [1]	t_{HIC}		–	3	–	PWM cycles

[1] Ensured by design and/or characterization, not production tested.

Continued on next page...

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS: Valid at 5 V ≤ V_{IN} ≤ 37 V, –40°C ≤ T_J ≤ 150°C, V_{EN} high, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
OUTPUT VOLTAGE PROTECTION						
Output Voltage Overvoltage A [2]	$V_{OUT(OV,A)}$	D_VOUTx_OV_SEL = 00	V_{OUT} + 2.5%	V_{OUT} + 7.5%	V_{OUT} + 12.5%	V
Output Voltage Overvoltage B [2]	$V_{OUT(OV,B)}$	D_VOUTx_OV_SEL = 01 with $V_{OUT(OV)} \le V_{OUT(OV,MAX)}$	V_{OUT} + 5%	V_{OUT} + 10%	V_{OUT} + 15%	V
Output Voltage Overvoltage C [2]	$V_{OUT(OV,C)}$	D_VOUTx_OV_SEL = 10 with $V_{OUT(OV)} \le V_{OUT(OV,MAX)}$	V_{OUT} + 7.5%	V_{OUT} + 12.5%	V_{OUT} + 17.5%	V
Output Voltage Overvoltage D [2]	$V_{OUT(OV,D)}$	D_VOUTx_OV_SEL = 11 with $V_{OUT(OV)} \le V_{OUT(OV,MAX)}$ (default)	V_{OUT} + 10%	V_{OUT} + 15%	V_{OUT} + 20%	V
Output Voltage Undervoltage	$V_{OUT(UV)}$		V_{OUT} – 15%	V_{OUT} – 10%	V_{OUT} – 5%	V
Output Voltage Deep Undervoltage	$V_{OUT(UV,DEEP)}$	Active during regulation	–50	–40	–30	%
V_{OUT} Overvoltage Detection Delay [1]	$t_{d(VOUT,OV)}$		10	–	40	µs
V_{OUT} Undervoltage Detection Delay [1]	$t_{d(VOUT,UV)}$		10	–	40	µs
Output Voltage Open Threshold SPI Rising	$V_{OUT(OPEN,SPI,rise,th)}$	Active during startup phase in SPI mode	1.96	2.45	2.94	V
Output Voltage Open Threshold SPI Falling	$V_{OUT(OPEN,SPI,fall,th)}$	Active during startup phase in SPI mode	1.48	1.85	2.22	V
Output Voltage Short to Ground Threshold SPI Rising	$V_{OUT(STG,SA,rise,th)}$	Active during startup phase in stand-alone mode	0.36	0.45	0.54	V
Output Voltage Open Pull-Up Current Startup SPI	$I_{VOUT(PU,OPEN,SPI)}$	Only at startup in SPI mode	8	10	12	µA
Output Voltage Open Pull-Up Current Startup Stand-Alone	$I_{VOUT(PU,OPEN,SA)}$	Only at startup in stand-alone mode	16	20	24	µA
Output Voltage Open Pull-Down Current Startup	$I_{VOUT(PD,OPEN,SPI)}$	Only at startup in SPI mode	16.8	21	25.2	µA
Output Voltage Stand-Alone Pull-Up Current Soft Start	$I_{VOUT(PU,SS,SA)}$	Active only during soft start in stand-alone mode	0.6	1	1.4	µA
Output Voltage Stand-Alone Pull-Down Current	$I_{VOUT(PD,SS,SA)}$	Active only during regulation in stand-alone mode	0.1	0.35	0.6	µA
BOOT VOLTAGE						
BOOT Charging Frequency [1]	f_{BOOT}		–	f_{PWM}	–	–
BOOT Voltage	V_{BOOT}	V_{IN} = 12 V, $V_{BOOT} – V_{SW}$	–	5	6	V
BOOT Undervoltage Falling	$V_{BOOT(UV,fall)}$	$V_{BOOT} – V_{SW}$ with V_{IN} = 12 V	3.25	3.5	3.75	V
BOOT Undervoltage Rising	$V_{BOOT(UV,rise)}$	$V_{BOOT} – V_{SW}$ with V_{IN} = 12 V	3.6	3.8	4.05	V
BOOT Undervoltage Deglitch Filter Time	$t_{d(BOOT,UV)}$		6	10	14	µs
BOOT Overvoltage Rising	$V_{BOOT(OV,rise)}$	$V_{BOOT} – V_{SW}$ with V_{IN} = 12 V	6.1	6.4	6.7	V
BOOT Overvoltage Falling	$V_{BOOT(OV,fall)}$	$V_{BOOT} – V_{SW}$ with V_{IN} = 12 V	5.9	6.2	6.5	V
BOOT Overvoltage Deglitch Filter Time	$t_{d(BOOT,OV)}$		80	100	120	µs

[1] Ensured by design and/or characterization, not production tested.
[2] $V_{OUT(OV)}$ shall be selected in order not to exceed $V_{OUT(AMR)}$.

Continued on next page...

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS: Valid at 5 V ≤ V_{IN} ≤ 37 V, –40°C ≤ T_J ≤ 150°C, V_{EN} high, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
DRIVER INTERNAL RAIL VOLTAGE						
VDRV Output Voltage	V_{DRV}	V_{IN} = 12 V	5.18	5.5	5.82	V
VDRV Low Drop Output Voltage	V_{DRV}	V_{IN} = 5V, I_{VDRV} = 30 mA	4.5	–	–	V
VDRV Undervoltage Threshold Falling	$V_{DRV(UV,fall)}$		3.9	4.2	4.5	V
VDRV Undervoltage Threshold Rising	$V_{DRV(UV,rise)}$		4.25	4.55	4.85	V
VDRV Overvoltage Threshold Rising	$V_{DRV(OV,fall)}$		6.1	6.3	6.5	V
VDRV Overvoltage Threshold Falling	$V_{DRV(OV,rise)}$		5.9	6.075	6.25	V
VDRV Current Limitation	I_{VDRV}		180	–	280	mA
CURRENT SENSE						
Voltage Sensed A [1]	$V_{RSH(A)}$	with RSH A	–25	–	155	mV
Voltage Sensed B [1]	$V_{RSH(B)}$	with RSH B	–50	–	310	mV
Voltage Sensed C [1]	$V_{RSH(C)}$	with RSH C	–75	–	465	mV
Voltage Sensed D [1]	$V_{RSH(D)}$	with RSH D	–100	–	620	mV
Overcurrent Threshold	$I_{OCL(TH)}$		23	27	31	A
Overcurrent Hysteresis	$I_{OCL(HYS)}$		–	5		%
Negative Overcurrent Threshold	$I_{NOCL(TH)}$		–4	–3.25	–2.5	A
Negative Overcurrent Hysteresis	$I_{NOCL(HYS)}$		–	3	–	%
Multiphase Current Limitation Threshold Boost	$I_{CLIM(TH,Boost)}$	Boost mode, V_{IN} = 13.5 V	–48%	5.66 [3]	48%	A
Multiphase Current Limitation Threshold Buck	$I_{CLIM(TH,Buck)}$	Buck mode, V_{OUT} = 6 V	–43%	12.3 [3]	43%	A
Multiphase Current Limitation Threshold Maximum	$I_{CLIM(TH,MAX)}$	Buck-boost mode and buck mode with V_{OUT} ≤ 5 V	–20%	15.5 [3]	20%	A
Multiphase Current Limitation Hysteresis	$I_{CLIM(HYS)}$	V_{IN} = 13.5 V	–	5.6	–	%
Multiphase Disable Threshold 1	$I_{MPX(TH1)}$	CH2, V_{IN} = 13.5 V	–	$I_{CLIM(TH)}$ × 0.75 × 1/2	–	A
Multiphase Disable Threshold 2	$I_{MPX(TH2)}$	CH3, V_{IN} = 13.5 V	–	$I_{CLIM(TH)}$ × 0.75 × 2/3	–	A
Multiphase Disable Threshold 3	$I_{MPX(TH3)}$	CH4, V_{IN} = 13.5 V	–	$I_{CLIM(TH)}$ × 0.75 × 3/4	–	A
Multiphase Disable Hysteresis 1	$I_{MPX(HYS1)}$	CH2, V_{IN} = 13.5 V	–	3	–	%
Multiphase Disable Hysteresis 2	$I_{MPX(HYS2)}$	CH3, V_{IN} = 13.5 V	–	3	–	%
Multiphase Disable Hysteresis 3	$I_{MPX(HYS3)}$	CH4, V_{IN} = 13.5 V	–	4	–	%

[1] Ensured by design and/or characterization, not production tested.
[3] See section Current Limitation Evaluation and Multiphase Disable Thresholds.

Continued on next page...

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS: Valid at 5 V ≤ V_{IN} ≤ 37 V, –40°C ≤ T_J ≤ 150°C, V_{EN} high, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
FAIL-SAFE						
Fail-Safe Switch Pulldown Current	$I_{FS(PD)}$	V_{FSG} > 2 V	40	50	60	µA
Fail-Safe Internal Switch Off Resistance	$R_{FS(SO)}$		350	500	650	kΩ
Fail-Safe Switch Timeout [1]	t_{FSG}		9.4	10.5	11.6	ms
COMP, SHARE, AND SYNC						
COMP Short to High Threshold	$V_{COMP(STH,th)}$	Active during startup phase in SPI and stand-alone modes	2.3	2.65	3	V
COMP Short to Ground Threshold	$V_{COMP(STG,th)}$	Active also during normal operation	0.120	0.145	0.170	V
COMP Check Source Current	$I_{COMP(PU)}$		–50	–40	–30	µA
COMP Check Sink Current	$I_{COMP(PD)}$		10	15	20	µA
COMP Clamp High Voltage	$V_{COMP(clamp,high)}$		–	–	3	V
COMP Clamp Low Voltage	$V_{COMP(clamp,low)}$		300	400	–	mV
SHARE Buffer Input Offset	$V_{SHARE(off)}$		–10	–	10	mV
SHARE Buffer Source Current	$I_{SHARE(PU)}$		–100	–	–	uA
SHARE Buffer Sink Current	$I_{SHARE(PD)}$		–	–	1.1	mA
SYNC Output Low Voltage	$V_{SYNC(OL)}$	$I_{SYNC(OL)}$ = 1 mA	–	–	0.4	V
SYNC Output High Voltage	$V_{SYNC(OH)}$	$I_{SYNC(OH)}$ = –1 mA	0.8 × V_{DRV}	–	–	V
SYNC Input High Voltage	$V_{SYNC(IH)}$	Voltage rising	0.6	0.95	1.3	V
SYNC Input Hysteresis	$V_{SYNC(HYS)}$		20	–	70	mV
INTERNAL LOOP PARAMETERS						
ErrAmp Transconductance [1]	gm_{EA}		600	800	1000	uA/V
ErrAmp Open Loop Gain [1]	G0		60	85	100	dB
ErrAmp Source Current	$I_{EA(PU)}$		–120	–	–80	µA
ErrAmp Sink Current	$I_{EA(PD)}$		80	–	120	µA
Boost Resistor Divider Ratio	$RatioFBK_{boost}$		–	43.333	–	V/V
Buck Resistor Divider Ratio	$RatioFBK_{buck}$		–	4	–	V/V
Buck-Boost Resistor Divider Ratio	$RatioFBK_{buckboost}$		–	14.667	–	V/V
Stand-Alone Resistor Divider Ratio	$RatioFBK_{SA}$		–	1	–	V/V
Power Transconductance	gm_{PWR}		–	15	–	A/V
ASC Reference Current	$I_{ASC(13.5V)}$	V_{IN} = 13.5 V	–	1800	–	nA
APL Current Limitation	$I_{APL(13.5V)}$	V_{IN} = 13.5 V	25	30.9	35.5	µA
Main Clock Frequency	$f_{mainOSC}$		7	8	9	MHz

[1] Ensured by design and/or characterization, not production tested.

Continued on next page...

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS: Valid at 5 V ≤ V_{IN} ≤ 37 V, –40°C ≤ T_J ≤ 150°C, V_{EN} high, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
THERMAL CHARACTERISTICS						
Temperature Warning Threshold [1]	T_{WARN}		150	–	–	°C
Temperature Warning Threshold Detection Delay [1]	$t_{d(WARN)}$		–	12	–	µs
Temperature Shutdown Threshold [1]	T_{SD}		160	175	–	°C
Temperature Shutdown Threshold Detection Delay [1]	$t_{d(SD)}$		–	12	–	µs
Thermal Warning/Shutdown Hysteresis [1]	T_{HYS}		–	10	–	°C
SPI INTERFACE						
VIO Undervoltage Threshold	$V_{IO(UV)}$		2.6	2.7	2.8	V
VIO Shutdown Threshold	$V_{IO(SD)}$		0.4	0.6	0.8	V
VIO Shutdown Deglitch Filter Time	$t_{d(VIO)}$		80	100	120	µs
VIO Current	I_{VIO}		–	–	100	µA
SPI Input High Voltage (CS, MOSI, SCK)	$V_{SPI(IH)}$	Voltage rising	–	–	2	V
SPI Input Low Voltage (CSn, MOSI, SCK)	$V_{SPI(IL)}$	Voltage falling	0.8	–	–	V
SPI Input Hysteresis (CSn, MOSI, SCK)	$v_{SPI(HYS)}$	All logic inputs	300	450	600	mV
SPI MOSI and SCK Input Pull-Down	R_{PD}	V_{MOSI} or V_{SCK} = 3.3 V	–	50	–	kΩ
SPI CSn Input Pull-Up to 3.3 V	R_{PU}		–	50	–	kΩ
SPI MISO Output Low Voltage	V_{OL}	I_{OL} = 1 mA	–	–	0.4	V
SPI MISO Output High Voltage	V_{OH}	I_{OH} = –1 mA	0.8 × V_{IO}	–	–	V
PGOOD Input High Voltage	$V_{PGOOD(HI)}$		0.6	0.95	1.3	V
PGOOD Input Hysteresis Voltage	$V_{PGOOD(HYS)}$		20	–	70	mV
PGOOD Pulldown Current	$I_{PGOOD(PD)}$	$V_{MISO/PGOOD}$ = 3.3 V	–	–	50	mA
SPI Clock Frequency [1]	f_{SCK}	MISO pins, C_L = 20 pF	0.1	–	10	MHz
SPI Frame Rate [1]	t_{SPI}		2.94	–	294	kHz
SPI Clock High Time [1]	$t_{SCK(H)}$	A in Figure 6	40	–	–	ns
SPI Clock Low Time [1]	$t_{SCK(L)}$	B in Figure 6	40	–	–	ns
SPI Chip Select Lead Time [1]	$t_{CS(LD)}$	C in Figure 6	30	–	–	ns
SPI Chip Select Lag Time [1]	$t_{CS(LG)}$	D in Figure 6	30	–	–	ns
SPI Chip Select High Time [1]	$t_{CS(H)}$	E in Figure 6	400	–	–	ns
SPI Data Out (MISO) Enable Time [1]	$t_{MISO(EN)}$	F in Figure 6	–	–	40	ns
SPI Data Out (MISO) Disable Time [1]	$t_{MISO(D)}$	G in Figure 6	–	–	30	ns
SPI Data Out (MISO) Valid Time from SCK Falling [1]	$t_{MISO(V)}$	H in Figure 6	–	–	40	ns
Data Out (MISO) Hold Time from SCK Falling [1]	$t_{MISO(H)}$	J in Figure 6	5	–	–	ns
Data In (MOSI) Set-Up Time to SCK Rising [1]	$t_{MOSI(SU)}$	K in Figure 6	15	–	–	ns
Data In (MOSI) Hold Time from SCK Rising [1]	$t_{MOSI(H)}$	L in Figure 6	10	–	–	ns

[1] Ensured by design and/or characterization, not production tested.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

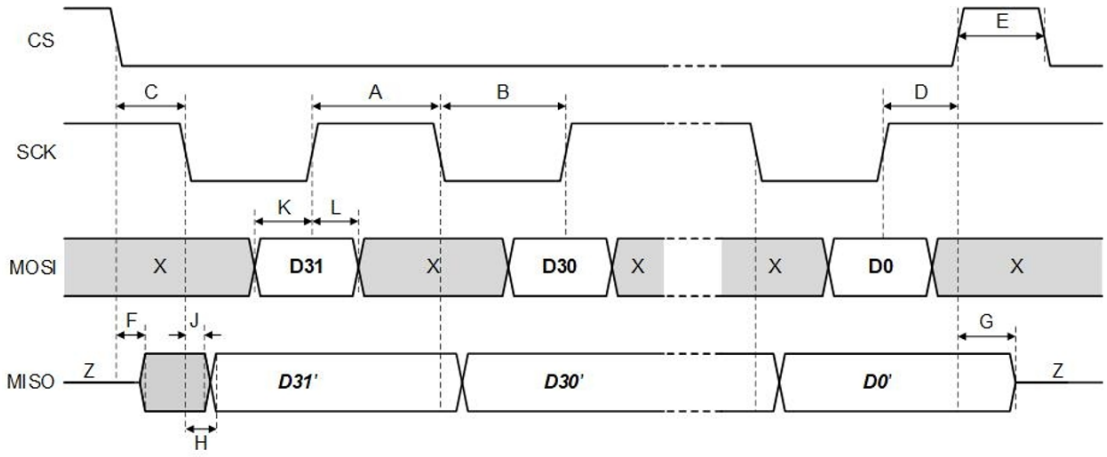


Figure 6: Serial Interface Timing for Write and Read Cycles

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

MAIN EXTERNAL COMPONENTS

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Shunt Resistor A	$R_{SH(A)}$	D_CSx_RSHUNT_SEL = 00 (default)	4.9	5	5.1	mΩ
Shunt Resistor B	$R_{SH(B)}$	D_CSx_RSHUNT_SEL = 01	9.8	10	10.2	mΩ
Shunt Resistor C	$R_{SH(C)}$	D_CSx_RSHUNT_SEL = 10	14.7	15	15.3	mΩ
Shunt Resistor D	$R_{SH(D)}$	D_CSx_RSHUNT_SEL = 11	19.6	20	20.4	mΩ
Cp Boost Capacitor	$C_{p(boost)}$		–	0.22	4	nF
Cz Boost Capacitor	$C_{z(boost)}$		10	150	200	nF
Rz Boost Resistor	$R_{z(boost)}$		4.7	22	33	kΩ
Cp Buck Capacitor	$C_{p(buck)}$		–	1.5	4	nF
Cz Buck Capacitor	$C_{z(buck)}$		10	15	200	nF
Rz Buck Resistor	$R_{z(buck)}$		4.7	22	33	kΩ
Cp Buck-Boost Capacitor	$C_{p(buckboost)}$		–	2.4	4	nF
Cz Buck-Boost Capacitor	$C_{z(buckboost)}$		10	47	200	nF
Rz Buck-Boost Resistor	$R_{z(buckboost)}$		4.7	10	33	kΩ
VDRV Capacitor	C_{VDRV}		–	4.7	–	µF
BOOT Capacitor	C_{BOOT}		110	220	286	nF
Inductor A	$L_{out(A)}$	D_CLK_PWM_FREQ_SEL = 200 kHz, 250 kHz	–	15	–	µH
Inductor B	$L_{out(B)}$	D_CLK_PWM_FREQ_SEL = 300 kHz, 350 kHz	–	10	–	µH
Inductor C	$L_{out(C)}$	D_CLK_PWM_FREQ_SEL = 400 kHz, 450 kHz	–	6.8	–	µH
FBxb Resistor	R_{fbxb}	Resistance for feedback to GND in stand-alone mode; Nph = number of phases	25/Nph	50/Nph	75/Nph	kΩ

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

FUNCTIONAL DESCRIPTION

Device Power-Up

The A81850 is powered up when the EN pin is high, the supply voltage (V_{IN}) is above the UVLO upper threshold ($V_{UVLO(ON)}$), and the VIO pin is high for SPI mode or tied to ground for stand-alone operation. The power-up sequence is shown in Figure 7. During the power-up sequence, if the EN pin stays high for shorter than the deglitch filter time ($t_{d(EN)}$), then the device is switched off immediately.

While operating in stand-alone mode, EN is never latched, and the device automatically shuts down when V_{EN} falls below $V_{EN(LO)}$.

While operating in SPI mode, after the deglitch filter time is exceeded, EN is latched, and the pin is used by the A81850 as an interrupt pin (FFn). The FFn toggles low once a fault is detected, as described in the fault table.

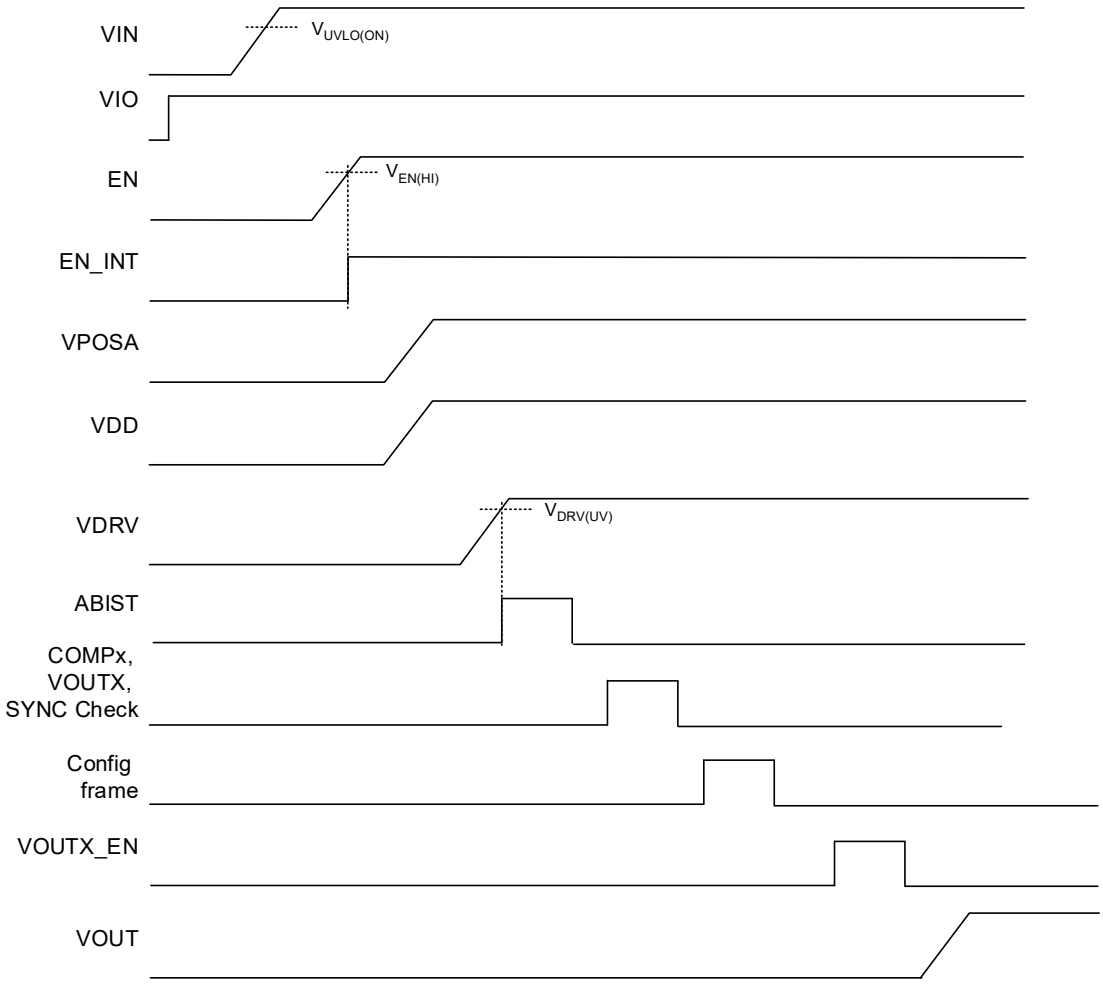


Figure 7: Power-Up Timing

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Power Down

The A81850 can be powered down in different ways either in SPI or standalone mode:

- **V_{IN} Lower Than UVLO Threshold (available for SPI and SA mode):** If the input voltage falls below $V_{UVLO(OFF)}$ threshold, then the A81850 shuts down all internal rails.

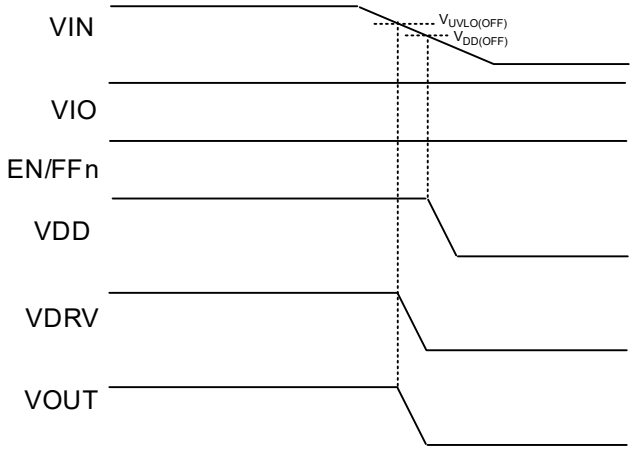


Figure 8: V_{IN} Lower Than UVLO Threshold

- **EN Unlatch (available in SPI mode):** In SPI mode, after the power sequence, the enable signal is latched and the EN/FFn pin works as FFn, fault pin. The enable signal can be unlatched writing the register bit EN_LAT_S = 0 and; as a result, if the signal on the EN/FFn pin is low, the device shuts down. The pin can either be low due to external forcing or due to internal activation of the pulldown, consequently, to a fault.

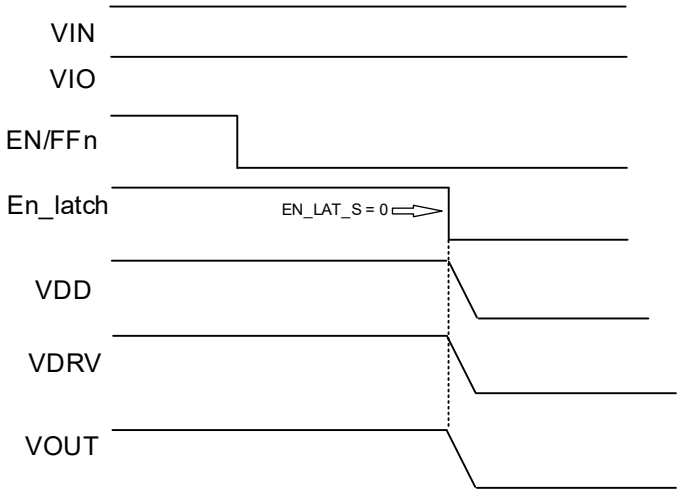


Figure 9: EN Unlatch

- **V_{IO} Lower Than Shutdown Threshold (available in SPI mode):** If V_{IO} goes below the undervoltage threshold, the fault is detected in SPI, and the microcontroller is able to detect the fault. The V_{IO} shutdown threshold, lower than the undervoltage threshold, is used to unlatch EN and force a shutdown in the device; therefore, the open-drain MOSFET forcing FFn low is released, and the pin returns to function as the EN pin waiting for a new power-up.

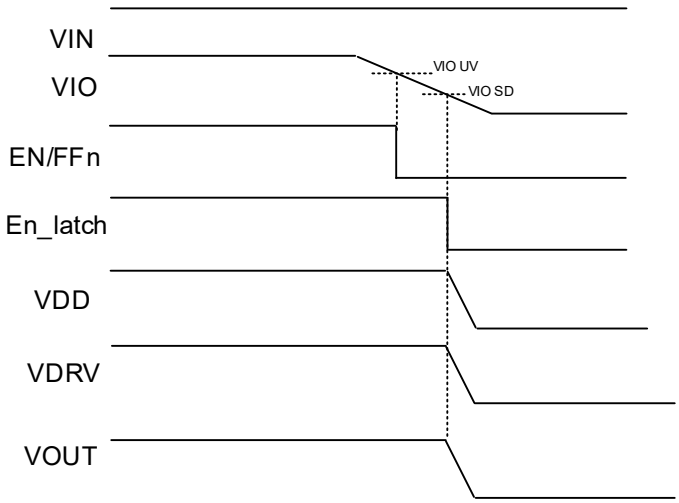


Figure 10: VIO Lower Than Shutdown Threshold

- **EN Forced Low (available in SA mode):** While operating in stand-alone mode, EN is never latched, and the device automatically shuts down when V_{EN} falls below $V_{EN(LO)}$.

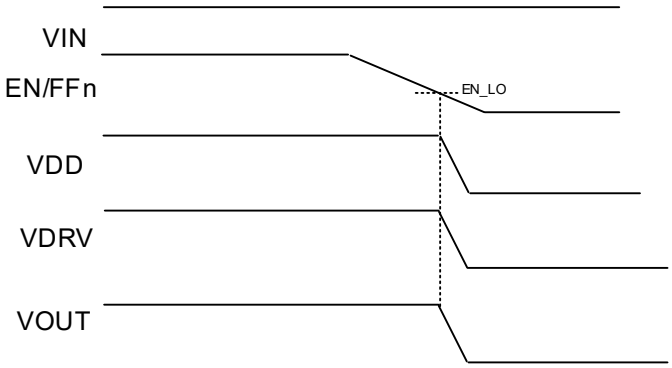


Figure 11: EN Forced Low

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Device Configurations

The A81850 integrates two half-bridge drivers able to create a dual-channel synchronous boost or buck converter or one channel synchronous buck-boost converter with adaptive output voltage input. The device is meant to create a stable, single or dual, higher or lower, voltage supply rail to be distributed to local or remote loads.

To fulfill all the applicative operations, both stand-alone mode and SPI mode are available for the A81850 device. Moreover, the device can be used in an array configuration delivering up to 320 W.

SPI Configuration

When the device is powered up in SPI mode, thus with V_{IO} higher than $V_{IO(UV)}$, it is necessary to send at least one configuration frame (configuration frame 5) for the device to operate.

A list of items can be configured only during the configuration window and only with a reset can these be changed. When a configuration frame with the DC-DC configuration bits is sent, the configuration is locked in the device. All the other elements, if not configured, will assume the default value.

Configuration frame 5 (mandatory):

- DC-DC configuration (boost 1ch, buck array master, etc.)
- Soft start ramp time
- Switching frequency
- Dithering amplitude
- Multiphase dynamic power

Configuration frame 4 allows the user to configure the shunt resistance used, this register needs to be configured before the Config_5 register, otherwise the default value is selected.

All other configurable items can always be modified during operative mode.

- Output voltage
- Output overvoltage threshold
- Battery undervoltage lockout threshold
- Dithering
- LS/HS gate drive resistances
- Gate driver non-overlap time

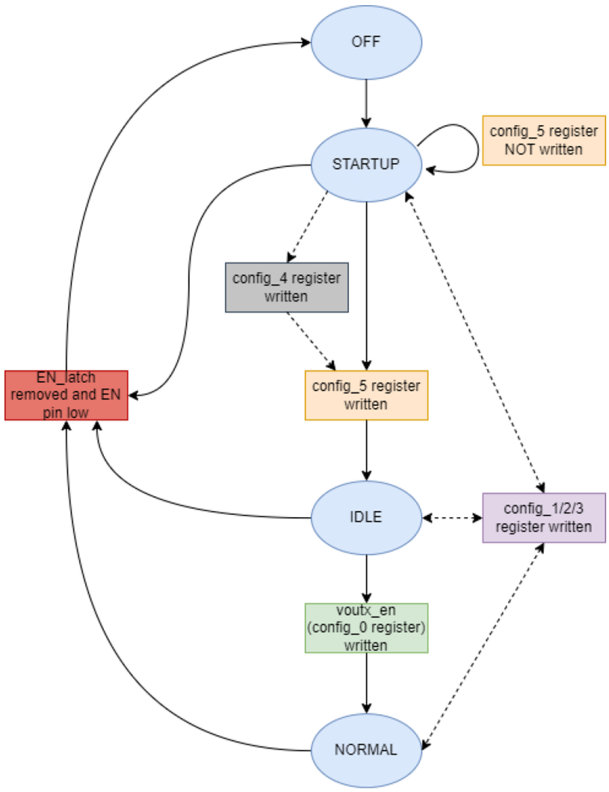


Figure 12

Array Configuration

The A81850 can be used in array configuration when used in boost or buck mode, allowing the device to use up to 2 units/4 channels in parallel. The channels have a 90° phase shift and the SYNC pin should be tied together for operations synchronization.

While working in array mode, the master channel should have the voltage feedback pin (VOUT1) connected to the output voltage and the compensation network connected only on COMP1 pin. The follower instead should have VOUTX and COMPx pin tied to ground; SHARE/COMP2 and EN/FFn should be connected to the master device.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

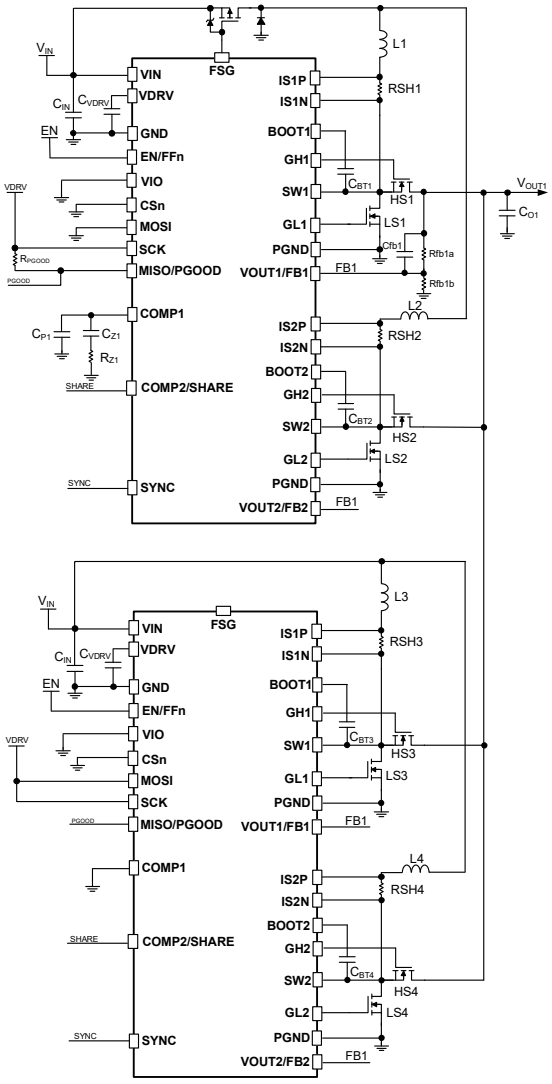


Figure 13: BOOST 320 W Stand-Alone Configuration

During the powerup sequence in array mode, each device checks the configuration received via SPI or SCK, CSn, and MOSI voltage to determine whether the IC is the master or the slave. The two device's EN/FFn pins should be tied together for coordinated fault detection and shutdown. SPI communication is enabled, registers are read, and internal parameters are set.

Stand-Alone Configurations

The A81850 can be used in stand-alone configuration when the SPI feature is not available. In this operative mode, it keeps available all types of configurations for buck, boost, or buck-boost, delivering up to 320 W at the output.

The pins SCK, CSn, and MOSI change their functionality and are used for selecting one of the available configurations as reported in Table 3.

If VIO is pulled low and EN is kept high, the device can power-up and provides the output voltage with respect to the resistor divider placed between the switching node and ground with the halfway point connected to the feedback pin.

The faults reaction is still present in stand-alone mode, and the device asserts the PGOOD pin low if a fault related to the output voltage functionality is triggered, as reported in the Fault Table.

COMPx Pin Check

During each power-up sequence, the device assesses the state of the COMPx pin to determine the intended operational mode (refer to the Device Operative Mode Configuration section) and to identify whether the pin is shorted to ground (GND), open, or connected to a compensation network.

This evaluation involves sourcing a pull-up current followed by sinking a pull-down current through the COMPx pin. Several scenarios and their corresponding device responses are outlined as follows:

1. Short to GND: If the short-to-ground comparator output is high at the conclusion of the pull-up phase, the device interprets the COMPx pin as being shorted to GND.
2. Open Circuit: If the short-to-high comparator output is high after the pull-up phase, and the short-to-ground comparator output is also high subsequent to the pull-down phase, the device concludes that the COMPx pin is open.
3. Compensation Network Connected: Any other combination of comparator outputs (different from the short-to-GND and open-circuit scenarios described above) suggests the presence of a compensation network connected to the COMPx pin.

Table 1

Pull-Up Result		Pull-Down Result		COMP Status
A_COMPX_STH	A_COMPX_STG	A_COMPX_STH	A_COMPX_STG	
1	0	0	1	Open
0	1	x	x	Short to ground
0	0	0	1	Compensation network
1	0	0	0	
0	0	0	0	

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Fail-Safe Driver

The A81850 integrates an optional fail-safe driver specifically designed to enhance the robustness of boost converter applications. This feature controls an external FET placed between the input supply and the boost inductor. In the event of an output short-circuit, the A81850 monitoring the output node can promptly detect the fault condition. Upon detection, the device disconnects the fail-safe FET, thereby interrupting the current path and providing critical protection to the battery and other power stage components.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

EXTERNAL COMPONENT SELECTION

Switching Frequency Coil Relation

The selection of the inductance should be decided with respect to the chosen operating switching frequency.

Table 2: Frequency Coil

f_{SW} × L = 3 Hz H; $V_{IN(TYP)}$ = 13.5 V; P_O = 80 W			
Frequency (kHz)	Inductance (µH)	Max PP Current Ripple (boost is worst case) @ V_{IN} Typ (A)	Max Crossover Frequency @ V_{IN} Typ (boost mode) (kHz)
200	15	5	12.9
250	15	4.3	12.9
300	10	5.4	19.3
350	10	4.6	19.3
400	6.8	6	28.5
450	6.8	5.3	28.5

Output Capacitance Evaluation

The output capacitance of the controller has an impact on the dynamic performances that are improved while the capacitance increases. Conversely, the behavior during soft start may be impacted if the capacitance is too high because the soft start time may end before the output charge is completed.

The minimum output capacitance suggested by Allegro is calculated using the following equations.

Equation 1:

$$C_{O(BOOST)} = \frac{P_O(max)}{\pi V_O^2 f_{P(BOOST)}} \text{ where } f_{P(BOOST)} = 150 \text{ Hz}$$

Equation 2:

$$C_{O(BUCK)} = \frac{P_O(max)}{\pi V_O^2 f_{P(BUCK)}} \text{ where } f_{P(BUCK)} = 550 \text{ Hz}$$

Equation 3:

$$C_{O(BUCKBOOST)} = 1 \text{ mF for } 5 \text{ V} \le V_O \le 13 \text{ V}$$

Equation 4:

$$C_{O(BUCKBOOST)} = \frac{P_O}{\pi V_O^2 f_{P(BUCKBOOST)}}$$

$$\text{where } f_{P(BUCKBOOST)} = 150 \text{ Hz for } V_O \ge 13 \text{ V}$$

Crossover Frequency and Compensation Network Evaluation

The compensation network listed in the Electrical Characteristics table, Main External Components section, represents a set of values that can fit all the range of work of the regulator in the specified mode (buck, boost, or buck-boost).

However, if the compensation network is changed, it is recommended to follow the guidelines below to keep the controller stable.

In boost mode, Allegro's suggestion is to keep the crossover frequency, f_C, below one third of the right-half plane zero (f_{zRHP}).

To evaluate the position of the zero, use the following formula.

Equation 5:

$$fz_{RHP} = \frac{V_{IN}^2}{2\pi L P_O} \qquad f_{C(BOOST)} \le \frac{1}{3} fz_{RHP}$$

Given the crossover frequency, it is possible to evaluate the zero resistance of the compensation network from the crossover frequency formula.

Equation 6:

$$R_z = f_{C(BOOST)} \times \frac{V_{OUT}}{V_{IN}} \times \frac{RATIO_{FBK(BOOST)}}{G_{M(EA)}} \times \frac{2\pi C_{O(BOOST)}}{G_{M(PWR)}}$$

The pole of the compensation network should be dimensioned with respect to the zero introduced by the ESR of the output capacitance.

Equation 7:

$$fz_{ESR} = fp_{CTRL}$$

$$\text{with } fz_{ESR} = \frac{1}{2\pi ESR_{CO} C_{O(BOOST)}} \qquad fp_{CTRL} = \frac{1}{2\pi R_Z C_P}$$

$$\text{so} \qquad C_P = \frac{ESR_{CO} C_{O(BOOST)}}{R_Z}$$

The zero capacitance is suggested to be dimensioned to have the compensation zero at a frequency lower than the output pole.

Equation 8:

$$f_{Z(CTRL)} = f_{P(BOOST)}$$

$$C_Z = \frac{1}{2\pi R_Z f_{P(BOOST)}}$$

In buck mode, the most stringent condition for crossover fre-

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

quency comes from the switching frequency. It is suggested to keep the crossover frequency at least 5 times below the switching frequency.

Equation 9:

$$f_{C(BUCK)} \leq \frac{1}{5} f_{SW}$$

From the crossover frequency formula of the buck, it is possible to evaluate the zero resistance of the compensation network.

Equation 10:

$$R_z = \frac{2\pi\, C_{O(BUCK)} f_{C(BUCK)}\, RATIO_{FBK(BUCK)}}{G_{M(EA)}\, G_{M(PWR)}}$$

The zero of the compensation network should be placed between the crossover frequency and the first pole of the power stage; as a result, it is possible to evaluate C_Z of the buck.

Equation 11:

$$\frac{4}{2\pi\, R_Z f_{C(BUCK)}} < C_Z < \frac{14}{2\pi\, R_Z\, 1.5\, f_{P(BUCK)}}$$

To maximize system stability, i.e., high gain and phase margins, use a higher value of C_Z. To optimize transient recovery time, although at the expense of low stability margins, use a lower value of C_Z.

The pole of the compensation network should be dimensioned with respect to the zero introduced by the ESR of the output capacitance.

Equation 12:

$$fz_{ESR} = fp_{CTRL}$$

$$\text{with } fz_{ESR} = \frac{1}{2\pi\, ESR_{CO} C_{O(BUCK)}} \qquad fp_{CTRL} = \frac{1}{2\pi\, R_Z C_P}$$

$$\text{so} \qquad C_P = \frac{ESR_{CO} C_{O(BUCK)}}{R_Z}$$

Peak Inductor Current Evaluation

It is possible to evaluate the peak inductor current with respect to the desired application conditions. The equations are the following.

Equation 13:

$$I_{LPEAK(BOOST)} = \frac{V_O\, D\, (1 - D)}{2\, f_{SW}\, L} = \frac{V_{IN}}{2\, f_{SW}\, L}\left(1 - \frac{V_{IN}}{V_O}\right)$$

Equation 14:

$$I_{LPEAK(BUCK)} = \frac{V_O\, D\, (1 - D)}{2\, f_{SW}\, L} = \frac{V_O}{2\, f_{SW}\, L}\left(1 - \frac{V_O}{V_{IN}}\right)$$

Current Limitation Evaluation and Multiphase Disable Thresholds

The device implements a current limitation feature to control the maximum current flowing. This parameter varies with respect to application.

In boost mode: $I_{CLIM} = \frac{P_O(max)}{V_{IN}}$, where $P_{O(MAX)} = 100$ W.

In buck-boost mode, I_{CLIM} is fixed to: $I_{CLIM(TH,MAX)} = 20$ A.

In buck mode: $I_{CLIM} = \frac{P_O(max)}{V_{OUT}}$ for $V_{OUT} > 5$ V,

$I_{CLIM(TH,MAX)} = 20$ A for $V_{OUT} \leq 5$ V.

If the multiphase dynamic power disable bit (configuration register 5) is enabled (default value is disabled), the device switches off the unused channels with respect to the power request.

As an example, consider an array configuration where the master device is configured as boost array master (>160 W) while the second as boost 2 channels – Slave (320 W), and V_{IN} is 13.5 V. The output voltage selected is 50 V and the output power request is 300 W; here, all four channels are working with the requested current of 6 A.

If the power request decreases to 150 W, and the multiphase dynamic power disable is enabled, the device starts switching off the unnecessary channels to increase overall efficiency. When the decreased current exceeds the multiphase disable threshold 1 at:

$$I_{CLIM(TH)} \times 0.75 \times 3/4 = 4.165 \text{ A},$$

then the 4th channel is no longer necessary and it is disabled. A factor of 0.75 is used as a margin between the enabling and disabling threshold in order to not have a channel disabled due to a load dump.

Since the power request is 150 W, the current is even more decreased and also overcomes the second threshold multiphase disable threshold 2 at:

$$I_{CLIM(TH)} \times 0.75 \times 2/3 = 3.7 \text{ A}$$

This leaves only two out of three channels active. If the power request increases, the device turns on the other channels as soon as the threshold is overcome. It may happen that the device communicates a BOOTx_UV fault after the channel turns on because the device is not masking this detection. The functionality is not affected, and the MCU can clear the fault.

ALLEGRO microsystems

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Gate Driver Functionality and External Components

The A81850 provides precise control over external FET switching characteristics by driving current through its GHx and GLx pins. This allows for versatile management of the gate drive. A key feature is the ability to modulate each of the four gate currents by adjusting the internal pull-up/pull-down resistance values, configurable via dedicated SPI bits in Config Register 2. This granular control over gate current enables optimization of the switching behavior of the external MOSFETs.

This gate current modulation is critical for optimizing system performance and managing inherent tradeoffs. Reducing the gate current increases the FET activation time, which in turn effectively dampens unwanted voltage overshoot on the gate and switching nodes. This slower switching profile can significantly improve electromagnetic interference (EMI) performance by spreading the switching energy over a longer period, thus reducing high-frequency noise. However, it is important to note that this approach comes with a tradeoff: the longer transition times lead to increased switching losses. For further fine-tuning of the switching speed and precise management of the rate of gate charge and discharge, an external series resistance can be added between the GHx/GLx pin and the gate of the FET, offering an additional layer of control for specific application requirements.

The A81850 incorporates robust gate control features to prevent unwanted turn-on of the external FETs, which can lead to critical issues such as shoot-through conditions, increased power losses, or system instability. To achieve this, the device provides both a resistive passive pull-down and an active pull-down mechanism on both the low-side (GLx) and high-side (GHx) gate drive pins.

The resistive passive pull-down offers a continuous, high-impedance path from the gate to ground (or source) when the gate driver is not actively driving the FET. This ensures that the gate voltage remains low, providing a baseline level of protection against noise or residual gate charge that could otherwise cause an unintended turn-on, particularly during power-up/down sequences or in idle states.

For more dynamic and robust protection, especially during high-speed switching transitions and even when the device is powered but the specific channel is not actively switching, the device features an active pull-down circuit. This active mechanism provides a low-impedance path to quickly discharge the gate capacitance and rapidly pull the gate voltage down to ground. This is crucial for effectively counteracting the Miller effect, where rapid voltage changes on the switching node can capacitively couple to the gate, potentially raising its voltage above the threshold and causing an unwanted turn-on. The active pull-down ensures a swift and definitive turn-off of the FET, enhancing overall system reliability, efficiency, and preventing hazardous shoot-through conditions.

Minimum Off-Time and On-Time Calculation

The maximum achievable duty cycle depends on the boost minimum off/on time the converter can achieve. In the A81850, this value depends on:

- Blanking time, t_{BLANK}
- Gate driver non overlap time, t_{NOx}, selectable for each channel through the dedicated configuration register
- The time needed to the external FET to reach the $V_{GS(XX,FALL)}$ threshold

A typical scenario is shown in Figure 14 and Figure 15 where the parameters in red represent the elements that contribute to the on-time calculation.

Considering that the gate current is:

$$I \cong \frac{V_{DRV}}{R_{gate}}$$

where R_{gate} is the sum between the external gate resistance, if placed, and the A81850 gate resistance, selectable through the dedicated configuration register.

The time needed to the external FET to reach the $V_{GS(XX,FALL)}$ threshold is:

$$t_{VGS} \cong \frac{\Delta Q}{I}$$

And as a result:

$$t_{boost(min,offtime)} \cong t_{VGS(HS)} + t_{VGS(LS)} + 2 \times t_{NOx} + t_{blank}$$

$$t_{buck(min,ontime)} \cong t_{VSG(HS)} + t_{NOx} + t_{blank}$$

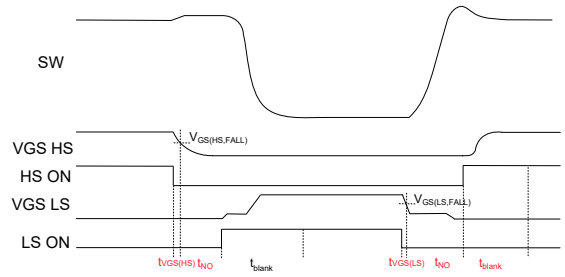


Figure 14: Boost Minimum Off-Time

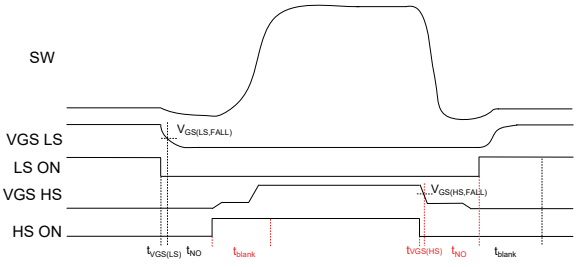


Figure 15: Buck Maximum On-Time

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

DEVICE OPERATIVE MODE CONFIGURATION

The device is configurable, both in SPI and stand-alone mode, in all the configurations reported in the table below.

Table 3: Device Configuration

Configuration	SPI	SA			SPI/SA				
	DCDC_MODE[2:0]	CSn	SCK	MOSI	COMP1	COMP2/SHARE	SYNC	VOUT1/FB1	VOUT2/FB2
Boost – 1 Channel (80 W)	000	GND	GND	GND	COMP NETWORK	GND	GND	CONNECTED	N/A
Boost Array – 1 Channel Slave Device (240 W)	000	GND	GND	GND	GND	CONNECTED TO MASTER	CONNECTED TO MASTER	CONNECTED	N/A
Boost – 2 Independent Channels (80 W / 80 W)	011	GND	VDRV	VDRV	COMP NETWORK	COMP NETWORK	VDRV	CONNECTED	CONNECTED
Boost Array – 2 Channels Slave Device (320 W)	011	GND	VDRV	VDRV	GND	CONNECTED TO MASTER	CONNECTED TO MASTER	CONNECTED	CONNECTED
Boost Array – 2 Channels Master Device (160 W)	010	GND	VDRV	GND	COMP NETWORK	GND	VDRV	CONNECTED	CONNECTED
Boost Array – 2 Channels Master Device (>160 W)	010	GND	VDRV	GND	COMP NETWORK	CONNECTED TO SLAVE	CONNECTED TO SLAVE	CONNECTED	CONNECTED
Buck – 1 Channel (80 W)	101	VDRV	GND	VDRV	COMP NETWORK	GND	GND	CONNECTED	N/A
Buck Array – 1 Channel Slave Device (240 W)	101	VDRV	GND	VDRV	GND	CONNECTED TO MASTER	CONNECTED TO MASTER	CONNECTED	N/A
Buck – 2 Independent Channels (80 W / 80 W)	110	VDRV	VDRV	GND	COMP NETWORK	COMP NETWORK	VDRV	CONNECTED	CONNECTED
Buck Array – 2 Channels Slave Device (320 W)	110	VDRV	VDRV	GND	GND	CONNECTED TO MASTER	CONNECTED TO MASTER	CONNECTED	CONNECTED
Buck Array – 2 Channels Master Device (160 W)	111	VDRV	VDRV	VDRV	COMP NETWORK	GND	VDRV	CONNECTED	CONNECTED
Buck Array – 2 Channels Master Device (>160 W)	111	VDRV	VDRV	VDRV	COMP NETWORK	CONNECTED TO SLAVE	CONNECTED TO SLAVE	CONNECTED	CONNECTED
Buck–Boost (80 W)	100	VDRV	GND	GND	COMP NETWORK	GND	VDRV	CONNECTED	N/A (SPI) / VOUT SENSE (SA)
Buck Channel 1 (80 W) Boost Channel 2 (80 W)	001	GND	GND	VDRV	COMP NETWORK	COMP NETWORK	GND	CONNECTED	CONNECTED

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

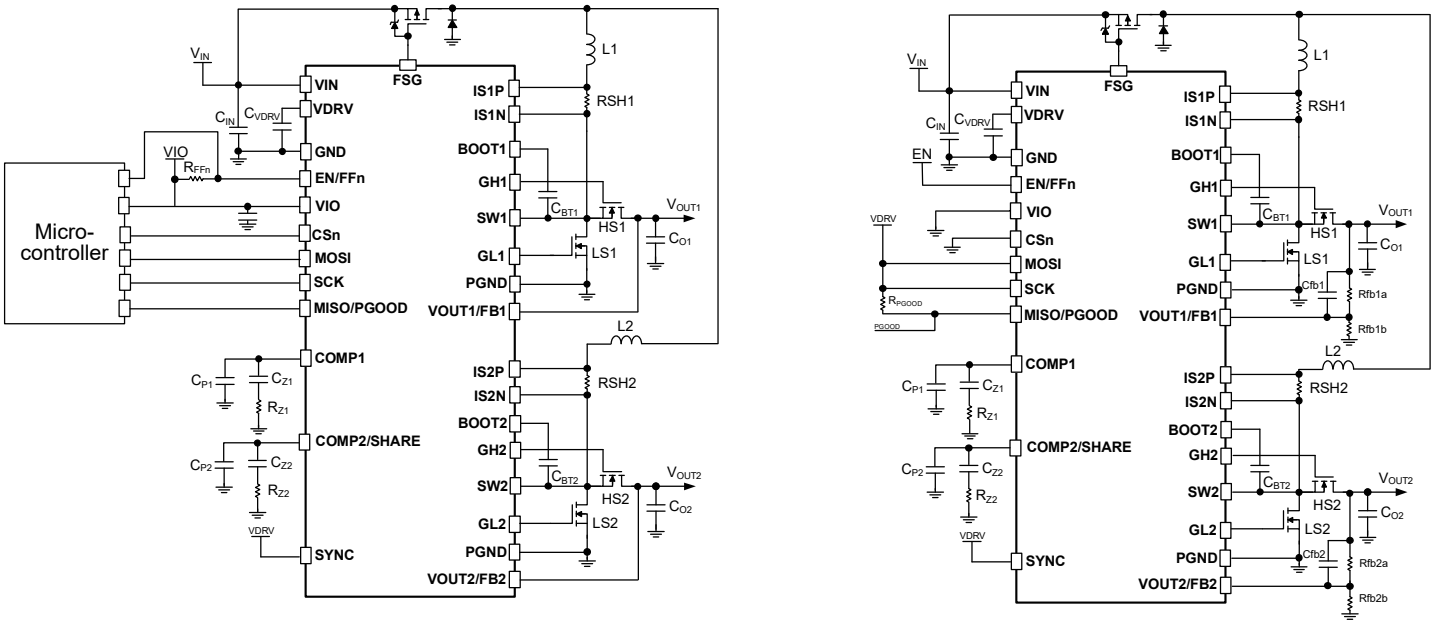


Figure 16: Boost 2 Independent Channels SPI (left) and Stand Alone (right)

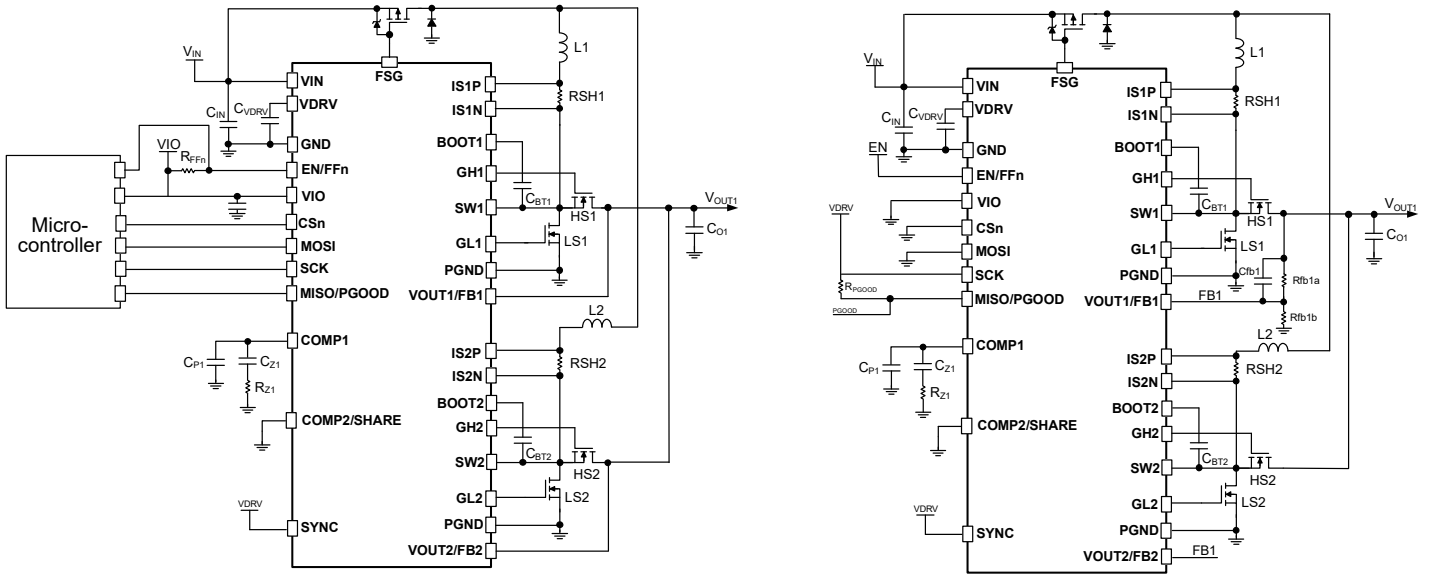


Figure 17: Boost Array 2 Channels SPI (left) and Stand Alone (right)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

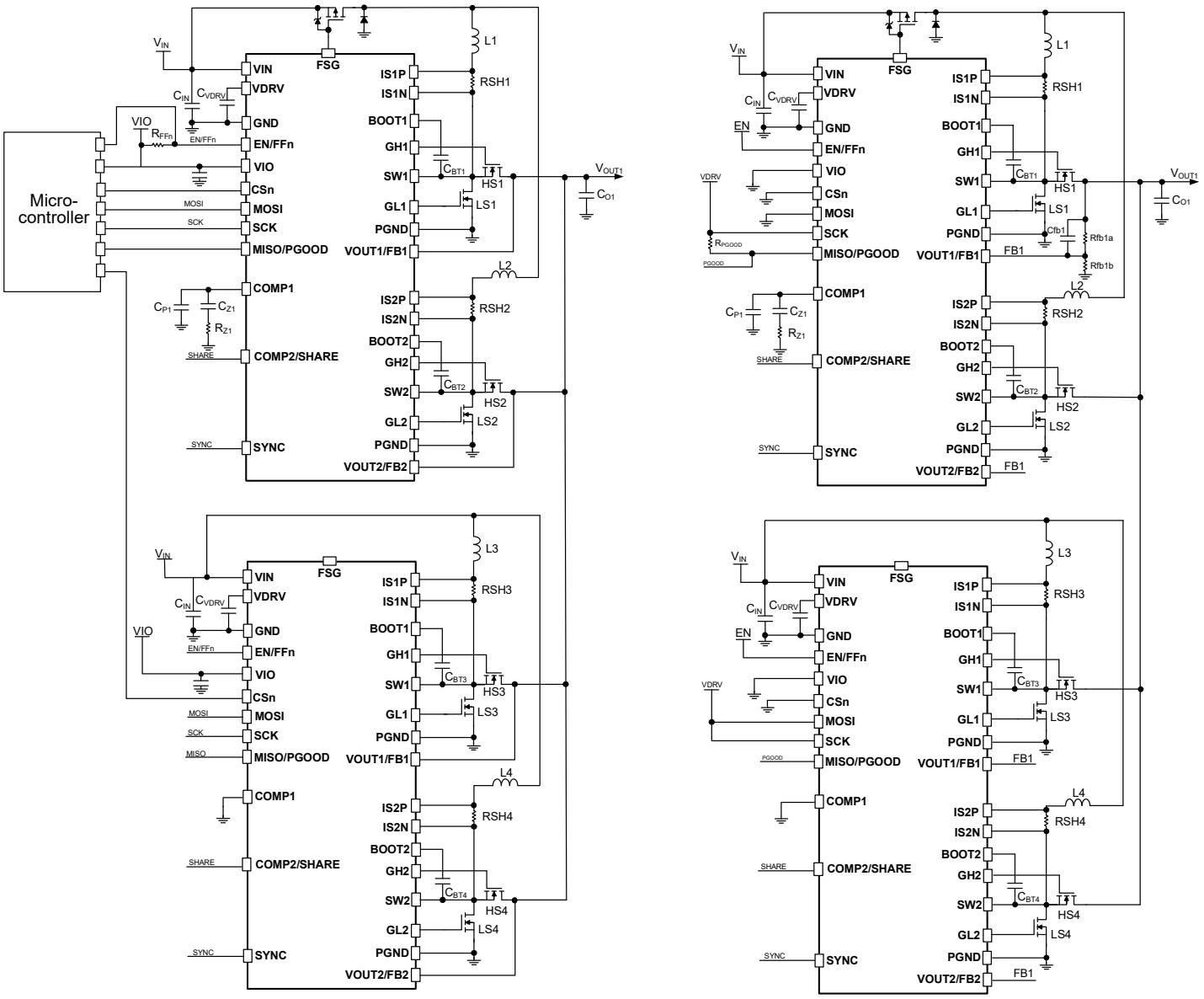


Figure 18: Boost Array 4 Channels SPI (left) and Stand Alone (right)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

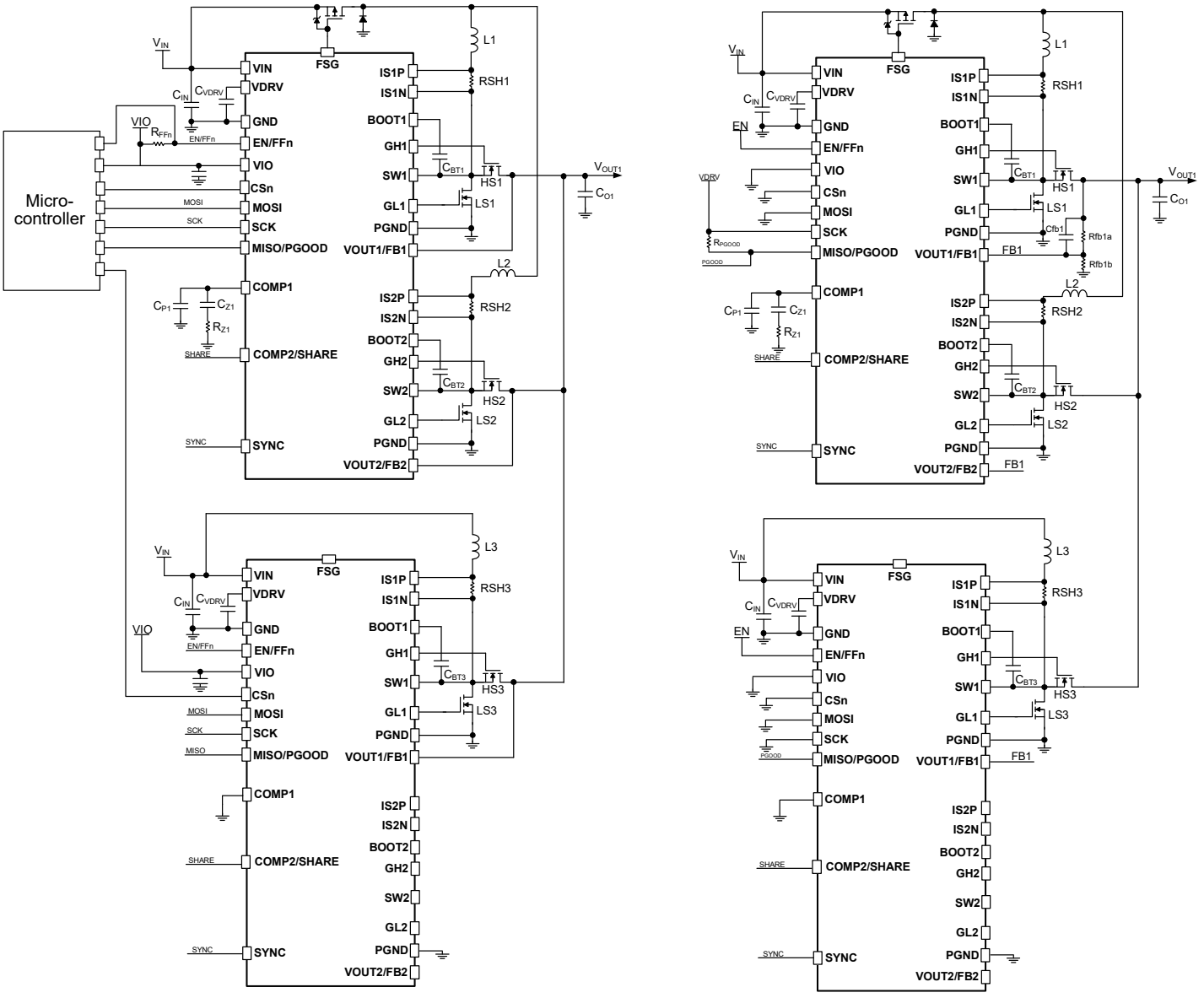


Figure 19: Boost Array 3 Channels SPI (left) and Stand Alone (right)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

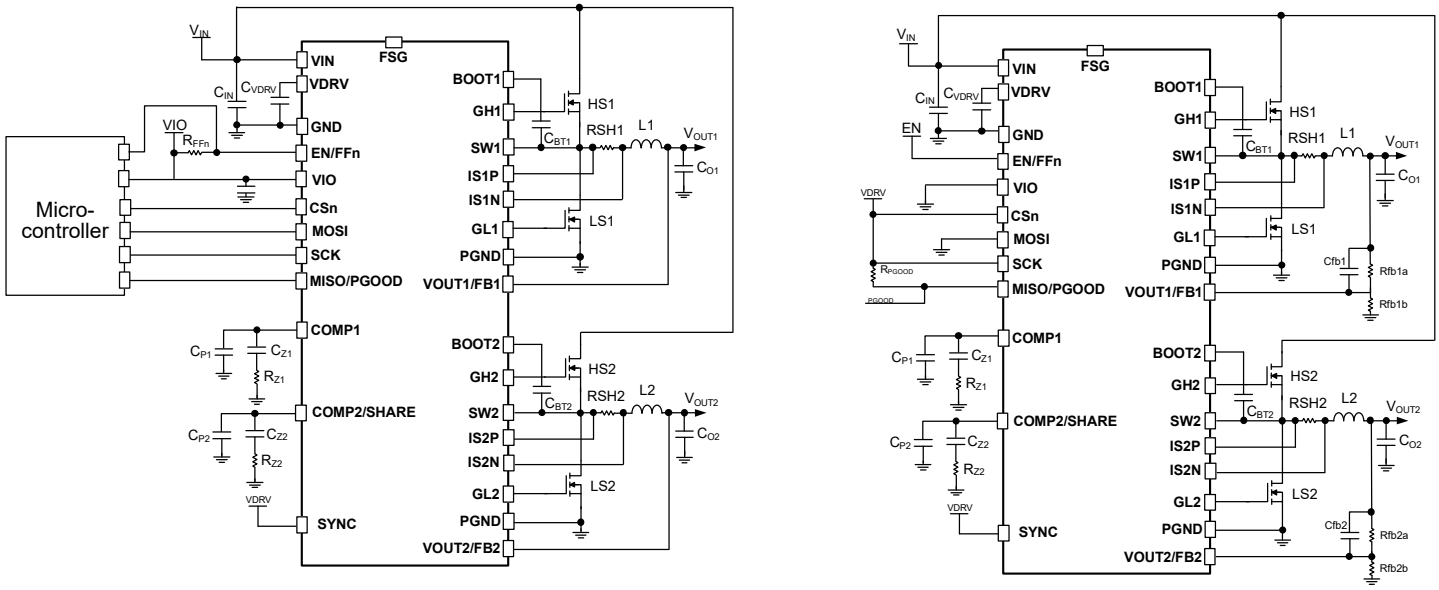


Figure 20: Buck 2 Independent Channels SPI (left) and Stand Alone (right)

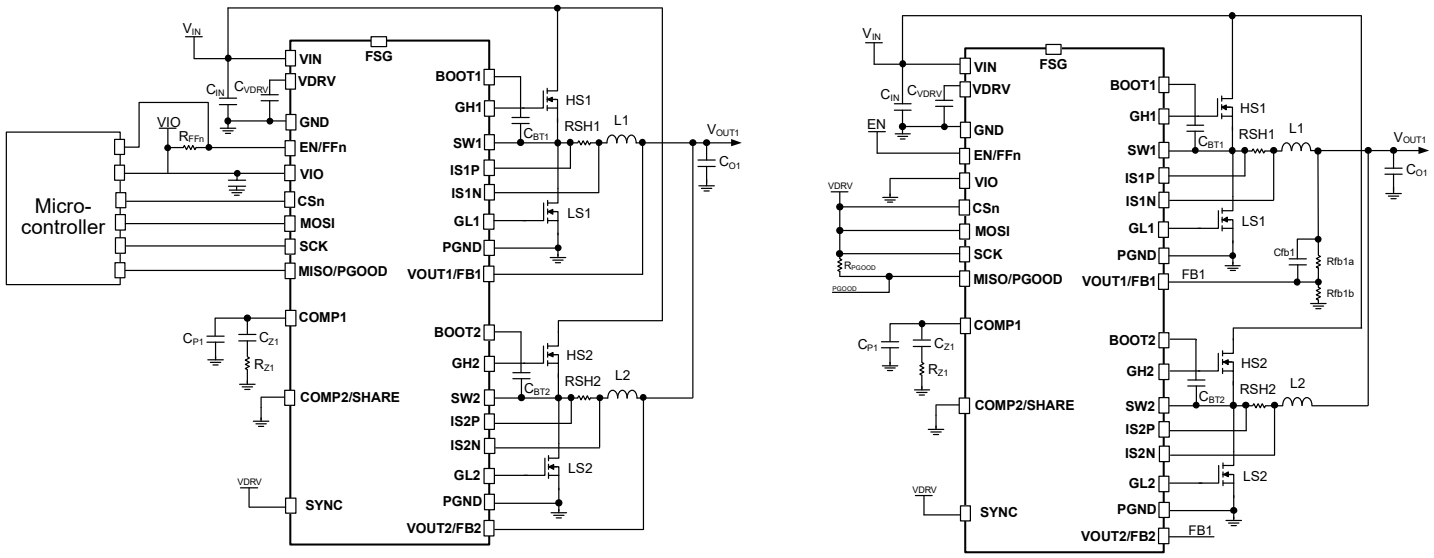


Figure 21: Buck Array 2 Channels SPI (left) and Stand Alone (right)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

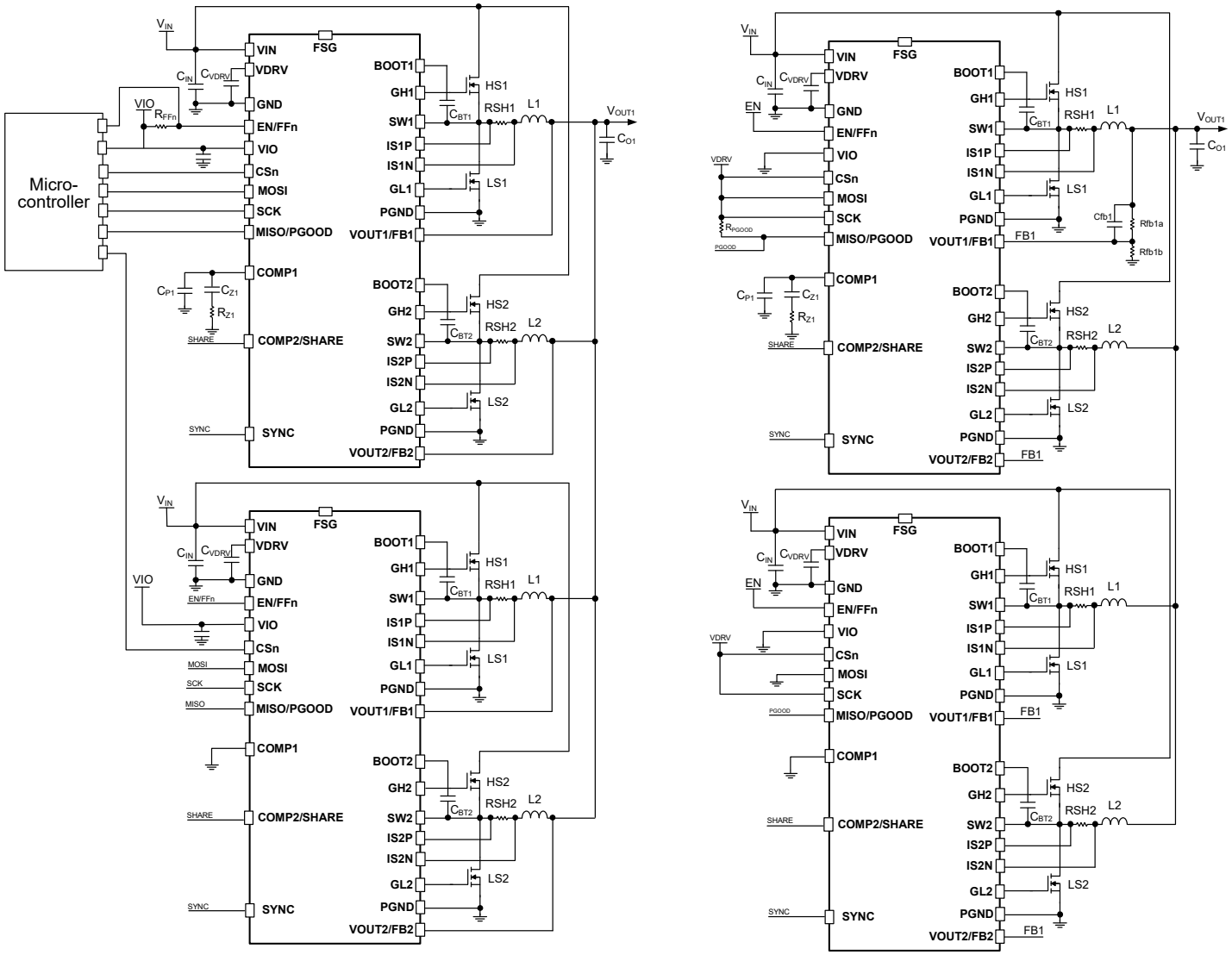


Figure 22: Buck Array 4 Channels SPI (left) and Stand Alone (right)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

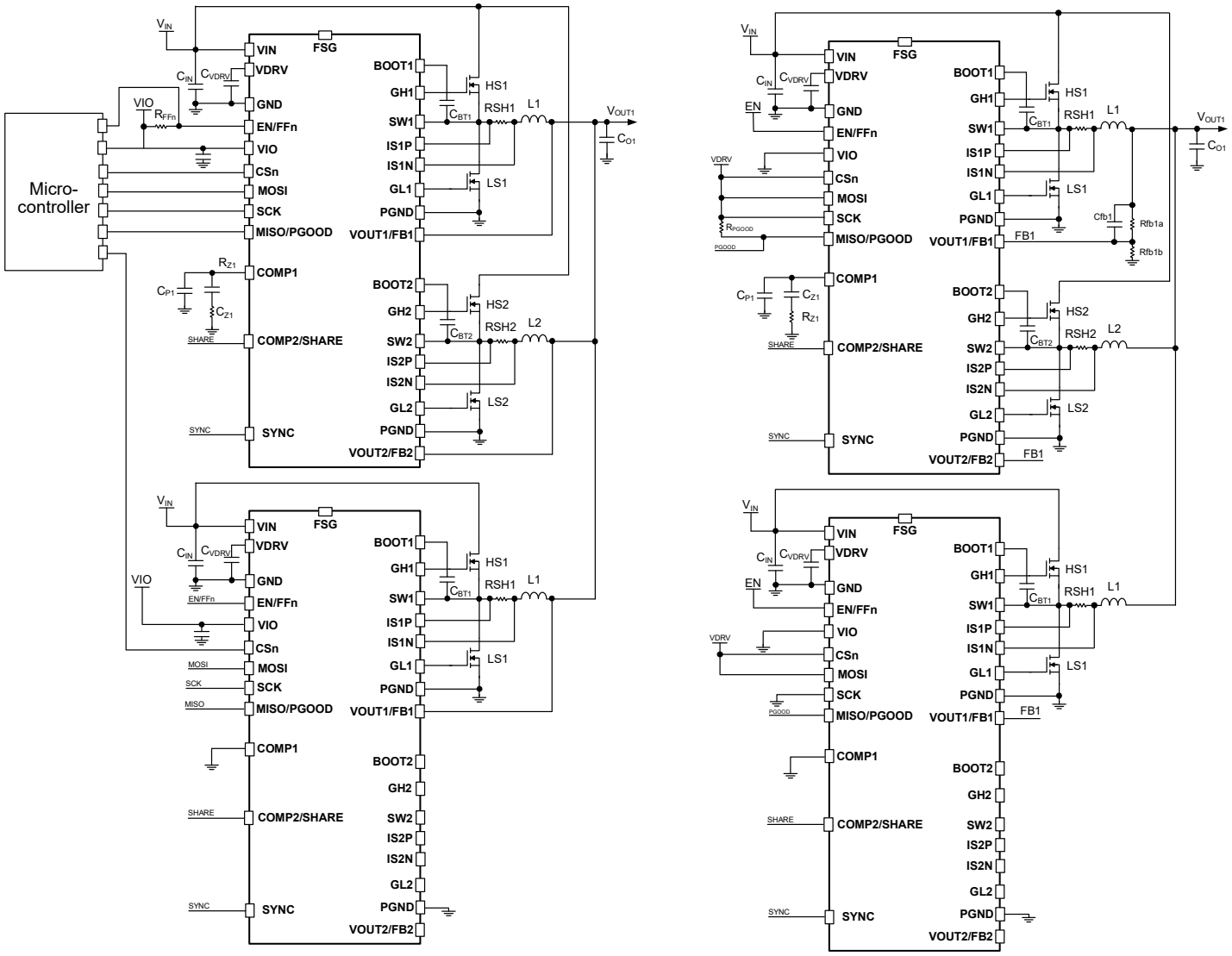


Figure 23: Buck Array 3 Channels SPI (left) and Stand Alone (right)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

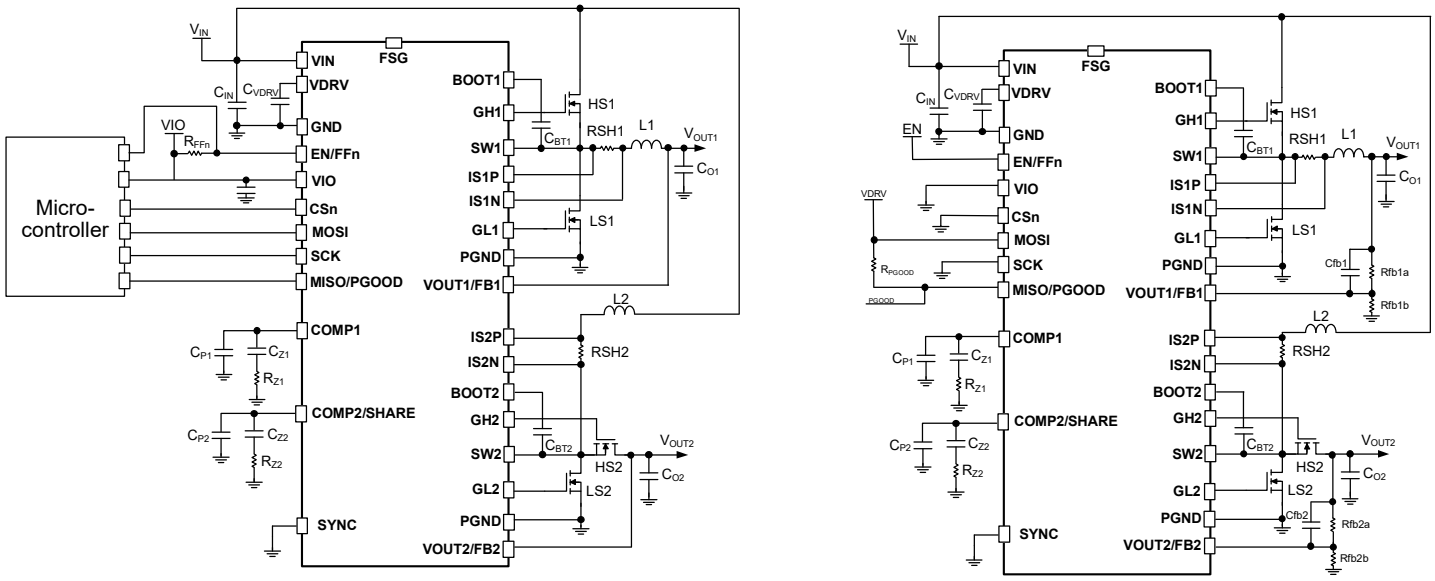


Figure 24: Buck + Boost SPI (left) and Stand Alone (right)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

FAULT TABLES

Normal Operation Faults

There are a few sets of faults (see Note column of Table 4) that are configurable between two states. When the fault is electrically removed, if FAULT_CONFIG is set to 1, it is necessary to write a VOUTX_EN = 1 command for restarting normal operation.

If there is an "*", then VOUT is switched off in both channels.

In SPI mode, FFn is latched once a fault is present. To have FFn return high, remove the electrical fault and write 1 to clear the dedicated fault register.

In SA mode, the PGOOD pin is asserted for a restricted set of faults related to VOUT. Once the fault is electrically removed, PGOOD returns high.

Table 4: Normal Operation Faults

Fault	To be observed after?	FSG	VOUTx	VDRV	FFn (latched) (Valid for SPI mode)	PGOOD (Valid for SA mode)	SPI	Reset (Recovery) Method	Note
VIN_UV	After EEPROM download	Off	Off *	Off	Hi_Z	–	Off	Increase V_{IN}	Device in power off
BOOTx_UV	After D_VOUTX_SS_EN goes to 1	–	Recovery Activation	–	–	–	–	Recovery feature activation	If the UV is not recovered (e.g. short) V_{DRV} will go in UV
VOUTx_UV	After D_VOUTX_SS_DONE	–	UV	–	Low	Low	–	–	
VIO_UV	After VIO check (SA vs. SPI mode detection)	-	-	-	Low		Off	Increase VIO	In SA mode, no effect; the pin shall be tied to GND
VIO_SD	After VIO check (SA vs. SPI mode detection), with EN low	Off	Off *	Off	Hi_Z	–	Off	–	EN latch is removed, SPI functionality not guaranteed. If enable is low, the device powers off. In SA mode, no effect; the pin shall be tied to GND.
VDRV_UV	After VIO check (SA vs SPI mode detection)	Off	Off *	Off	Hi_Z		Off	Increase VIO	If VDRV_UV_CONFIG = 0 → normal operation when fault is removed. If VDRV_UV_CONFIG = 1 → write VOUTx_EN = 1 to return in normal operation.
FSG_OPEN	Only after FailSafe activation	OPEN	–	–	Low	–	–	Connect the external FET	Only for Boost mode
COMP1_OPEN	After D_VOUTX_SS_EN goes to 1	–	VOUTx_UV/ VOUTx_OV/ VOUTx_OCL	–	Low	–	–	Connect the compensation network to the pin	During PWM activity, device detects overcurrent
COMP2_OPEN	After D_VOUTX_SS_EN goes to 1	–	VOUTx_UV/ VOUTx_OV/ VOUTx_OCL	–	Low	–	–	Connect the compensation network to the pin	During PWM activity, device detects overcurrent
		–	–	–	–	–	Stand–alone case	–	Device in stand-alone mode and in one of these configurations: –Buck/Boost 1 Channel – Slave (240 W) –Buck/Boost 2 Channels – Slave (320 W) –Buck/Boost Array Master (>160 W)
VOUTx_SENSE_ FAULT	After D_VOUTX_SS_DONE goes to 1	–	Hiccup	–	Low	Low	–	Connect capacitance or check connection	
VIN_OV	After VIO check (SA vs SPI mode detection)	–	–	–	Low	–	–	Remove OV factor	If VIN_OV_CONFIG = 0 → normal operation when fault is removed. If VIN_OV_CONFIG = 1 → write VOUTx_EN = 1 to return in normal operation.
BOOTx_OV	After D_VOUTX_SS_EN goes to 1	–	Hiccup	–	Low	–	–	–	
VOUTx_OV	After D_VOUTX_SS_DONE goes to 1	–	Off	–	Low	Low	–	–	
VDRV_OV	After VIO check (SA vs SPI mode detection)	–	Off *	OV	Low	–	–	–	If VDRV_OV_CONFIG = 0 → normal operation when fault is removed. If VDRV_OV_CONFIG = 1 → write VOUT_EN = 1 to return in normal operation.
SWx_SHORT	LS/HS monitors enabled After D_DRVX_ASM_COUNTERS_ EN goes to 1	Off Or –	Hiccup Or OFF	–	Low	–	–	–	If SWx_STG_CONFIG = 0 → hiccup. If SWx_STG_CONFIG = 1 → OFF and write VOUT_EN = 1 to return in normal operation.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Continued on next page...

Table 4: Normal Operation Faults (continued)

Fault	To be observed after?	FSG	VOUTx	VDRV	FFn (latched) (Valid for SPI mode)	PGOOD (Valid for SA mode)	SPI	Reset (Recovery) Method	Note
VOUTx_OCL	After D_VOUTX_SS_EN goes to 1	Off Or –	Hiccup Or OFF	–	Low	Low	–	–	If VOUTx_OCL_CONFIG = 0 → hiccup. If VOUTx_OCL_CONFIG = 1 → OFF and write VOUT_EN = 1 to return in normal operation.
GHx_STG	After D_DRVX_ASM_ COUNTERS_EN goes to 1 VGS comparator, GH - SW	Off Or –	Hiccup Or OFF	–	Low	–	–	–	If GATE_STG_CONFIG = 0 → hiccup. If GATE_STG _CONFIG = 1 → OFF and write VOUT_EN = 1 to return in normal operation. Note. GHx shorted to GND is a destructive fault.
GLx_STG	After D_DRVX_ASM_ COUNTERS_EN goes to 1	Off Or –	Hiccup Or OFF	–	Low	–	–	–	If GATE_STG _CONFIG = 0 → hiccup. If GATE_STG _CONFIG = 1 → OFF and write VOUT_EN = 1 to return in normal operation.
RSHx missing	After D_VOUTX_SS_DONE	–	UV	–	Low	–	–	–	
CDRV missing	After VIO check (SA vs SPI mode detection)	–	Off *	–	Low	–	–	–	
ABIST FAULT	Only after ABIST procedure	–	–	–	Low	–	–	–	
EEPROM FAULT	After EEPROM download	–	–	–	Low	–	–	–	
Pin Checker FAULT	After EEPROM download	–	–	–	Low	–	–	–	Pin Checker fault is a “clear on write” fault both for Live and Diagnostic mode
SE FAULT	After EEPROM download	–	–	–	Low	–	–	–	
INTERNAL LOGIC ERROR	After reset release	Off	Off *	Off	Low	Low	–	–	Main FSM reached a wrong state
Master clock stuck high/ low	After reset release	–	–	–	Low	Low	No communication	–	
PWM clock stuck high/ low	After EEPROM download	Off	Off *	Off	Low	Low	–	Only on master device	
TWARN	After EEPROM download				Low	–	–	–	MCU informed
TSD	After EEPROM download	Off	Off *	Off	Low	–	–	–	

Start-Up Operation Faults

Table 5: Start-Up Operation Faults

Fault	To be observed after?	FSG	VOUTx	VDRV	FFn	PGOOD	SPI	Reset (Recovery) Method	Note
VIO_UV	During VIO check (SA vs SPI mode detection) to latch SA/ SPI mode	–	–	–	–		Off	–	Stand Alone mode activation
VOUTx_OPEN/STG	After Configuration Lock	–	Off	–	Low	Low	–	Connect capacitance	
Configuration Error	After Configuration Lock	Off	Off *	Off	Low	Low		–	Check the DCDC_MODE bits (SPI) or MOSI, CSn and SCK with respect to the COMPx and SYNC pins

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SERIAL COMMUNICATION INTERFACE

The A81850 provides the user with a full-duplex, four-wire, synchronous serial interface, compatible with the serial peripheral interface (SPI) standard using mode 3 (CPOL = 1, CPHA = 1). The SPI interface uses an out-of-frame communications protocol, meaning the logical response of the slave is within the next frame of the master, as shown in Figure 25. The serial interface timing requirements are specified in the electrical characteristics table and illustrated in Figure 6.

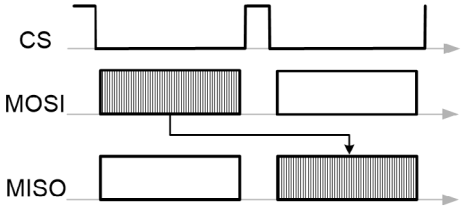


Figure 25: Out-of-Frame SPI Communication

Each 32-bit frame has a read/write bit, WR (bit 30). This bit must be set to 1 to write the subsequent bits into the selected register. If WR is set to 0 (a read), then the data bits (21 to 6) are ignored. The state of the WR bit also determines the data output on MISO. If WR is set to 1, then general diagnostic information is output. If WR is set to 0, then the contents of the register selected by the address bits is output.

MOSI: Master-output slave-input (data input from the master). A 32-bit word sent/received MSB first. When CS is low, data from the master is received on this pin. The slave reads/latches the data on the rising edge of SCK. The master advances to the next bit on the falling edge of SCK.

MISO: Master-input slave-output (data output from the slave, or A81850). A 32-bit word is sent/received MSB first. This pin is high impedance when CS is high or when the CHIP_ID (bit 22 from the previous frame) was incorrect. When CS is low, data from the slave is sent on this pin. The master reads/latches the data on the rising edge of SCK. The slave advances to the next bit on the falling edge of SCK.

SCK: Serial clock (input) from the master. There must be 32 rising clock edges per frame. During each clock cycle, a full duplex data transmission occurs. The master sends a bit on the MOSI line and the slave reads it, while the slave sends a bit on the MISO line and the master reads it. This sequence is maintained even when only one-directional data transfer is intended. Data changes state on the falling edge of SCK and is latched on the rising edge of SCK. SCK must be set high before CS transitions.

CS: Chip select (input) from the master. When CS is high, MISO is high impedance, and activity on MOSI and SCK is ignored. This allows multiple SPI slaves to have common MISO, SCK, and MOSI connections. However, each slave must have a dedicated CS signal. CS is brought low to initiate a serial transfer. When 32 data bits have been clocked into the shift register, CS must be taken high to latch the data into the selected register. When this occurs, the internal control circuits act on the new data.

If CS transitions high and there are fewer than 32 rising edges on SCK, the write will be cancelled, and no data will be written to the registers. Similarly, if there are more than 32 rising edges on SCK while CS is low, the write will be cancelled, and no data will be written. In both cases, the SE (serial error) and FF (fault flag) bits will be set high, and FFn pin (microcontroller interrupt) pulled low to indicate a data transfer error.

The device also integrates a timeout that checks the inactivity on SPI CS pin. This additional checker can enabled/disabled using the SPI bit CSN_TO_EN. If CS pin is inactive for longer than the timeout threshold (configured by SPI CSN_TO_THR) latched bit is set which asserts FFn low and puts MISO to Hi-Z until the bit is cleared.

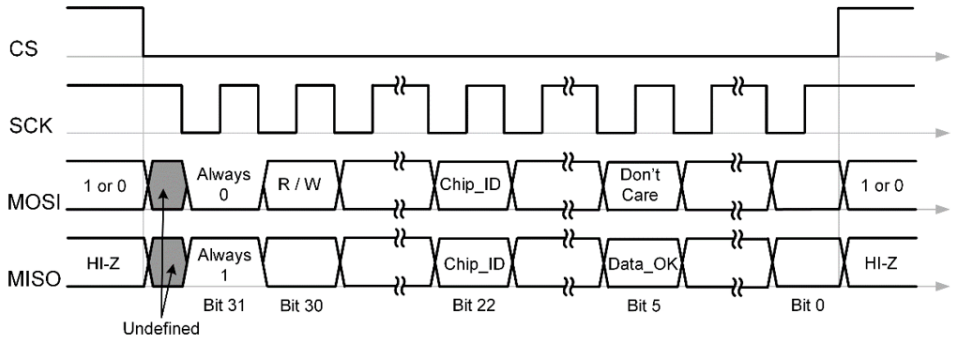


Figure 26: SPI Communications Example

Data changes on the falling edge of SCK. Data is latched on the rising edge of SCK.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SPI Frame Definition

1. Request register ID is the host command's address, from the previous SPI message.
2. CHIP_ID, bit 22 in both the MISO and MOSI frames, ensures that the A81850 only accepts commands meant for it when it shares SPI with a second device. For the A81850, the CHIP_ID shall be internally fixed at 0. For the second device on SPI, CHIP_ID should be internally fixed at 1.
3. MOSI and MISO frames: include a 5-bit CRC calculated from bits 30 to bit 5.
   A. The MSB is static, so it does not need to be included in the CRC calculation. It can be checked at the host or device side independently.
   B. Polynomial of 0x12 ($x^5 + x^2 + 1$) is used, with a start value of 11111b and a target of 00000b.
   C. Covers every single- and dual-bit error.
   D. Achieves a Hamming distance of 3.
   E. Every 4 consecutive bit error.
   F. Line stuck low/high detected.
   G. If a CRC error occurs, the SE and FF bits are set to 1, and the FFn pin is pulled low.
4. MISO frame includes a 5-bit request register ID, bits 30 to 26.
5. MISO frame includes a 3-bit frame counter, bits 25 to 23. It is a simple modulo-8 (0→1→2→…→7→0→…) counter value, that is incremented at every SPI message.
6. Writing and reading 2-bit patterns to the read-back register checks SPI integrity.

Table 6: Write command from the host to the MOSI pin

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	1	5-bit address					DC		0	16-bit data																DC	5-bit CRC					

Host Commands

Bit 31 is static, fixed at 0.

Bit 30 indicates a write or a read: 1 = Write, 0 = Read.

Bit 22, the CHIP_ID, is fixed at 0 for the A81850.

For a read command, the data bits are considered not applicable (DC).

Write command from the host to the MOSI pin:

Table 7: Read command from the host to the MOSI pin

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	5-bit address					DC		0	16-bit data																DC	5-bit CRC					

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Device Responses

Bit 31 is static, fixed at 1.

Bit 22, CHIP_ID, is fixed at 0 for the A81850.

Bit 5, DATA_OK, indicates if the 16-bit data of the previous frame is valid:

1 = valid data, no errors detected.

0 = normal response after a MOSI write or an error was detected (i.e., SE or CRC), so general status bits are sent.

Table 8: Pattern at the MISO pin after a MOSI read where the 16-bit data is valid (i.e. no errors detected)

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	1	Request Register ID					Frame Counter			0	16-bit data																VLD	5-bit CRC					

Table 9: Pattern at the MISO pin after a MOSI write, or pattern at the MISO pin after a MOSI read where an error was detected

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	1	Request Register ID					Frame Counter			0	Status Register 0																VLD	5-bit CRC					

Status Updates and SPI Procedure if FFn→0

The SPI fault status bits of the A81850 are updated at the beginning of each SPI frame (i.e., when CSn transitions low). This is shown by the STATUS Latched signal in Figure 27.

If the FFn signal transitions low, it is up to the MCU to read the fault registers on the A81850.

The A81850 uses out-of-frame communication, so the actual response is available in the next frame.

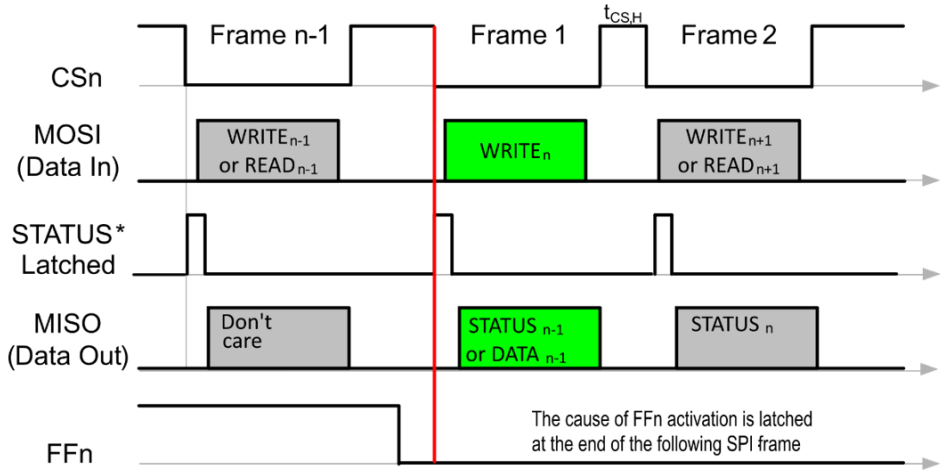


Figure 27

* The STATUS Latched signal is internal to the IC.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

REGISTER MAPS

Table 10: Register Map

Hex.	Dec.	Register Name	Data Bit							
			D21	D20	D19	D18	D17	D16	D15	D14
			D13	D12	D11	D10	D9	D8	D7	D6
0x00	0	STATUS_0	FF	VOUT2_SENSE_OCL_S	VOUT2_OV_S	VOUT2_UV_S	VOUT2_SS_DONE_S	VOUT1_SENSE_OCL_S	VOUT1_OV_S	VOUT1_UV_S
			VOUT1_SS_DONE_S	VDRV_S	TWARN_S	VIN_OV_S	EN_LAT_S	EN_S	SPI_RDY_S	INVALID_CONF_S
0x01	1	FAULT_0	FF	EEPROM_F	ABIST_F	INT_LOGIC_ERR_F	–	FFn_PIN_CHCK_F	TWARN_F	TSD_F
			DEAD_PEM_CLK_F	VDRV_OV_F	VDRV_UV_F	VIN_OV_F	VIN_UV_F	FSG_OPEN_F	VIO_UV_F	SE_F
0x02	2	FAULT_1	–	–	–	–	–	–	–	VOUT1_SENSE_F
			GL1_STG_F	GH1_STG_F	SW1_SHORT_F	VOUT1_OCL_F	VOUT1_OV_F	VOUT1_UV_F	BOOT1_OV_F	BOOT1_UV_F
0x03	3	FAULT_2	–	–	–	–	–	–	–	VOUT2_SENSE_F
			GL2_STG_F	GH2_STG_F	SW2_SHORT_F	VOUT2_OCL_F	VOUT2_OV_F	VOUT2_UV_F	BOOT2_OV_F	BOOT2_UV_F
0x04	4	STARTUP_0	CFG_LOCK	INVALID_CONF_F	–	–	–	STARTUP_COMP2_STG	STARTUP_COMP2_OPEN	STARTUP_COMP1_STG
			STARTUP_COMP1_OPEN	STARTUP_VOUT2_SENSE_FAULT	STARTUP_VOUT1_SENSE_FAULT	STARTUP_SYNCH [1:0]		SLAVE_DEVICE	MASTER_DEVICE	D_STANDALONE
0x05	5	CONFIG_0	–	–	–	–	–	–	–	–
			–	–	–	–	–	–	VOUT2_EN	VOUT1_EN
0x06	6	CONFIG_1	VOUT2_REGVOLT_SEL							
			VOUT1_REGVOLT_SEL							
0x07	7	CONFIG_2	D_VOUT2_OV_SEL		D_VOUT1_OV_SEL		VOUT2_DEADTIME_SEL		VOUT1_DEADTIME_SEL	
			D_DRV2_GATE_RES_LS_SEL		D_DRV1_GATE_RES_LS_SEL		D_DRV2_GATE_RES_HS_SEL		D_DRV1_GATE_RES_HS_SEL	
0x08	8	CONFIG_3	–	–	–	–	–	–	–	–
			GATE_STG_CONFIG	SW2_SHORT_CONFIG	SW1_SHORT_CONFIG	VOUT2_OCL_CONFIG	VOUT1_OCL_CONFIG	VDRV_OV_CONFIG	VDRV_UV_CONFIG	VIN_OV_CONFIG
0x09	9	CONFIG_4	–	–	–	–	–	–	–	–
			–	–	–	–	D_CS2_RSHUNT_SEL		D_CS1_RSHUNT_SEL	
0x0A	10	CONFIG_5	–	DYS_PWR_DIS	VOUT2_SS_SEL			VOUT1_SS_SEL		
			D_CLK_PWM_DITH_AMPL_SEL		D_CLK_PWM_FREQ_SEL			DCDC_MODE		
0x0B	11	VERIFY_RESULT_0	–	–	–	–	–	VOUT2_OV_FAIL	VOUT2_UV_FAIL	VOUT1_OV_FAIL
			VOUT1_UV_FAIL	TSD_FAIL	VIN_OV_FAIL	VIN_UV_FAIL	VDRVOV_INT_FAIL	VDRVUV_INT_FAIL	VDDOK_INT_FAIL	VPOSOK_INT_FAIL

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 11: 0x00 – Status Register 0

Data Bit / Name	D21	D20	D19	D18	D17	D16	D15	D14
	FF	VOUT2_SENSE_OCL_S	VOUT2_OV_S	VOUT2_UV_S	VOUT2_SS_DONE_S	VOUT1_SENSE_OCL_S	VOUT1_OV_S	VOUT1_UV_S
Data Bit / Name	D13	D12	D11	D10	D9	D8	D7	D6
	VOUT1_SS_DONE_S	VDRV_S	TWARN_S	VIN_OV_S	EN_LAT_S	EN_S	SPI_RDY_S	INVALID_CONF_S

ADDRESS: 00000b

FF [D21]	RO	Fault Flag
0		No Fault (default)
1		Fault detected
VOUT2_SENSE_OCL_S [D20]	**RO**	**VOUT2 SENSE or OCL fault status**
0		No error (default)
1		Fault on VOUT2, overcurrent / open / short to ground
VOUT2_OV_S [D19]	**RO**	**VOUT2 Overvoltage status**
0		No fault (default)
1		Fault
VOUT2_UV_S [D18]	**RO**	**VOUT2 Undervoltage status**
0		No fault (default)
1		Fault
VOUT2_SS_DONE_S [D17]	**RO**	**VOUT2 soft start status**
0		Soft Start is not started or finished (default)
1		Soft Start is finished
VOUT1_SENSE_OCL_S [D16]	**RO**	**VOUT1 SENSE or OCL fault status**
0		No error (default)
1		Fault on VOUT1, overcurrent / open / short to ground
VOUT1_OV_S [D15]	**RO**	**VOUT1 Overvoltage status**
0		No fault (default)
1		Fault
VOUT1_UV_S [D14]	**RO**	**VOUT1 Undervoltage status**
0		No fault (default)
1		Fault
VOUT1_SS_DONE_S [D13]	**RO**	**VOUT1 soft start status**
0		Soft start is not started or finished (default)
1		Soft start is finished
VDRV_S [D12]	**RO**	**VDRV status**
0		No fault (default)
1		Fault, at least one of the VDRV_X_F is 1
TWARN_S [D11]	**RO**	**Thermal warning status**
0		Temperature is below 155°C (default)
1		Temperature is above 155°C
VIN_OV_S [D10]	**RO**	**VIN Overvoltage status**
0		No fault (default)
1		Fault
EN_LAT_S [D9]	**RW**	**Latch on the EN status**
0		EN_LAT is low (default)
1		EN_LAT is high
EN_S [D8]	**RO**	**EN status**
0		EN is low (default)
1		EN is high
SPI_RDY_S [D7]	**RO**	**SPI configuration status**
0		Startup protocol is not finished (default)
1		SPI is ready to be configured
INVALID_CONF_S [D6]	**RO**	**Device configuration status**
0		Wrong configuration selected with respect to pin status (default)
1		DCDC_MODE and pin status match

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 12: 0x01 – Fault Register 0

Data Bit / Name	D21	D20	D19	D18	D17	D16	D15	D14
	FF	EEPROM_F	ABIST_F	INT_LOGIC_ERR_F	–	FFn_PIN_CHCK_F	TWARN_F	TSD_F
Data Bit / Name	D13	D12	D11	D10	D9	D8	D7	D6
	DEAD_PEM_CLK_F	VDRV_OV_F	VDRV_UV_F	VIN_OV_F	VIN_UV_F	FSG_OPEN_F	VIO_UV_F	SE_F

ADDRESS: 00001b

FF [D21]	**RO**	**Fault Flag**
0		No fault (default)
1		Fault detected
EEPROM_F [D20]	**RO**	**EEPROM error fault**
0		No error (default)
1		Fault
ABIST_F [D19]	**RO**	**Analog BIST fault**
0		No fault (default)
1		Fault, in order to clear, all the bits in VERIFY_RESULT_0 must be cleared
INT_LOGIC_ERR_F [D18]	**RO**	**Main FSM ECC error fault**
0		No fault (default)
1		Fault
- [D17]		
0		
1		
FFn_PIN_CHCK_F [D16]	**R/W1C**	**FFn pin checker fault**
0		No error (default)
1		Fault
TWARN_F [D15]	**R/W1C**	**Thermal warning fault**
0		Temperature is below 155°C (default)
1		Temperature is above 155°C
TSD_F [D14]	**R/W1C**	**Thermal Shutdown status fault**
0		Temperature is OK (default)
1		Over temperature event
DEAD_PWM_CLK_F [D13]	**R/W1C**	**PWM clock fault**
0		No fault (default)
1		Fault
VDRV_OV_F [D12]	**R/W1C**	**VDRV Overvoltage fault**
0		No fault (default)
1		Fault
VDRV_UV_F [D11]	**R/W1C**	**VDRV Undervoltage fault**
0		No fault (default)
1		Fault
VIN_OV_F [D10]	**R/W1C**	**VIN Undervoltage fault**
0		No fault (default)
1		Fault
VIN_UV_F [D9]	**R/W1C**	**VIN Overvoltage fault**
0		No fault (default)
1		Fault
FSG_OPEN_F [D8]	**RO**	**Fail-Safe Open fault**
0		No fault (default)
1		Fault
VIO_UV_F [D7]	**R/W1C**	**VIO Undervoltage fault**
0		No fault (default)
1		Fault
SE_F [D6]	**R/W1C**	**Serial Communication Error Fault**
0		No error (default)
1		Fault: less than or more than 32 rising SCK edges in a frame, or CRC Error

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 13: 0x02 – Fault Register 1

Data Bit / Name	D21	D20	D19	D18	D17	D16	D15	D14
	-	-	-	-	-	-	-	VOUT1_SENSE_F
Data Bit / Name	D13	D12	D11	D10	D9	D8	D7	D6
	GL1_STG_F	GH1_STG_F	SW1_SHORT_F	VOUT1_OCL_F	VOUT1_OV_F	VOUT1_UV_F	BOOT1_OV_F	BOOT1_UV_F

ADDRESS: 00010b

– [D21]		
0		
1		
– [D20]		
0		
1		
– [D19]		
0		
1		
– [D18]		
0		
1		
– [D17]		
0		
1		
– [D16]		
0		
1		
– [D15]		
0		
1		
VOUT1_SENSE_F [D14]	**R/W1C**	**VOUT1 Sense fault**
0		No error (default)
1		Fault on VOUT1, open / short to ground
GL1_STG_F [D13]	**R/W1C**	**GL1 Ground fault**
0		No fault (default)
1		Fault
GH1_STG_F [D12]	**R/W1C**	**GH1 Ground fault**
0		No fault (default)
1		Fault
SW1_SHORT_F [D11]	**R/W1C**	**SW1 Ground or High fault**
0		No fault (default)
1		Fault, short to ground or high
VOUT1_OCL_F [D10]	**R/W1C**	**VOUT1 Overcurrent fault**
0		No fault (default)
1		Fault
VOUT1_OV_F [D9]	**R/W1C**	**VOUT1 Overvoltage fault**
0		No fault (default)
1		Fault
VOUT1_UV_F [D8]	**R/W1C**	**VOUT1 Undervoltage fault**
0		No fault (default)
1		Fault
BOOT1_OV_F [D7]	**R/W1C**	**BOOT1 Overvoltage fault**
0		No fault (default)
1		Fault
BOOT1_UV_F [D6]	**R/W1C**	**BOOT1 Undervoltage fault**
0		No fault (default)
1		Fault

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 14: 0x03 – Fault Register 2

Data Bit / Name	D21	D20	D19	D18	D17	D16	D15	D14
	–	–	–	–	–	–	–	VOUT2_SENSE_F
Data Bit / Name	D13	D12	D11	D10	D9	D8	D7	D6
	GL2_STG_F	GH2_STG_F	SW2_SHORT_F	VOUT2_OCL_F	VOUT2_OV_F	VOUT2_UV_F	BOOT2_OV_F	BOOT2_UV_F

ADDRESS: 00011b

– [D21]		
0		
1		
– [D20]		
0		
1		
– [D19]		
0		
1		
– [D18]		
0		
1		
– [D17]		
0		
1		
– [D16]		
0		
1		
– [D15]		
0		
1		
VOUT2_SENSE_F [D14]	**R/W1C**	**VOUT2 Sense fault**
0		No error (default)
1		Fault on VOUT2, open / short to ground
GL2_STG_F [D13]	**R/W1C**	**GL2 Ground fault**
0		No fault (default)
1		Fault
GH2_STG_F [D12]	**R/W1C**	**GH2 Ground fault**
0		No fault (default)
1		Fault
SW2_SHORT_F [D11]	**R/W1C**	**SW2 Ground or High fault**
0		No fault (default)
1		Fault, short to ground or high
VOUT2_OCL_F [D10]	**R/W1C**	**VOUT2 Overcurrent fault**
0		No fault (default)
1		Fault
VOUT2_OV_F [D9]	**R/W1C**	**VOUT2 Overvoltage fault**
0		No fault (default)
1		Fault
VOUT2_UV_F [D8]	**R/W1C**	**VOUT2 Undervoltage fault**
0		No fault (default)
1		Fault
BOOT2_OV_F [D7]	**R/W1C**	**BOOT2 Overvoltage fault**
0		No fault (default)
1		Fault
BOOT2_UV_F [D6]	**R/W1C**	**BOOT2 Undervoltage fault**
0		No fault (default)
1		Fault

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 15: 0x04 – Startup Register 0

Data Bit / Name	D21	D20	D19	D18	D17	D16	D15	D14
	CFG_LOCK	INVALID_CONF_F	–	–	–	STARTUP_COMP2_STG	STARTUP_COMP2_ OPEN	STARTUP_COMP1_STG
Data Bit / Name	D13	D12	D11	D10	D9	D8	D7	D6
	STARTUP_COMP1_ OPEN	STARTUP_VOUT2_ SENSE_FAULT	STARTUP_VOUT1_ SENSE_FAULT	STARTUP_SYNCH [1:0]		SLAVE_DEVICE	MASTER_DEVICE	D_STANDALONE

ADDRESS: 00100b

CFG_LOCK [D21]	RO	Configuration Lock
0		Configuration non locked (default)
1		Configuration is locked, CONFIG_5 has been written
INVALID_CONF_F [D20]	**RO**	**Device configuration fault**
0		Wrong configuration selected with respect to pin status (default)
1		DCDC_MODE and pin status match
– [D19]		
0		
1		
- [D18]		
0		
1		
- [D17]		
0		
1		
STARTUP_COMP2_STG [D16]		**COMP2 startup Short to ground fault**
0		No fault (default)
1		Fault
STARTUP_COMP2_OPEN [D15]		**COMP2 startup Open fault**
0		No fault (default)
1		Fault
STARTUP_COMP1_STG [D14]	**RO**	**COMP1 startup Short to ground fault**
0		No fault (default)
1		Fault
STARTUP_COMP1_OPEN [D13]	**RO**	**COMP1 startup Open fault**
0		No fault (default)
1		Fault
STARTUP_VOUT2_SENSE_FAULT [D12]	**RO**	**VOUT1 startup Sense fault**
0		No error (default)
1		Fault on VOUT1
STARTUP_VOUT1_SENSE_FAULT [D11]	**RO**	**VOUT2 startup Sense fault**
0		No error (default)
1		Fault on VOUT2
STARTUP_SYNC [D10:D9]	**RO**	**SYNC startup fault**
00		invalid (default)
01		GND
10		VDRV
11		Open
SLAVE_DEVICE [D8]	**RO**	**Slave Device**
0		It is not the slave device (default)
1		It is the slave device
MASTER_DEVICE [D7]	**RO**	**Master Device**
0		It is not the master device (default)
1		It is the master device
D_STANDALONE [D6]	**RO**	**Stand-Alone mode**
0		SPI mode
1		Stand-alone mode

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 16: 0x05 – Config Register 0

Data Bit / Name	D21	D20	D19	D18	D17	D16	D15	D14
	–	–	–	–	–	–	–	–
Data Bit / Name	D13	D12	D11	D10	D9	D8	D7	D6
	–	–	–	–	–	–	VOUT2_EN	VOUT1_EN

ADDRESS: 00101b

– [D21]		
0		
1		
– [D20]		
0		
1		
– [D19]		
0		
1		
– [D18]		
0		
1		
– [D17]		
0		
1		
– [D16]		
0		
1		
– [D15]		
0		
1		
– [D14]		
0		
1		
– [D13]		
0		
1		
– [D12]		
0		
1		
– [D11]		
0		
1		
– [D10]		
0		
1		
– [D9]		
0		
1		
– [D8]		
0		
1		
VOUT2_EN [D7]	**RW**	**VOUT2 enable**
0		Disabled (default)
1		Enabled, request to start VOUT FSM
VOUT1_EN [D6]	**RW**	**VOUT1 enable**
0		Disabled (default)
1		Enabled, request to start VOUT FSM

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 17: 0x06 – Config Register 1

Data Bit / Name	D21	D20	D19	D18	D17	D16	D15	D14
	VOUT2_REGVOLT_SEL							
Data Bit / Name	D13	D12	D11	D10	D9	D8	D7	D6
	VOUT1_REGVOLT_SEL							

ADDRESS: 00110b

VOUT2_REGVOLT_SEL [D21:D14]	RW	VOUT2 output voltage selection
00000000		$V_{OUTx(MIN)}$ (Boost or Buck-Boost) / V_{OUT} = 3.3 V (Buck)
00000001		$V_{OUTx(MIN)}$ +1 LSB (Boost or Buck-Boost) / V_{OUT} = 4.5 V (Buck)
00000010		$V_{OUTx(MIN)}$ +2 LSB (Boost or Buck-Boost) / V_{OUT} = 5 V (Buck)
00000011		$V_{OUTx(MIN)}$ +3 LSB (Boost or Buck-Boost) / V_{OUT} = 5.5 V (Buck)
00000100		$V_{OUTx(MIN)}$ +4 LSB (Boost or Buck-Boost) / V_{OUT} = 6 V (Buck)
0…		$V_{OUTx(MIN)}$ + n LSB (Boost or Buck-Boost) / V_{OUT} = 6 V (Buck)
11111111		$V_{OUTx(MAX)}$ (Boost or Buck-Boost) / V_{OUT} = 6 V (Buck)
VOUT1_REGVOLT_SEL [D13:D6]	**RW**	**VOUT1 output voltage selection**
00000000		$V_{OUTx(MIN)}$ (Boost or Buck-Boost) / V_{OUT} = 3.3 V (Buck)
00000001		$V_{OUTx(MIN)}$ + 1 LSB (Boost or Buck-Boost) / V_{OUT} = 4.5 V (Buck)
00000010		$V_{OUTx(MIN)}$ + 2 LSB (Boost or Buck-Boost) / V_{OUT} = 5 V (Buck)
00000011		$V_{OUTx(MIN)}$ + 3 LSB (Boost or Buck-Boost) / V_{OUT} = 5.5 V (Buck)
00000100		$V_{OUTx(MIN)}$ + 4 LSB (Boost or Buck-Boost) / V_{OUT} = 6 V (Buck)
0…		$V_{OUTx(MIN)}$ + n LSB (Boost or Buck-Boost) / V_{OUT} = 6 V (Buck)
11111111		$V_{OUTx(MAX)}$ (Boost or Buck-Boost) / V_{OUT} = 6 V (Buck)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 18: 0x07 – Config Register 2

Data Bit / Name	D21	D20	D19	D18	D17	D16	D15	D14
	D_VOUT2_OV_SEL		D_VOUT1_OV_SEL		VOUT2_DEADTIME_SEL		VOUT1_DEADTIME_SEL	
Data Bit / Name	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**
	D_DRV2_GATE_RES_LS_SEL		D_DRV1_GATE_RES_LS_SEL		D_DRV2_GATE_RES_HS_SEL		D_DRV1_GATE_RES_HS_SEL	

ADDRESS: 00111b

D_VOUT2_OV_SEL [D21:D20]	RW	VOUT2 Overvoltage selection
00		6.5%
01		10%
10		12.5%
11		15% (default)
D_VOUT1_OV_SEL [D19:D18]	**RW**	**VOUT1 Overvoltage selection**
00		6.5%
01		10%
10		12.5%
11		15% (default)
VOUT2_DEADTIME_SEL [D17:D16]	**RW**	**Gate drive CH2 non-overlap time selection**
00		10 ns
01		20 ns (default)
10		40 ns
11		60 ns
VOUT1_DEADTIME_SEL [D15:D14]	**RW**	**Gate drive CH1 non-overlap time selection**
00		10 ns
01		20 ns (default)
10		40 ns
11		60 ns
D_DRV2_GATE_RES_LS_SEL [D13:D12]	**RW**	**Low-side driver CH2 PU/PD resistance selection**
00		5.55 Ω
01		2.8 Ω
10		1.85 Ω default)
11		1.4 Ω
D_DRV1_GATE_RES_LS_SEL [D11:D10]	**RW**	**Low-side driver CH1 PU/PD resistance selection**
00		5.55 Ω
01		2.8 Ω
10		1.85 Ω default)
11		1.4 Ω
D_DRV2_GATE_RES_HS_SEL [D9:D8]	**RW**	**High-side driver CH2 PU/PD resistance selection**
00		5.55 Ω
01		2.8 Ω
10		1.85 Ω default)
11		1.4 Ω
D_DRV1_GATE_RES_HS_SEL [D7:D6]	**RW**	**High-side driver CH1 PU/PD resistance selection**
00		5.55 Ω
01		2.8 Ω
10		1.85 Ω default)
11		1.4 Ω

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 19: 0x08 – Config Register 3

Data Bit / Name	D21	D20	D19	D18	D17	D16	D15	D14
	–	–	–	–	–	–	–	–
Data Bit / Name	D13	D12	D11	D10	D9	D8	D7	D6
	GATE_STG_CONFIG	SW2_SHORT_CONFIG	SW1_SHORT_CONFIG	VOUT2_OCL_CONFIG	VOUT1_OCL_CONFIG	VDRV_OV_CONFIG	VDRV_UV_CONFIG	VIN_OV_CONFIG

ADDRESS: 01000b

- [D21]		
0		
1		
- [D20]		
0		
1		
- [D19]		
0		
1		
- [D18]		
0		
1		
- [D17]		
0		
1		
- [D16]		
0		
1		
- [D15]		
0		
1		
- [D14]		
0		
1		
GATE_STG_CONFIG [D13]	**RW**	**Gate Short to ground configuration**
0		Fault triggers hiccup (default)
1		Fault resets VOUTx_EN
SW2_SHORT_CONFIG [D12]	**RW**	**SW2 Short configuration**
0		Fault triggers hiccup (default)
1		Fault resets VOUT2_EN
SW1_SHORT_CONFIG [D11]	**RW**	**SW1 Short configuration**
0		Fault triggers hiccup (default)
1		Fault resets VOUT1_EN
VOUT2_OCL_CONFIG [D10]	**RW**	**VOUT2 Overcurrent configuration**
0		Fault triggers hiccup (default)
1		Fault resets VOUT2_EN
VOUT1_OCL_CONFIG [D9]	**RW**	**VOUT1 Overcurrent configuration**
0		Fault triggers hiccup (default)
1		Fault resets VOUT1_EN
VDRV_OV_CONFIG [D8]	**RW**	**VDRV Overvoltage configuration**
0		Resume normal operation when fault is removed (default)
1		Fault resets VOUT1/2_EN
VDRV_UV_CONFIG [D7]	**RW**	**VDRV Undervoltage configuration**
0		Resume normal operation when fault is removed (default)
1		Fault resets VOUT1/2_EN
VIN_OV_CONFIG [D6]	**RW**	**VIN Overvoltage configuration**
0		Resume normal operation when fault is removed (default)
1		Fault resets VOUT1/2_EN

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 20: 0x09 – Config Register 4

Data Bit / Name	D21	D20	D19	D18	D17	D16	D15	D14
	–	–	–	–	–	–	–	–
Data Bit / Name	D13	D12	D11	D10	D9	D8	D7	D6
	–	–	–	–	D_CS2_RSHUNT_SEL		D_CS1_RSHUNT_SEL	

ADDRESS: 01001b

– [D21]		
0		
1		
– [D20]		
0		
1		
– [D19]		
0		
1		
– [D18]		
0		
1		
– [D17]		
0		
1		
– [D16]		
0		
1		
– [D15]		
0		
1		
– [D14]		
0		
1		
– [D13]		
0		
1		
– [D12]		
0		
1		
– [D11]		
0		
1		
– [D10]		
0		
1		
D_CS2_RSHUNT_SEL [D9:D8]	**RW**	**Shunt resistor selection for current sense of CH2**
00		5 mΩ (default)
01		10 mΩ
10		15 mΩ
11		20 mΩ
D_CS1_RSHUNT_SEL [D7:D6]	**RW**	**Shunt resistor selection for current sense of CH1**
00		5 mΩ (default)
01		10 mΩ
10		15 mΩ
11		20 mΩ

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 21: 0x0A – Config Register 5

Data Bit / Name	D21	D20	D19	D18	D17	D16	D15	D14
	–	DYS_PWR_DIS	VOUT2_SS_SEL			VOUT1_SS_SEL		
Data Bit / Name	D13	D12	D11	D10	D9	D8	D7	D6
	D_CLK_PWM_DITH_AMPL_SEL		D_CLK_PWM_FREQ_SEL			DCDC_MODE		

ADDRESS: 01010b

- [D21]		
0		
1		
DYS_PWR_DIS [D20]		**Multiphase dynamic power disable**
0		Enabled
1		Disabled (default)
VOUT2_SS_SEL [D19:D17]	**RW**	**VOUT2 Soft start time selection**
000		1 ms
001		1.5 ms
010		2.7 ms
011		5 ms (default)
100		7.5 ms
101		10 ms
110		15 ms
111		20 ms
VOUT1_SS_SEL [D16:D14]	**RW**	**VOUT1 Soft start time selection**
000		1 ms
001		1.5 ms
010		2.7 ms
011		5 ms (default)
100		7.5 ms
101		10 ms
110		15 ms
111		20 ms
D_CLK_PWM_DITH_AMPL_SEL [D13:D12]	**RW**	**Dithering amplitude selection**
00		±5%
01		0
10		±10% (default)
11		±15%
D_CLK_PWM_FREQ_SEL [D11:D9]	**RW**	**Frequency selection**
000		200 kHz
001		250 kHz (default)
010		300 kHz
011		350 kHz
100		400 kHz
101		450 kHz
DCDC_MODE [D8:D6]	**RW**	**DCDC Operative mode selection**
000		Boost 1 Channel (80 W) or Boost 1 Channel - Slave (240 W) (default)
001		Buck Channel 1 + Boost Channel 2
010		Boost Array Master (160 W) or Boost Array Master (>160 W)
011		Boost 2 Channels (80 W / 80 W) or Boost 2 Channels - Slave (320 W)
100		Buck-Boost
101		Buck 1 Channel (80 W) or Buck 1 Channel - Slave (240 W)
110		Buck 2 Channels (80 W / 80 W) or Buck 2 Channels - Slave (320 W)
111		Buck Array Master (160 W) or Buck Array Master (>160 W)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Table 22: 0x0B – Verify Register 0

Data Bit / Name	D21	D20	D19	D18	D17	D16	D15	D14
	–	–	–	–	–	VOUT2_OV_FAIL	VOUT2_UV_FAIL	VOUT1_OV_FAIL
Data Bit / Name	D13	D12	D11	D10	D9	D8	D7	D6
	VOUT1_UV_FAIL	TSD_FAIL	VIN_OV_FAIL	VIN_UV_FAIL	VDRVOV_INT_FAIL	VDRVUV_INT_FAIL	VDDOK_INT_FAIL	VPOSOK_INT_FAIL

ADDRESS: 01011b

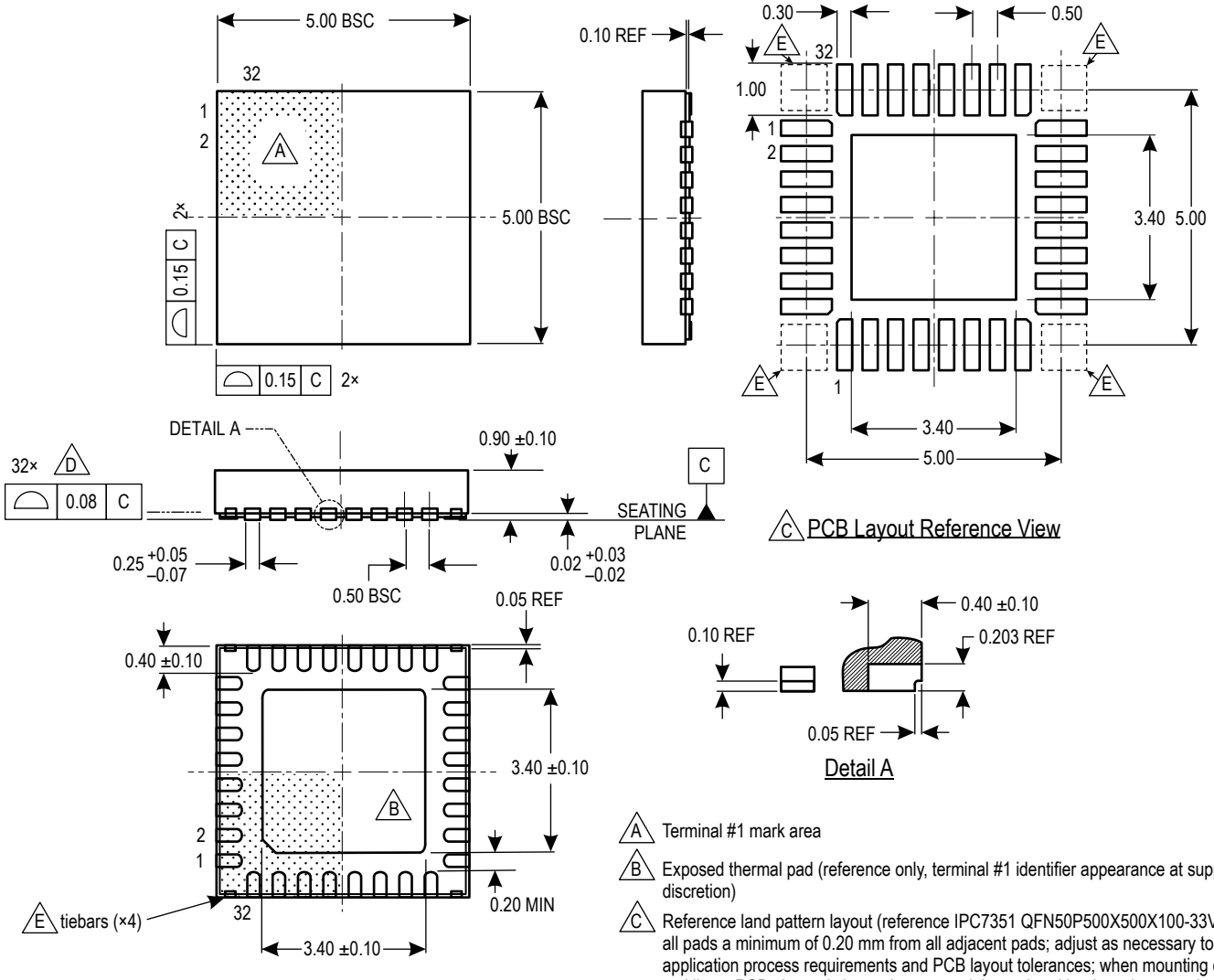
- [D21]		
0		
1		
- [D20]		
0		
1		
- [D19]		
0		
1		
- [D18]		
0		
1		
- [D17]		
0		
1		
VOUT2_OV_FAIL [D16]	**R/W1C**	**Indicates if the VOUT2 overvoltage circuit failed its self-test**
0		Self-test passed (default value at power-up).
1		Self-test failed. FFn set low, write 1 to clear and re-gain FFn functionality.
VOUT2_UV_FAIL [D15]	**R/W1C**	**Indicates if the VOUT2 undervoltage circuit failed its self-test**
0		Self-test passed (default value at power-up).
1		Self-test failed. FFn set low, write 1 to clear and re-gain FFn functionality.
VOUT1_OV_FAIL [D14]	**R/W1C**	**Indicates if the VOUT1 overvoltage circuit failed its self-test**
0		Self-test passed (default value at power-up).
1		Self-test failed. FFn set low, write 1 to clear and re-gain FFn functionality.
VOUT1_UV_FAIL [D13]	**R/W1C**	**Indicates if the VOUT1 undervoltage circuit failed its self-test**
0		Self-test passed (default value at power-up).
1		Self-test failed. FFn set low, write 1 to clear and re-gain FFn functionality.
TSD_FAIL [D12]	**R/W1C**	**Indicates if the TSD circuit failed its self-test**
0		Self-test passed (default value at power-up).
1		Self-test failed. FFn set low, write 1 to clear and re-gain FFn functionality.
VIN_OV_FAIL [D11]	**R/W1C**	**Indicates if the VIN overvoltage circuit failed its self-test**
0		Self-test passed (default value at power-up).
1		Self-test failed. FFn set low, write 1 to clear and re-gain FFn functionality.
VIN_UV_FAIL [D10]	**R/W1C**	**Indicates if the VIN undervoltage circuit failed its self-test**
0		Self-test passed (default value at power-up).
1		Self-test failed. FFn set low, write 1 to clear and re-gain FFn functionality.
VDRVOV_INT_FAIL [D9]	**R/W1C**	**Indicates if the VDRV overvoltage circuit failed its self-test**
0		Self-test passed (default value at power-up).
1		Self-test failed. FFn set low, write 1 to clear and re-gain FFn functionality.
VDRVUV_INT_FAIL [D8]	**R/W1C**	**Indicates if the VDRV undervoltage circuit failed its self-test**
0		Self-test passed (default value at power-up).
1		Self-test failed. FFn set low, write 1 to clear and re-gain FFn functionality.
VDDOK_INT_FAIL [D7]	**R/W1C**	**Indicates if the VDD undervoltage circuit failed its self-test**
0		Self-test passed (default value at power-up).
1		Self-test failed. FFn set low, write 1 to clear and re-gain FFn functionality.
VPOSOK_INT_FAIL [D6]	**R/W1C**	**Indicates if the VPOSA undervoltage circuit failed its selftest**
0		Self-test passed (default value at power-up).
1		Self-test failed. FFn set low, write 1 to clear and re-gain FFn functionality.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000378, Rev. 3 and JEDEC MO-220VHHD-5)
Dimensions in millimeters – NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P500X500X100-33V6M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Tiebars (×4) are electrically connected to thermal pad. Avoid active traces in this area to avoid shorts. Ground plane in this area is acceptable when appropriate.

Figure 28: Package ET, 32-Pin QFN with Exposed Pad and Wettable Flank

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

REVISION HISTORY

Number	Date	Description
–	February 3, 2026	Initial release

Copyright 2026, Allegro MicroSystems.

Allegro MicroSystems reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.

Allegro's products are not to be used in any devices or systems, including but not limited to life support devices or systems, in which a failure of Allegro's product can reasonably be expected to cause bodily harm.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

Copies of this document are considered uncontrolled documents.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com