A8426

High Performance Photoflash Capacitor Charger with IGBT Driver

Discontinued Product

This device is no longer in production. The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: June 30, 2017

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, contact Allegro Sales.

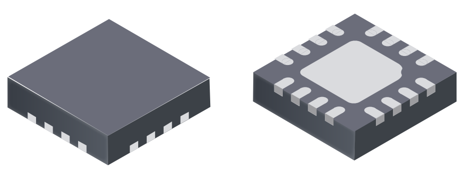
NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

High Performance Photoflash Capacitor Charger with IGBT Driver

Features and Benefits

- Wide battery voltage range: 1.5 to 11 V
- Integrated 55 V DMOS switch with 3.2 A current capability
- User-adjustable peak current limit, from 1 to 3.2 A
- Secondary-side voltage sensing for easily-adjustable output voltage
- >75% efficiency
- Fast charging time
- Charge complete indication
- Flexible, high current IGBT driver
  - Independent IGBT driver supply
  - Separate sink and source pins with 6 Ω pull-up and 20 Ω pull-down
  - Interlocked trigger pins improve noise immunity
- No primary-side Schottky diode needed

Package: 16-contact TQFN (suffix ES)



Not to scale

Description

The A8426 is a highly integrated IC that rapidly charges photoflash capacitors for SLR cameras, digital cameras, and camcorders with integrated digital cameras. A flexible IGBT driver is integrated to save board space.

The A8426 integrates a 3.2 A-capable, 55 V-rated DMOS switch that drives the transformer in flyback configuration, allowing optimized design with tight coupling and high efficiency. The peak switch current is user-adjustable between 1 and 3.2 A, using a resistor to ground. A proprietary control scheme optimizes the capacitor charging time. Low quiescent current and low-power Standby mode current further improve system efficiency and extend battery life.

The A8426 is available in a 16-contact 3 mm × 3 mm TQFN package with exposed pad for enhanced thermal performance. This small, very thin profile (0.75 mm nominal overall height) package is ideal for space-constrained applications. It is lead (Pb) free, with 100% matte-tin leadframe plating.

Applications include:

- SLR camera flash
- Digital camcorder/DSC combo flash
- 2 Li+ input strobe

Typical Application

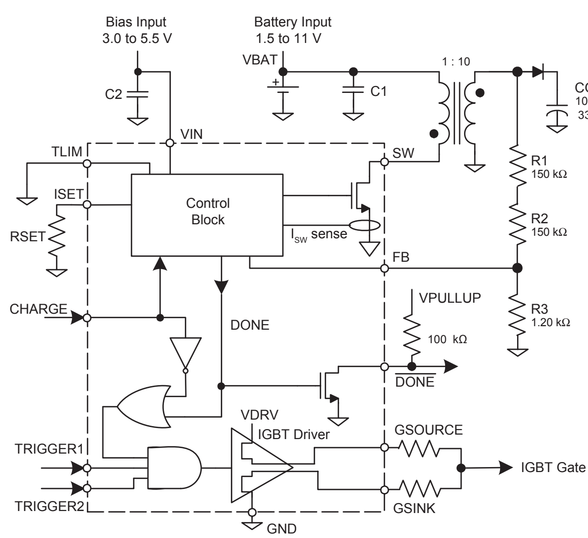


Figure 1. Typical application circuit with resistor bridge control of feedback.

Selection Guide

Part Number	Packing*
A8426EESTR-T	Tape and reel, 1500 pieces/reel

*Contact Allegro for additional packing options.

Absolute Maximum Ratings

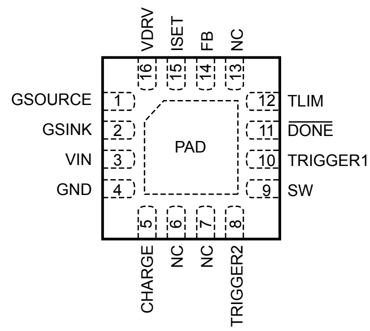
Characteristic	Symbol	Notes	Rating	Units
SW Pin	V_{SW}		–0.3 to 55	V
VIN Pin	V_{IN}		–0.3 to 7	V
Remaining Pins			–0.3 to V_{IN} + 0.3 V	V
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
Maximum Junction	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	47	ºC/W

*Additional thermal information available on Allegro website.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Pin-out Diagram



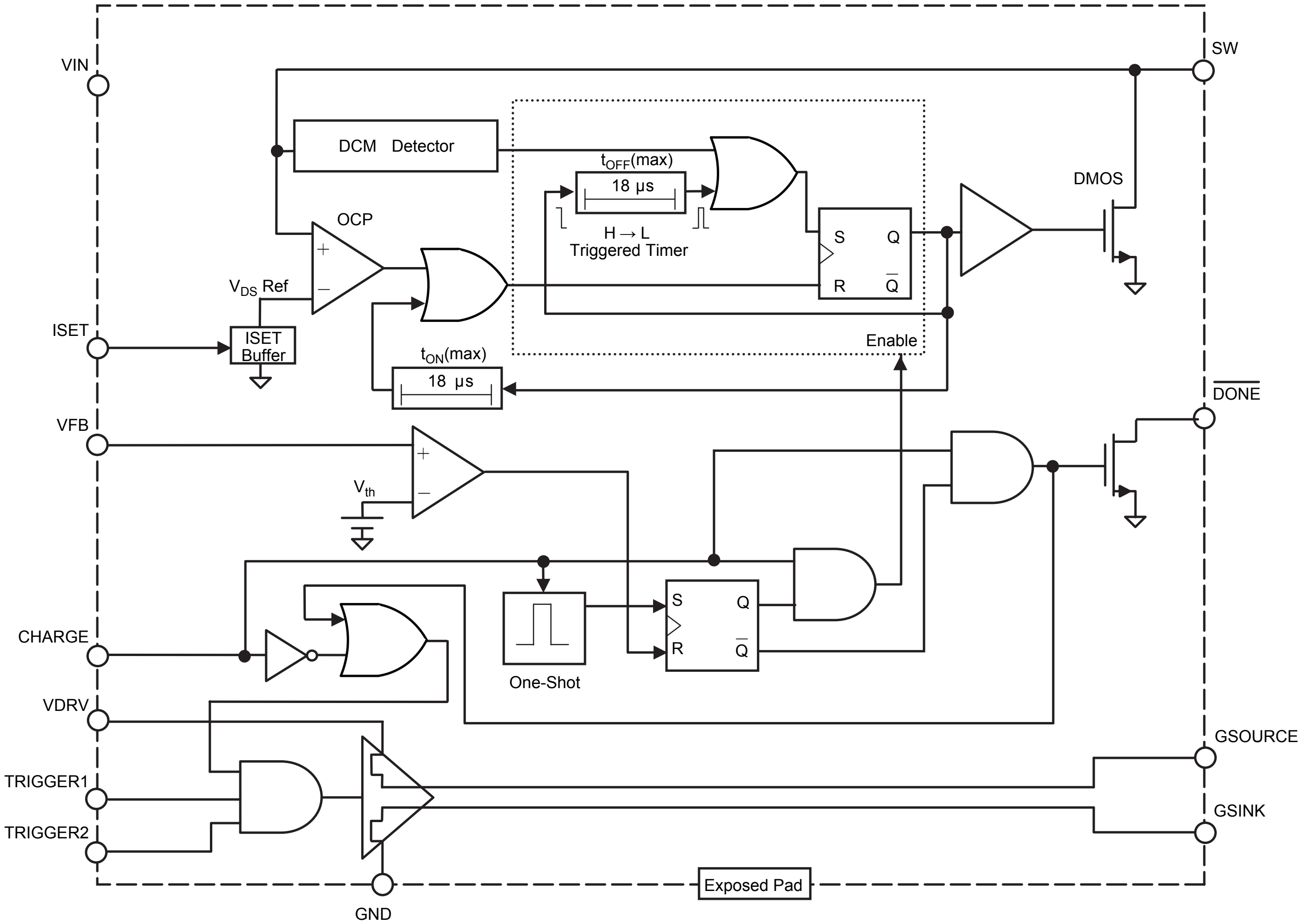
(Top View)

Terminal List Table

Number	Name	Function
1	GSOURCE	IGBT gate drive – source connection
2	GSINK	IGBT gate drive – sink connection
3	VIN	IC bias input, connect to a 3.0 to 5.5 V supply; for single Li+ battery applications this pin may be connected to the battery with sufficient decoupling
4	GND	Ground connection
5	CHARGE	Pull high to initiate charging; pull low to enter low-power standby mode
6, 7, 13	NC	No connection
8	TRIGGER2	IGBT input trigger 2; internally ANDed with TRIGGER1 pin
9	SW	Swtich pin; drain connection of internal power DMOSFET switch
10	TRIGGER1	IGBT input trigger 1; internally ANDed with TRIGGER2 pin
11	$\overline{\text{DONE}}$	Open drain pin; indicates charge complete when pulled low by internal MOSFET
12	TLIM	For production test only; connect to GND on PCB
14	FB	Output feedback
15	ISET	Sets the maximum switch current; connect an external resistor to GND to set the target peak current
16	VDRV	Supply for IGBT gate driver
–	EP	Exposed pad for enhanced thermal dissipation

ALLEGRO microsystems
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Functional Block Diagram



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ELECTRICAL CHARACTERISTICS typical values valid at V_{IN} = 3.6 V, R_{SET} = 33.2 kΩ, I_{SWlim} = 2.0 A, and T_A=25°C, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VBAT Pin Voltage Range[1]	V_{BAT}		1.5	–	11	V
VIN Pin Voltage Range[1]	V_{IN}		3.0	–	5.5	V
UVLO Enable Threshold	V_{INUV}	V_{IN} rising	2.55	2.65	2.75	V
UVLO Hysteresis	$V_{INUVhys}$		–	150	–	mV
Switch Current Limit[2]	$I_{SWlimMAX}$	Maximum, R_{SET} = 21.8 kΩ	2.9	3.2	3.5	A
	$I_{SWlimMIN}$	Minimum, R_{SET} = 72 kΩ	–	1.0	–	A
SW Current Limit to ISET Current Ratio	I_{SWlim}/I_{SET}	R_{SET} = 21.8 kΩ, CHARGE = high	–	58.5	–	kA/A
ISET Pin Voltage While Charging	V_{SET}	R_{SET} = 35 kΩ, CHARGE = high	–	1.2	–	V
ISET Pin Internal Resistance	$R_{SET(INT)}$		–	330	–	Ω
Switch On-Resistance	$R_{SWDS(on)}$	V_{IN} = 3.6 V, I_D = 800 mA, T_A = 25°C	–	0.2	–	Ω
Switch Leakage Current[1]	I_{SWlk}	V_{SW} = V_{BAT}(max), in shutdown	–	–	1	μA
VIN Pin Supply Current	I_{VIN}	Shutdown (CHARGE = low, TRIGGER = low)	–	0.01	1	μA
		Charging done (CHARGE = high, $\overline{\text{DONE}}$ = low)	–	25	100	μA
		Charging (CHARGE = high, TRIGGER = low)	–	2	–	mA
CHARGE Pin Input Current	I_{CHARGE}	CHARGE = V_{IN}	–	36	–	μA
CHARGE Pin Input Voltage High[1]	$I_{CHARGE(H)}$	Over input supply range, V_{IN}	1.4	–	–	V
CHARGE Pin Input Voltage Low[1]	$I_{CHARGE(L)}$	Over input supply range, V_{IN}	–	–	0.4	V
CHARGE Pin Pull-down Resistor	R_{CHARGE}		–	100	–	kΩ
Maximum Switch-off Timeout	t_{offMAX}		–	18	–	μs
Maximum Switch-on Timeout	t_{onMAX}		–	18	–	μs
$\overline{\text{DONE}}$ Pin Output Leakage Current[1]	I_{DONElk}		–	–	1	μA
$\overline{\text{DONE}}$ Pin Output Low Voltage[1]	V_{DONEL}	32 μA into $\overline{\text{DONE}}$ pin	–	–	100	mV
FB Threshold[1]	V_{FBth}		1.187	1.205	1.223	V
FB Input Current	I_{FB}	V_{FB} = 0 V to VIN	–	12	–	nA
Minimum dV/dt for ZVS Comparator	dV/dt	Measured at SW pin	–	20	–	V/μs
IGBT Driver						
VDRV Pin Supply Voltage (for IGBT Driver)[1]	V_{DRV}		3	–	5.5	V
TRIGGERx Pins Input Current	I_{TRIG}	$V_{TRIGGER}$ = VIN	–	36	–	μA
TRIGGERx Pins High Input Voltage[1]	$V_{TRIG(H)}$	Over input supply range, V_{IN}	1.4	–	–	V
TRIGGERx Pins Low Input Voltage[1]	$V_{TRIG(L)}$	Over input supply range, V_{IN}	–	–	0.4	V
TRIGGERx Pins Pull-down Resistor	R_{TRIGPD}		–	100	–	kΩ
GSOURCE On-Resistance to VDRV	$R_{SrcDS(on)}$	V_{DRV} = 3.6 V, $V_{GSOURCE}$= 1.8 V	–	6	–	Ω
GSINK On-Resistance to GND	$R_{SnkDS(on)}$	V_{DRV} = 3.6 V, V_{GSINK}= 1.8 V	–	20	–	Ω
Propagation Delay (Rising)	t_{dr}	Connect GSOURCE to GSINK, R_{GATE} = 12 Ω, C_{LOAD}= 6500 pF, V_{DRV} = 3.6 V	–	30	–	ns
Propagation Delay (Falling)	t_{df}		–	140	–	ns
Output Rise Time	t_r		–	80	–	ns
Output Fall Time	t_f		–	320	–	ns

[1]Specifications over the range T_A= –40°C to 85°C; guaranteed by design and characterization.
[2]Current limit guaranteed by design and correlation to static test. Refer to Application Information section for peak current in actual circuits.

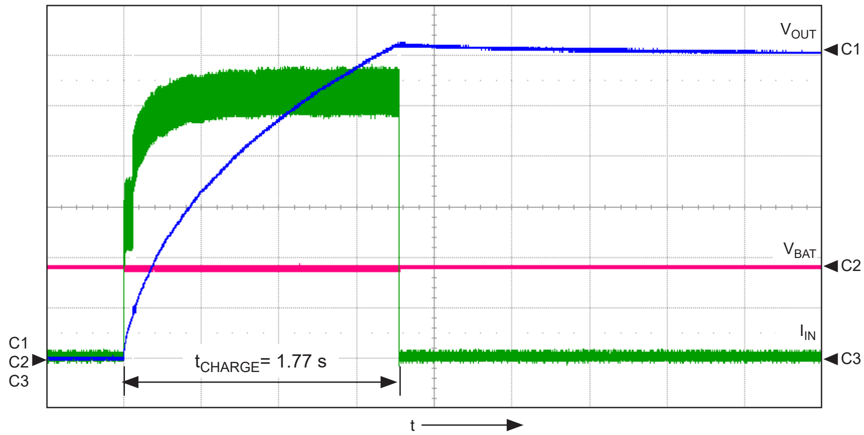
Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Performance Characteristics

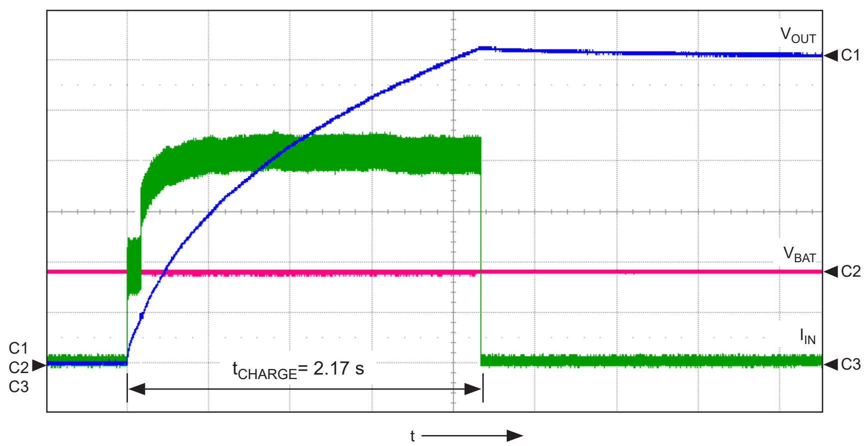
Charging Time at Various Peak Current Levels

Common Parameters		
Symbol	Parameter	Units/Division
C1	V_{OUT}	50 V
C2	V_{BAT}	2 V
C3	I_{IN}	250 mA
t	time	500 ms
Conditions	Parameter	Value
	V_{IN}	3.6 V
	V_{BAT}	3.6 V
	C_{OUT}	100 µF/330 V
Transformer = DCT9.5/5ER, L_P = 7 µH, N = 10		

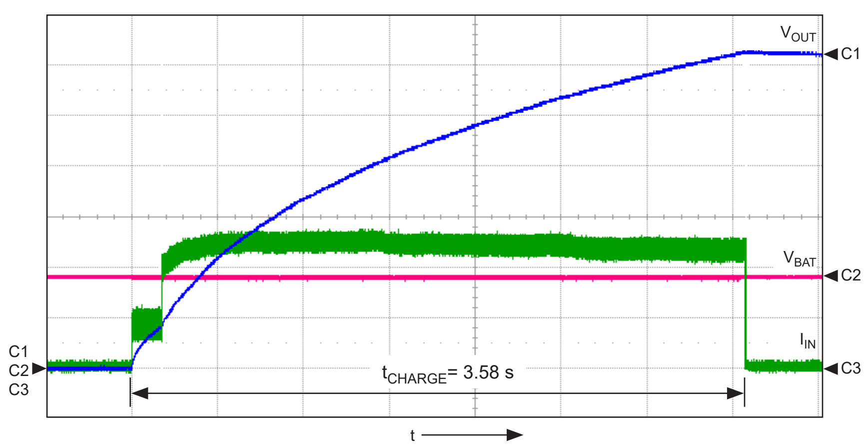
Conditions	Parameter	Value
	R_{SET}	25 kΩ
	I_P	≈3.15 A



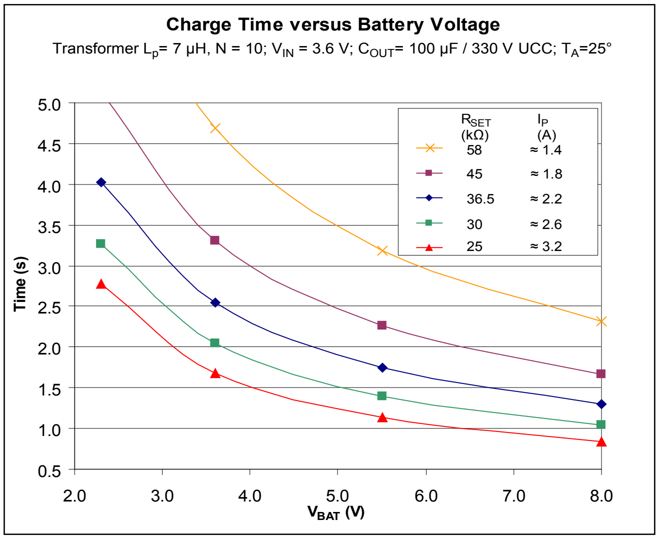
Conditions	Parameter	Value
	R_{SET}	30 kΩ
	I_P	≈2.6 A



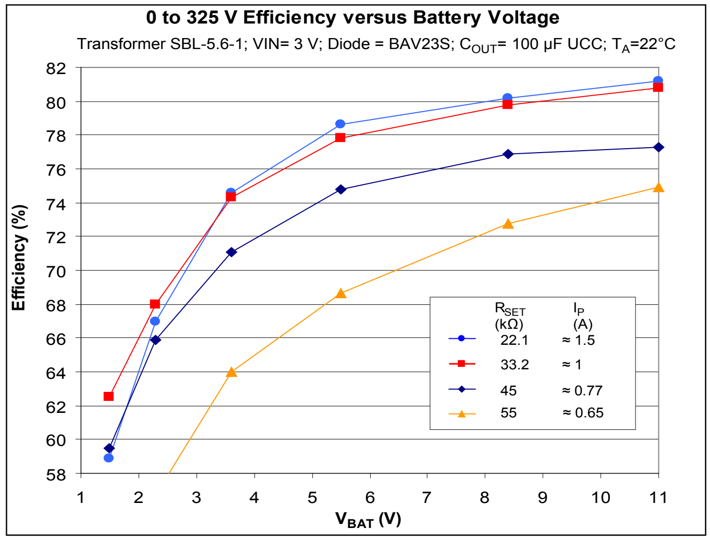
Conditions	Parameter	Value
	R_{SET}	45 kΩ
	I_P	≈1.8 A



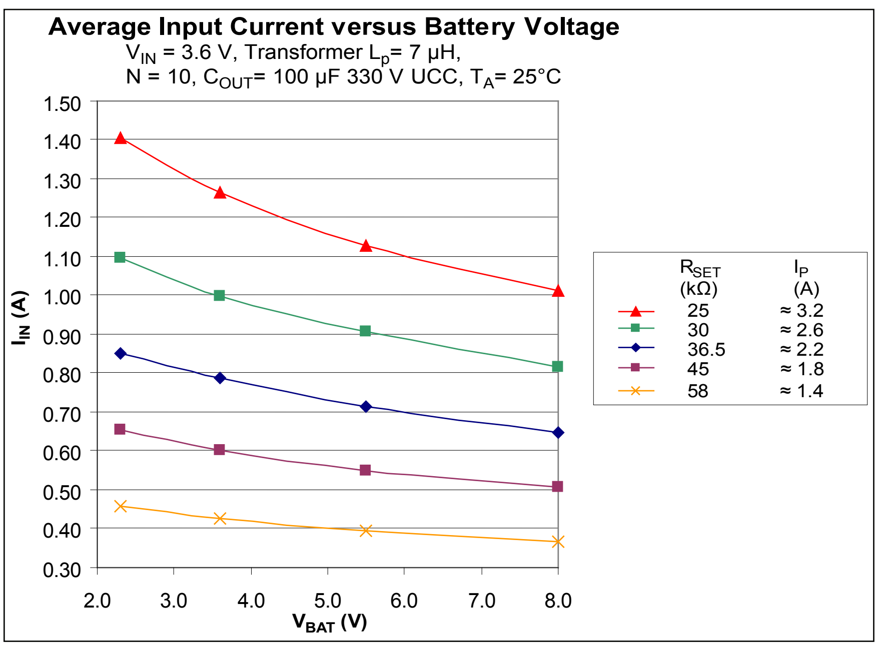
Performance Characteristics



C_{OUT}= 100 µF. For larger or smaller capacitances, charging time scales proportionally.



This data was obtained using a Kijima-Musen SBL-5.6-1 transformer (L_P = 9.8 µH, N = 10.2). Highest efficiency is achieved at high battery voltage and large peak current (1 to 1.5 A). At lower current (< 1 A), switching frequency increases and so do switching losses. Therefore a transformer with higher primary inductance is preferred when operating at lower current.

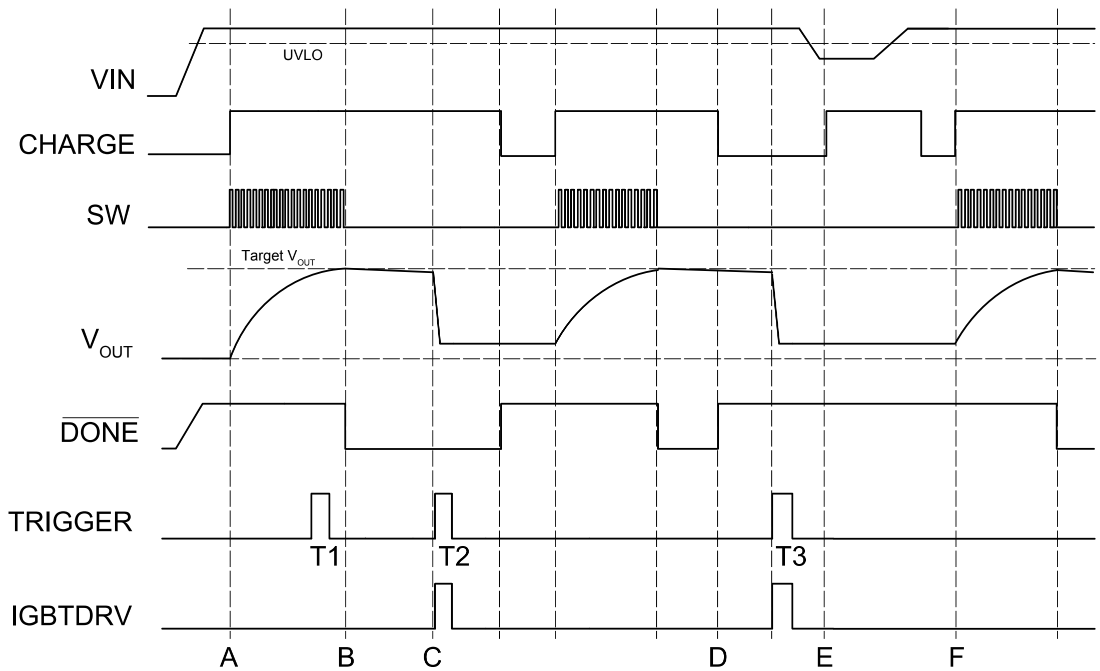


The average input current decreases with higher V_{BAT}. .

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Timing and IGBT Interlock Function

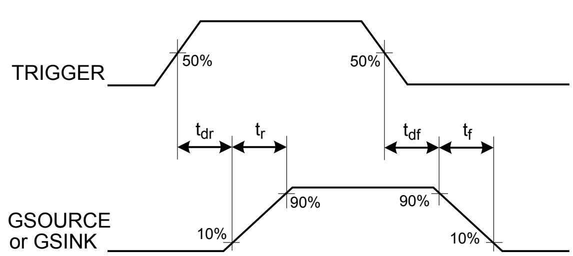
The two TRIGGER signals are internally ANDed together. As shown in the timing diagram, below, triggering is prohibited during the initial charging process. This prevents premature firing of the flash before the output capacitor has been charged to its target voltage. Refer to the section IGBT Gate Driver Interlock for details.



Explanation of Events

A	Start charging process by pulling CHARGE pin high, provided that V_{IN} is above the UVLO level. Triggering (T1) is blocked during the charging process (CHARGE and $\overline{\text{DONE}}$ pins are both high).
B	Charging stops when V_{OUT} reaches the target voltage level. Triggering (T2) is enabled after completion of charging (CHARGE pin is high and $\overline{\text{DONE}}$ pin is low).
C	Start a new charging process with a low-to-high transition at the CHARGE pin.
D	Pull the CHARGE pin low to put the controller into the low-power Standby mode. Triggering (T3) is always enabled when CHARGE is low.
E	Charging does not start, because V_{IN} is below the UVLO level when the CHARGE pin goes high.
F	After V_{IN} goes above the UVLO level, another low-to-high transition at the CHARGE pin is required to start the charging process.

IGBT Drive Timing Definition



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Application Information

Circuit Description

The A8426 is a photoflash capacitor charger control IC with a high current limit (up to 3.2 A) and low $R_{DS(on)}$ (0.23 Ω maximum). The IC also integrates an IGBT driver for strobe operation of the flash, dramatically saving board space in comparison with discrete solutions for strobe flash operation.

The IC is turned on by a low-to-high signal on the CHARGE pin, provided that V_{IN} is above the UVLO level. Note that if CHARGE is already high before V_{IN} reaches the UVLO threshold, charging will not start until CHARGE goes through another low-to-high transition. When the charging cycle is initiated, the primary current ramps up linearly at a rate determined by the battery voltage and the primary side inductan ce. When the primary current reaches the set limit, the internal MOSFET is turned off immediately to allow the energy to be dumped into the photoflash capacitor through the secondary winding. The secondary current drops linearly as the output capacitor is charged. The charging cycle starts again when the transformer flux is reset or after a predetermined time period (18 μs maximum off-time) has passed, whichever occurs first.

Target Output Voltage

Output voltage sensing is done using a resistor divider network (see figure 1: R1, R2 and R3) on the secondary side of the transformer. The target output voltage is determined by the ratio of the voltage divider:

$$(R_1+R_2+R_3)/R_3 = (V_{OUT}+V_d)/V_{FB}\ , \quad (1)$$

where V_d is the diode voltage drop (typically 1 to 2 V). R1 and R2 together must have a breakdown voltage of at least 300 V. A typical type 1206 surface mount resistor has a 150 V breakdown voltage rating. It is recommended that R1 and R2 have similar values to ensure an even voltage stress between them. Recommended values are:

$R_1 = R_2 = 150$ kΩ (type 1206), and

$R_3 = 1.20$ kΩ (type 0603),

which together yield a target voltage of 300 V.

Using higher resistance ratings for R1, R2, and R3 does not offer significant efficiency improvement, because the power loss of the feedback network occurs mainly during switch off-time, and off-time is only a small fraction of each charging cycle. Furthermore, if values of R1 and R2 are too high, effects of parasitic capacitance from the sensing network to GND may affect the accuracy of the target voltage.

When the designated output voltage is reached, the A8426 stops the charging until the CHARGE pin is toggled again. Alternatively, pulling the CHARGE pin low also stops the charging. The $\overline{\text{DONE}}$ pin is an open-drain indicator of when the designated output is reached. Pulling the CHARGE pin low puts the A8426 into the low-current Standby mode and it forces the $\overline{\text{DONE}}$ pin into a high impedence mode, irrespective of the output voltage.

Switch Current Limiting

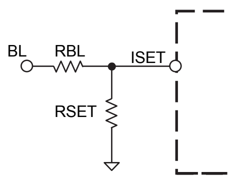
The peak switch current limit is determined by a resistor, RSET, connected between the ISET pin and GND. The value of RSET can be between 22 and 72 kΩ. This generates an ISET current between 17 and 55 μA, which corresponds to a desired peak switch current in a range from 1 to 3.2 A.

Smart Current Limit (Optional)

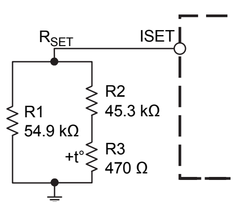
With the help of some simple external logic, the user can change the charging current according to the battery voltage. For example, assume that I_{SET} is normally 50 μA (for $I_{SWlim} = 2.75$ A). Referring to the

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

following illustration, when the battery voltage drops below 2.5 V, the signal at BL (battery-low) should go high. The resistor RBL, connecting BL to the ISET pin, then injects 20 μA into RSET. This effectively reduces ISET current to 30 μA (for I_{SWLIM} = 1.65 A). The disadvantage of this method is that 20 μA flows continuously while BL is high.



In another example of a possible application, we can make use of a PTC thermistor to decrease the switch current limit when the board temperature exceeds 65°C. Refering to the following figure, R3 is a PTC type thermistor such as the Murata PRF18BG471QB1RB.



In this configuration, the peak currents at various PCB temperatures are as follows:

T_{PCB} (°C)	R_3 (kΩ)	R_{SET} (kΩ)	I_{SWpeak} (A)
25	0.470	25.0	3.2
65	4.7	26.2	3.0
80	47.0	34.4	2.3

Selection of Transformer

1. The primary inductance, L_P, determines the on-time of the switch, as follows:

$$t_{on} = -L_P / R \times \ln(1 - I_{SWlim} \times R / V_{BAT}) , \quad (2)$$

where R is the total resistance in the primary current path (including $R_{SWDS(on)}$ and the DC resistance of the transformer).

If V_{BAT} is much larger than $I_{SWlim} \times R$, then t_{on} can be approximated using the following formula:

$$t_{on} = I_{SWlim} \times L_P / V_{BAT} . \quad (3)$$

2. The secondary inductance, L_S, determines the off-time of the switch, as follows:

$$t_{off} = (I_{SWlim} / N) \times L_S / V_{OUT} . \quad (4)$$

Because $L_S / L_P = N \times N$:

$$t_{off} = (I_{SWlim} \times L_P \times N) / V_{OUT} . \quad (5)$$

The minimum pulse width for t_{off} determines the minimum primary inductance required for the transformer. For example, if I_{SWlim} = 1.0 A, N = 10, and V_{OUT} = 315 V, then L_P must be at least 6.3 μH in order to keep t_{off} at 200 ns or longer. In general, choosing a transformer with larger L_P results in higher efficiency (because the higher the value of L_P, the lower the switch frequency, and hence the lower the switching loss). But transformers with higher L_P ratings also require more windings and larger magnetic cores. Therefore a trade-off must be made between transformer size and efficiency.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Selection of Switching Current Limit

The A8426 features continuously adjustable peak switching current between 1.0 and 3.2 A. This is done by selecting the value of the external resistor RSET (connected between the ISET pin and GND), which determines the ISET bias current, and therefore the switching current limit, I_{SWlim}.

To the first order approximation, I_{SWlim} is related to I_{SET} and R_{SET} by the following equation:

$$I_{SWlim} = I_{SET} \times \mathrm{K}$$

$$= (V_{SET} \times R_{SET}) \times \mathrm{K}\,, \qquad (6)$$

where K ≈ 60000 when the IC bias voltage, V_{IN}, is 3.6 V.

In real applications, the switching current limit is affected by bias voltage, battery voltage, and the transformer primary inductance, L_P. If necessary, the following expressions can be used to determine I_{SWlim} more accurately:

$$I_{SET} = V_{SET} / (R_{SET} + \mathrm{R}_{SET(INT)} - \mathrm{K} \times \mathrm{R}_{G(INT)})\,, \qquad (7)$$

where $R_{SET(INT)}$ is the internal resistance of the ISET pin (330 Ω typical), $R_{G(INT)}$ is the internal resistance of the bonding wire for the GND pin (27 mΩ typical), and:

$$I_{SWlim} = I_{SET} \times (\mathrm{K'} + V_{IN} \times \mathrm{K''}) + (V_{BAT} / L_P) \times t_d\,, \qquad (8)$$

where K' = 47500, K" = 3500, and t_d = delay in SW turn-off (0.12 µs typical).

Figure 2 shows the relationship between R_{SET} and I_{SWlim} at different bias voltages, V_{IN}, when battery voltage, V_{BAT}, is fixed at 3.6 V.

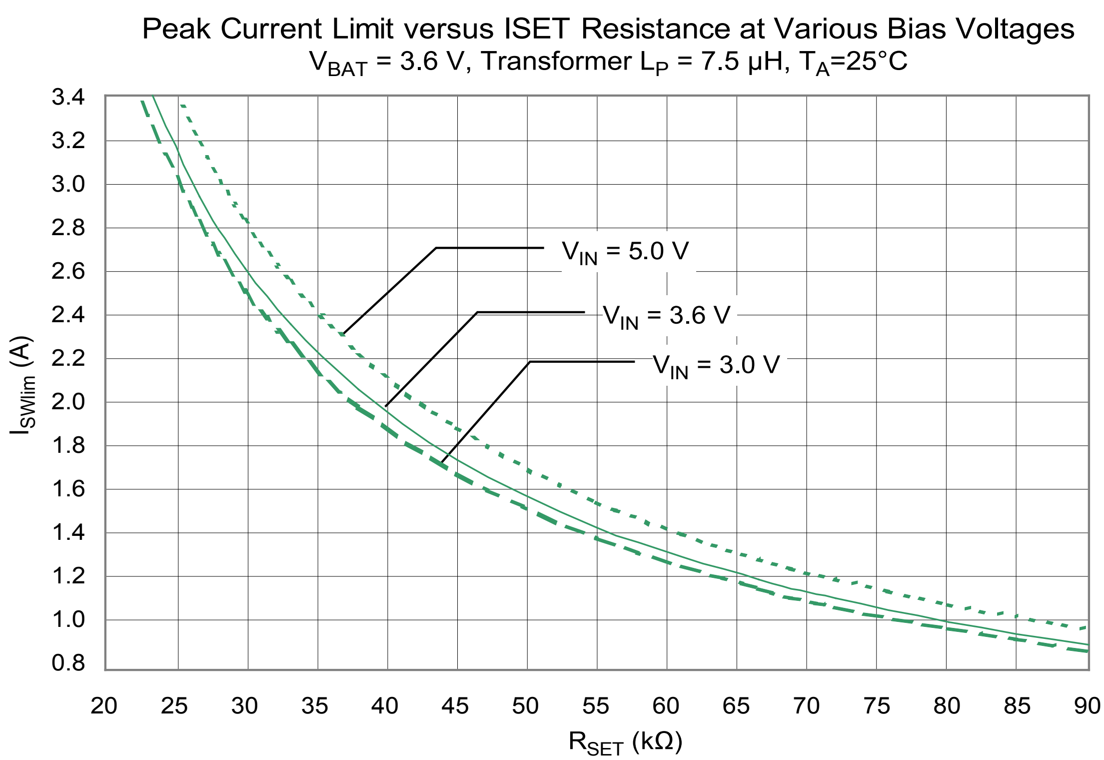


Figure 2. Chart of current versus limit settings, at fixed battery voltage

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Figure 3 shows the relation between RSET and I_{SWlim} at different battery voltages, when bias voltage is fixed at 3.6 V). Note that the spread is inversely proportional to the primary inductance of transformer used.

Fast Charging and Timer Modes

The A8426 achieves fast charging time and high efficiency by operating in discontinuous conduction mode (DCM) with zero-voltage-switching (ZVS). This operation is shown in figure 4.

The IC operates in the Timer mode when beginning to charge a completely discharged photoflash capacitor, usually when the output voltage, V_{OUT}, is less than approximately 35 V (depending on the inductance of transformer used). Timer mode is a fixed 18 µs off-time control. One advantage of the timer mode is that it limits the initial battery current surge and thus acts as a “soft-start,” as shown in figure 5.

As soon as sufficient voltage has built up at the output capacitor, the IC changes into fast-charging mode.

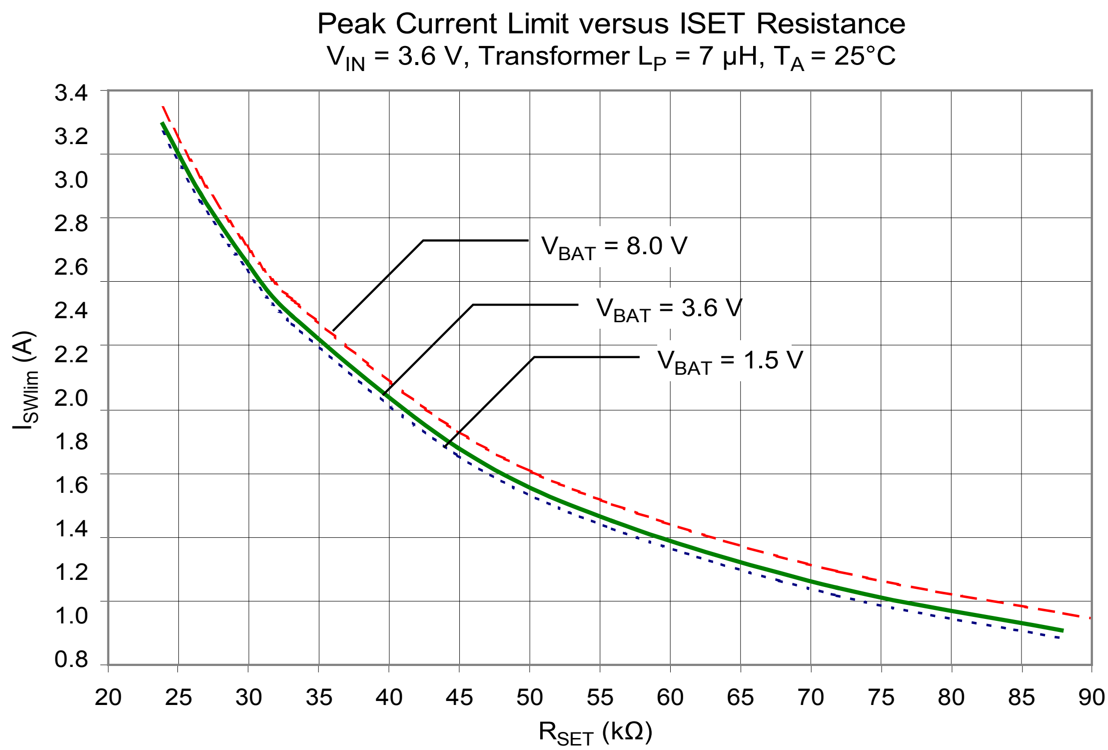
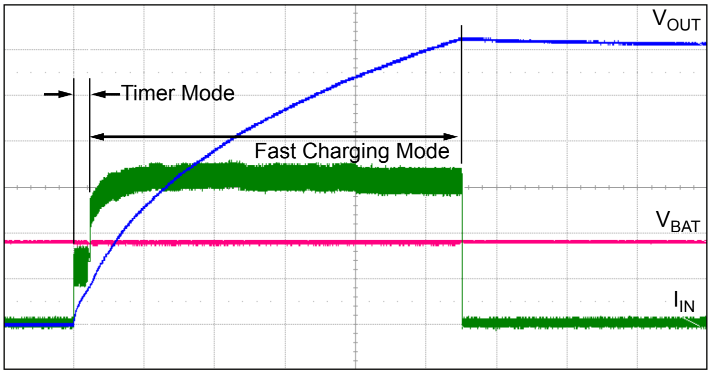


Figure 3. Chart of current versus limit settings, at fixed bias voltage

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

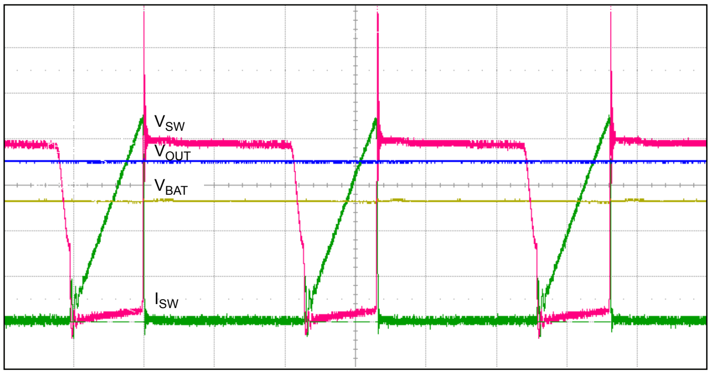
As shown in figure 6, in this mode the next switching cycle starts after the secondary-side current has stopped flowing, and the switch voltage has dropped to a minimum value. A special dV/dt detection circuit is used to allow minimum-voltage switching, even if the SW voltage does not drop to zero volts. This enables fast-charging to start earlier than previously possible, thereby reducing the overall charging time.

When output voltage is high enough (such that $V_r = V_{OUT}/ N$ is greater than V_{BAT}), true zero-voltage switching is achieved, which further improves efficiency as well as reducing switching noises (figure 7).



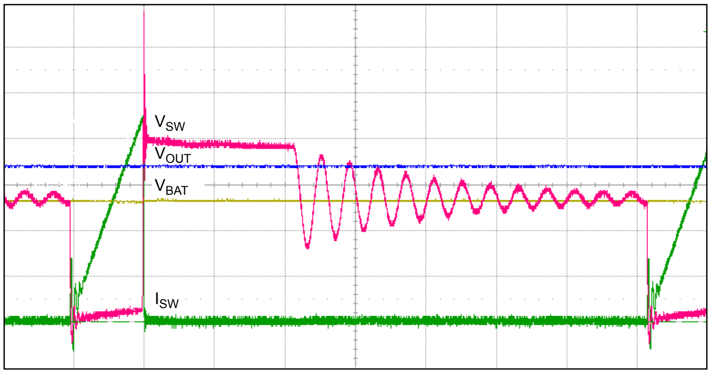
t =500 ms/div; V_{OUT} =50 V/div; V_{BAT} =1 V/div.; I_{IN} =250 mA/div.
V_{BAT} =3.6 V; C_{OUT} =100 µF/330 V; R_{SET}=36.5 kΩ (I_P≈ 2.2 A)

Figure 4. Relationship of Timer mode and Fast Charging mode



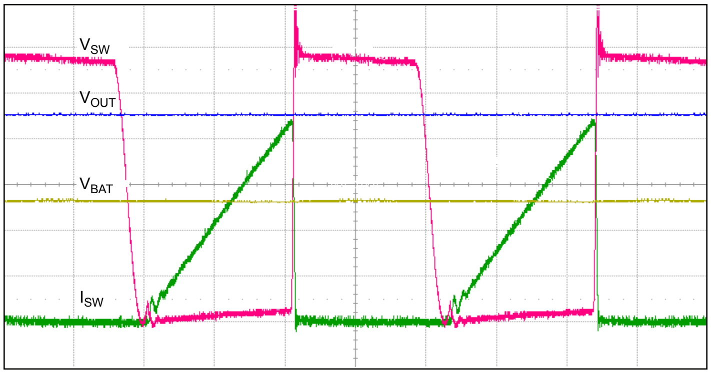
t = 2 µs/div; V_{OUT} =10 V/div; V_{BAT} =3 V/div.; V_{SW} =3 V/div;
I_{SW} =500 mA/div. V_{IN} = 3.6 V; V_{BAT} =8.0 V; R_{SET}=36.5 kΩ (I_P≈ 2.2 A);
Transformer =DCT9.5/5ER, L_P= 7 µH, N = 10

Figure 6. Fast-charging mode (DCM), V_{OUT} > 35 V



t = 2 µs/div; V_{OUT} =10 V/div; V_{BAT} =3 V/div.; V_{SW} =3 V/div;
I_{SW} =500 mA/div. V_{IN} = 3.6 V; V_{BAT} =8.0 V; R_{SET}=36.5 kΩ (I_P≈ 2.2 A);
Transformer =DCT9.5/5ER, L_P= 7 µH, N = 10

Figure 5. Timer mode (CCM), V_{OUT} < 35 V



t = 1 µs/div; V_{OUT} =20 V/div; V_{BAT} =3 V/div.; V_{SW} =3 V/div;
I_{SW} =500 mA/div. V_{IN} = 3.6 V; V_{BAT} =8.0 V; R_{SET}=36.5 kΩ (I_P≈ 2.2 A);
Transformer =DCT9.5/5ER, L_P= 7 µH, N = 10

Figure 7. Zero-voltage switching

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Components Recommendation

The A8426 uses secondary-side sensing, so the turns ratio, N, of the transformer is not critical for the final target voltage. However, using transformers with higher turns ratios (N = 12 or higher) generally results in lower efficiency and longer charge time.

Selection of the flyback transformer should be based on the peak current, according to the following table:

I_{Peak} Range (A)	Sup-plier	Part Number	L_P (μH)	N
1.0 to 2.0	TDK	LDT565630T-001	6	10.4
1.0 to 3.2	TDK	DCT9.5/5ER-UxxS003	7.6	10
1.4 to 3.2	TCE	T-17-160 (TTRN-060)	5.6	10.2

IGBT Gate Driver Application

The integrated IGBT driver is used to drive an external flash trigger IGBT. A dedicated VDRV pin is provided to supply optimum voltage for the internal IGBT. Separate GSOURCE and GSINK pins allow the user to adjust IGBT turn-on and turn-off rise times. For the Electrical Characteristics table in this document, IGBT drive timing is defined with the GSOURCE and GSINK pins connected together, and supplying a load comprising a 12 Ω resistor and a 6500 pF capacitor.

IGBT Gate Driver Interlock

The TRIGGER1 and TRIGGER2 pins are ANDed together inside the IC to control the IGBT gate driver. If only one TRIGGER pin is used, the other TRIGGER pin must be tied to the VIN pin to ensure that the unused TRIGGER pin is at logic high.

Triggering is disabled (locked) during charging. This is to prevent switching noise from interfering with the IGBT driver. After the CHARGE pin goes high (at the start of a charging cycle), the IC must wait for completion of the charging cycle ($\overline{\text{DONE}}$ goes low) before triggering can be enabled, according to the following chart:

Conditions		Resulting State
CHARGE	$\overline{\text{DONE}}$	IGBT Gate Driver
Low	Don't Care	Enabled
High	High	Disabled
High	Low	Enabled

The IGBT gate driver is always enabled when the CHARGE pin is low.

It is up to the system-level programming to ensure that a trigger signal is not applied without sufficient voltage at the output capacitor.

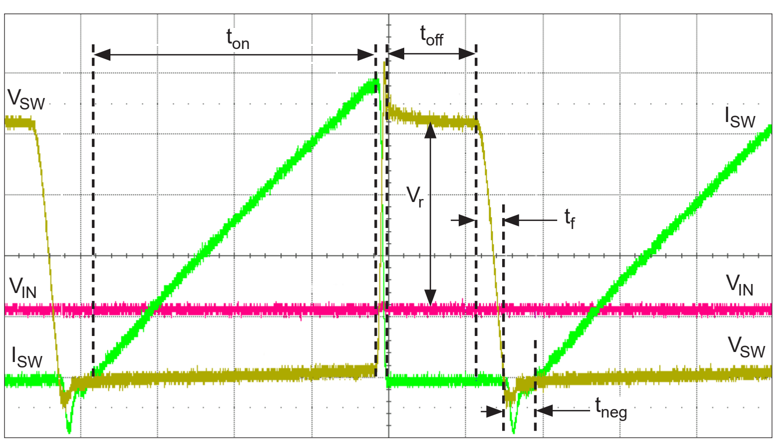
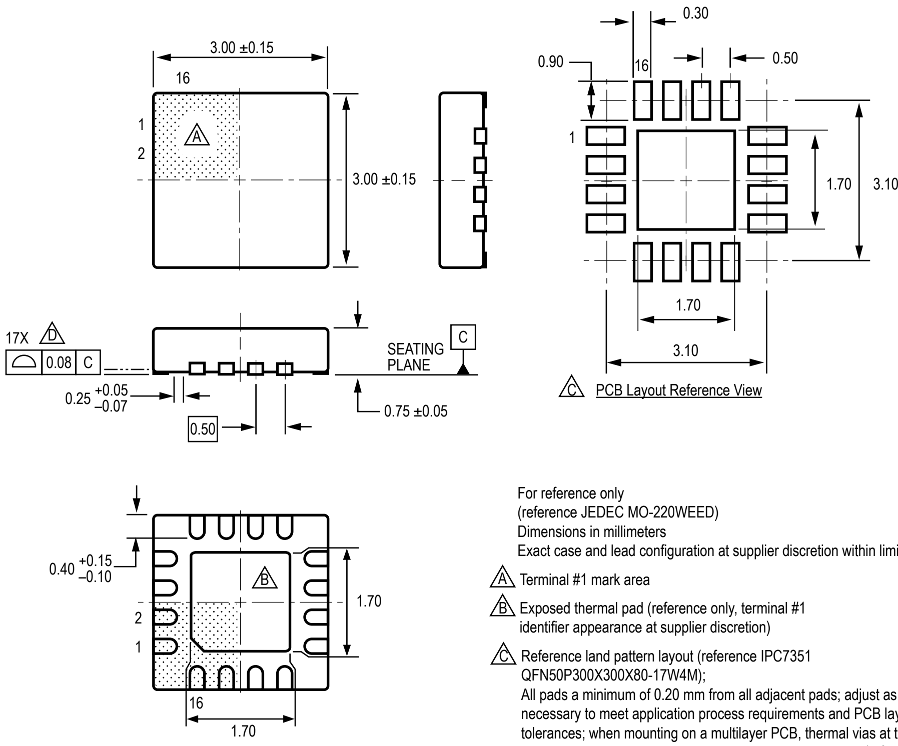


Figure 8. Relationship of t_{off} and switch output.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Package ES, 3 mm x 3 mm 16-Contact TQFN
with Exposed Thermal Pad



For reference only
(reference JEDEC MO-220WEED)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P300X300X80-17W4M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Revision History

Number	Date	Description
1	April 19, 2012	Update Selection Guide, miscellaneous format changes
2	December 5, 2016	Updated product status to Last Time Buy
3	June 30, 2017	Updated product status to Discontinued
4	June 20, 2018	Minor editorial updates
5	July 2, 2019	Minor editorial updates

For the latest version of this document, visit our website:
www.allegromicro.com

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com