Photoflash Capacitor Charger with Primary Side Sensing, Flexible Current Limit, and 55 V Power DMOS Switch

Discontinued Product

This device is no longer in production. The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: December 10, 2012

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, contact Allegro Sales.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

Photoflash Capacitor Charger with Primary Side Sensing, Flexible Current Limit, and 55 V Power DMOS Switch

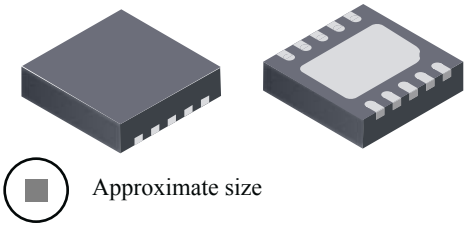
Features and Benefits

- Wide battery voltage range: 1.5 to 11 V
- Low quiescent current draw (1 µA max in shutdown mode)
- Flexible current limit:
  - External resistor sets default current (0.7 to 1.5 A)
  - Optional single-wire current limit programming through CHARGE pin
- Rugged and compact design:
  - Integrated 55 V DMOS switch
  - No feedback resistors
  - ISET open/short protection
  - Open diode/secondary winding protection
  - 3 mm × 3 mm footprint
- Charge Complete indication
- Flexible IGBT driver with separate sink and source

Applications

- Digital and film camera flash
- Digital video camera flash

Package: 10-contact TDFN (suffix EJ)



Approximate size

Description

The A8724 provides a robust Xenon photoflash solution for a wide range of cameras. Its wide battery voltage specifications allow designers to use a common device for camera using 2 or 4 cell Alkaline batteries as well as 1 or 2 cell Lithium ion batteries. Its 55V rated integrated power switch provides ample design margin, even for the 2 cell Lithium ion battery designs.

The A8724 detects the output voltage on the primary side and it eliminates the external feedback resistors. If the output diode or the secondary winding are disconnected, it prevents the output capacitor from being overcharged.

The A8724 features a flexible current limit scheme. The current limit is set by an external resistor at ISET, allowing designers to optimize the camera performance. The A8724 is protected against open circuit and short circuit condition on the ISET pin. Once the current limit is set, it can be optionally programmed as a percentage of the set current through a single wire interface, through the CHARGE pin.

The A8724 features an integrated flexible IGBT gate driver, with independent source and sink pins.

The A8724 is available in a 10-contact 3 mm × 3 mm TDFN package. This small, low profile (0.75 mm) package is ideal for space-constrained applications. It is lead (Pb) free, with 100% matte-tin leadframe plating.

Typical Applications

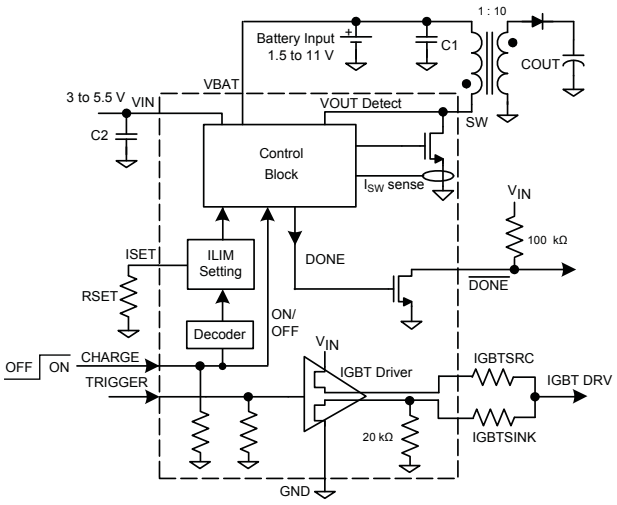


Figure 1a. Current set by RSET

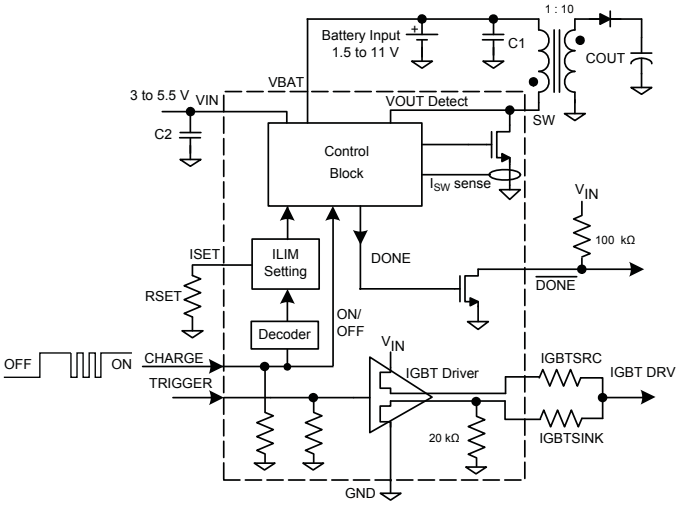


Figure 1b. Current programmed by CHARGE pin

Selection Guide

Part Number	Package	Packing
A8724EEJTR-T	10-contact TDFN	Tape and reel, 1500 pieces per reel

*Contact Allegro for additional ordering information.

Absolute Maximum Ratings

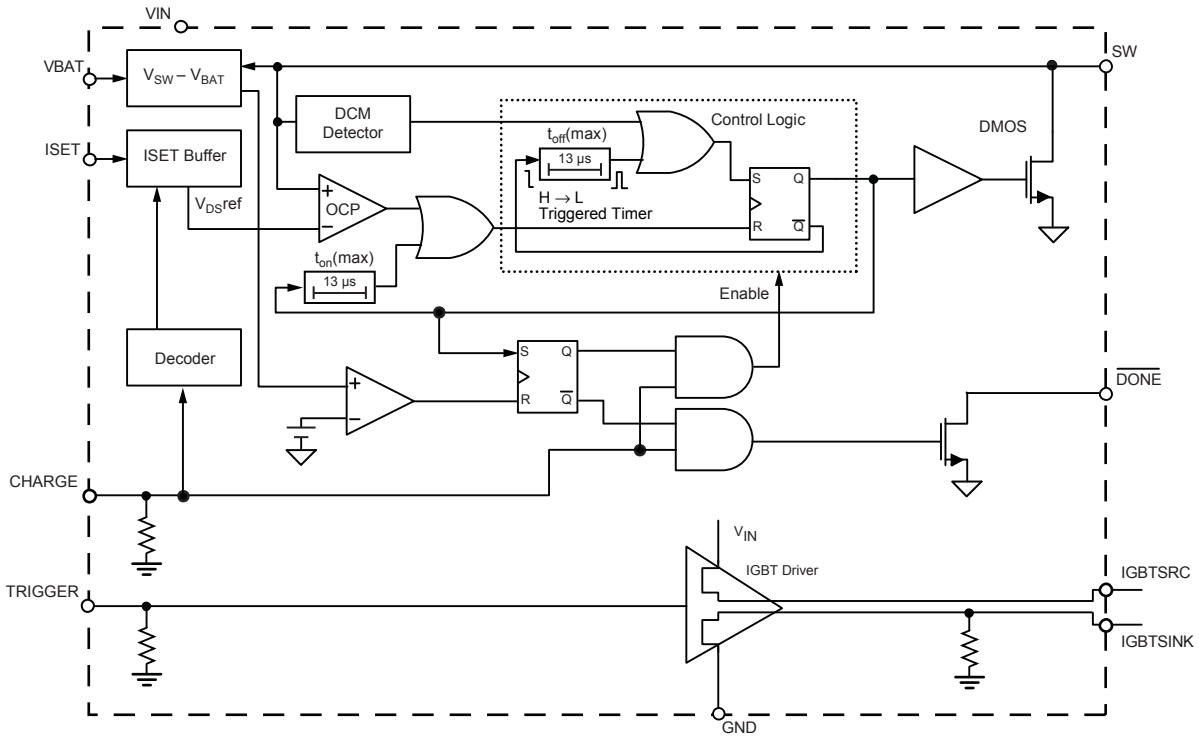
Characteristic	Symbol	Notes	Rating	Units
SW Pin	V_{SW}		–0.3 to 55	V
VBAT Pin	V_{BAT}		–0.3 to 12	
VIN Pin	V_{IN}		–0.3 to 6.0	V
Remaining Pins	V_I	Care should be taken to limit the current when –0.6 V is applied to these pins.	–0.6 to V_{IN} + 0.3	V
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

Thermal Characteristics

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	45	ºC/W

*Additional thermal information available on the Allegro website

Functional Block Diagram



ELECTRICAL CHARACTERISTICS Valid at V_{IN} = V_{BAT} = 3.6 V, R_{SET} = 22.6 kΩ, T_A = 25°C except • indicates specifications guaranteed from −40°C to 85°C ambient, unless otherwise specified

Characteristics	Symbol	Test Conditions		Min	Typ	Max	Unit
VIN Voltage Range[1]	V_{IN}		•	3	–	5.5	V
VBAT Pin Voltage Range[1]	V_{BAT}		•	1.5	–	11	V
UVLO Enable Threshold	V_{INUV}	V_{IN} rising through threshold		2.55	2.65	2.80	V
UVLO Hysteresis	$V_{INUVhys}$			–	150	–	mV
Supply Current	I_{IN}	Shutdown (CHARGE = 0 V, TRIGGER = 0 V)		–	0.01	1	µA
		Charging done (CHARGE = V_{IN}, DONE = 0 V)		–	10	50	µA
		Charging (CHARGE = V_{IN}, TRIGGER = 0 V)		–	2	–	mA
VBAT Pin Supply Current	I_{BAT}	Shutdown (CHARGE = 0 V, TRIGGER = 0 V)		–	0.01	1	µA
		Charging done (CHARGE = V_{IN}, DONE = 0 V)		–	–	1	µA
		Charging (CHARGE = V_{IN}, TRIGGER = 0 V)		–	–	50	µA
Current Limits							
Switch Current Limit	ILIM	100% setting		1.35	1.5	1.65	A
ILIM / ISET Current Ratio	ILIM / I_{SET}	CHARGE = high, 100% setting		–	27.8	–	kA/A
ISET Pin Voltage While Charging	V_{SET}	CHARGE = high, 100% setting		–	1.2	–	V
Switch Current Limit (ILIM Programming Input on CHARGE Pin)	I_{SWlim1}	Default setting		–	100	–	%
	I_{SWlim2}	One pulse applied to CHARGE pin		–	93	–	%
	I_{SWlim3}	Two pulses applied to CHARGE pin		–	86	–	%
	I_{SWlim4}	Three pulses applied to CHARGE pin		–	79	–	%
	I_{SWlim5}	Four pulses applied to CHARGE pin		–	71	–	%
	I_{SWlim6}	Five pulses applied to CHARGE pin		–	64	–	%
	I_{SWlim7}	Six pulses applied to CHARGE pin		–	57	–	%
	I_{SWlim8}	Seven pulses applied to CHARGE pin		–	50	–	%
Switch On-Resistance	$R_{DS(on)}$	I_{SW} = 800 mA		–	0.35	–	Ω
Switch Leakage Current[1]	I_{SWlk}	V_{SW} = 11 V, in shutdown	•	–	–	1	µA
TRIGGER and CHARGE Input Current	I_{CHARGE}, $I_{TRIGGER}$	V_{CHARGE} = $V_{TRIGGER}$ = V_{IN}		–	36	–	µA
TRIGGER and CHARGE Input Voltage High[1]	$V_{CHARGE(H)}$, $V_{TRIGGER(H)}$	Over V_{IN} supply range	•	1.2	–	–	V
TRIGGER and CHARGE Input Voltage Low[1]	$V_{CHARGE(L)}$, $V_{TRIGGER(L)}$	Over V_{IN} supply range	•	–	–	0.4	V

Continued on the next page…

ELECTRICAL CHARACTERISTICS (continued) Valid at $V_{IN} = V_{BAT} = 3.6$ V, $R_{SET} = 22.6$ kΩ, $T_A = 25°C$ except • indicates specifications guaranteed from −40°C to 85°C ambient, unless otherwise specified

Characteristics	Symbol	Test Conditions		Min	Typ	Max	Unit
ILIM Programming High Time at CHARGE Pin[2]	$t_{ILIM(H)init}$	Initial pulse		15	–	–	µs
	$t_{ILIM(H)}$	Subsequent pulses		0.2	–	–	µs
ILIM Programming Low Time at CHARGE Pin[2]	$t_{ILIM(L)}$			0.2	–	–	µs
Total ILIM Setup Time at CHARGE Pin[2]	$t_{ILIM(SU)}$			–	45	–	µs
Switch-Off Timeout	t_{off}			–	13	–	µs
Switch-On Timeout	t_{on}			–	13	–	µs
$\overline{DONE}$ Output Leakage Current[1]	I_{DONElk}		•	–	–	1	µA
$\overline{DONE}$ Output Low Voltage[1]	V_{DONEL}	32 µA into $\overline{DONE}$ pin	•	–	–	100	mV
Output Comparator Trip Voltage[1]	$V_{OUTTRIP}$	Measured as $V_{SW} - V_{BAT}$	•	31	31.5	32	V
Output Comparator Overdrive	V_{OUTOV}	200 ns pulse width (90% to 90% points)		–	200	400	mV
dV/dt Threshold of ZVS Comparator	dV/dt	Measured at SW node		–	20	–	V/µs
IGBT Driver							
IBGTSRC Resistance to V_{IN}	$R_{IGBTSRC}$	$V_{IGBTSRC} = 1.8$ V		–	6	–	Ω
IBGTSNK Resistance to GND	$R_{IGBTSNK}$	$V_{IGBTSNK} = 1.8$ V		–	24	–	Ω
Propagation Delay (Rising)[3]	t_{dr}	IGBTSRC and IGBTSNK connected together, measurement taken at pin; $R_{GATE} = 12$ Ω, $C_{LOAD} = 6500$ pF		–	16	–	ns
Propagation Delay (Falling)[3]	t_{df}			–	50	–	ns
Output Rise Time[3]	t_r			–	80	–	ns
Output Fall Time[3]	t_f			–	320	–	ns

[1]Specification over the range $T_A = –40°C$ to 85°C guaranteed by design and characterization.
[2]See figure 6 timing diagram for further explanation.
[3]See figure 2 timing diagram for further explanation.

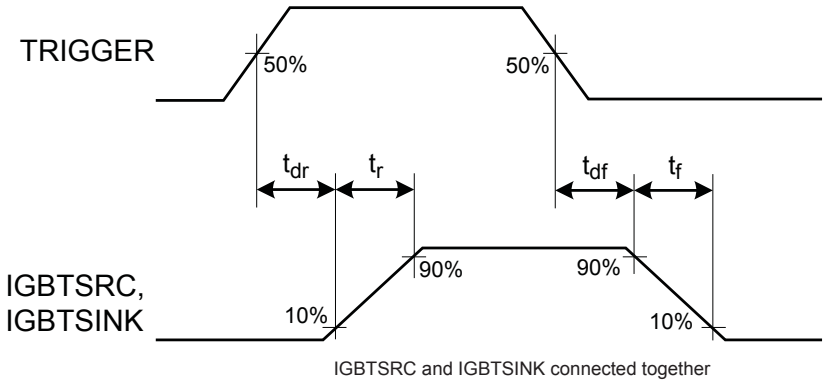
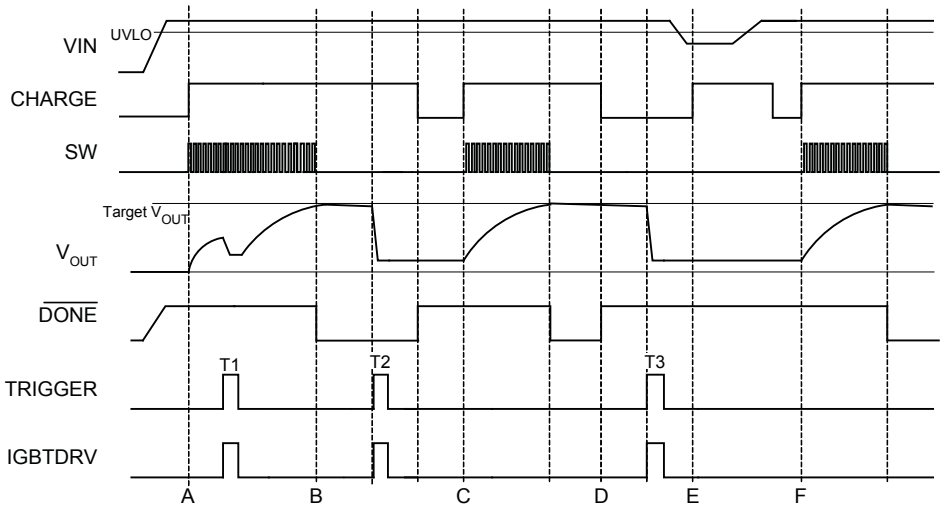


Figure 2. IGBT Drive Timing Definition

Operation Timing Diagram



Explanation of Events

A: Start charging by pulling CHARGE to high, provided that V_{IN} is above UVLO level.

B: Charging stops when V_{OUT} reaches the target voltage.

C: Start a new charging process with a low-to-high transition at the CHARGE pin.

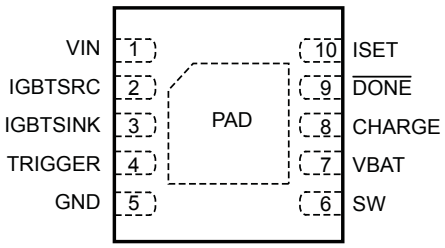
D: Pull CHARGE to low to put the controller in low-power standby mode.

E: Charging does not start, because V_{IN} is below UVLO level when CHARGE goes high.

F: After V_{IN} goes above UVLO, another low-to-high transition at the CHARGE pin is required to start the charging.

T1, T2, T3 (Trigger instances): IGBT driver output pulled high whenever the TRIGGER pin is at logic high. It is recommended to avoid applying any trigger pulses during charging.

Pin-out Diagram



(Top View)

Terminal List Table

Number	Name	Function
1	VIN	Input voltage. Connect to 3 to 5.5 V bias supply. Decouple VIN voltage with 0.1 µF ceramic capacitor placed close to this pin.
2	IGBTSRC	IGBT gate drive source output.
3	IGBTSINK	IGBT gate drive sink output.
4	TRIGGER	IGBT trigger input.
5	GND	Ground connection.
6	SW	Drain connection of internal DMOS switch. Connect to transformer primary winding.
7	VBAT	Battery voltage.
8	CHARGE	Charge enable and current limit serial programming pin. Set this pin low to shut down the chip.
9	$\overline{\text{DONE}}$	Open collector output, pulls low when output reaches target value and CHARGE is high. Goes high during charging or whenever CHARGE is low.
10	ISET	Connect an external resistor to GND to set default peak switch current limit.
–	PAD	Exposed pad for enhanced thermal dissipation. Connect to ground plane.

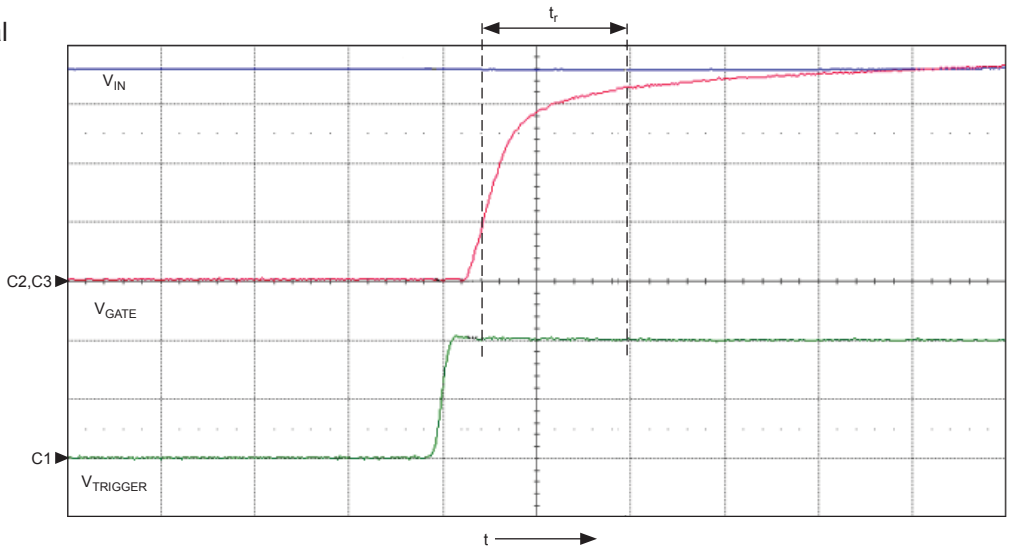
Characteristic Performance

IGBTSRC and IGBTSINK connected together and IGBT Drive waveforms are measured at pin with R-C load (12 Ω, 6800 pF).

IGBT Drive Performance

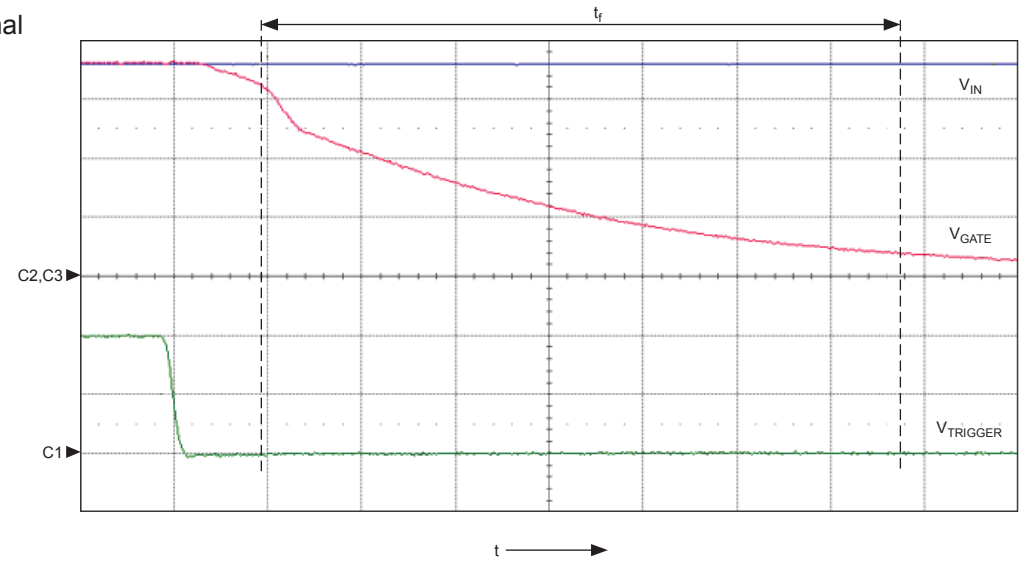
Rising Signal

Symbol	Parameter	Units/Division
C1	$V_{TRIGGER}$	1 V
C2	V_{GATE}	1 V
C3	V_{IN}	1 V
t	time	50 ns
Conditions	**Parameter**	**Value**
	t_{Dr}	16 ns
	t_r	81.5 ns
	C_{LOAD}	6.8 nF
	R_{gate}	12 Ω



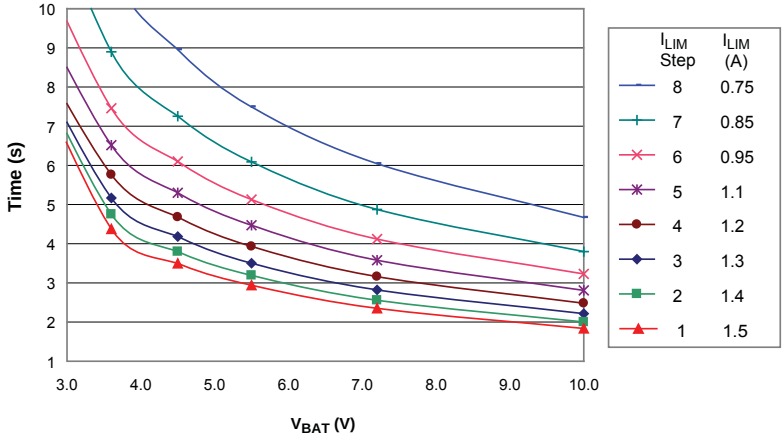
Falling Signal

Symbol	Parameter	Units/Division
C1	$V_{TRIGGER}$	1 V
C2	V_{GATE}	1 V
C3	V_{IN}	1 V
t	time	50 ns
Conditions	**Parameter**	**Value**
	t_{Dr}	46 ns
	t_r	342 ns
	C_{LOAD}	6.8 nF
	R_{gate}	12 Ω



Charge Time versus Battery Voltage

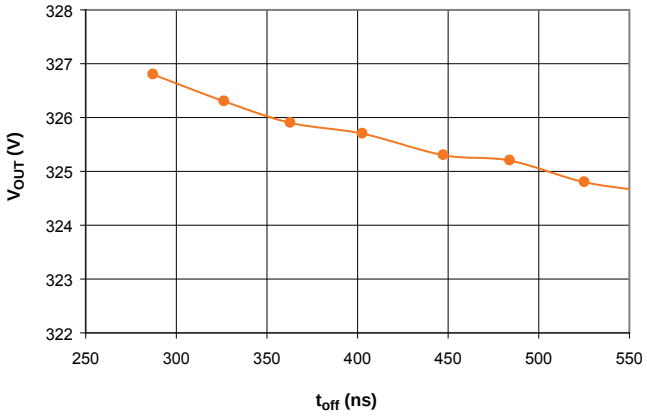
Transformer L_P = 12.8 µH, N = 10.25, V_{IN} = 3.6 V, C_{OUT} = 100 µF, R_{ISET} = 22.6 kΩ, , $T_A \approx 25°C$



Output voltage is sensed from the primary side winding when the switch turns off. This duration, t_{off}, has to be long enough (>200 ns) in order to obtain an accurate measurement (see Final Output Voltage versus Secondary Side Conduction Time chart).

Final Output Voltage versus Secondary Side Conduction Time

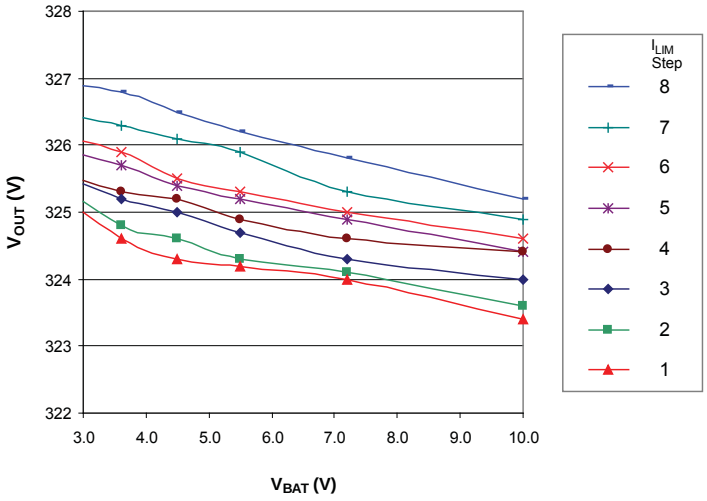
Transformer L_P = 12.8 µH, N = 10.25, V_{IN} = 3.6 V, C_{OUT} = 100 µF, R_{ISET} = 22.6 kΩ, , $T_A \approx 25°C$



The value of t_{off} depends on I_{SWlim}, primary inductance, $L_{Primary}$, and turns ratio, N, as given by: $t_{off} = (I_{SWlim} \times L_{Primary} \times N) / V_{OUT}$.

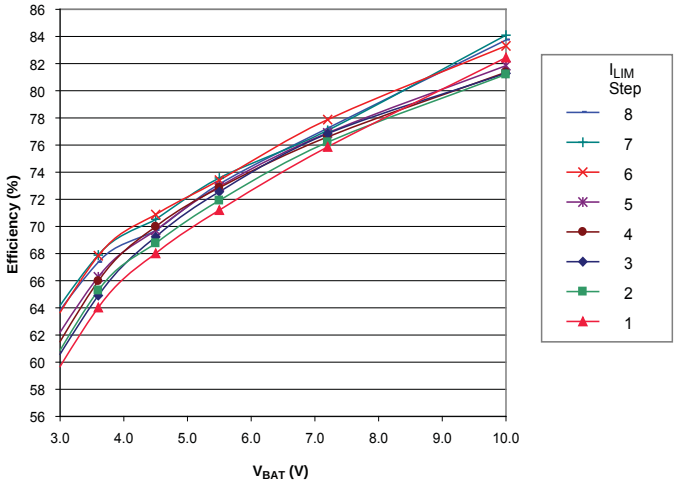
Final Output Voltage versus Battery Voltage

Transformer L_P = 12.8 µH, N = 10.25, V_{IN} = 3.6 V, C_{OUT} = 100 µF, R_{ISET} = 22.6 kΩ, , $T_A \approx 25°C$



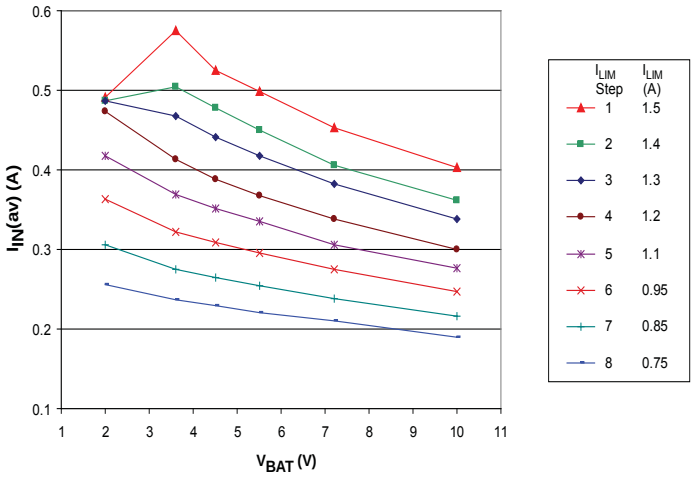
Efficiency versus Battery Voltage

Transformer L_P = 12.8 µH, N = 10.25, V_{IN} = 3.6 V, C_{OUT} = 100 µF, R_{ISET} = 22.6 kΩ, , $T_A \approx 25°C$



Average Input Current versus Battery Voltage

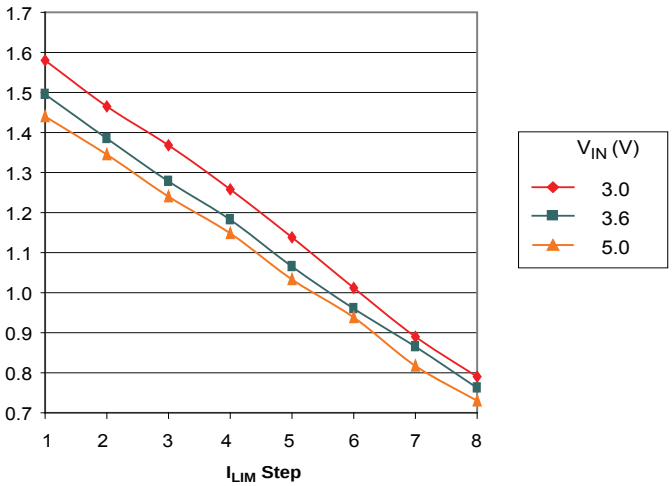
Transformer L_P = 12.8 µH, N = 10.25, V_{IN} = 3.6 V, R_{ISET} = 22.6 kΩ, , $T_A \approx 25°C$



Note: Peak switch current is limited by maximum on-time and di/dt of transformer primary current; therefore, average current drops at very low battery voltage.

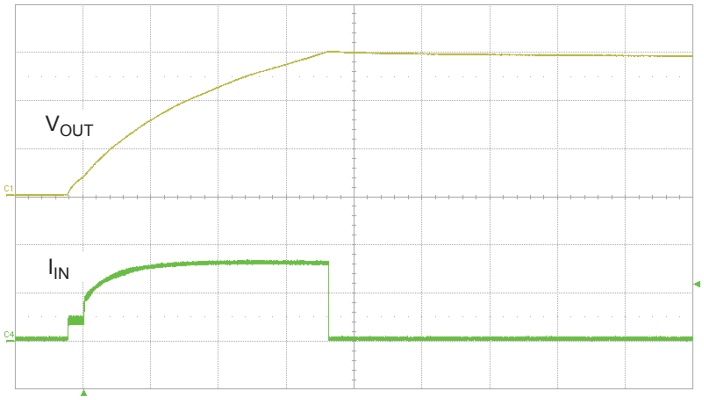
I_{LIM} versus I_{LIM} Steps at Various V_{IN}

Transformer L_P = 12.8 µH, N = 10.25, V_{IN} = 3.6 V, C_{OUT} = 100 µF, R_{ISET} = 22.6 kΩ, , $T_A \approx 25°C$

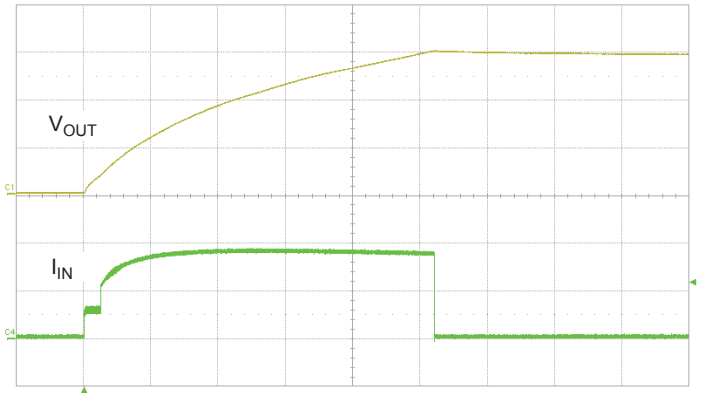


V_{OUT} Charging at Various V_{BAT}

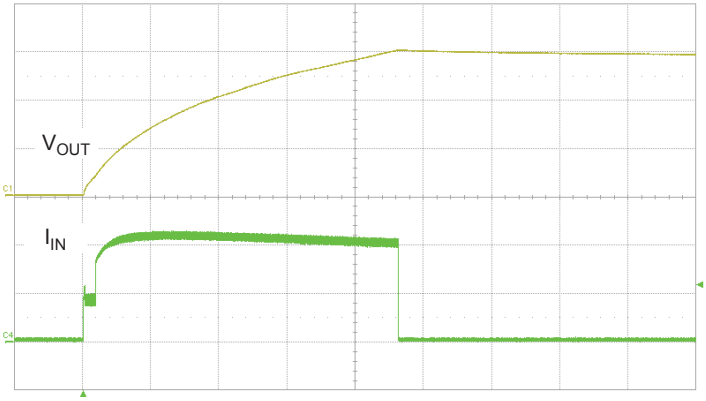
V_{IN} = 3.6 V, C_{OUT} = 100 µF, I_{SWlim} = 1.2 A



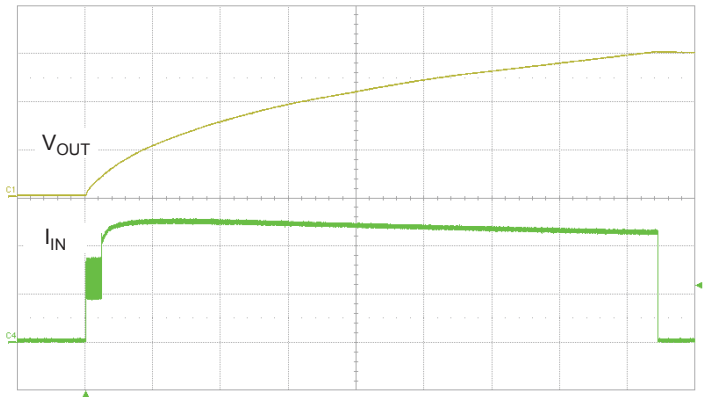
V_{BAT} = 11 V. C1, V_{OUT} 100 V/div; C4, I_{IN}(av) 200 mA/div; Time 500 ms/div.



V_{BAT} = 7.2 V. C1, V_{OUT} 100 V/div; C4, I_{IN}(av) 200 mA/div; Time 500 ms/div.



V_{BAT} = 3.6 V. C1, V_{OUT} 100 V/div, C4; I_{IN}(av) 200 mA/div; Time 1s/div.



V_{BAT} = 2 V. C1, V_{OUT} 100 V/div; C4, I_{IN}(av) 200 mA/div; Time 1s/div.

Functional Description

Overview

The A8724 integrates a flyback converter and an IGBT gate driver to provide a compact solution for Xenon flash applications. The charging operation of the A8724 is started by a low-to-high signal on the CHARGE pin, provided that V_{IN} is above V_{UVLO} level. It is strongly recommended to keep the CHARGE pin at logic low during power-up. After V_{IN} exceeds the UVLO level, a low-to-high transition on the CHARGE pin is required to start the charging.

Toggling the CHARGE pin reinitiates the charging operation.

The A8724 implements an adaptive off-time, t_{off}, control. After the switch is turned off, a sensing circuit tracks the flyback voltage at the SW node. A proprietary dV/dt detection circuit is used to allow minimum-voltage switching, even if the SW voltage does not drop to zero volts. This enables fast-charging to start earlier, thereby reducing the overall charging time.

The A8724 senses output voltage indirectly on the primary side. The flyback converter stops switching when output voltage reaches:

$$V_{OUT} = K \times N - V_d \quad ,$$

where:
K = 31.5 typically,
V_d is the forward drop of the output diode (around 2 V), and
N is transformer turns ratio.

Switch On-Time and Off-Time Control

The A8724 implements an adaptive on-time/off-time control. On-time duration, t_{on}, is equal to $t_{on} = I_{SWlim} \times L_P / V_{BAT}$. Off-time duration, t_{off}, depends on the operating conditions during switch off-time. The A8724 applies its two charging modes, Fast Charging mode and Timer mode, according to those conditions.

Timer Mode and Fast Charging Mode

The A8724 achieves fast charging times and high efficiency by operating in discontinuous conduction mode (DCM) through most of the charging process The relationship of Timer mode and Fast Charging mode is shown in figure 3.

The IC operates in Timer mode when beginning to charge a completely discharged photoflash capacitor, usually when the output voltage, V_{OUT}, is less than approximately 15 to 20 V. Timer mode is a fixed period, 13 µs, off-time control. One advantage of having Timer mode is that it limits the initial battery current surge and thus acts as a "soft-start." A time-expanded view of a Timer mode interval is shown in figure 4.

During Fast-Charging mode, when V_{OUT} is high enough (over 50 V), true zero-voltage switching (ZVS) is achieved. This further improves efficiency as well as reduces switching noise. A ZVS interval is shown in figure 5.

Switch Current Limit Setting The peak switch current limit is set through a resistor RSET connected between the ISET pin and

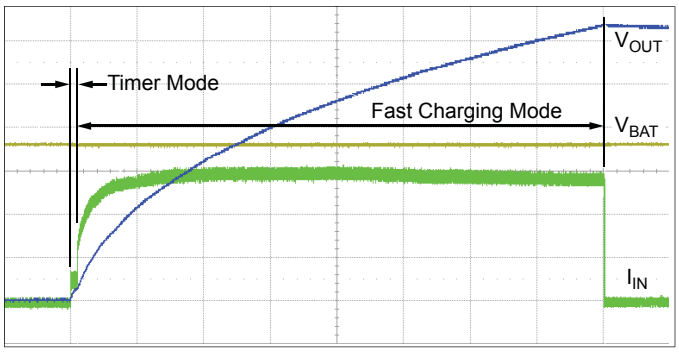


Figure 3. Timer mode and Fast Charging mode: t = 200 ms/div; V_{OUT} = 50 V/div; V_{BAT} = 1 V/div.; I_{IN} = 100 mA/div., V_{BAT} = 3.6 V; C_{OUT} = 20 µF / 330 V; and I_{SWlim} ≈ 0.75 A.

GND. The value of R_{SET} can be between 22.6 and 48 kΩ, setting the peak switch current from 1.5 to 0.7 A. Select the value for the RSET resistor as:

$$R_{SET} = 1.2 \times 27800 / I_{LIM} \ ,$$

where:

I_{LIM} is the target current limit, in A,
R_{SET} is in Ω.

The resistor sets the 100% current level, I_{LIM}, which can be programmed by applying pulses on the CHARGE pin.

The peak current limit can be programmed to eight different levels, from 100% to 50%, with a 7% decrement per programming step on charge pin. An internal digital circuit decodes the input clock signals, which sets the switch current limit. This flexible scheme allows the user to operate the A8724 according to different battery input voltages. The battery life can be effectively extended by setting a lower current limit at low battery voltages.

Figure 6 shows the ILIM clock timing scheme protocol. The total ILIM setup time, $t_{ILIM(SU)}$, denotes the time needed for the decoder circuit to receive ILIM inputs and set I_{SWLIM} , and has a typical duration of 45 µs (minimum 40 µs).

Figure 7 shows the timing definition of the primary current limiting circuit. At the end of the setup period, $t_{ILIM(SU)}$, primary current starts to ramp up to the set I_{SWLIM}. The I_{SWLIM} setting remains in effect as long as the CHARGE pin is high. To reset the ILIM decoder, pull the CHARGE pin low before clocking in the new setting.

After the first start-up or an ILIM decoder reset, each new current limit can be set by sending a burst of pulses to the CHARGE pin. The first rising edge starts the ILIM decoder, and up to 8 rising edges will be counted to set the I_{SWLIM} level. The first pulse width, $t_{ILIM1(H)}$, must be at least 15 µs long. Subsequent pulses (up to 7 more) can be as short as 0.2 µs. The last low-to-high edge must arrive within 40 µs from the first edge. The CHARGE pin will stay high afterwards.

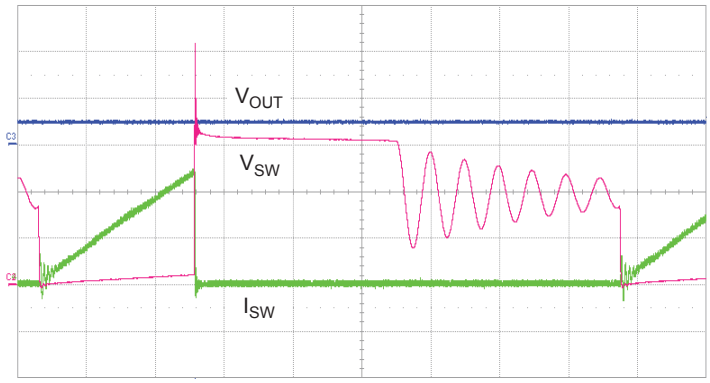


Figure 4. Expanded view of Timer Mode, V_{BAT} = 3.6 V, I_{SWlim} = 1.2 A. C2, V_{SW} = 2 V/div; C3, V_{OUT} = 50 V/div; C4, I_{SW} = 500 mA/div; Time = 2 µs/div.

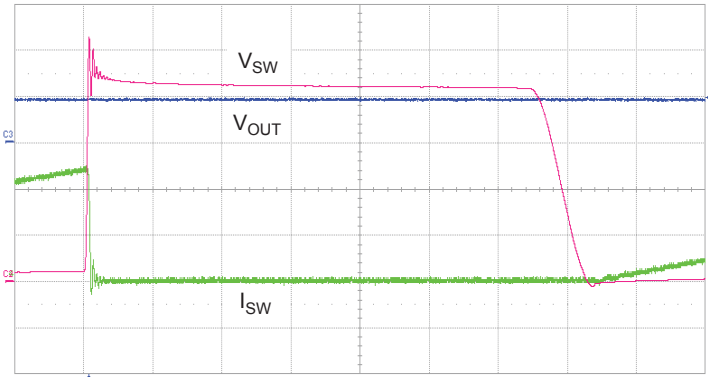


Figure 5. Zero-Voltage Switching (ZVS) V_{BAT} = 3.6 V, I_{SWlim} = 1.2 A. C2, V_{SW} = 2 V/ div; C3, V_{OUT} = 50 V; C4, I_{SW} = 500 mA/div; Time = 0.5 µs/div.

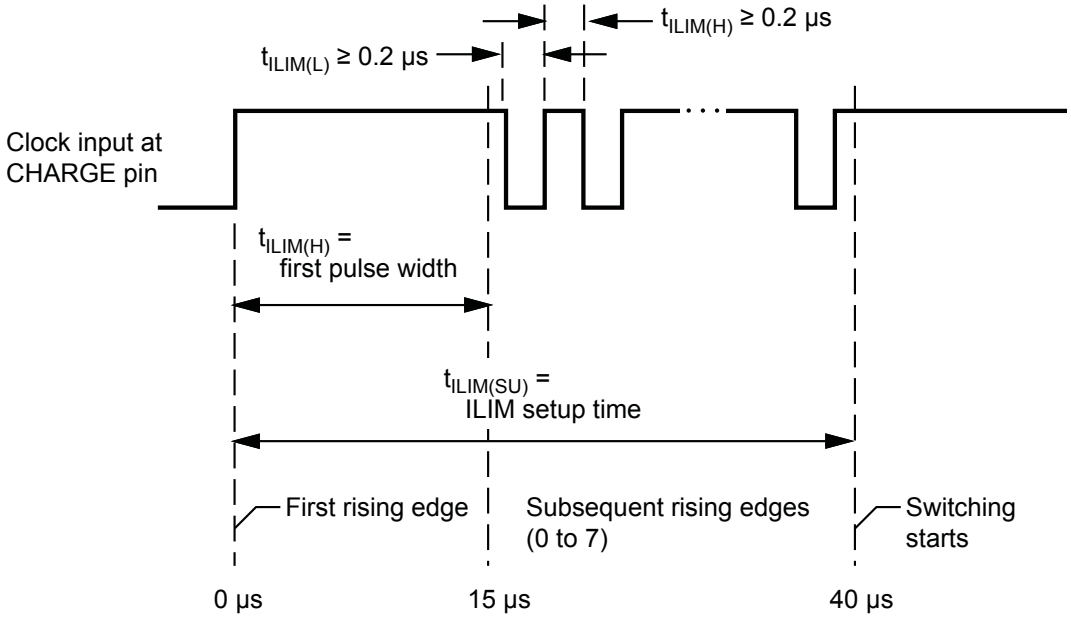


Figure 6. ILIM Program Timing Definition

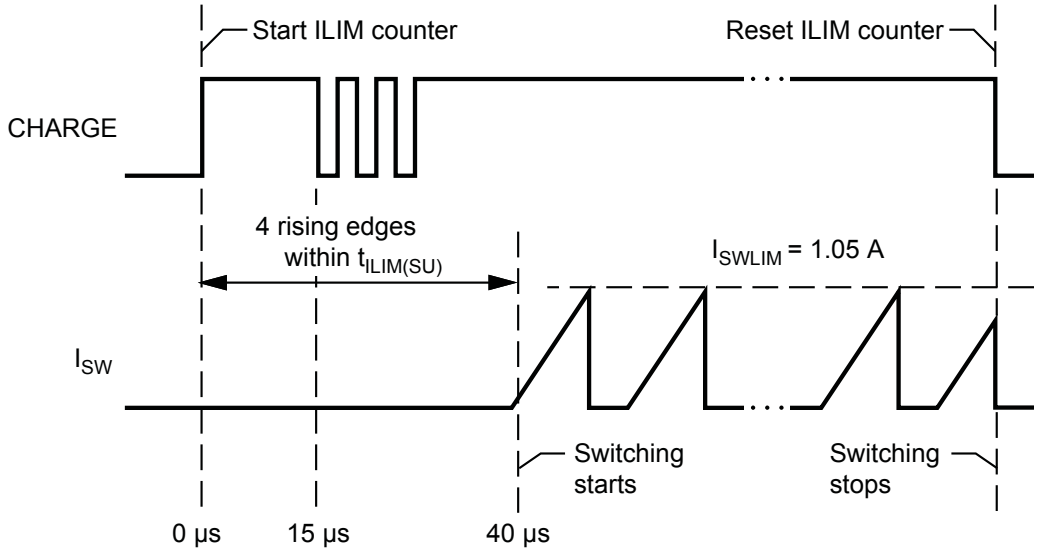


Figure 7. Current Limit Programming Example (I_{swlim4} selected)

Smart Current Limit (Optional)

Current limit reduction with V_{BAT} The switch peak current limit can be varied according to the battery voltage, as shown in figure 8.

For example, ISET current is normally set to 54 µA (ILIM = 1.5 A). When the battery voltage drops below 2.5 V, a BL (battery-low) signal from external controller goes high. A resistor connecting from BL to ISET pin then injects 15 µA into RSET. This effectively reduces ISET current to 39 µA (for ILIM = 1.08 A).

IGBT Driver Application

The integrated IGBT driver is used to drive external flash trigger IGBT. Separate IGBTSRC and IGBTSNK pins allow the user to adjust IGBT turn-on and turn-off rise times. IGBT drive timing is defined when these pins are connected together supplying a load comprising 12 Ω resistor and a 6500 pF capacitor. These pins can be connected together to use a single resistor drive.

Open Secondary Protection

The A8724 is protected against open secondary winding or secondary diode. When a secondary diode or winding is open, the energy stored in the transformer during on-time generates voltage at the SW pin greater than $V_{OUTTRIP}$ +V_{BAT}. Internal DMOS clamp the voltage and dissipate energy for one cycle. Internal switch stops switching and the $\overline{DONE}$ pin is pulled low as shown in figure 9.

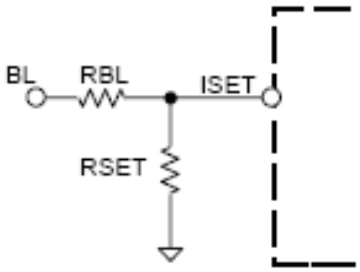


Figure 8. Optional Smart Current Limit configuration

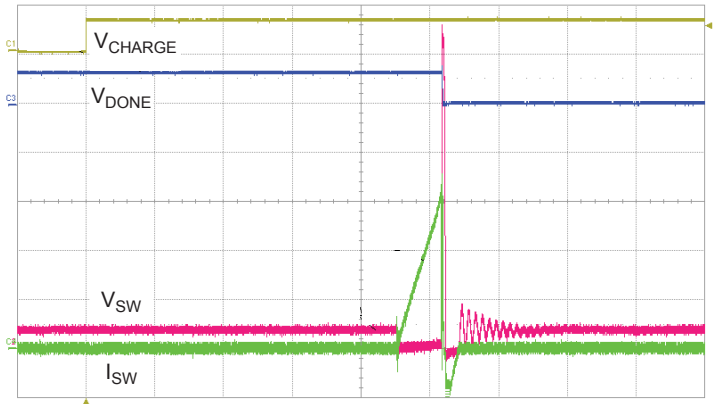


Figure 9. Operation under open diode fault (I_{SWlim} = 1.5 A, V_{BAT} = 3.6 V, $L_{primary}$ = 12.8 µH). C1, V_{CHARGE}, 5 V/div; C2, V_{SW} 10 V/div; C3, $\overline{DONE}$ 5 V/div; C4, I_{SW} 500 mA/div; Time, 10 µs/div.

Application Information

Transformer Design

1. The transformer turns ratio, N, determines the output voltage:

$$N = N_S / N_P$$

$$V_{OUT} = 31.5 \times N - V_d \ ,$$

where 31.5 is the typical value of $V_{OUTTRIP}$, and V_d is the forward drop of the output diode.

2. The primary inductance, $L_{Primary}$, determines the on-time of the switch:

$$t_{on} = (-L_{Primary}/R) \times \ln(1 - I_{SWlim} \times R/V_{IN}) \ ,$$

where R is the total resistance in the primary current path (including $R_{SWDS(on)}$ and the DC resistance of the transformer).

If V_{IN} is much larger than $I_{SWlim} \times R$, then t_{on} can be approximated by:

$$t_{on} = I_{SWlim} \times L_P / V_{IN} \ .$$

3. The secondary inductance, L_S, determines the off-time of the switch. Given:

$$L_S / L_{Primary} = N \times N \text{ , then}$$

$$t_{off} = (I_{SWlim} / N) \times L_S / V_{OUT}$$

$$= (I_{SWlim} \times L_{Primary} \times N) / V_{OUT} \ .$$

The minimum pulse width for t_{off} determines what is the minimum $L_{Primary}$ required for the transformer. For example, if I_{SWlim} = 0.7 A, N = 10, and V_{OUT} = 315 V, then $L_{Primary}$ must be at least 9 µH in order to keep t_{off} at 200 ns or longer. These relationships are illustrated in figure 10.

In general, choosing a transformer with a larger $L_{Primary}$ results in higher efficiency (because a larger $L_{Primary}$ means lower switch frequency and hence lower switching loss). But transformers with a larger $L_{Primary}$ also require more windings and larger magnetic cores. Therefore, a trade-off must be made between transformer size and efficiency.

Leakage Inductance and Secondary Capacitance

The transformer design should minimize the leakage inductance to ensure the turn-off voltage spike at the SW node does not exceed the 55 V limit. An achievable minimum leakage inductance for this application, however, is usually compromised by an increase in parasitic capacitance. Furthermore, the transformer secondary capacitance should be minimized. Any secondary

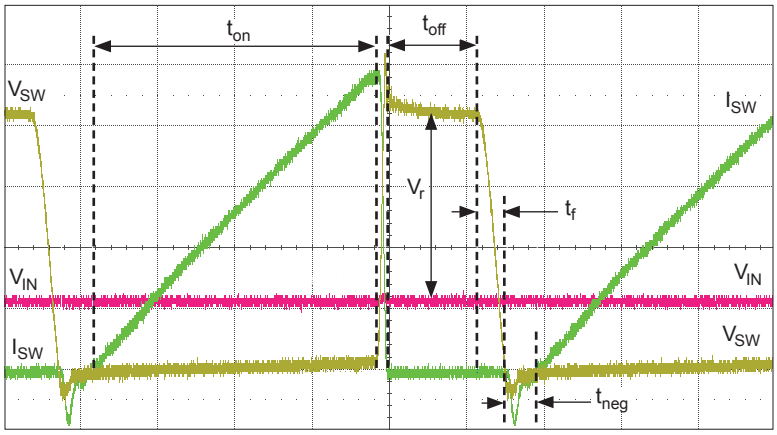


Figure 10. Transformer Selection Relationships

capacitance is multiplied by N^2 when reflected to the primary, leading to high initial current swings when the switch turns on, and to reduced efficiency.

Input Capacitor Selection

Ceramic capacitors with X5R or X7R dielectrics are recommended for the input capacitor, C1. During initial timer mode the device operates with 13 µs off-time. A typical input section for a photoflash module with input filter inductor, or a test setup with long connecting wires is shown in figure 11. The resonant period caused by input filter inductor and capacitor should be at least 2 times greater or smaller than the 13 µs timer period, to reduce input ripple current during this period. Effect of input capacitor is shown in figures 12 and 13.

The resonant period is given by:

$$T_{res} = 2 \times \pi \times (L_{IN} \times C_1)^{1/2}$$

It is recommended to use at least 4.7 µF / 6.3 V to decouple the battery input, V_{BAT}, at the primary of the transformer. Decouple the V_{IN} pin using a 0.1 µF / 6.3 V bypass capacitor.

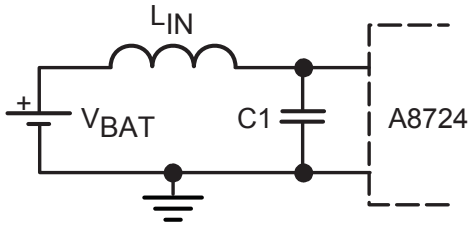


Figure 11. Typical input section with input inductance (inductance, L_{IN}, may be an input filter inductor or inductance due to long wires in test setup)

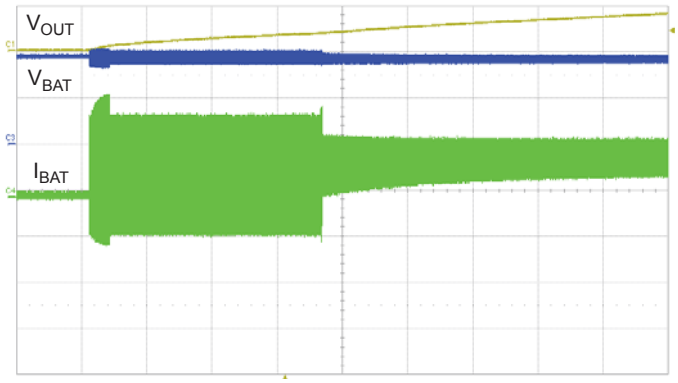


Figure 12. Input current waveforms with Li+ battery connected by 5-in. wire and decoupled by 4.7 µF capacitor. C1, V_{OUT} 100 V/div; C3, V_{BAT} 2 V/div; C4, I_{BAT} 500 mA/div; Time, 50 ms/div.

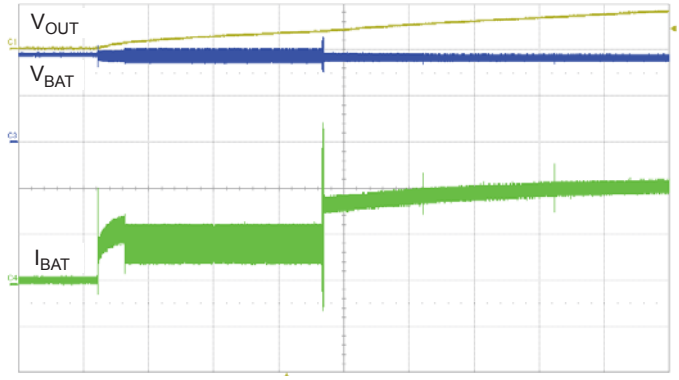


Figure 13. Input current waveforms with Li+ battery connected through 10 µH inductor and 4.7 µF capacitor. C1, V_{OUT} 100 V/div; C3, V_{BAT} 2 V/div; C4, I_{BAT} 200 mA/div; Time, 50 ms/div.

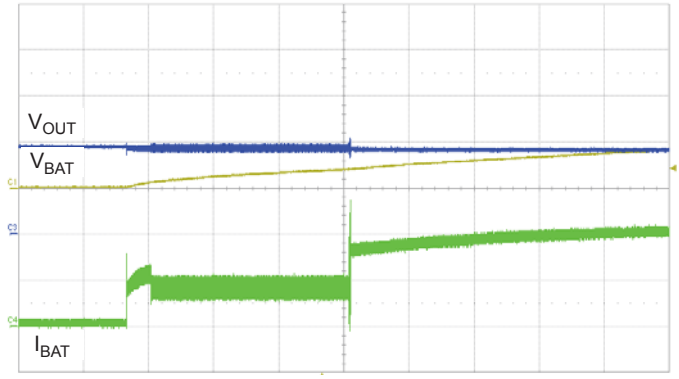


Figure 14. Input current waveforms with Li+ battery connected through 10 µH inductor and 10 µF capacitor. C1, V_{OUT} 100 V/div; C3, V_{BAT} 2 V/div; C4, I_{BAT} 200 mA/div; Time, 50 ms/div.

Output Diode Selection

Choose the rectifying diode(s), D1, to have small parasitic capacitance (short reverse recovery time) while satisfying the reverse voltage and forward current requirements. The peak reverse voltage of the diode, V_{D_Peak} , occurs when the internal MOSFET switch is closed. It can be calculated as:

$$V_{D\_Peak} = V_{OUT} + N \times V_{BAT}$$

The peak current of the rectifying diode, I_{D_Peak}, is calculated as:

$$I_{D\_Peak} = I_{Primary\_Peak} / N$$

Layout Guidelines

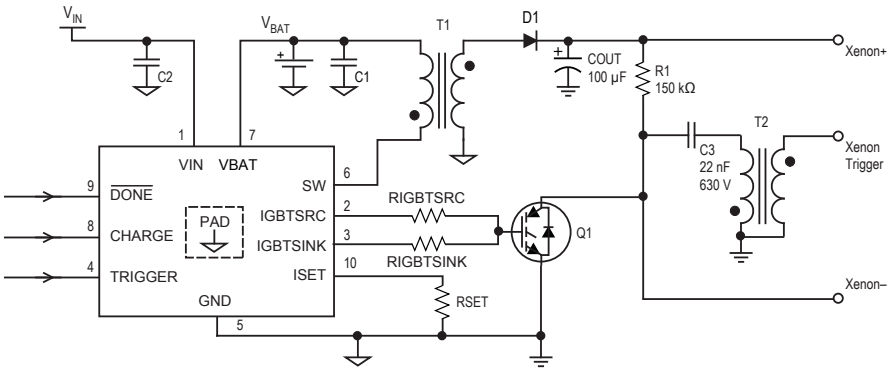
Key to a good layout for the photoflash capacitor charger circuit is to keep the parasitics minimized on the power switch loop (transformer primary side) and the rectifier loop (secondary side). Use short, thick traces for connections to the transformer primary and SW pin. It is important that the $\overline{\text{DONE}}$ signal trace and other signal traces be routed away from the transformer and other switching traces, in order to minimize noise pickup. In addition, high voltage isolation rules must be followed carefully to avoid breakdown failure of the circuit board.

Avoid locating the ground plane underneath transformer secondary and diode to minimize parasitic capacitance.

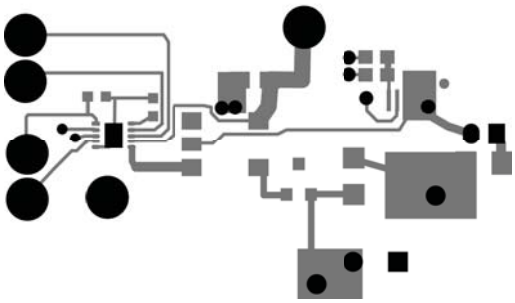
For low threshold logic (<1.3 V) add 1 nF capacitors across the CHARGE and TRIGGER pins to GND to avoid malfunction due to noise. Refer to the figures on the next page for recommended layout.

Recommended Layout

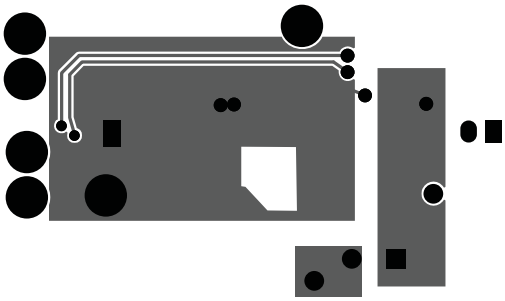
Schematic



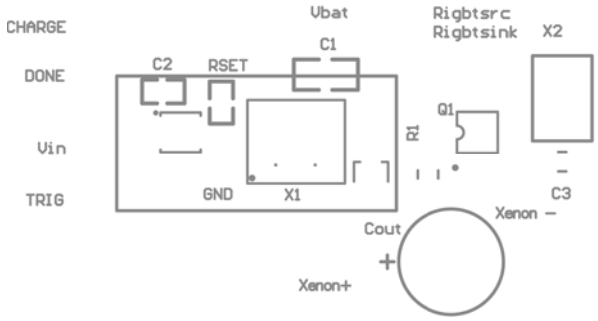
Top side



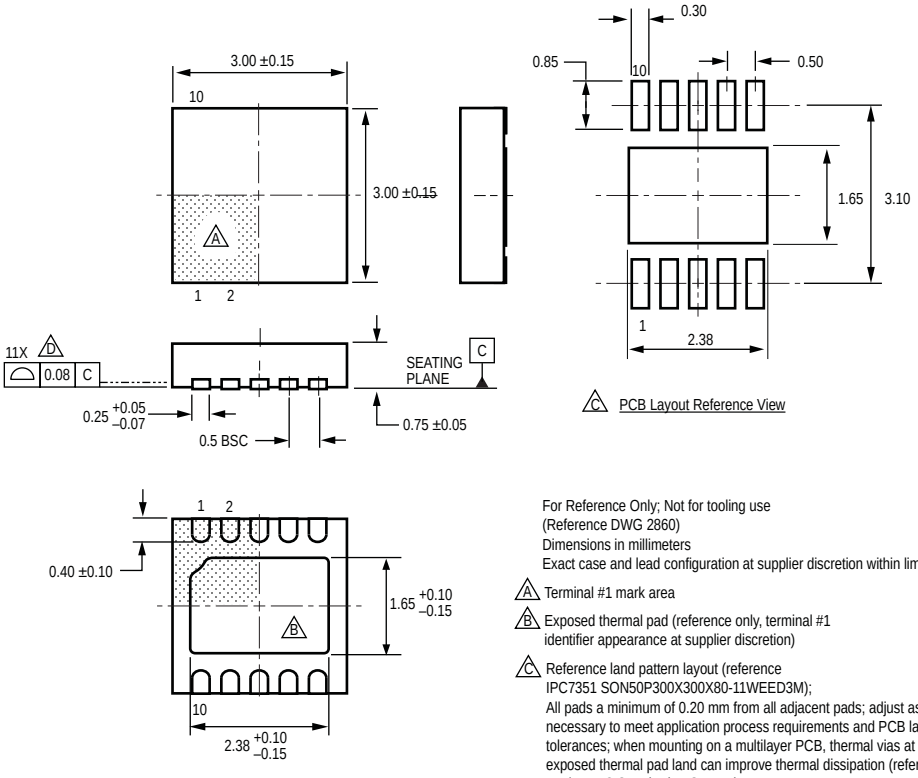
Bottom side



Top components



Package EJ 10-Contact TDFN with Exposed Thermal Pad



For Reference Only; Not for tooling use
(Reference DWG 2860)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 SON50P300X300X80-11WEED3M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Revision History

Revision	Revision Date	Description of Revision
Rev. 2	April 19, 2012	Miscellaneous format changes

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