A8731

Mobile Phone Xenon Photoflash Capacitor Charger With IGBT Driver

Discontinued Product

This device is no longer in production. The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: March 4, 2013

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, contact Allegro Sales.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

Mobile Phone Xenon Photoflash Capacitor Charger With IGBT Driver

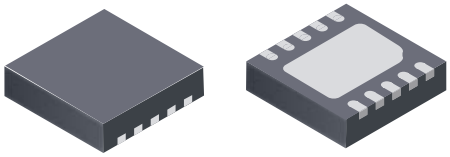
Features and Benefits

- **Low quiescent current draw (0.01 µA in shutdown mode)**
- **Primary-side output voltage sensing; no resistor divider required**
- **User-adjustable current limit from 0.4 to 1.2 A**
- **1.1 V logic (V_{HI}(min)) compatibility**
- **Integrated IGBT driver with internal gate resistors**
- **Flexible dual trigger inputs for IGBT driver**
- Optimized for mobile phone, 1-cell Li+ battery applications
- No primary-side Schottky diode needed
- Zero-voltage switching for lower loss
- >75% efficiency
- Charge complete indication
- Integrated 40 V DMOS switch

Applications

- Mobile phone flash
- Digital and film camera flash

Package: 10-contact DFN with exposed thermal pad (package EJ)



Approximate Scale 1:1

Description

The Allegro® A8731 Xenon photoflash charger IC is designed to meet the needs of ultra-low power, small form factor cameras, particularly camera-phones.

The charge time is adjustable by setting the charge current limit from 0.4 to 1.2 A maximum. By using primary-side voltage sensing, the need for a secondary-side resistive voltage divider is eliminated. This has the additional benefit of reducing leakage currents on the secondary side of the transformer. To extend battery life, the A8731 features very low supply current draw—typically 0.01 µA in shutdown mode and 10 µA in standby mode.

The A8731 has a flash dual trigger IGBT driver. The IGBT driver also has internal gate resistors for minimum external component count. The charge and trigger voltage logic thresholds are set at 1.1 V_{HI} (min) to support applications implementing low voltage control logic.

The A8731 is available in a 10-contact 3 mm × 3 mm DFN package with a 0.75 nominal overall package height, and an exposed pad for enhanced thermal performance.

Typical Applications

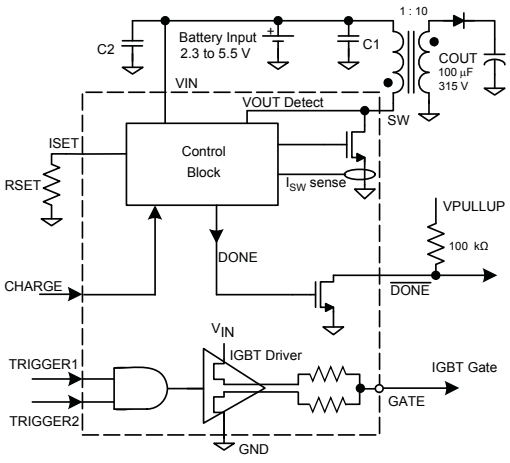


Figure 1. Typical application with separate trigger inputs.

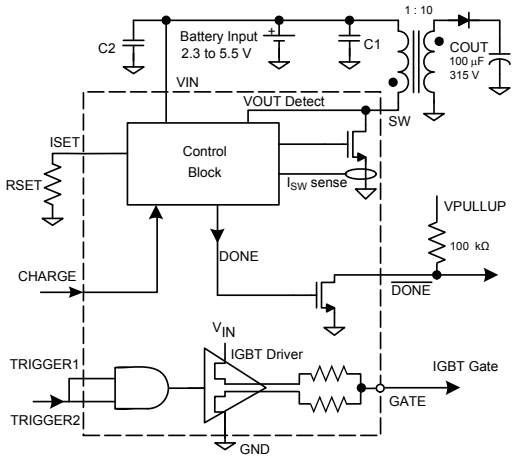


Figure 2. Typical application with single trigger input.

Selection Guide

Part Number	Package	Packing
A8731EEJTR-T	10-contact DFN	Tape and reel, 1500 pieces per reel

*Contact Allegro for additional ordering information.

Absolute Maximum Ratings

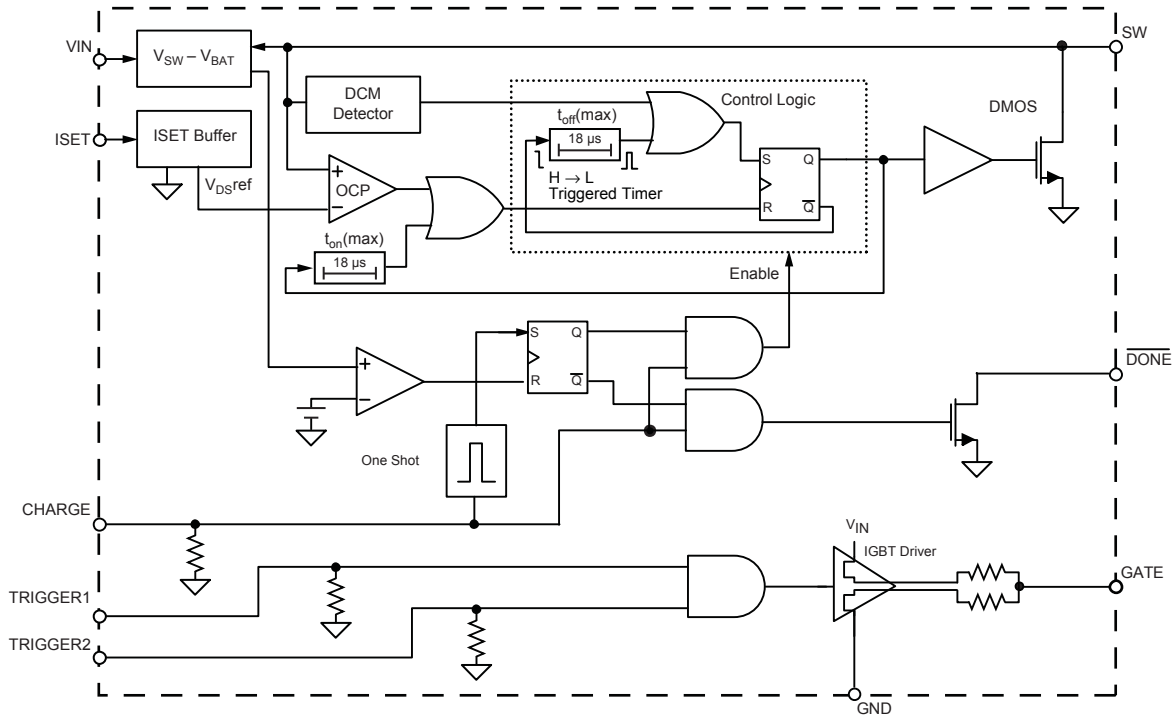
Characteristic	Symbol	Notes	Rating	Units
SW Pin	V_{SW}	DC voltage. (V_{SW} is self-clamped by internal active clamp and is allowed to exceed 40 V during flyback spike durations. Maximum repetitive energy during flyback spike: 0.5 µJ at frequency ≤ 400 kHz.)	–0.3 to 40	V
VIN Pin	V_{IN}		–0.3 to 6.0	V
CHARGE, TRIGGER*x*, $\overline{\text{DONE}}$ Pins		Care should be taken to limit the current when –0.6 V is applied to these pins.	–0.6 to V_{IN} + 0.3 V	V
Remaining Pins			–0.3 to V_{IN} + 0.3 V	V
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
Maximum Junction	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

Thermal Characteristics

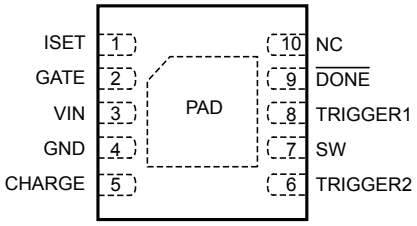
Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	On 2-layer PCB with 0.88 in.^{2} area of 2 oz. copper each side, based on JEDEC standard	65	ºC/W
		On 4-layer PCB based on JEDEC standard	45	ºC/W

*Additional thermal information available on Allegro website.

Functional Block Diagram



Pin-out Diagram



(Contacts Down View)

Terminal List Table

Number	Name	Function
1	ISET	Sets the maximum switch current; connect an external resistor to GND to set the desired peak current
2	GATE	IGBT gate drive – sink/source
3	VIN	Input voltage; connect to a 2.3 to 5.5 V battery supply
4	GND	Ground connection
5	CHARGE	Pull high to initiate charging; pull low to enter low-power standby mode
6	TRIGGER2	IGBT input trigger 2
7	SW	Drain connection of internal power MOSFET switch; connect to transformer primary winding
8	TRIGGER1	IGBT input trigger 1
9	$\overline{\text{DONE}}$	Pulls low when output reaches target value and CHARGE pin is high; goes high during charging or whenever CHARGE pin is low
10	NC	No connection , electrically floating pin
–	PAD	Exposed pad for enhanced thermal dissipation; connect to ground plane

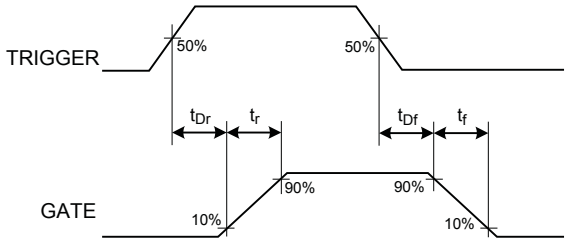
ELECTRICAL CHARACTERISTICS typical values valid at V_{IN} = 3.6 V, R_{SET} = 33 kΩ, I_{SWlim} = 1.0 A, and T_A=25°C, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VIN Voltage Range	V_{IN}		2.3	–	5.5	V
UVLO Enable Threshold	V_{INUV}	V_{IN} rising	–	2.05	2.2	V
UVLO Hysteresis	$V_{INUVhys}$		–	150	–	mV
VIN Supply Current	I_{IN}	Shutdown (CHARGE = 0 V, TRIGGER1 and TRIGGER2 = 0 V)	–	0.01	0.5	µA
		Charging complete	–	10	50	µA
		Charging (CHARGE = VIN, TRIGGER1 and TRIGGER2 = 0 V)	–	2	–	mA
Current Limits						
Switch Current Limit[1]	$I_{SWlimMAX}$	R_{SET} = 26.7 kΩ	1.08	1.2	1.32	A
	$I_{SWlimMIN}$	R_{SET} = 85 kΩ	–	0.4	–	A
SW / ISET Current Ratio	I_{SW}/I_{SET}	CHARGE = high	–	28	–	kA/A
ISET Pin Voltage While Charging	V_{SET}	CHARGE = high	–	1.2	–	V
ISET Pin Internal Resistance	$R_{SET(INT)}$		–	1000	–	Ω
Switch On-Resistance	$R_{SWDS(on)}$	V_{IN} = 3.6 V, I_D = 800 mA, T_A = 25°C	–	0.25	–	Ω
Switch Leakage Current[2]	I_{SWlk}	V_{SW} = V_{IN}(max), over temperature range	–	–	2	µA
		Combined V_{IN} and SW leakage current at T_A=25°C V_{IN}= 5.5 V in Shutdown	–	–	0.5	µA
CHARGE Input Current	I_{CHARGE}	V_{CHARGE} = V_{IN}	–	36	–	µA
CHARGE Input Voltage[2]	V_{CHARGE}	High, over input supply range	1.1	–	–	V
		Low, over input supply range	–	–	0.4	V
CHARGE Pull-Down Resistor Value	R_{CHPD}		–	100	–	kΩ
CHARGE ON/OFF Delay	t_{CH}	Time between CHARGE = 1 and charging enabled	–	20	–	us
Maximum Switch-Off Timeout	t_{offMAX}		–	18	–	µs
Maximum Switch-On Timeout	t_{onMAX}		–	18	–	µs
$\overline{DONE}$ Output Leakage Current[2]	I_{DONElk}		–	–	1	µA
$\overline{DONE}$ Output Low Voltage[2]	V_{DONEL}	32 µA into $\overline{DONE}$ pin	–	–	100	mV
Output Comparator Trip Voltage[2]	$V_{OUTTRIP}$	Measured as V_{SW} – V_{IN}	31	31.5	32	V
Output Comparator Overdrive	V_{OUTOV}	Pulse width = 200 ns (90% to 90%)	–	200	400	mV
dV/dt Threshold of ZVS Comparator	dV/dt	Measured at SW pin	–	20	–	V/µs
IGBT Driver						
TRIGGER, TRIGGER2 Input Voltage[2]	$V_{TRIG(H)}$	Input = logic high, over input supply range	1.1	–	–	V
	$V_{TRIG(L)}$	Input = logic low, over input supply range	–	–	0.4	V
TRIGGER, TRIGGER2 Pull-Down Resistor	R_{TRIGPD}		–	100	–	kΩ
GATE Resistance to VIN	$R_{SrcDS(on)}$	V_{IN} = 3.6 V, V_{GATE} =1.8 V	–	23	–	Ω
GATE Resistance to GND	$R_{SnkDS(on)}$	V_{IN} = 3.6 V, V_{GATE} = 1.8 V	–	30	–	Ω
Propagation Delay (Rising)	t_{Dr}	Measurement taken at pin, C_L= 6500 pF, V_{IN}= 3.6 V	–	110	–	ns
Propagation Delay (Falling)	t_{Df}		–	140	–	ns
Output Rise Time	t_r		–	290	–	ns
Output Fall Time	t_f		–	360	–	ns

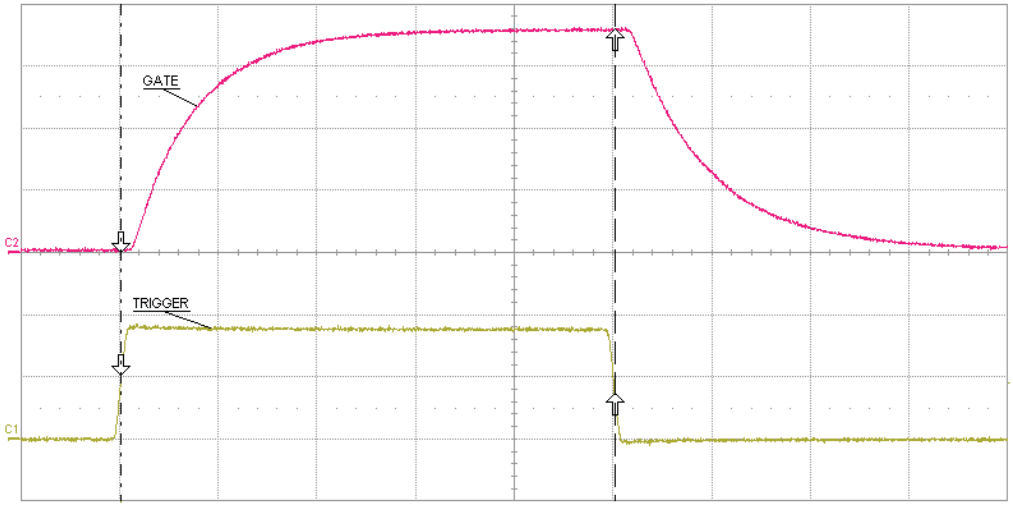
[1]Current limit guaranteed by design and correlation to static test. Refer to application section for peak current in actual circuits.

[2]Specifications over the range T_A= –40°C to 85°C; guaranteed by design and characterization.

IGBT Drive Timing Definition

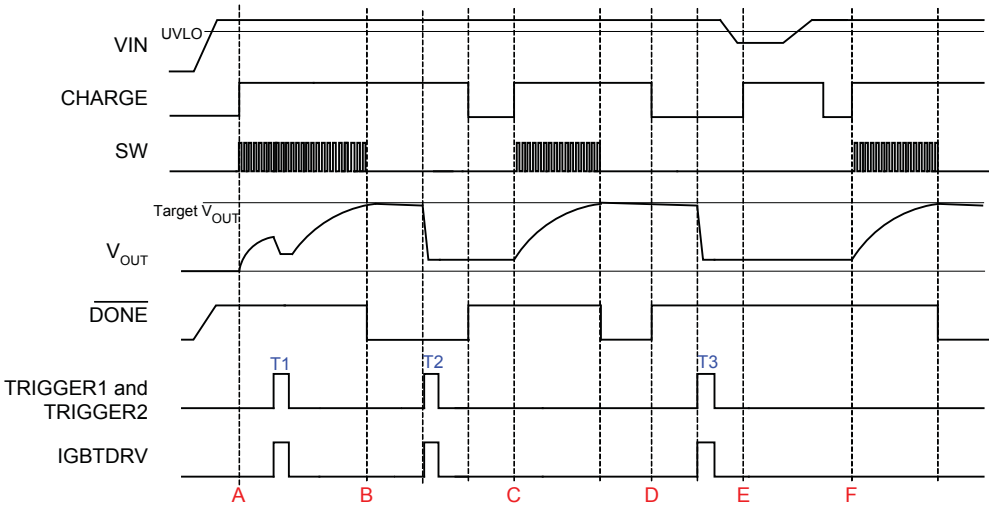


IGBT Drive Timing Characteristic Performance



C_{GATE} = 6200 pF. V_{IN} = 3.6 V, Time = 200 ns/div; CH1 = TRIGGER input, 2 V/div, CH2 = Gate driver output, 1 V/div

A8731 Operation Timing Diagram



Explanation of Events

A: Start charging by pulling CHARGE to high, provided that V_{IN} is above UVLO level.

B: Charging stops when V_{OUT} reaches the target voltage.

C: Start a new charging process with a low-to-high transition at the CHARGE pin.

D: Pull CHARGE to low to put the controller in low-power standby mode.

E: Charging does not start, because V_{IN} is below UVLO level when CHARGE goes high.

F: After V_{IN} goes above UVLO, another low-to-high transition at the CHARGE pin is required to start the charging.

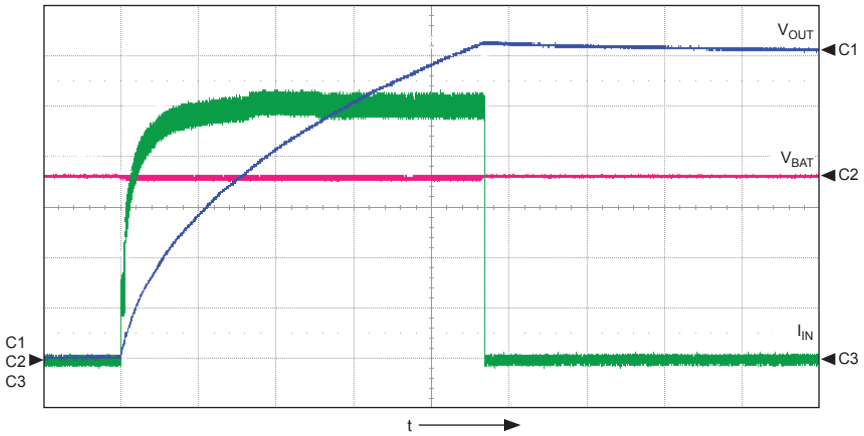
T1, T2, T3 (Trigger instances): IGBT driver output pulled high whenever both TRIGGER pins are logic high. It is recommended to avoid applying any trigger pulses during charging.

Performance Characteristics

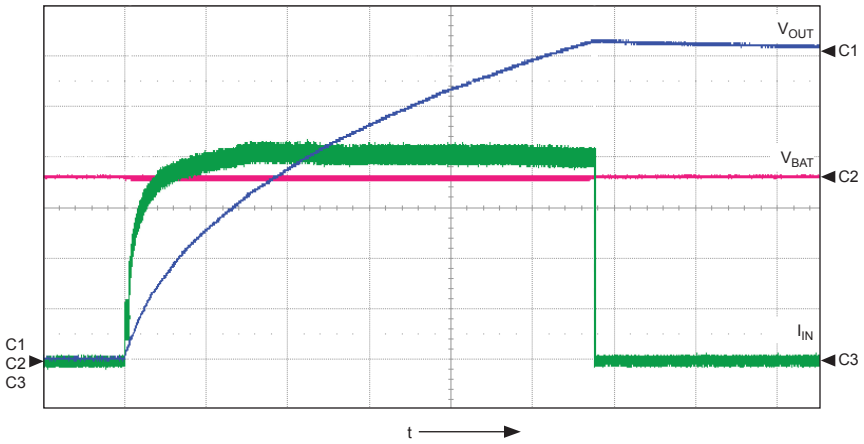
Charging Time at Various Peak Current Levels

Common Parameters		
Symbol	Parameter	Units/Division
C1	V_{OUT}	50 V
C2	V_{BAT}	1 V
C3	I_{IN}	100 mA
t	time	200 ms
Conditions	**Parameter**	**Value**
	V_{BATT}	3.6 V
	C_{OUT}	20 µF

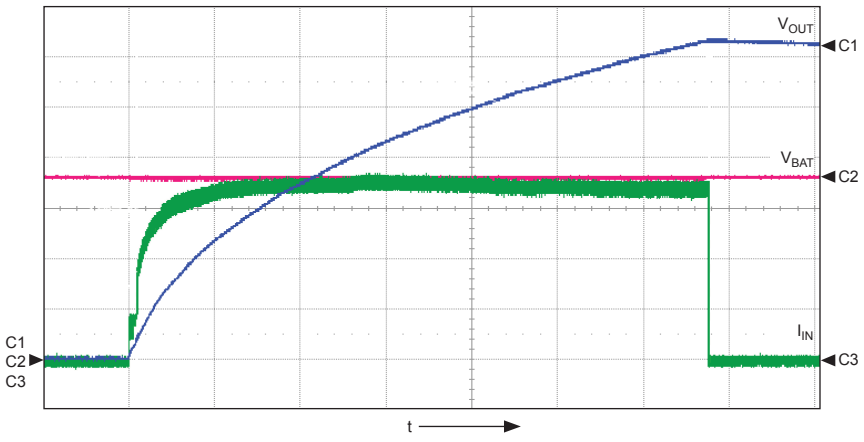
Conditions	Parameter	Value
	R_{SET}	26.7 kΩ
	I_{SWlim}	≈1.2 A

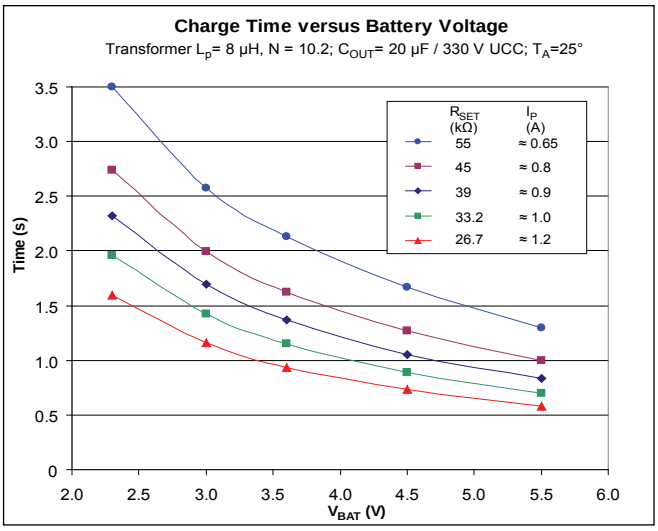


Conditions	Parameter	Value
	R_{SET}	33.2 kΩ
	I_{SWlim}	≈1.0 A

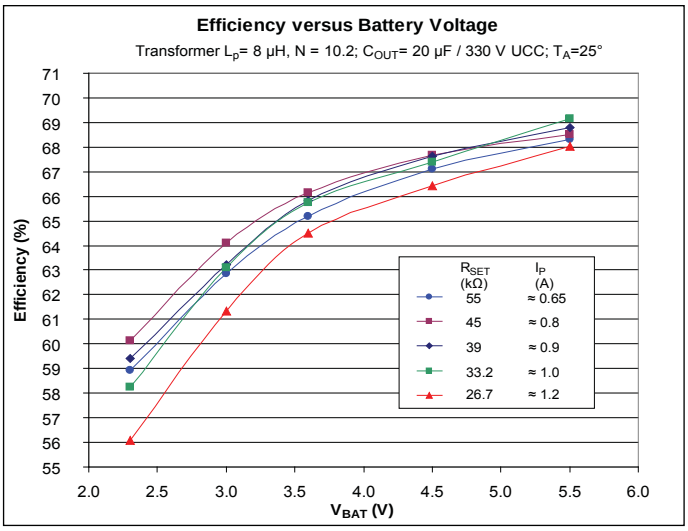


Conditions	Parameter	Value
	R_{SET}	39 kΩ
	I_{SWlim}	≈0.9 A

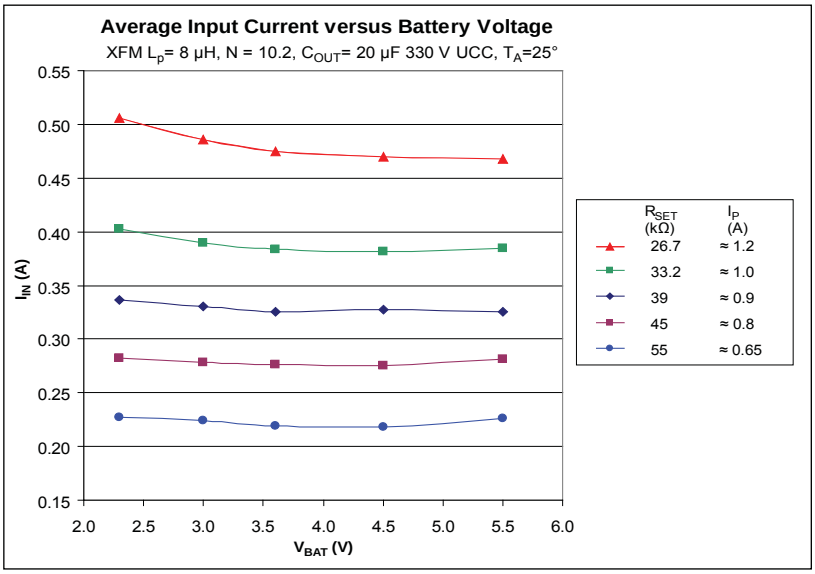




C_{OUT}= 20 µF. For larger or smaller capacitances, charging time scales proportionally.



Special low-profile transformer with relatively low inductance (Lp= 8 µH) and high winding resistance (Rp = 0.37 Ω). Higher efficiency can be achieved by using transformers with higher Lp, which reduces switching frequency and therefore switching loses, and lower resistance, which reduces conduction losses.



An increase in I_{SWlim} with respect to V_{BAT} actually keeps the average input current roughly constant throughout the battery voltage range. Normally, if I_{SWlim} is kept constant, the average current will drop as V_{BAT} goes higher.

Application Information

General Operation Overview

The CHARGE pin enables the part and starts charging. The $\overline{\text{DONE}}$ open-drain indicator is pulled low when CHARGE is high and target output voltage is reached. Pulling the CHARGE pin low stops charging and forces the chip into low-power standby mode.

Selection of Switching Current Limit

The A8731 features continuously adjustable peak switching current between 0.4 and 1.2A. This is done by selecting the value of an external resistor RSET, connected from the ISET pin to GND, which determines the ISET bias current, and therefore the switching current limit, I_{SWlim}.

To the first order approximation, I_{SWlim} is related to I_{SET} and R_{SET} according to the following equations:

$$I_{SWlim} = I_{SET} \times K = V_{SET} / R_{SET} \times K , \qquad (1)$$

where K = 28000 when battery voltage is 3.6 V.

In real applications, the actual switching current limit is affected by input battery voltage, and also the transformer primary inductance, Lp. If necessary, the following expressions can be used to determine I_{SWlim} more accurately:

$$I_{SET} = V_{SET} / (R_{SET} + R_{SET(INT)} - K \times R_{GND(INT)}), \quad (2)$$

where:

$R_{SET(INT)}$ is the internal resistance of the I_{SET} pin (1 kΩ typical),

$R_{GND(INT)}$ is the internal resistance of the bonding wire for the GND pin (27 mΩ typical), and

$K = (K' + V_{IN} \times K'')$, with $K' = 24350$ and $K'' \approx 1040$ at $T_A = 25°C$. Then,

$$I_{SWlim} = I_{SET} \times K + V_{BAT} / L_P \times t_D , \qquad (3)$$

where t_D is the delay in SW turn-off (0.1 µs typical).

Figure 3 can be used to determine the relationship between R_{SET} and I_{SWlim} at various battery voltages.

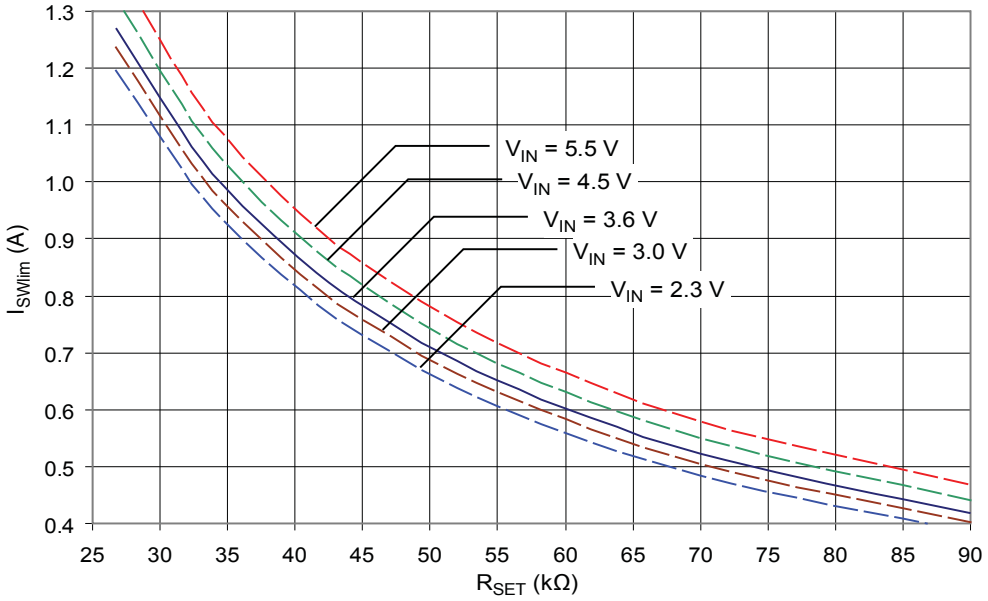


Figure 3. Peak Current Limit versus ISET Resistance. $V_{IN} = V_{BAT}$, transformer L_P = 8 µH, T_A = 25°C.

Smart Current Limit (Optional)

With the help of some simple external logic, the user can change the charging current according to the battery voltage. For example, assume that I_{SET} is normally 36 µA (for I_{SWlim} = 1.0 A). Referring to figure 4, when the battery voltage drops below 2.5 V, the signal at BL (battery-low) goes high. The resistor RBL, connecting BL to the ISET pin, then injects 10 µA into RSET. This effectively reduces ISET current to 26 µA (for I_{SWLIM} = 0.73 A).

Timer Mode and Fast Charging Mode

The A8731 achieves fast charging times and high efficiency by operating in discontinuous conduction mode (DCM) through most of the charging process The relationship of Timer Mode and Fast Charging Mode is shown in figure 5.

The IC operates in Timer Mode when beginning to charge a completely discharged photoflash capacitor, usually when the output voltage, V_{OUT}, is less than approximately 15 to 20 V. Timer Mode is a fixed period, 18 µs, off-time control. One advantage of having Timer Mode is that it limits the initial battery current surge and thus acts as a "soft-start." A time-expanded view of a Timer Mode interval is shown in figure 6.

As soon as a sufficient voltage has built up at the output capacitor, the IC enters Fast-Charging Mode. In this mode, the next switching cycle starts after the secondary side current has stopped flowing, and the switch voltage has dropped to a minimum value. A proprietary circuit is used to allow minimum-voltage switching, even if the SW pin voltage does not drop to 0 V. This enables Fast-Charging Mode to start earlier

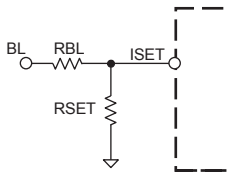


Figure 4. Smart Current Limit reference circuit

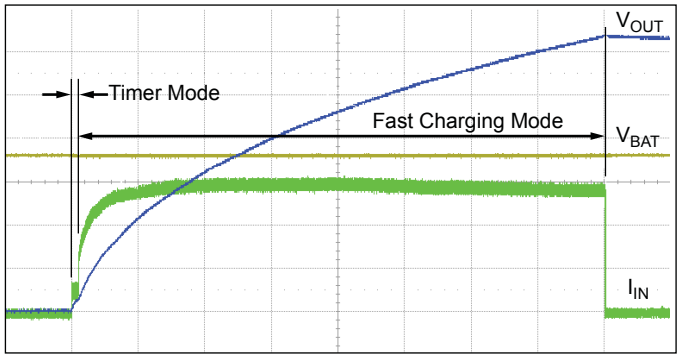


Figure 5. Timer Mode and Fast Charging Mode. t =200 ms/div, V_{OUT} =50 V/div, V_{BAT} =1 V/div., I_{IN} =100 mA/div., V_{BAT} =3.6 V, C_{OUT} =20 µF/330 V, R_{SET}=46 kΩ (I_{SWlim}≈0.75 A).

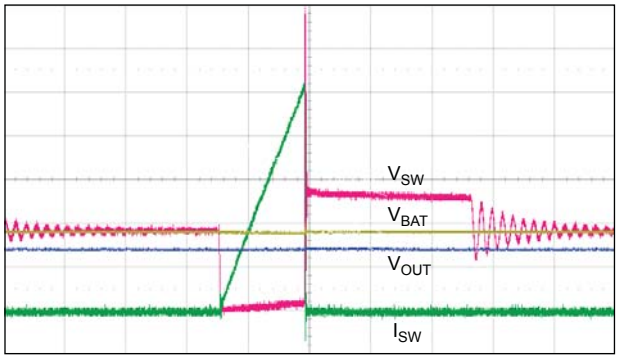


Figure 6. Timer Mode expanded view. V_{OUT} ≤ 14 V, t = 2 µs / div., V_{BAT} = 3.6 V, R_{SET} = 33.2 kΩ.

than previously possible, thereby reducing the overall charging time. Minimum-voltage switching is shown in figure 7.

During Fast-Charging Mode, when V_{OUT} is high enough (over 50 V), true zero-voltage switching (ZVS) is achieved. This further improves efficiency as well as reduces switching noise. A ZVS interval is shown in figure 8.

IGBT Gate Driver Inputs

The TRIGGER1 and TRIGGER2 pins are ANDed together inside the IC to control the IGBT gate driver. If only one trigger signal is needed, tie both trigger pins together and use as a single input.

Ambient Light Sensing

Ambient Light Sensing (ALS) can be easily implemented for the A8731 using the TRIGGER2 pin plus three external components. This configuration is shown in figure 9.

The phototransistor current is proportional to the intensity of the light that it receives. When there is sufficient ambient light (for example, during daylight outdoor photographing), a current of about 30 µA can flow through the phototransistor. This forces the voltage at TRIGGER2 pin to fall to 0.8 V or lower, so it prohibits TRIGGER1 from firing the flash. The exact threshold of ambient light required to prohibit flash firing can be adjusted by R_{TGR1}. The smaller this resistance, the brighter the ambient light must be to prohibit flash firing.

When ambient conditions are dark, the current flowing through the phototransistor is in less than 1 µA. Because the TRIGGER2 pin is biased at 1.4 V or higher, TRIGGER1 is allowed to activate the IGBT gate driver (and thereby fire the flash).

The capacitor CTGR1 and resistor RTGR1 form an integrator for light exposure. When the flash fires, bright light bounces back from subject and enters the phototransistor. In example A in figure 10, the flash terminates after just 30 µs, without fully discharging the photoflash capacitor.

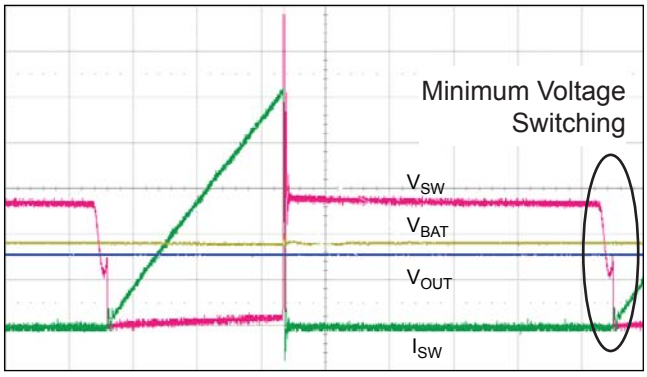


Figure 7. Minimum voltage switching. V_{OUT} ≥ 15 V; t =1 µs/div., V_{BAT} = 3.6 V, R_{SET} = 33.2 kΩ.

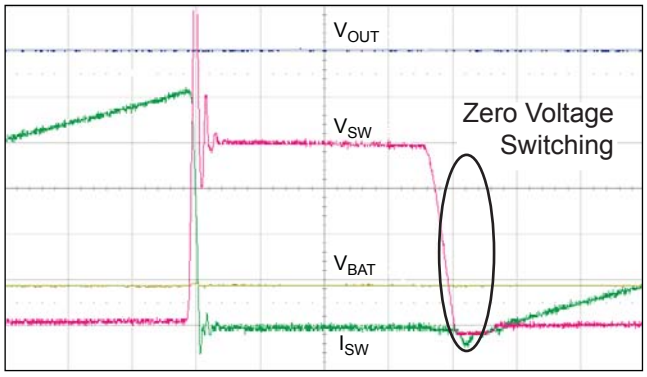


Figure 8. Zero voltage switching. V_{OUT} = 120 V. t = 0.2 µs/div., V_{BAT} = 3.6 V, R_{SET} = 33.2 kΩ.

If the subject is far away, the reflected light intensity is lower, so the phototransistor current is also lower. In example B, the flash stays on for longer time (60 µs) and discharges more energy from the photoflash capacitor.

Using a larger C_{TGR1} causes the time constant of the integrator to increase, so a longer pulse is required before the flash is terminated.

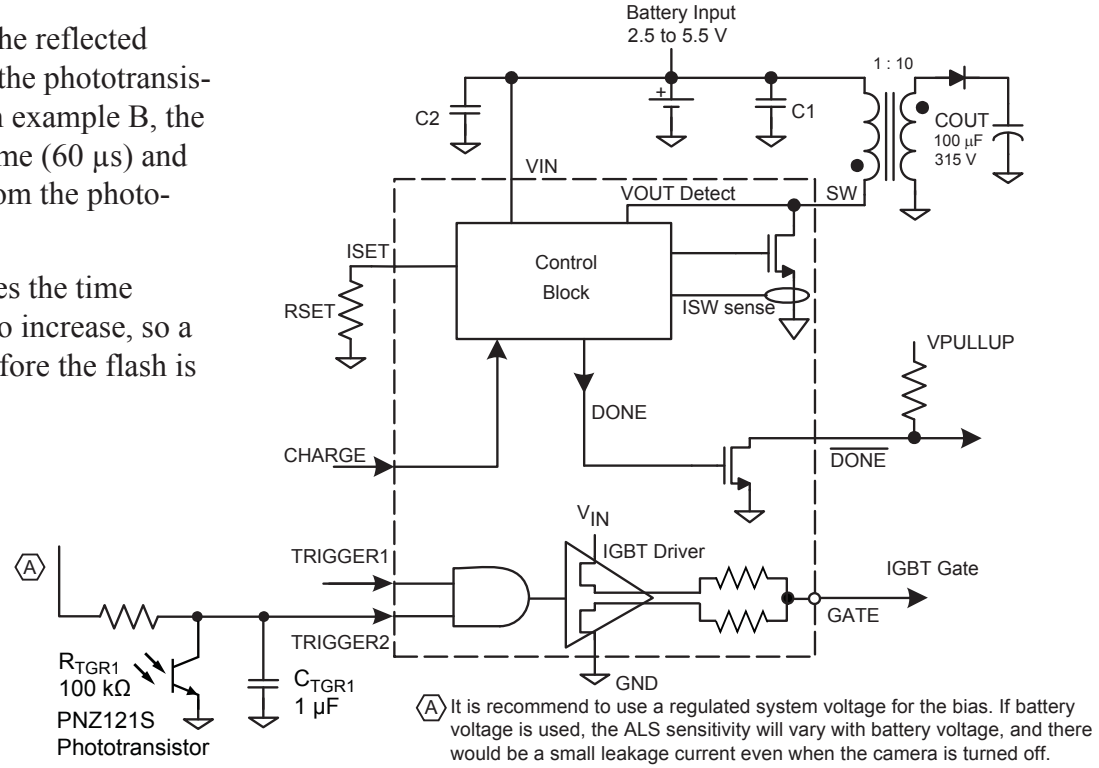
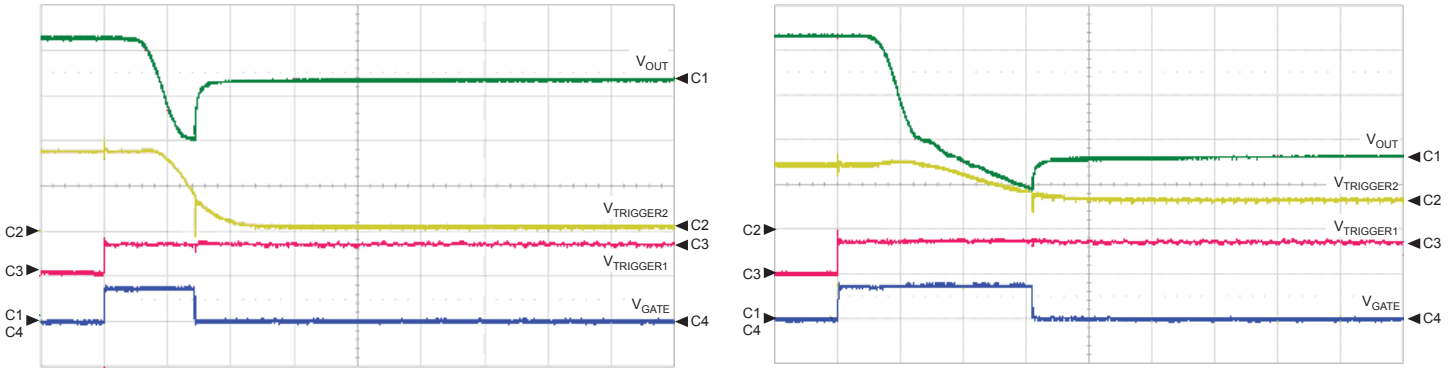


Figure 9. ALS typical application



Common Parameters		
Symbol	Parameter	Units/Division
C1	V_{OUT}	50 V
C2	$V_{TRIGGER2}$	1 V
C3	$V_{TRIGGER1}$	5 V
C4	V_{GATE}	5 V
t	time	20 µs

Figure 10. Adaptive timing of photoflash. (A) Subject near to camera, and (B) subject far from camera.

Transformer Selection

1. The transformer turns ratio, N, determines the output voltage:

$$N = N_S / N_P \quad , \tag{4}$$

$$V_{OUT} = 31.5 \times N - V_d \quad , \tag{5}$$

where 31.5 is the typical value of $V_{OUTTRIP}$, and V_d is the forward drop of the output diode.

2. The primary inductance, L_P, determines the on-time of the switch:

$$t_{on} = (-L_P / R) \times \ln(1 - I_{SWlim} \times R / V_{IN}) \quad , \tag{6}$$

where R is the total resistance in the primary current path (including $R_{SWDS(on)}$ and the DC resistance of the transformer).

If V_{IN} is much larger than $I_{SWlim} \times R$, then t_{on} can be approximated by:

$$t_{on} = I_{SWlim} \times L_P / V_{IN} \quad . \tag{7}$$

3. The secondary inductance, L_S, determines the off-time of the switch. Given:

$$L_S / L_P = N \times N \text{ , then}$$

$$t_{off} = (I_{SWlim} / N) \times L_S / V_{OUT} \tag{8}$$

$$= (I_{SWlim} \times L_P \times N) / V_{OUT} \quad . \tag{9}$$

The minimum pulse width for t_{off} determines what is the minimum L_P required for the transformer. For example, if I_{SWlim} = 0.7 A, N = 10, and V_{OUT} = 315 V, then L_P must be at least 9 µH in order to keep t_{off} at 200 ns or longer. These relationships are illustrated in figure 11.

In general, choosing a transformer with a larger L_P results in higher efficiency (because a larger L_P means lower switch frequency and hence lower switching loss). But transformers with a larger L_P also require more windings and larger magnetic cores. Therefore, a trade-off must be made between transformer size and efficiency.

Component Selection

Selection of the flyback transformer should be based on the peak current, according to the following table:

I_{Peak} Range (A)	Supplier	Part Number	L_P (µH)
0.4 to 1.0	TDK	LDT565630T-002	14.5
0.5 to 1.2	TDK	LDT565630T-003	10.5
0.7 to 1.0	TDK	LDT565620ST-203	8.2
0.7 to 1.2	Mitsumi	C5-KT2.2L	8.0
0.8 to 1.2	Tokyo Coil	T-19-243	6.5

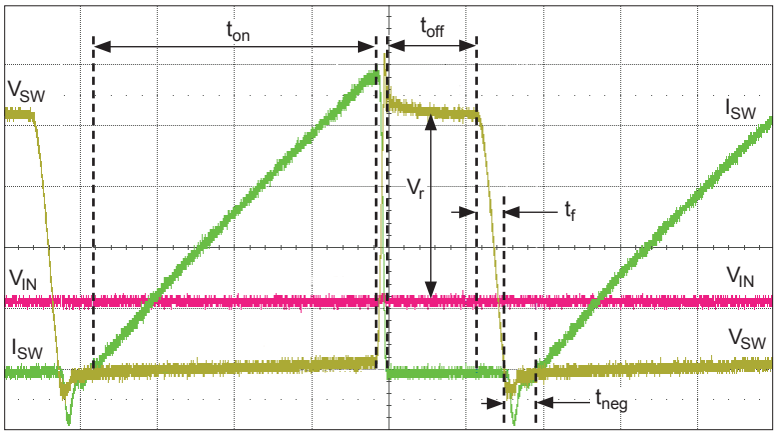
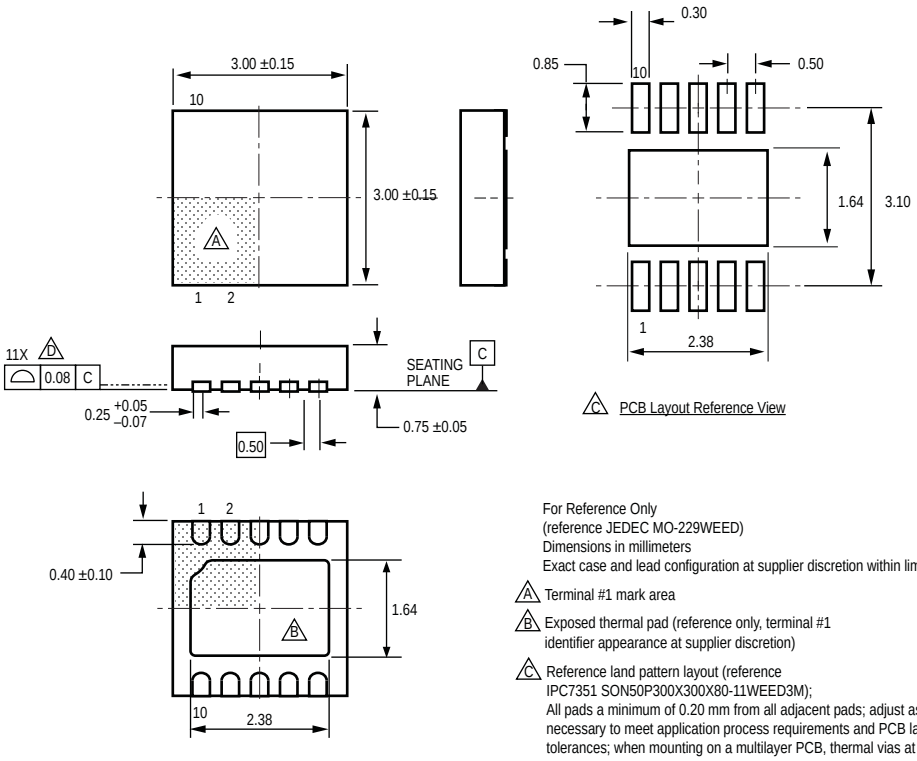


Figure 11. Pulse width relationship definitions.

Package EJ, 3 mm x 3 mm 10-Contact DFN
with Exposed Thermal Pad



For Reference Only
(reference JEDEC MO-229WEED)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 SON50P300X300X80-11WEED3M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Revision History

Revision	Revision Date	Description of Revision
Rev. 1	April 19, 2012	Miscellaneous format changes

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