Industrial, Three-Phase Integrated MOSFET Driver

FEATURES AND BENEFITS

- 3-phase integrated MOSFET driver
- Cross-conduction protection with integrated dead-time
- Charge pump for low supply voltage operation
- 4.5 to 40 V supply voltage operating range
- Integrated logic supply
- High output current capability, up to 4.3 A
- Low MOSFET on-state resistance
  - 240 mΩ (typ) $R_{DS(ON)}$ (high-side + low-side) at T_A = 25°C
- Multiple control interface options
  - 6× PWM control interface
  - 3× PWM control interface
- 2 MHz 16-bit SPI-compatible serial interface
- SPI-compatible serial interface
- Bridge control by direct logic inputs
- Programmable gate drive
- Current sense amplifier
- Programmable diagnostics

APPLICATIONS

- Bridge 12 V Robotics
- Finger joint
- Electric blinds
- Small appliances
- Pumps and fans

DESCRIPTION

The A89110N is an integrated N-channel power MOSFET driver and is specifically designed for industrial and robotics applications with inductive loads, such as BLDC motors and stepper motors.

A unique charge pump regulator provides the supply for full gate drive from 4.5 to 40 V. Gate drive voltage and strength are programmable to improve the EMC performance.

Integrated diagnostics provide indication of multiple internal faults, system faults, and power bridge faults, and can be configured to protect the power MOSFETs under most short-circuit conditions.

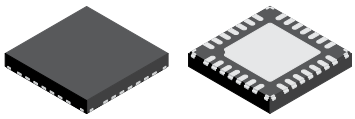
Full control is provided over all six power MOSFETs in the three-phase bridge, allowing motors to be driven with block commutation or sinusoidal excitation. The power MOSFETs are protected from shoot-through by integrated crossover control and integrated dead-time.

Detailed diagnostic information can be read through the serial interface.

The A89110N is supplied in a 28-contact wettable flank QFN (ET), with exposed pad for enhanced thermal dissipation. This device is lead (Pb) free, with 100% matte tin leadframe plating.

PACKAGE

5 mm × 5 mm × 0.9 mm, 28-contact QFN
with exposed thermal pad and wettable flank (ET package)



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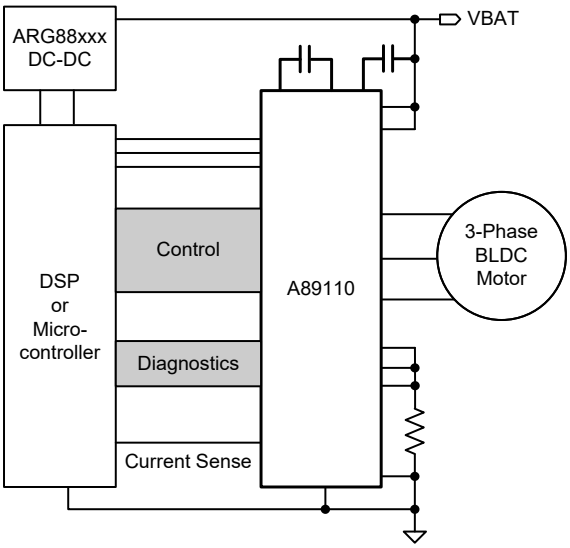

Figure 1: Typical Application

SELECTION GUIDE

Part Number	I/O Logic	Packing	Package
A89110NKETSR-3	3.3 V	6000 pieces per 13-in. reel	5 mm × 5 mm, 0.9 mm nominal height, 28-contact QFN with exposed thermal pad and wettable flank
A89110NKETSR-5	5 V		

ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
Load Supply Voltage	V_{BB}	VBB1, VBB2	–0.3 to 42	V
Pumped Regulator Supply	V_{CP}	VCP	V_{BB} – 0.3 to V_{BB} + 6.6	V
Charge Pump Capacitor Terminal	V_{CP1}	CP1	–0.3 to V_{BB} + 0.3	V
Charge Pump Capacitor Terminal	V_{CP2}	CP2	V_{BB} – 0.3 to V_{BB} + 6.6	V
Logic Inputs	V_I	HA, HB, HC, LA, LB, LC, STRn, SCK, SDI, RESETn	–0.3 to 6	V
Logic Outputs	V_O	SDO	–0.3 to 6	V
Diagnostic Output Terminal	V_{DIAG}	DIAG	–0.3 to 6	V
Sense Amplifier Inputs	V_{CSI}	CSP, CSM	–1 to 4	V
Sense Amplifier Outputs	V_{CSO}	CSO	–0.3 to 6	V
Motor Phase Terminals	V_{SX}	OUTA, OUTB, OUTC	V_{LSSX} – 1 to V_{BB} + 1	V
Bridge Low-Side Source Terminal	V_{LSS}	LSSA, LSSB, LSSC	–0.5 to 1	V
Ambient Operating Temperature Range	T_A	Limited by power dissipation	–40 to 150	°C
Maximum Continuous Junction Temperature	$T_{J(max)}$		165	°C
Transient Junction Temperature	T_{Jt}	Overtemperature event not exceeding 10 seconds; lifetime duration not exceeding 10 hours; guaranteed by design characterization.	180	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

[1] With respect to GND. Ratings apply when no other circuit operating constraints are present. Not production tested. Guaranteed by characterization.

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [1]	Value	Unit
ET Package Thermal Resistance	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	30	°C/W
		2-layer PCB with 3.8 in^2 copper each side	44	°C/W
	$R_{\theta JP}$		2	°C/W

[1] Additional thermal information are available on the Allegro website.

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RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Notes	Min	Typ	Max	Units
Supply Voltage	V_{BB}		4.5	12	40	V
RMS Phase Current	I_{OUT}		–	–	1.5 [1]	A
Logic Voltage Range	V_I		–0.3	–	5.5	V
Operating Ambient Temperature Range	T_A		–40	–	125	°C
Operating Junction Temperature Range	T_J		–40	–	150	°C
Motor PWM Frequency	f_{PWM}		–	24	–	kHz

[1] Power dissipation and thermal limits must be observed.

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PINOUT DIAGRAM AND TERMINAL LIST

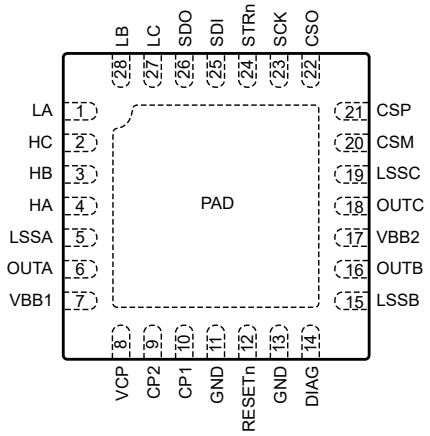

Figure 2: Package ET-28 Pinouts

Terminal List

Number	Name	Description
1	LA	Control Input A Low Side
2	HC	Control Input C High Side
3	HB	Control Input B High Side
4	HA	Control Input A High Side
5	LSSA	Low-Side Source Phase A
6	OUTA	Motor Connection Phase A
7	VBB1	Main Power Supply
8	VCP	Pumped Supply
9	CP2	Pump Capacitor
10	CP1	Pump Capacitor
11	GND1	Ground
12	RESETn	Standby Mode Control
13	GND2	Ground
14	DIAG	Programmable Diagnostic Output

Number	Name	Description
15	LSSB	Low-Side Source Phase B
16	OUTB	Motor Connection Phase B
17	VBB2	Main Power Supply
18	OUTC	Motor Connection Phase C
19	LSSC	Low-Side Source Phase C
20	CSM	Current Sense Amplifier –Input
21	CSP	Current Sense Amplifier +Input
22	CSO	Current Sense Amplifier Output
23	SCK	Serial Clock Input
24	STRn	Serial Strobe (Chip Select) Input
25	SDI	Serial Data Input
26	SDO	Serial Data Output
27	LC	Control Input C Low Side
28	LB	Control Input B Low Side
–	PAD	Connect to Ground

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FUNCTIONAL BLOCK DIAGRAM

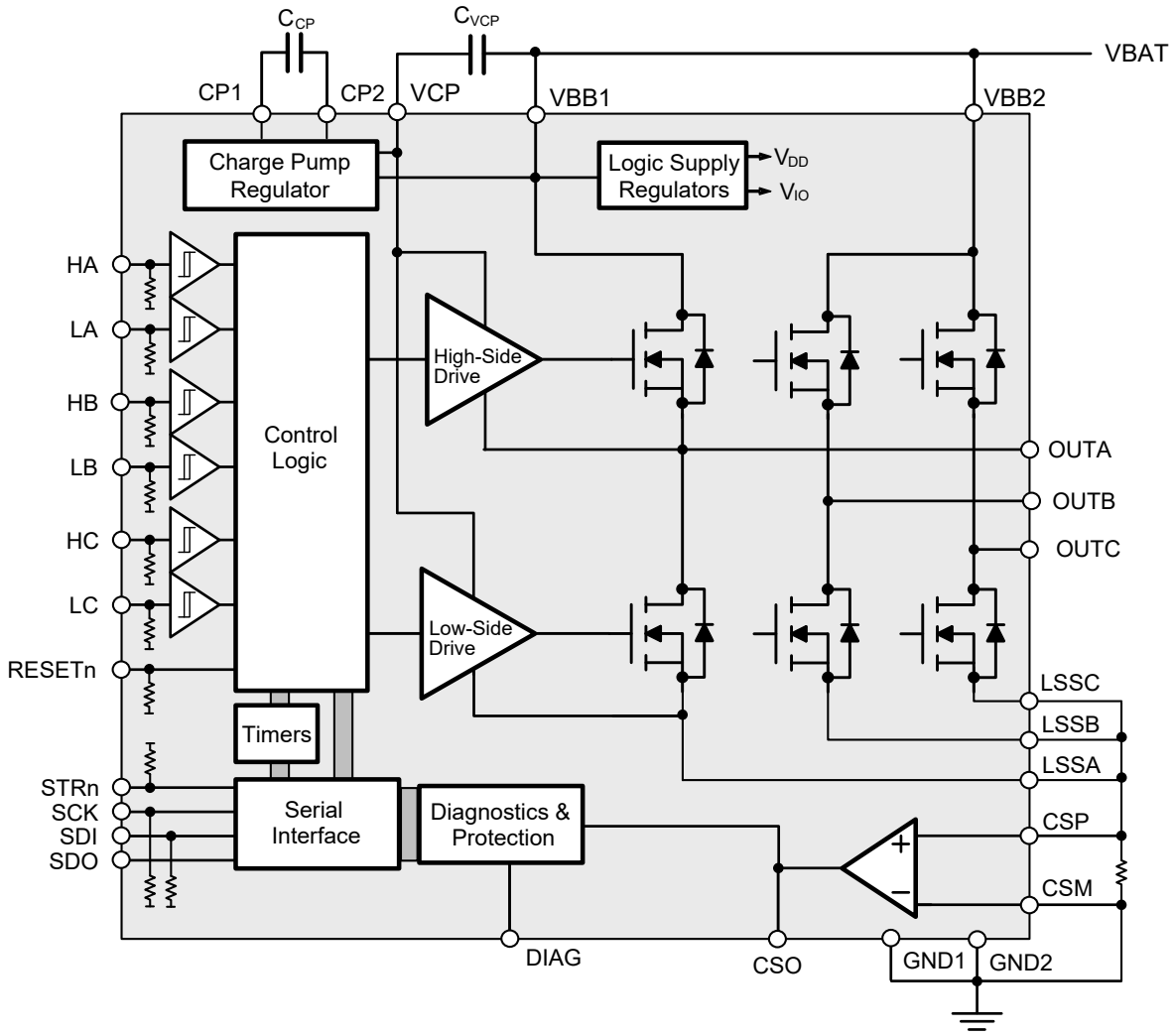

Figure 3: Functional Block Diagram

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ELECTRICAL CHARACTERISTICS: Valid at T_J = –40°C to 150°C, V_{BB} = 4.5 to 40 V, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY AND REFERENCE						
VBB Functional Operating Range	V_{BB}	Operating; outputs active	4.5	–	40	V
		Digital logic active	4.1	–	40	V
		No unsafe states	0	–	40	V
VBB Quiescent Current	$I_{BB(Q)}$	V_{BB} = 12 V, RESETn = high, all gate drive outputs low	–	8.5	9.5	mA
	$I_{BB(S)}$	V_{BB} = 12 V, V_{RESETn} ≤ 300 mV, sleep mode, T_J = 25°C	–	–	4	µA
		V_{BB} = 40 V, V_{RESETn} ≤ 300 mV, sleep mode, T_J = 25°C	–	–	8	µA
VCP Output Voltage	V_{CP}	V_{BB} > 7 V, V_{CP} = V_{VCP} – V_{BB}, I_{VCP} = 0 to –1 mA [1]	5.4	6	6.6	V
		4.5 V < V_{BB} < 7 V, V_{CP} = V_{VCP} – V_{BB}, I_{VCP} = 0 to –1 mA [1]	3.7	–	–	V
Internal Logic Supply Regulator Voltage [2][3]	V_{DD}		3	3.3	3.6	V
Internal Logic I/O Regulator Voltage	V_{IO}	V_{BB} > 4.5 V, A89110NKETSR-3	3	3.3	3.6	V
		V_{BB} > 6 V, A89110NKETSR-5	4.5	5	5.5	V
POWER DRIVER						
Total Driver $R_{DS(ON)}$ (Sink + Source)	$R_{DS(ON)}$	V_{BB} = 12 V, I = 1.5 A, T_J = 25°C	195	240	300	mΩ
		V_{BB} = 12 V, I = 1.5 A, T_J = 150°C [3]	290	400	495	mΩ
High-Side Driver $R_{DS(ON)}$	$R_{DS(ON)SRC}$	V_{BB} = 12 V, T_J = 25°C	95	120	150	mΩ
Low-Side Driver $R_{DS(ON)}$	$R_{DS(ON)SNK}$	V_{BB} = 12 V, T_J = 25°C	90	120	150	mΩ
Sx Pin Slew-Rate Switching 20% to 80% (Rising), 80% to 20% (Falling)	$t_{OUT(SLEW)}$	V_{BB} = 12 V, TSR/TSF = 0	–	50	72	ns
		V_{BB} = 12 V, TSR/TSF = 1, default	–	90	124	ns
		V_{BB} = 12 V, TSR/TSF = 2	–	137	188	ns
		V_{BB} = 12 V, TSR/TSF = 3	–	177	260	ns
Turn-On Propagation Delay	$t_{p(on)}$	V_{BB} = 12 V, Input change to phase output change, TSR/TSF = 1, default	–	–	1	µs
Turn-Off Propagation Delay	$t_{p(off)}$	V_{BB} = 12 V, Input change to phase output change, TSR/TSF = 1, default	–	–	1	µs
Rising Dead Time [3]	$t_{DEAD(r)}$	TSR = 0	–	500	600	ns
		TSR = 1, Default	–	550	650	ns
		TSR = 2	–	575	675	ns
		TSR = 3	–	625	725	ns
Falling Dead Time [3]	$t_{DEAD(f)}$	TSF = 0	–	410	600	ns
		TSF = 1, Default	–	360	580	ns
		TSF = 2	–	330	560	ns
		TSF = 3	–	320	560	ns
Motor PWM Frequency [3]	f_{OSC}		–	24	–	kHz

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
LOGIC INPUTS AND OUTPUTS						
Input Low Voltage	V_{IL}		–	–	0.3 × V_{IO}	V
Input High Voltage	V_{IH}	All logic inputs	0.7 × V_{IO}	–	–	V
Input Hysteresis	V_{Ihys}	All logic inputs	–	0.08 × V_{IO}	–	mV
Input Pull-Down	R_{PD}	All logic inputs	–	50	70	kΩ
Input Pull-Up (STRn to V_{IO})	R_{PU}	All logic inputs	–	50	70	kΩ
Output Low Voltage	V_{OL}	I_{OL} = 1 mA [1]	–	–	0.4	V
Output High Voltage (SDO)	V_{OH}	I_{OH} = –1 mA [1]	0.7 × V_{IO}	–	–	V
Output Current Limit (DIAG)	$I_{OD(LIM)}$		–	10	–	mA
Output Leakage DIAG	I_{OD}	V_{DIAG} = 6 V	–	–	1	µA
CURRENT SENSE AMPLIFIER						
Input Offset Voltage	V_{IOS}		–10	–	10	mV
Input Offset Voltage Drift [3]	ΔV_{IOS}		–	±4	–	µV/°C
Input Bias Current [1]	I_{BIAS}	V_{ID} = 0 V, V_{CM} in range	–50	–	5	µA
Input Offset Current [1]	I_{OS}	V_{ID} = 0 V, V_{CM} in range	–1.5	–	1.5	µA
Input Common-Mode Range (DC)	V_{CM}	V_{ID} = 0 V	–1	–	2	V
Gain	A_V	SAG[1:0] = 01	–	20	–	V/V
Gain Error	E_A	V_{CM} in range	–1.6	–	1.6	%
Pedestal Voltage	V_{OOS}	Programmable typical range, controlled by SAO[2:0]	0.2	–	1.6	V
Pedestal Voltage Error	E_{VO}	V_{ID} = 0 V, V_{CM} in range, V_{OOS} = programmable output range	–10	±2	10	%
Small Signal –3 dB Bandwidth at Gain = 20 [3]	BW	V_{IN} = 10 mV_{PP}	2	–	–	MHz
Output Settling Time (to within 40 mV) [3]	t_{SET}	V_{CSO} = 1 V_{PP} square wave, Gain = 20, C_{OUT} = 50 pF	0.2	–	1	µs
Output Dynamic Range	$V_{CS(OUT)}$	–100 µA < I_{CSO} < 100 µA, V_{BB} = 12 V	0.45	–	4	V
Output Voltage Clamp	$V_{CS(CL)}$	I_{CSO} = –500 µA, V_{BB} = 12 V	5.3	5.9	6.3	V
Output Current Sink [1]	$I_{CS(SINK)}$	V_{ID} = 0 V, V_{CSO} = V_{OOS} = 0.8 V, Gain = 20	230	–	490	µA
Output Current Sink (Boosted) [1][4]	$I_{CS(SINKB)}$	V_{OOS} = 0.8 V, V_{ID} = –50 mV, Gain = 20, V_{CSO} = 1.5 V	1.8	–	4.4	mA
Output Current Source [1]	$I_{CS(SOURCE)}$	V_{OOS} = 0.8 V, V_{ID} = 200 mV, V_{CSO} = 1.5 V, Gain = 20	–5	–	–1.7	mA
VBB Supply Ripple Rejection Ratio	PSRR	V_{ID} = 0 V, 100 kHz, Gain = 20 [3]	–	65	–	dB
		V_{CSP} = V_{CSM} = 0 V, DC, Gain = 20	–	110	–	dB
Common-Mode Rejection Ratio	CMRR	V_{CM} step from 0 V to 200 mV, Gain = 20	–	100	–	dB
		V_{CM} = 200 mV_{PP}, 100 kHz, Gain = 20 [3]	–	62	–	dB
		V_{CM} = 200 mV_{PP}, 1 MHz, Gain = 20 [3]	–	43	–	dB
		V_{CM} = 200 mV_{PP}, 10 MHz, Gain = 20 [3]	–	25	–	dB
Common-Mode Recovery Time (to within 100 mV) [3]	$t_{CM(rec)}$	V_{CM} step from –1 V to 1 V, Gain = 20, C_{OUT} = 50 pF	–	–	2.1	µs
Output Slew Rate 10% to 90%	SR	V_{ID} step from 0 V to 175 mV, Gain = 20, C_{OUT} = 50 pF	1.8	–	7.5	V/µs
Input Overload Recovery (to within 40 mV) [3]	$t_{ID(rec)}$	V_{ID} step from 200 V to 0 V, V_{CSO} ≤ 4.2 V, Gain = 20, C_{OUT} = 50 pF	0.4	–	2.1	µs

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
DIAGNOSTICS AND PROTECTION						
VBB Overvoltage Warning	$V_{BB(OV)}$	V_{BB} rising	32	34	36	V
VBB Overvoltage Hysteresis	$V_{BB(OV)Hys}$		2.5	2.8	3.1	V
VBB Undervoltage	$V_{BB(UV)}$	V_{BB} falling	4	–	4.2	V
VBB Undervoltage Hysteresis	$V_{BB(UV)Hys}$		150	225	300	mV
VBB POR Voltage	$V_{BB(POR)}$	V_{BB} falling	3.8	4	4.1	V
VBB POR Voltage Hysteresis	$V_{BB(POR)Hys}$		90	110	135	mV
VCP Undervoltage Threshold	$V_{CP(ON)}$	$V_{CP} = V_{VCP} – V_{BB}$, V_{CP} rising	3.15	3.3	3.45	V
	$V_{CP(OFF)}$	$V_{CP} = V_{VCP} – V_{BB}$, V_{CP} falling	2.95	3.1	3.25	V
Overcurrent Threshold Voltage	V_{OCT}	Default power-up value	–	1.4	–	V
Overcurrent Qualify Time	t_{OCQ}	Default power-up value	–	7.5	–	µs
Temperature Warning Threshold [3]	T_{JW}	Temperature increasing	120	135	150	°C
Temperature Warning Threshold [3]	T_{JWHys}		–	15	–	°C
Overtemperature Threshold [3]	T_{JF}	Temperature increasing	160	175	190	°C
Overtemperature Hysteresis [3]	T_{JFHys}	Recovery = $T_{JF} – T_{JFHys}$	–	15	–	°C
LOGIC I/O – DYNAMIC PARAMETERS [3]						
Reset Pulse Width	t_{RST}	Outputs disabled	1	–	4.5	µs
Reset Shutdown Time	t_{RSD}	Sleep	30	–	–	µs
SPI Clock Frequency	f_{SCK}	50 pF load on SDI	2	–	–	MHz
Clock High Time	$t_{SCK(H)}$	A in Figure 5	250	–	–	ns
Clock Low Time	$t_{SCK(L)}$	B in Figure 5	250	–	–	ns
Strobe Lead Time to SCK Low	$t_{STR(LD)}$	C in Figure 5	1.5	–	–	µs
Strobe Lag Time	$t_{STR(LG)}$	D in Figure 5	500	–	–	ns
Strobe High Time	$t_{STR(H)}$	E in Figure 5	6	–	–	ns
Data Out Enable Time	$t_{SDO(E)}$	F in Figure 5	400	–	–	ns
Data Out Disable Time	$t_{SDO((D)}$	G in Figure 5	300	–	–	ns
Data Out Valid Time from Clock Falling	$t_{SDO(V)}$	H in Figure 5	400	–	–	ns
Data Out Hold Time from Clock Falling	$t_{SDO(H)}$	J in Figure 5	50	–	–	ns
Data In Set-Up Time to Clock Rising	$t_{SDI(S)}$	K in Figure 5	150	–	–	ns
Data In Hold Time from Clock Rising	$t_{SDI(H)}$	L in Figure 5	100	–	–	ns
SCK High from STRn Rising	$t_{SCK(STR)}$	M in Figure 5	300	–	–	ns
SCK High to STRn Rising	$t_{STR(SCK)}$	N in Figure 5	300	–	–	ns
Wake Up From Sleep	t_{EN}	C_{VCP} = 1 µF	–	–	3	ms

[1] For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device terminal.
[2] V_{DD} derived from V_{BB} for internal use only. Not accessible on any device terminal.
[3] Limits ensured by design, characterization, and statistical correlation. Only functionally tested in production.
[4] If the amplifier output voltage (V_{CSO}) is more positive than the value demanded by the applied differential input (V_{ID}) and output offset (V_{OOS}) conditions, output current sink capability is boosted to enhance negative going transient response.

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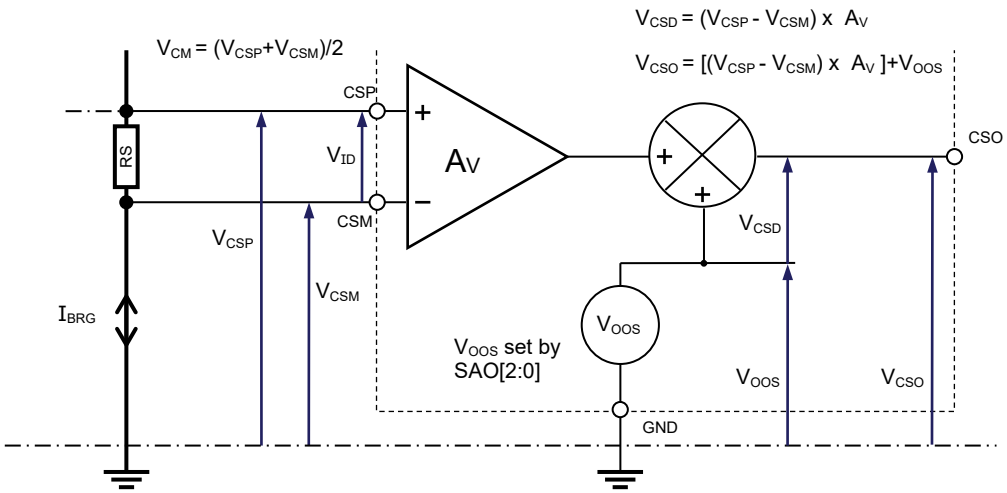

Figure 4: Sense Amplifier Voltage Definitions

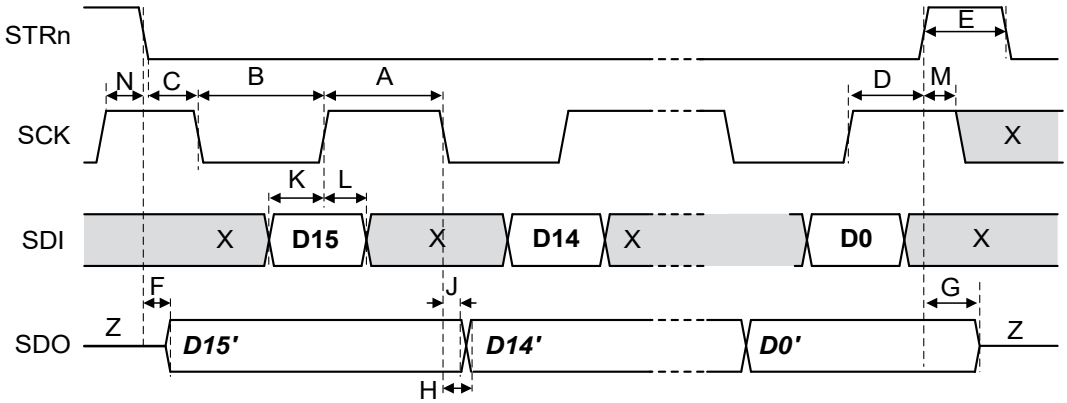

Figure 5: Serial Interface Timing
X = immaterial, Z = high impedance (tri-state)

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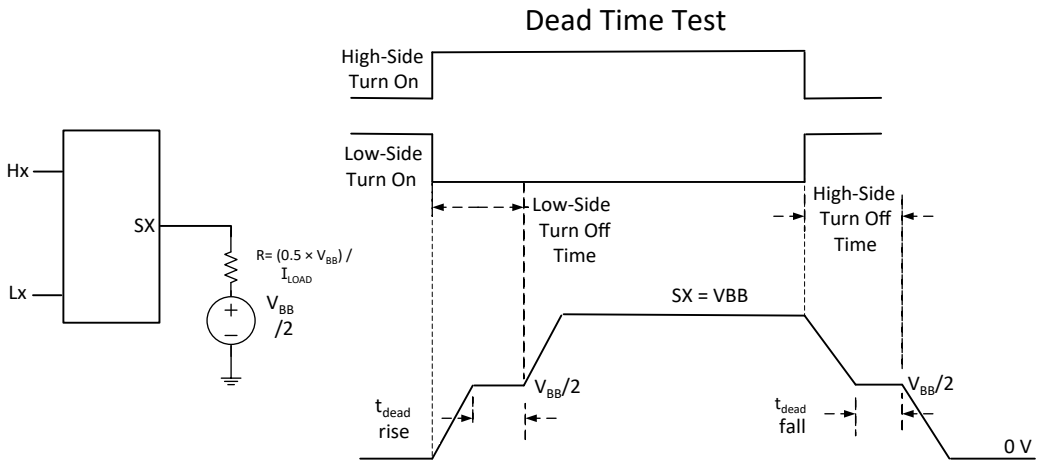

Figure 6: Dead Time Definitions

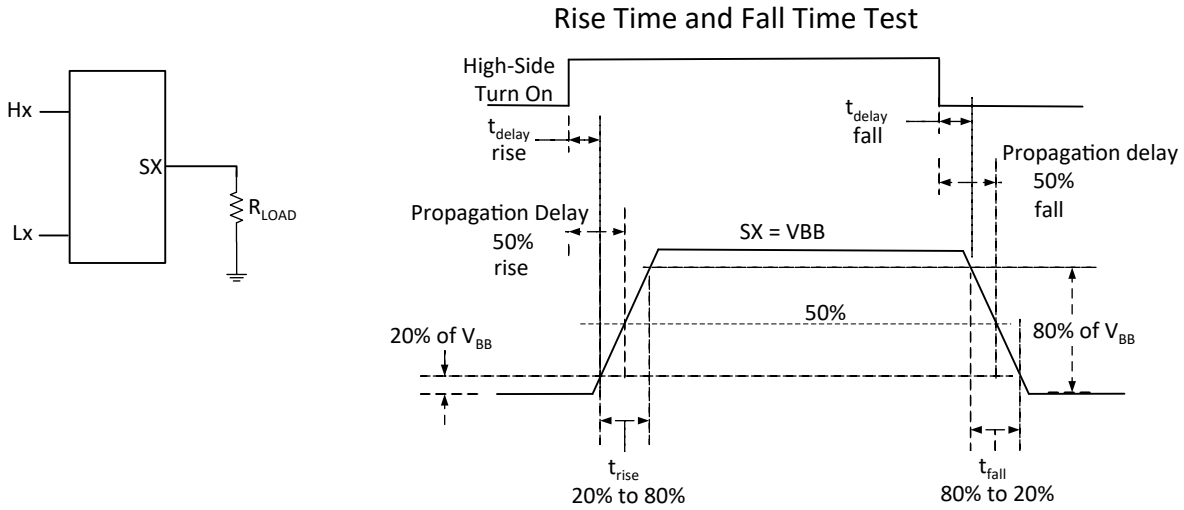

Figure 7: Rise and Fall Time Definitions

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FUNCTIONAL DESCRIPTION

The A89110N contains six N-channel power MOSFETs configured as three half bridges. The three half bridges can be operated independently or together as a three-phase bridge driver for BLDC or PMSM motors.

Gate MOSFETs can be controlled individually with logic inputs. The high-side and the low-side gate drive control logic inputs provide a very flexible solution for many motor control applications. Independent control over each MOSFET allows each driver to be driven with an independent PWM signal for full sinusoidal excitation. Configuring the A89110N to block control allows the three phases to be fully controlled with only three logic inputs. All logic inputs are standard CMOS levels and can be compatible with 3.3 V or 5 V logic outputs depending on part number selection.

The A89110N requires a single unregulated supply of 4.5 V to 40 V and includes a charge-pump regulator and two internal integrated linear regulators. The charge pump regulator provides the regulated gate drive voltage used for turning on the low-side and high-side MOSFETs. One linear regulator provides the internal logic supply voltage, V_{DD}, and a second independent regulator provides the supply and reference, V_{IO}, for the digital input and output terminals. This can be 3.3 V or 5 V determined by part number selection.

Circuit functions are provided within the A89110N to ensure that, under normal operating conditions, all power MOSFETs are operational at supply voltages down to 4.5 V. For extreme battery voltage drop conditions, the A89110N is guaranteed not to reset any internal states at supply voltages down to 4.2 V. However, below 4.5 V, it is possible that the gate drive output may fall below a safe level and be disabled. A low-power sleep mode allows the A89110N to remain connected to a battery supply without the need for an additional supply switch.

The A89110N includes diagnostic features to provide indication of and/or protection against undervoltage, overvoltage, and overtemperature faults. Detailed diagnostic information is available through the serial interface.

The serial interface also provides access to programmable, fault blanking time, and programmable thresholds for overcurrent fault detection.

The A89110N includes a low-side current-sense amplifier with programmable output offset and programmable gain.

Input and Output Terminal Functions

VBB1, VBB2: Main power supply for internal regulators and charge pump. The main power supply should be connected to VBB through a reverse-voltage protection circuit and should be decoupled with ceramic capacitors connected close to the supply and ground terminals. For normal operation, the two VBB pins must be tied together.

CP1, CP2: Pump capacitor connection for charge pump. Connect a capacitor with a recommended minimum value of 470 nF between CP1 and CP2.

GND: Ground. Connect both GND terminals together at the A89110N. See Layout Recommendations section for further information.

OUTA, OUTB, OUTC: Load phase connections.

LSSA, LSSB, LSSC: Low-side return path for each phase.

HA, HB, HC: Logic inputs to control the high-side gate drive outputs. A pull-down is connected to each input.

LA, LB, LC: Logic inputs to control the low-side gate drive outputs. A pull-down is connected to each input.

SDI: Serial data logic input with pull-down. 16-bit serial word input MSB first.

SDO: Serial data output. High impedance when STRn is high. Outputs bit 15 of the status register, the fault flag, as soon as STRn goes low. When STRn is high, this pin is a back-bias protected push-pull driver which allows the serial bus to be shared with multiple devices.

SCK: Serial clock logic input with pull-down. Data is latched in from SDI on the rising edge of SCK. There must be 16 rising edges per write and SCK must be held high when STRn changes.

STRn: Serial data strobe and serial access enable logic input with pull-up. When STRn is high, any activity on SCK or SDI is ignored and SDO is high impedance, allowing multiple SDI slaves to have common SDI, SCK and SDO connections.

CSP, CSM: Current-sense amplifier inputs.

CSO: Current-sense amplifier output.

DIAG: Diagnostic output. Programmable output to provide fault flag.

RESETn: Resets fault states when pulsed low. Forces low-power shutdown (sleep) when held low for more than the RESET shutdown time, t_{RSD}.

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Power Supplies

A single power supply voltage is required. The main power supply, V_{BB}, should be connected to the VBB pins through a reverse-voltage protection circuit. A 100 nF ceramic decoupling capacitor must be connected close to the supply and ground terminals.

An independent internal regulator provides the supply voltage, V_{DD}, to the internal logic. A second integrated linear regulator provides the supply voltage, V_{IO}, to all logic inputs and push-pull outputs. This digital I/O supply is set to 5 V.

All internal logic is guaranteed to operate correctly to below the regulator undervoltage levels, ensuring that the A89110N continues to operate safely until all logic is reset when a power-on-reset state is present.

Low Supply Voltage Operation

The A89110N operates within specified parameters with V_{BB} from 4.5 V to 40 V. For V_{BB} less than 4.5 V, the outputs may be disabled but the internal logic circuits and the diagnostic output continue to operate with a V_{BB} supply down to 4.1 V. Operation of other digital inputs and outputs, within specified parameters, are limited by V_{BB} relative to the logic I/O voltage, V_{IO}.

In all cases, the A89110N operates safely between 0 V and 40 V under all supply switching conditions. This provides a very rugged solution for use in the harsh industrial and robotics environment.

Pump Regulator

The gate drivers are powered by a programmable voltage internal regulator which limits the supply to the drivers and therefore the maximum gate voltage. This regulator uses a charge pump scheme with a switching frequency at nominally 62.5 kHz. The charge pump operates as a regulated doubler or a linear step-down regulator depending on the input voltage at VBB. An external pump capacitor is required for the regulator to operate. At low supply voltage, the regulated supply is maintained by a charge pump boost converter which requires a pump capacitor connected between the CP1 and CP2 terminals. The pump capacitor should have a nominal value of 470 nF, rated working voltage of at least 16 V and a tolerance of ±20% or better. The pump capacitor, C_P, should have a value of at least 470 nF and is connected between the CP1 and CP2 terminals. The storage capacitor, C_{VCP}, is connected between VCP and VBB. C_{VCP} should have a nominal value of at least 1 µF, rated working voltage of at least 16 V, and a tolerance of ±20% or better.

Power-On Reset

The A89110N monitors the VBB terminal supply voltage to ensure there is sufficient voltage present to operate device functions. If the supply voltage is below the specified $V_{BB(POR)}$ threshold, the device is forced into a known initialization state known as power-on reset (POR).

When in POR, the SPI registers are reset to their default values except for the latched fault status bits FF and POR which are set to 1. The DIAG terminal is pulled low due to the FRESET status bit if sufficient supply voltage is present to drive the pulldown device. All internal MOSFETs are turned off.

The A89110N can be taken out of POR by increasing V_{BB} above the rising threshold ($V_{BB(POR)} + V_{BB(POR)Hys}$).

After a POR event, the POR and FF latched fault bits can be cleared by applying a pulse to RESETn or writing 1 to the corresponding status bits. Although the fault bits are latched, the POR fault state is not latched so the A89110N can operate normally. The graph below shows the operation of the V_{BB} thresholds.

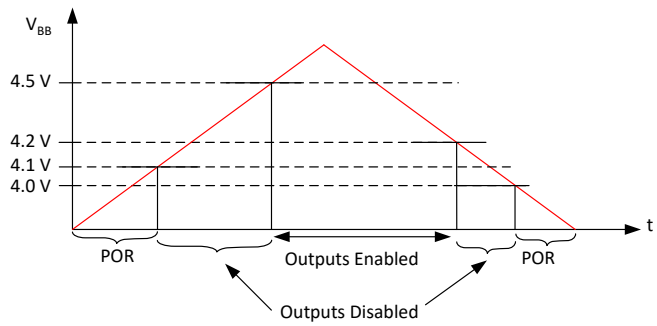

Figure 8: V_{BB} Thresholds

Dead Time

To prevent cross conduction (shoot through) in any phase of the power MOSFET bridge, it is necessary to have a dead-time delay between a high- or low-side turn off and the next complementary turn-on event. The potential for cross conduction occurs when any complementary high-side and low-side pair of MOSFETs are switched at the same time, for example, at the PWM switch point. In the A89110N, the dead time for all phases is internally generated.

External dead time can be generated by the user. However, if it is less than the internally generated dead time, the A89110N ignores it to ensure cross conduction does not occur.

If using gate drive control, the extended MOSFET switching times that result must be accounted for when setting dead time as described in the Gate Drive Control section below.

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The internally generated dead time is only present if the on command for one MOSFET occurs within one dead time after the off command for its complementary partner. In the case where one side of a phase drive is permanently off, for example when using diode rectification with slow decay, then the dead time does not occur. In this case, the gate drive turns on within the specified propagation delay after the corresponding phase input goes high (see Figure 5).

Gate Drive Control

MOSFET gate drives are controlled according to the values set in the Config 2 register.

The time for off-to-on transitions, t_r, is defined by the following equation:

$$t_r = (n + 1) \times 50\ ns$$

where n is a positive integer defined by TSR[1:0].

The default t_r time is 100 ns.

The time for on-to-off transitions, t_f, is defined by the following equation:

$$t_f = (n + 1) \times 50\ ns$$

where n is a positive integer defined by TSF[1:0].

The default t_f time is 100 ns.

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Logic Control Inputs

Six logic level digital inputs, HA, LA, HB, LB, HC, and LC, provide direct control for the internal MOSFETs, one for each MOSFET. The Hx inputs correspond to the high-side MOSFETs and the Lx inputs correspond to the low-side MOSFETs. All logic inputs are standard CMOS levels referenced to the voltage of the logic I/O regulator. Logic inputs have a typical hysteresis of 550 mV to improve noise performance.

SIX-WIRE DRIVE OPTION

The operation of the inputs is shown in Table 1. A pull-down resistor is connected to each input to ensure a safe state if the control becomes disconnected. The CTL bit found in the Config1 register determine how the input pins operate. When CTL is set to its default value of 0, the six logic pins are controlled independently.

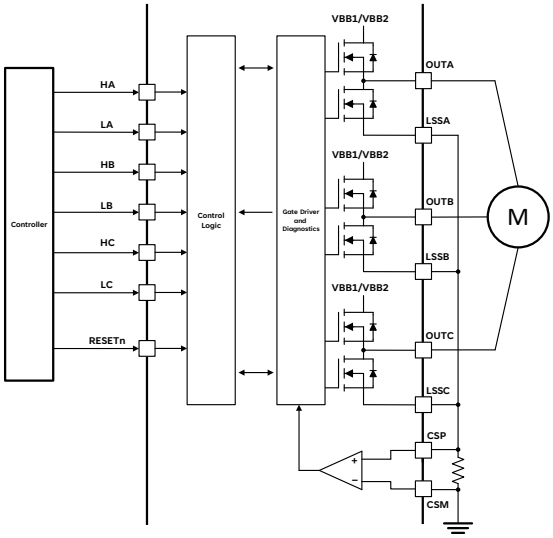

Figure 9: Six-Wire Drive Option

Table 1: Six-Wire Drive Option

Input			Phase
CTL	Hx	Lx	OUTx
0	L	L	Z
0	L	H	LO
0	H	L	HI
0	H	H	Z

H = High Signal
L = Low Signal
Z = High Impedance
LO = Phase is inactive
HI = Phase is active

THREE-WIRE DRIVE OPTION

When CTL is set to 1, the three Hx pins operate as the control pins and the Lx pins operate as the enable pin for each phase as shown in Table 2. Toggling the Hx pin controls both MOSFETs in the corresponding H-bridge. The dead time is applied between the high- and low-side transitions for each phase. When the Lx pins are pulled low, control of the corresponding phase output is disabled and it goes into high impedance.

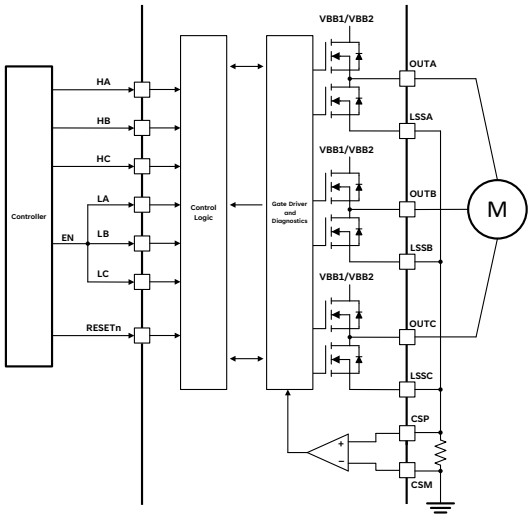

Figure 10: Three-Wire Drive Option

Table 2: Three-Wire Drive Option

Input			Phase
CTL	Hx	Lx	OUTx
1	L	L	Z
1	L	H	LO
1	H	L	Z
1	H	H	HI

H = High Signal
L = Low Signal
Z = High Impedance
LO = Phase is inactive
HI = Phase is active

Internal lockout logic ensures that the high-side gate drive output and low-side gate drive output drive on the same phase cannot be active (high) simultaneously. If the control inputs request both the high-side and the low-side gate drives to be active at the same time, then both high-side and low-side gate drives are switched into the inactive (low) state.

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Sleep Mode

RESETn is an active-low input that commands the A89110N to enter sleep mode, in which the part is inactive and current consumption from the V_{BB} supply is reduced to a low level as defined by the I_{BBS} quiescent current limit. The A89110N enters sleep mode when RESETn is held low for longer than the reset shutdown time, t_{RSD}. The half-bridge outputs are disabled and quiescent current consumption begins to decay toward I_{BBS} within a reset shutdown time, t_{RSD}, of RESETn going low.

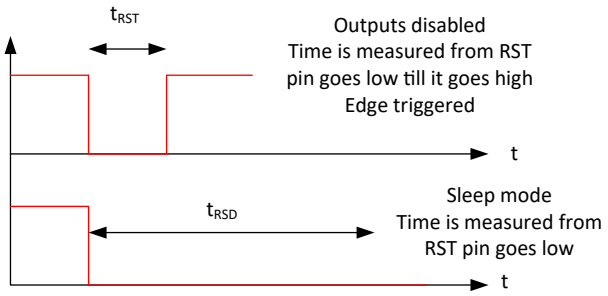

Figure 11: Sleep Mode

When RESETn is taken high to wake from sleep mode, any fault states existing before sleep was initiated are cleared, and all serial registers are set to their default power-on reset values. This takes approximately 1200 µs, after which the part may be considered operational: the serial interface may be read/written, the state of the general fault flag on the DIAG terminal may be considered valid, and the gate drive outputs are enabled (assuming V_{BB} has exceeded its undervoltage threshold, $V_{BB(UV)}$). Transient system conditions present during the wakeup process may influence the state of the general fault flag and the bit values reported in the Diagnostic and status registers when first read. For example, the first time the diagnostic and status registers are read, the POR and FF bits are set to indicate that the part has been in sleep. The VSU bit may also be set, as the voltage on VBB rises relatively slowly and may not have exceeded $V_{BB(UV)}$ prior to the fault detection circuitry becoming active.

Pulsing RESETn low for a duration equal to the reset pulse width, t_{RST}, clears any faults, sets the general fault flag on DIAG high, and re-enables any internal MOSFET that have been disabled as a result of fault conditions (Table 4) without entering sleep mode. All device registers retain their values during and after RESETn pulses of duration t_{RST}.

Current-Sense Amplifier

A programmable-gain/programmable-offset differential sense amplifier is provided to allow the use of a low value sense resistor or current shunt as a current sensing element in the low-side connection of the three-phase bridge. The input common mode range of the CSP and CSM inputs allows below ground current sensing typically required for low-side current sense in PWM control of motors, or other inductive loads, during switching transients. The output of the sense amplifier is available at the CSO output. The output can drive up to 4 V to permit maximum dynamic range with higher input voltage A-to-D converters. Maximum output voltage is clamped to $V_{CS(CL)}$ as defined in the Electrical Characteristics table.

The gain, A_V, of the sense amplifier is independently programmable and defined by the contents of the SAG[1:0], variables as:

SAG	Gain
0	10
1	20
2	30
3	40

The output offset of all three sense amplifiers, V_{OOS}, is defined by the contents of the SAO[2:0] variable as:

SAO	V_{OS}
0	200 mV
1	400 mV
2	600 mV
3	800 mV
4	1 V
5	1.2 V
6	1.4 V
7	1.6 V

Equations describing the relationship between sense amplifier gain and output offset are shown in Figure 4.

Diagnostic Monitors

Multiple diagnostic features provide three levels of fault monitoring. These include critical protection for the A89110N, monitors for operational voltages and states, and detection of power bridge and load fault conditions. The V_{BB} overvoltage and temperature warning can be masked by setting the appropriate bit in the mask registers.

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The fault status is available from two sources: the DIAG output terminal, and the diagnostic and status registers accessed through the serial interface.

Table 3: Diagnostic Functions

Name	Diagnostic	Level
POR	Internal logic supply undervoltage causing power-on reset	Chip
OT	Chip junction over temperature	Chip
SE	Serial transmission error or system error	Chip
TW	High chip junction temperature warning	Monitor
VSO	V_{BB} supply overvoltage (load dump detection)	Monitor
VSU	V_{BB} supply undervoltage	Monitor
VCP	Charge pump undervoltage	Monitor
OC	Overcurrent on sense amp	Bridge

DIAG DIAGNOSTIC OUTPUT

The DIAG terminal is a single diagnostic output signal that outputs a general fault flag.

At power-up, or after a power-on-reset, the DIAG terminal outputs a general logic-level fault flag which is active-low if a fault is present. This fault flag remains low while the fault is present or if one of the latched faults has been detected and the outputs disabled. When the general fault flag is reset, the DIAG output goes high.

CHIP-LEVEL PROTECTION

Chip-wide parameters critical for correct operation of the A89110N are monitored. These include maximum chip temperature and the serial interface transmission. These monitors are necessary to ensure that the A89110N is able to respond as specified.

CHIP FAULT STATE: OVERTEMPERATURE

If the chip temperature rises above the overtemperature threshold, T_{JF}, the overtemperature bit, OT, is set in the status register and, if FOT = 1, all half-bridge outputs are be disabled. When the temperature drops below T_{JF} by more than the hysteresis value, T_{JFHys}, the fault is reset and the half-bridge outputs are enabled but the overtemperature bit remains set in the status register until reset. If FOT = 0 fault reporting is the same but the half-bridge outputs are not disabled and action must be taken by the user to limit the power dissipation in some way to prevent overtemperature damage to the chip and unpredictable device operation. When the temperature drops below T_{JF} by more than the hysteresis value, T_{JFHys}, the general fault flag will be reset but the overtemperature bit remains in the Status 0 register until reset.

CHIP FAULT STATE: SERIAL ERROR

The data transfer into the A89110N through the serial interface is monitored for two fault conditions; transfer length and parity. A transfer length fault is detected if there are more than 16 rising edges on SCK or if STRn goes high and there have been fewer than 16 rising edges on SCK. A parity fault is detected if the total number of logic 1 states in the 16-bit transfer is an even number. In both cases, the write will be cancelled without writing data to the registers. In addition, the status register will not be reset and the FF bit and SE bit will be set to indicate a data transfer error.

If a serial error is detected and FSE = 1 then all six MOSFETs are driven low (disabled). If FSE = 0 no further action will be taken.

The A89110N can be taken out of the serial error fault state by sending a valid data transaction with the correct transfer length and parity.

Operational Monitors

Parameters related to the safe operation of the A89110N in a system are monitored. These include parameters associated with external active and passive components, power supplies, and interaction with external controllers.

The main supply voltage, V_{BB}, is monitored for overvoltage and undervoltage events.

MONITOR: TEMPERATURE WARNING

If the chip temperature rises above the temperature warning threshold, T_{JW}, the hot warning bit, TW, will be set in the status register, and if FTW = 1, all six internal MOSFETs go low. If FTW = 0, the internal MOSFETs remain active. When the temperature drops below T_{JW} by more than the hysteresis value, T_{JWHys}, the fault is reset and, if FTW = 1, the outputs are re-enabled. The TW bit remains in the Status 0 register until reset.

MONITOR: VBB SUPPLY OVERVOLTAGE AND UNDERVOLTAGE

The main supply to the A89110N on the VBB terminal, V_{BB}, is monitored to indicate if the supply voltage has exceeded its normal operating range (for example, during a load dump event). If V_{BB} rises above the V_{BB} overvoltage warning threshold, $V_{BB(OV)}$, then the VSO bit will be set in the Status 1 register and, if FVSO = 1, all six internal MOSFETs are driven low (disabled). When V_{BB} drops below the falling V_{BB} overvoltage warning threshold, $V_{BB(OV)} - V_{BB(OV)Hys}$, the fault is cleared and the internal MOSFETs are re-enabled but the VSO bit remains set until 1 is written to VSO in the Status 1 register or RESETn is pulsed low for t_{RST}. If FVSO = 0, fault reporting is the same but

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the internal MOSFETs are not disabled.

If V_{BB} falls below the V_{BB} undervoltage warning threshold, $V_{BB(UV)}$, the VSU bit will be set in the Status 1 register and, if FVSU = 1, all internal MOSFETs are driven low (disabled). When V_{BB} rises above the rising V_{BB} undervoltage threshold, $V_{BB(UV)} + V_{BB(UV)Hys}$, the fault is cleared and the internal MOSFETs is re-enabled but the VSU bit remains set until 1 is written to VSU in the Status 1 register or RESETn is pulsed low for t_{RST}. If FVSU = 0 fault reporting is the same but the internal MOSFETs is not disabled.

MONITOR: VCP UNDERVOLTAGE

The internal charge-pump regulator supplies the gate drivers. It is critical to ensure that the regulated voltage, V_{CP}, at the VCP terminal is sufficiently high before enabling any of the gate drive outputs.

If V_{CP} goes below the V_{CP} undervoltage threshold, $V_{CP(OFF)}$, the V_{CP} undervoltage bit, VCP, is set in the Status 1 register.

If a V_{CP} undervoltage state is present, all phase outputs go low. When V_{CP} rises above the rising threshold, $V_{CP(ON)}$, the fault is cleared and the gate drive outputs are re-enabled but the VCP bit remains set until 1 is written to VCP in the Status 1 register or RESETn is pulsed low for t_{RST}.

The V_{CP} undervoltage monitor circuit is active during power-up. All gate drives are low until V_{CP} is greater than $V_{CP(ON)}$.

Internal Monitors

The A89110N has internal monitors that ensure safe operation of the device. These monitors are the internal logic undervoltage monitor, internal MOSFET gate-source undervoltage monitor, and the internal MOSFET drain-source overvoltage monitor.

LOGIC UNDERVOLTAGE MONITOR

The logic I/O voltage, V_{IO}, is monitored to ensure that the logic interface voltage is high enough to permit correct operation of the logic input buffers. If V_{IO} drops below the falling undervoltage threshold, a logic undervoltage fault is detected. The regulator undervoltage bit, VLU, is set in the status register, the general fault flag is set low, and all internal MOSFETs are disabled. When V_{IO} rises above the rising threshold, the gate drive outputs revert to the commanded state and the general fault flag is reset. The VLU fault bit remains set in the status register until 1 is written to VLU in the Status 1 register or RESETn is pulsed low for t_{RST}.

VDS MONITOR

Each internal MOSFET has an associated V_{DS} overvoltage monitor. The V_{DS} overvoltage monitor activates when the related MOSFET is commanded on. If V_{DS} rises above the V_{DS} overvoltage threshold, a fault is detected. The DSO bit is set in the Status 1 register and all six internal MOSFETs are disabled. This results in the outputs going into high-impedance state. When V_{DS} falls below the overvoltage falling threshold, the fault is cleared; however, the internal MOSFETs remains latched off until the fault state is cleared by writing 1 to DSO in the Status 1 register or RESETn is pulsed low for t_{RST}.

GSU MONITOR

The gate voltage of each internal MOSFET is monitored in relation to the source using a V_{GS} monitor. The V_{GS} monitor activates when the related MOSFET is commanded on. If V_{GS} falls below the V_{GS} undervoltage threshold, a fault is detected. The GSU bit is set in the Status 1 register and all six internal MOSFETs are disabled. This results in the outputs going into high-impedance state. When V_{GS} rises above the undervoltage rising threshold, the fault is cleared; however, the internal MOSFETs remains latched off until the fault state is cleared by writing 1 to GSU in the Status 1 register or RESETn is pulsed low for t_{RST}.

Power Bridge and Load Faults

BRIDGE: OVERCURRENT DETECT

The output from the sense amplifier is fed into a comparator referenced to the overcurrent threshold voltage, V_{OCT}, to provide indication of overcurrent events. V_{OCT}, is generated by a 4-bit DAC with a resolution of 200 mV and defined by the contents of the OCT[3:0] variable. V_{OCT} is approximately defined as:

$$V_{OCT} = (n + 1) \times 200\ mV$$

where n is a positive integer defined by OCT[3:0]

Any offset programmed on SAO[2:0] is applied to both the current sense amplifier output and the V_{OCT} threshold and therefore has no effect on the overcurrent threshold, I_{OCT}. In effect, V_{CSD} is compared with V_{OCT} and the relationship between the threshold voltage and threshold current is given by:

$$I_{OCT} = V_{OCT} / (R_S \times A_V)$$

where V_{OCT} is the overcurrent threshold voltage programmed by OCT[3:0], I_{OCT} is the corresponding current value, R_S is the sense resistor value in Ω, and A_V is the sense amplifier gain defined by SAG.

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The output from the overcurrent comparator is filtered by an overcurrent qualifier circuit. This circuit uses a timer to verify that the output from the comparator indicates a valid overcurrent event. The qualifier operates in debouncing mode.

A timer is started each time a comparator output indicates an overcurrent detection. This timer is reset when the comparator changes back to indicate normal operation. If the debounce timer reaches the end of the timeout period, set by t_{OCQ}, then the overcurrent event is considered valid and the corresponding overcurrent bit (OC) will be set in the Status 0 register.

The duration of the overcurrent qualifying timer, t_{OCQ}, is determined by the contents of the TOC[4:0] variable. t_{OCQ} is approximately defined as:

$$t_{OCQ} = (n + 1) \times 500\ ns$$

where n is a positive integer defined by TOC[4:0]

The overcurrent comparator is activated when at least one MOSFET is turned on. If all the MOSFETs are off, the overcurrent comparator does not operate.

When a valid overcurrent is detected with FOC = 1, the general fault flag is set, all internal MOSFETs are driven inactive (low), and the corresponding OC bit is set. The MOSFETs remain inactive (low) until the fault state is reset by a low pulse on the RESETn input by writing 1 to OC in the Status 0 register or by a power-on reset.

If FOC = 0 and an overcurrent is detected, the general fault flag is not affected, the outputs remain active, and only the corresponding FF and OC bits are set in the Status 0 register.

FAULT ACTION

The action taken when one of the diagnostic functions indicates a fault is listed in Table 4.

When a fault is detected, a corresponding fault state is considered to exist. In some cases, the fault state only exists during the time the fault is detected. In other cases, when the fault is only detected for a short time, the fault state is latched (held in the fault state) until reset. The faults that are latched are indicated in Table 4. Latched fault states are always reset when a power-on-reset state is present by a low pulse on the RESETn input, or when 1 is written to the associated fault bit in the status register.

For most of the diagnostic functions, the action taken—when a fault state is detected—can be programmed to force the internal MOSFETs into the inactive (low) state or to leave them active. The action is selected by setting a 1 or 0 in specific stop on fault (SoF) bit associated with the diagnostic. The specific SoF bits for each diagnostic and the actions taken for each setting are listed in Table 4.

If a power-on-reset state is detected, then all MOSFETs in the bridge are held in the off state. This persists until the power-on-reset state is cleared.

Setting any of the FOT, FTW, FSE, FOC, FVSO, or FVSU bits in the Stop-on-Fault register to 0—such that the gate drive outputs are not disabled in the event of the corresponding fault being detected—means that the A89110N will not take any action to protect itself or the external bridge MOSFETs and damage may occur. Appropriate action must be taken by the external controller.

Table 4: Fault Actions

Fault Description	SoF Bit Name	Disable Outputs		Fault State Latched
		SoF Bit = 0	SoF Bit = 1	
No Fault	–	No	No	–
Power-on-Reset	–	Yes [1]	Yes [1]	No
Internal Logic Undervoltage	–	Yes [1]	Yes [1]	No
VGS Undervoltage	–	Yes [1]	Yes [1]	Yes
VDS Overvoltage	–	Yes [1]	Yes [1]	Yes
Over temperature	FOT	No [2]	Yes [1]	No
Serial Transmission Error	FSE	No	Yes [1]	No
V_{BB} Undervoltage	FVSU	No	Yes [1]	No
V_{BB} Overvoltage	FVSO	No [2]	Yes [1]	No
Temperature Warning	FTW	No	Yes [1]	No
Overcurrent	FOC	No	Yes [1]	Yes

[1] All MOSFETs off.
[2] Stated fault condition may damage the A89110N and/or bridge MOSFETs unless appropriate action taken by the external controller.

FAULT MASKS

The individual diagnostics—except power-on-reset, overtemperature, serial transmission error, and supply undervoltage—can be disabled by setting the corresponding bit in the mask registers. Power-on-reset cannot be disabled because the diagnostics and the output control depend on the logic regulator for the internal logic to operate correctly. If a bit is set to one in the mask register, then the corresponding diagnostic is completely disabled. No fault states for the disabled diagnostic is generated, no fault flags or diagnostic bits are set, and no action is taken. See Mask Register definition for bit allocation.

Care must be taken when diagnostics are disabled to avoid potentially damaging conditions.

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SERIAL INTERFACE

Serial Registers Definition [1]

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0: Config 0	0	0	0	0	0	WR	OCT3	OCT2	OCT1	OCT0	TOC4	TOC3	TOC2	TOC1	TOC0	P
							0	1	1	0	0	1	1	1	1	
1: Config 1	0	0	0	0	1	WR			CTL		SAG1	SAG0	SAO2	SAO1	SAO0	P
									0		1	0	1	1	1	
2: Config 2	0	0	0	1	0	WR						TSR1	TSR0	TSF1	TSF0	P
												0	1	0	1	
3: Stop on Fault	0	0	0	1	1	WR			FOT	FTW	FSE		FOC	FVSO	FVSU	P
									1	0	1		1	1	1	
4: Mask 0	0	0	1	0	0	WR		TW	OC	VSO	VCP		GSU	DSO	VLU	P
								0	0	0	0		0	0	0	
Status 0	0	0	1	0	1	R/ WR1C	FF	POR	SE	OT	TW	OC				P
							1	1	0	0	0	0				
Status 1	0	0	1	1	0	R/ WR1C	GSU	DSO	VLU	VSO	VSU	VCP				P
							0	0	0	0	0	0				

[1] Power-on reset value shown below each input register bit.

A three-wire synchronous serial interface, compatible with SPI, is used to control the features of the A89110N. In addition, the SDO terminal can be used during a serial transfer to provide diagnostic feedback and read back of the register contents.

The A89110N can operate without the serial interface using the default settings and the logic control inputs; however, application specific configurations and several verification functions are only possible by setting the appropriate register bits through the serial interface. If the serial interface is not used, then some diagnostics cannot be cleared without a power off-on cycle.

The serial interface timing requirements are specified in the Electrical Characteristics table, and illustrated in Figure 5. Data is received on the SDI terminal and clocked through a shift register on the rising edge of the clock signal input on the SCK terminal. STRn is normally held high, and is only brought low to initiate a serial transfer. No data is clocked through the shift register when STRn is high, allowing multiple slave units to use common SDI and SCK connections. Each slave then requires an independent STRn connection. The SDO output assumes a high-impedance state when STRn is high allowing a common data read-back connection.

After 16 data bits have been clocked into the shift register, STRn must be taken high to latch the data into the selected register. When this occurs, the internal control circuits act on the new data and the registers are reset depending on the type of transfer.

If there are more than 16 rising edges on SCK or if STRn goes high and there are fewer than 16 rising edges on SCK (either being described as a framing error), then the write is cancelled without latching data to the register. The Status register is not reset.

The first five bits, D[15:11], in a serial word are the register address bits, giving the possibility of 32 register addresses. The sixth bit, WR (D[10]), is the write/read bit. When WR is 1, the following 9 bits, D[9:1], clocked in from the SDI terminal are written to the addressed register. When WR is 0, the following 9 bits, D[9:1], clocked in from the SDI terminal are ignored, no data is written to the serial registers, and the contents of the addressed register are clocked out on the SDO terminal.

The last bit in any serial transfer, D[0], is a parity bit that is set to ensure odd parity in the complete 16-bit word. Odd parity means that the total number of 1s in any transfer should always be an odd number. This ensures that there is always at least one bit set

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		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Header	SDI	Address					CMD	Data									P
Response	SDO	Status 0						Status1/Data									P

to 1 and one bit set to 0 and allows detection of stuck-at faults on the serial input and output data connections. The parity bit is not stored but generated on each transfer.

In addition to the addressable registers, two read write 1 to clear status registers are output on SDO. For all serial transfers, the first six bits output on SDO are always the first six bits from the Status 0 register. Register data is output on the SDO terminal msb first while STRn is low and changes to the next bit on each falling edge of SCK. The first bit, which is always the FF bit from the status register, is output as soon as STRn goes low. The contents of the status registers can only be cleared when 1 is written to the corresponding bits or RESETn is pulsed low for t_{RST}.

If a framing error is detected and/or the parity of any received transfer is even rather than odd, the SE bit is set in the status register to indicate a data transfer error. Any data write is cancelled without latching data to the register and read-only registers are not reset. This fault condition can be cleared by a subsequent valid serial write or by a power-on-reset.

Configuration Registers

Three registers are used to configure the operating parameters of the A89110N.

Config 0: Overcurrent settings:

- OCT[3:0], a 4-bit integer to set the overcurrent threshold voltage, V_{OCT}, in 200 mV increments
- TOC[4:0], a 5-bit integer to set the overcurrent verification time, t_{OCQ}, in 500 ns increments

Config 1: Control logic and sense amplifier setting:

- CTL, selects 3-pin or 6-pin control
- SAG[1:0], a 2-bit integer to set sense amplifier gain between 10 and 40 V/V
- SAO[2:0], a 3-bit integer to set the sense amplifier output offset of between 0.2 V and 1.6 V

Config 2: Slew rate control:

- TSR[1:0], a 2-bit integer to set the internal MOSFET rising time in 50 ns increments
- TSF[1:0], a 2-bit integer to set the internal MOSFET falling time in 50 ns increments

Stop-On-Fault Register

One register controls whether the three-phase outputs (SA, SB, SC) are to remain enabled or be disabled in response to faults. See Diagnostics section for further details of fault actions.

One bit per fault type defines stop-on-fault behavior for OT, TW, SE, OC, VSU, and VSO diagnostics.

Status Registers

There are two status registers in addition to the addressable registers. When any register transfer takes place, the first six bits output on SDO are always the most-significant six bits of the Status 0 register, irrespective of whether the addressed register is being read or written (see Figure 5). The content of the remaining ten bits depend on the state of the WR bit input on SDI. When WR is 1, the addressed register is written and the remaining nine bits output on SDO are the nine bits of the Status 1 register followed by a parity bit. When WR is 0, the addressed register is read and the remaining ten bits are the contents of the addressed register followed by a parity bit.

The status registers are read write 1 to clear registers. For a successful write to the status registers, 1 is written to the R/W1C bit. Therefore, to clear a fault, 1 is written to both the R/W1C bit and the corresponding fault bit. If multiple faults are present, the FF bit remains set until all the faults are cleared.

The status registers provide a summary of the chip status by indicating if any diagnostic monitors have detected a fault. The most significant three bits of the Status 0 register indicate critical system faults. The remaining bits in the Status 0 register and the bits in the Status 1 register provide indicators for specific individual monitors.

The first most-significant bit in the Status 0 register is the diagnostic status flag, FF. This is high if any bits in the status registers are set. If there are no fault bits in the Status 0 or Status 1 registers, then FF is zero. When STRn goes low to start a serial write, SDO outputs the diagnostic status flag. This allows the main controller to poll the A89110N through the serial interface to determine if a fault has been detected. If no faults have been detected, then the serial transfer may be terminated without generating a serial read fault by ensuring that SCK remains high while STRn is low. When STRn goes high, the transfer is terminated and SDO goes into its high impedance state.

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The second most-significant bit in the Status 0 register is the POR bit. At power-up or after a power-on-reset, the FF bit and the POR bit are set, indicating to the external controller that a power-on-reset has taken place. All other diagnostic bits are reset and all other registers are returned to their default state. Note that a power-on-reset only occurs when the output of the internal logic regulator rises above its undervoltage threshold. Power-on-reset is not affected by the state of the V_{BB} supply.

The third bit in the Status 0 register is the SE bit, which indicates that the previous serial transfer was not completed successfully.

Of the remaining bits, the contents of OT, TW, OC, DSO, GSU, VLU, VSO, VSU, and VCP are determined by individual diagnostics. These bits along with the POR and SE bits are reset when 1 is written to the corresponding bit or when the RESET pin is pulsed low for t_{RST}. Resetting only affects latched fault bits for faults that are no longer present. For any static faults that are still present, for example overtemperature, the fault flag remains set after the reset.

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Serial Registers Reference [1]

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0: Config 0	0	0	0	0	0	WR	OCT3	OCT2	OCT1	OCT0	TOC4	TOC3	TOC2	TOC1	TOC0	P
							0	1	1	0	0	1	1	1	1	
1: Config 1	0	0	0	0	1	WR			CTL		SAG1	SAG0	SAO2	SAO1	SAO0	P
									0		1	0	1	1	1	

[1] Power-on reset value shown below each input register bit.

CONFIG 0

OCT[3:0]: Overcurrent threshold.

$$V_{OCT} = (n + 1) \times 200\ mV$$

where n is a positive integer defined by OCT[3:0],

e.g., for the power-on-reset condition.

OCT[3:0] = [0110] then V_{OCT} = 1.4 V

The range of V_{OCT} is 0.2 V to 3.2 V.

Note: At least one MOSFET must be turned on for the overcurrent comparator to operate.

TOC[4:0]: Overcurrent qualify time.

$$t_{OCQ} = (n + 1) \times 500\ ns$$

where n is a positive integer defined by TOC[4:0],

e.g., for the power-on-reset condition.

TOC[4:0] = [0 1111] then t_{OCQ} = 7.5 µs

The range of t_{OCQ} is 0.5 µs to 16 µs.

P: Parity bit. Ensures an odd number of 1s in any serial transfer.

CONFIG 1

CTL: Input control bit.

CTL	Control	Default
0	Independent control of MOSFETs	D
1	Each phase is controlled by Hx pin	

SAG[1:0]: Sense amplifier 1 gain.

SAG	Gain	Default
0	10	
1	20	
2	30	D
3	40	

where SAG are positive integers defined by SAG[1:0].

SAO[2:0]: Sense amplifier offset.

SAO	Offset	Default
0	200 mv	
1	400 mV	
2	600 mV	
3	800 mV	
4	1 V	
5	1.2 V	
6	1.4 V	
7	1.6 V	D

where SAO is a positive integer defined by SAO[2:0]

P: Parity bit. Ensures an odd number of 1s in any serial transfer.

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Serial Registers Reference (continued) [1]

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2: Config 2	0	0	0	1	0	WR						TSR1	TSR0	TSF1	TSF0	P
												0	1	0	1	
3: Stop on Fault	0	0	0	1	1	WR			FOT	FTW	FSE		FOC	FVSO	FVSU	P
									1	0	1		1	1	1	

[1] Power-on reset value shown below each input register bit.

CONFIG 2

TSR[1:0]: Slew rate rising time.

TSR	Slew Rate Rising	Default
0	50	
1	90	D
2	137	
3	177	

TSF[1:0]: Slew rate falling time.

TSF	Slew Rate Rising	Default
0	50	
1	90	D
2	137	
3	177	

P: Parity bit. Ensures an odd number of 1s in any serial transfer.

STOP ON FAULT

FOT: Overtemperature

FTW: Temperature Warning

FSE: Serial error

FOC: Overcurrent

FVSO: V_{BB} Overvoltage

FVSU: V_{BB} Undervoltage

For Stop on Fault Register

xxx	Gate Drive Output	Default
0	No stop on fail. Report fault.	
1	Stop on fail. Report fault.	D

See Table 3 for details of each diagnostic.

P: Parity bit. Ensures an odd number of 1s in any serial transfer.

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Serial Registers Reference (continued) [1]

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4: Mask 0	0	0	1	0	0	WR		TW	OC	VSO	VCP		GSU	DSO	VLU	P
								0	0	0	0		0	0	0	
Status 0	0	0	1	0	1	R/ WR1C	FF	POR	SE	OT	TW	OC				P
							1	1	0	0	0	0				
Status 1	0	0	1	1	0	R/ WR1C	GSU	DSO	VLU	VSO	VSU	VCP				P
							0	0	0	0	0	0				

[1] Power-on reset value shown below each input register bit.

MASK 0

TW: Temperature warning

OC: Overcurrent

VSO: VBB overvoltage

VCP: Charge pump undervoltage

GSU: Gate-source undervoltage

DSO: Drain-source overvoltage

VLU: Logic regulator undervoltage

P: Parity bit. Ensures an odd number of 1s in any serial transfer.

STATUS 0

FF: Status register flag

POR: Power-on-reset

SE: Serial Error

OT: Overtemperature

TW: High temperature warning

OC: Overcurrent

STATUS 1

GSU: Gate-source undervoltage

DSO: Drain-source overvoltage

VLU: Logic regulator undervoltage

VSO: VBB overvoltage

VSU: VBB undervoltage

VCP: Charge pump undervoltage

xxx	Status
0	No fault detected
1	Fault detected

P: Parity bit. Ensures an odd number of 1s in any serial transfer.

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APPLICATION INFORMATION

Current-Sense Amplifier Configuration

Amplifier gain, A_V, and output offset zero point voltage, V_{OOS}, may be set to a range of values by the SAG[1:0] and SAO[2:0] variables respectively as defined in the Current-Sense Amplifiers section above. It is important that both values are selected to ensure the absolute voltage at the CSO output, V_{CSO}, remains within the amplifier's dynamic range, $V_{CS(OUT)}$, and the dynamic range of any downstream signal processing circuitry. Allowance must be made for both positive and negative current flows within the sense resistor.

With reference to Figure 4, the relationship between bridge current (I_{BRG}), sense resistor value (R_S), and differential amplifier input voltage (V_{ID}) is given by:

$$V_{ID} = V_{CSP} - V_{CSM} = I_{PH} \times R_S$$

The current-sense amplifier's output voltage on CSO with respect to the programmed value of output offset is:

$$V_{CSO} = [(V_{CSP} - V_{CSM}) \times A_V] + V_{OOS}$$

If, for example, the following parameter values are assumed:

$R_S = 20\ m\Omega$
$I_{PH} = -2.5\ A$ to $+3.5\ A$
$A_V = 20$ (SAG[2:0] = 0b01)
$V_{OOS} = 1.6\ V$ (SAO[2:0] = 0b1111)

V_{ID} ranges between –50 mV and +70 mV and V_{CSO} between 0.6 V and 3 V. V_{CSO} remains within the amplifier dynamic range, $V_{CS(OUT)}$, of 0.45 V to 4 V. However, if A_V is increased to 40, V_{CSO} attempts to drive to –0.4 V and 4.4 V, the amplifier dynamic range limits are not complied with, and the amplifier output saturates at its negative limit. This situation could be remedied by reducing A_V to 20 or reducing R_S to 10 mΩ (0.6 V < V_{CSO} < 3 V).

Current-Sense Amplifier Output Signals

As defined in Figure 4, the current-sense amplifier output signals on the CSO pin is internally referenced to the output offset. The sense-amplifier output voltage and the output offset voltage may be measured consecutively with respect to ground, and the values subtracted to give the required output signal voltages as:

$$V_{CSD} = V_{CSO} - V_{OOS}.$$

The input offset voltage, V_{IOS}, and the associated drift, ΔV_{IOS}, multiplied by the selected amplifier gain, A_V, represent the offset and offset drift limits that apply to V_{CSD}. The pedestal voltage error limits, E_{VO}, apply directly to V_{OOS}. E_{VO} does not affect current-sense output accuracy.

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INPUT/OUTPUT STRUCTURES

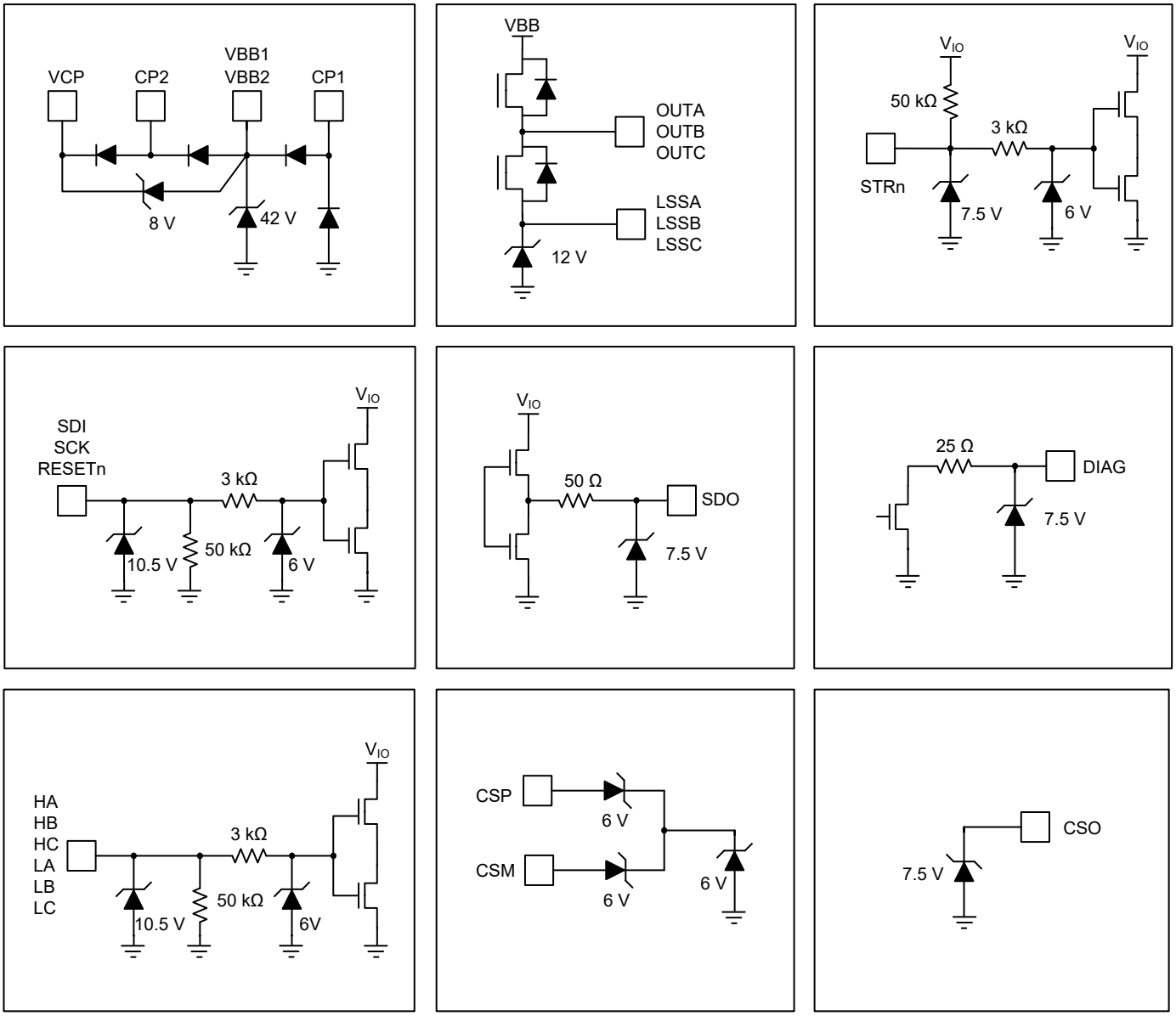

Figure 12: Input/Output Structures

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LAYOUT RECOMMENDATIONS

Careful consideration must be given to PCB layout when designing high-frequency, fast-switching, high-current circuits.

- The exposed thermal pad should be connected to the GND terminal.
- Minimize stray inductance by using short, wide copper tracks at the source terminals of all power MOSFETs. This includes load lead connections and the input power bus. This minimizes voltages induced by fast switching of large load currents.
- Consider the addition of a small (100 pF) ceramic decoupling capacitor between the phase outputs and ground to limit fast transient voltage spikes caused by track inductance.
- Keep the gate discharge return connections OUTx and LSSx as short as possible. Any inductance on these tracks causes negative transitions on the corresponding A89110N terminals, which may exceed the absolute maximum ratings. If this is likely, consider the use of clamping diodes to limit the negative excursion on these terminals with respect to the GND terminal.
- Supply decoupling, typically a 10 nF ceramic capacitor for each VBB terminal, should be connected between VBB and GND as close to the A89110N terminals as possible.
- LSS tracks must be as short as possible to reduce track inductance. The three LSS pins must be tied together with short tracks.
- A low-cost diode can be placed in the connection to VBB to provide reverse-battery protection. In reverse-battery conditions, the additional diode in the VBB connection prevents damage to the A89110N.

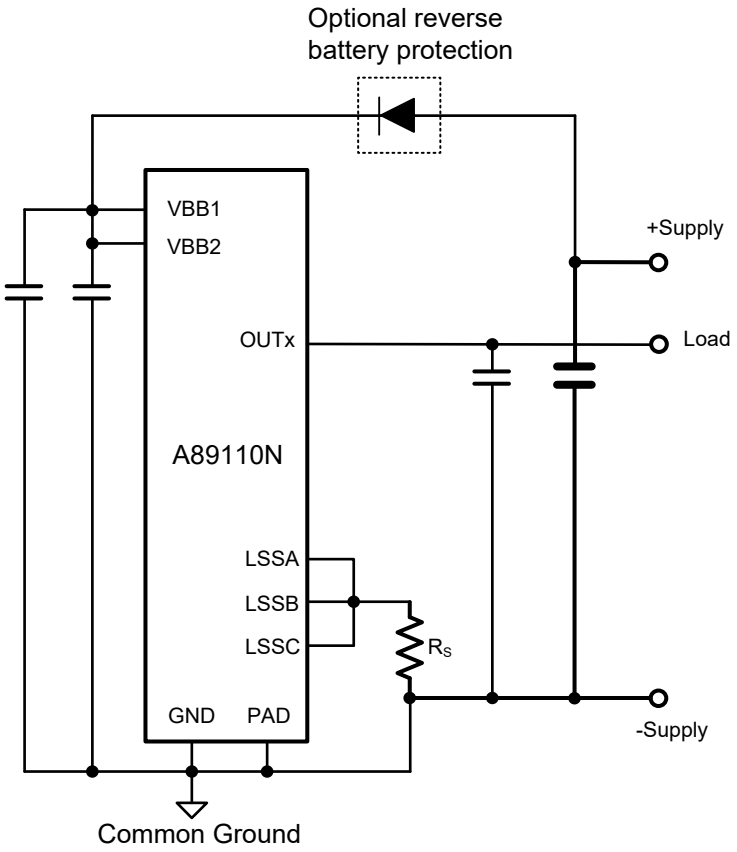

Figure 13: Layout Recommendations

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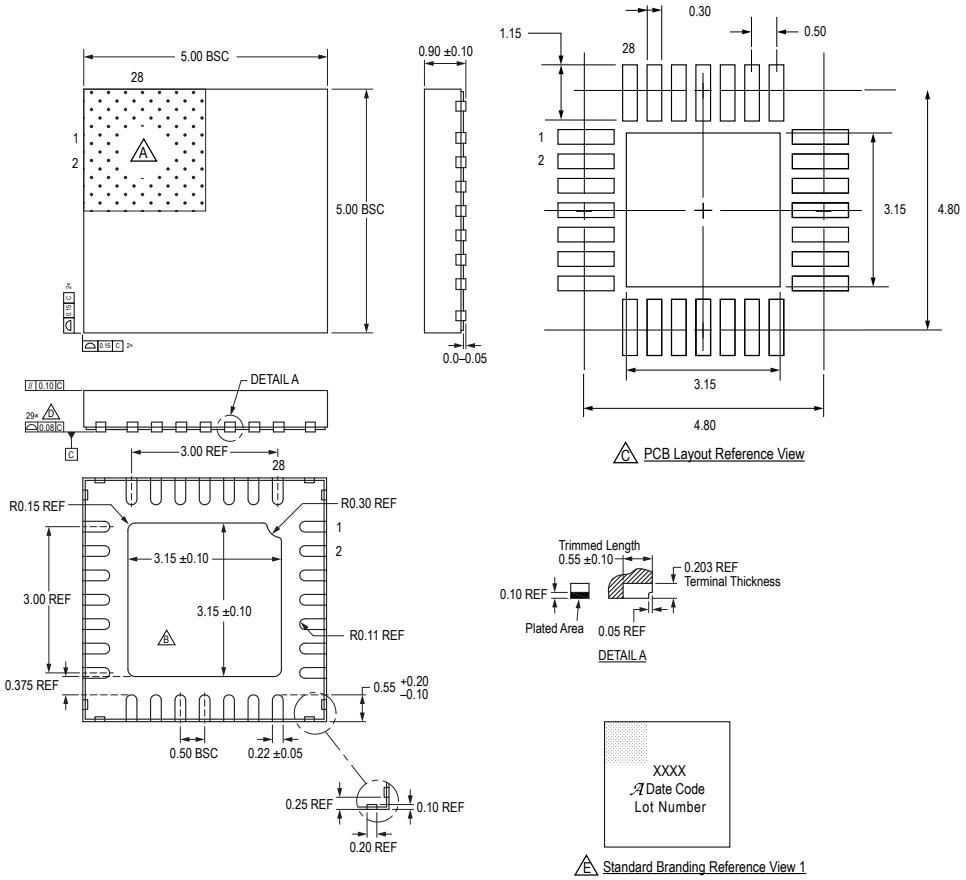
PACKAGE OUTLINE DRAWING

For Reference Only – Not For Tooling Use

(Reference Allegro DWG-0000378, Rev. 3 or JEDEC MO-220VHHD-1)
NOT TO SCALE
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P500X500X100-29V1M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Branding scale and appearance at supplier discretion

Figure 14: Package ET, 28-Contact QFN with Exposed Pad and Wettable Flank

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REVISION HISTORY

Number	Date	Description
–	May 26, 2026	Preliminary
1	October 5, 2026	Initial release to Allegro website

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