A89120

58 V Three-Phase MOSFET Driver

FEATURES AND BENEFITS

- 5.5 to 58 V supply voltage operating range
- 85 V part variant available (A89121)
- 3.3 V or 5 V low quiescent current (I_Q; typically, 8.5 µA) low-dropout (LDO) regulator, active during sleep mode
- Three-phase bridge MOSFET driver with bootstrap gate drive for N-channel MOSFET bridge
- Charge pump for low-supply-voltage operation.
- Cross-conduction protection with adjustable dead time
- Bridge control by direct logic inputs for maximum flexibility

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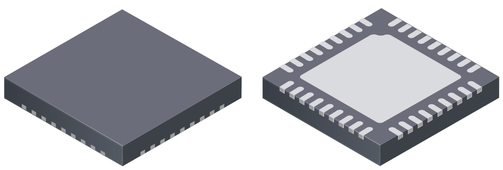
PACKAGE

Not to scale



36-contact QFN with exposed thermal pad (suffix EV)

DESCRIPTION

The A89120 is designed to satisfy the demanding power requirements of brushless DC (BLDC) power tools from 12 V to 24 V with ultra-low current consumption.

The A89120 is optimized for pulse-width-modulated (PWM) current control of three-phase BLDC motors and is capable of high-current, robust gate driving for six external N-channel power MOSFETs. An internal charge pump ensures full gate drive capability over the full supply-voltage range, from 5.5 V to 58 V. A bootstrap capacitor is used to generate a supply

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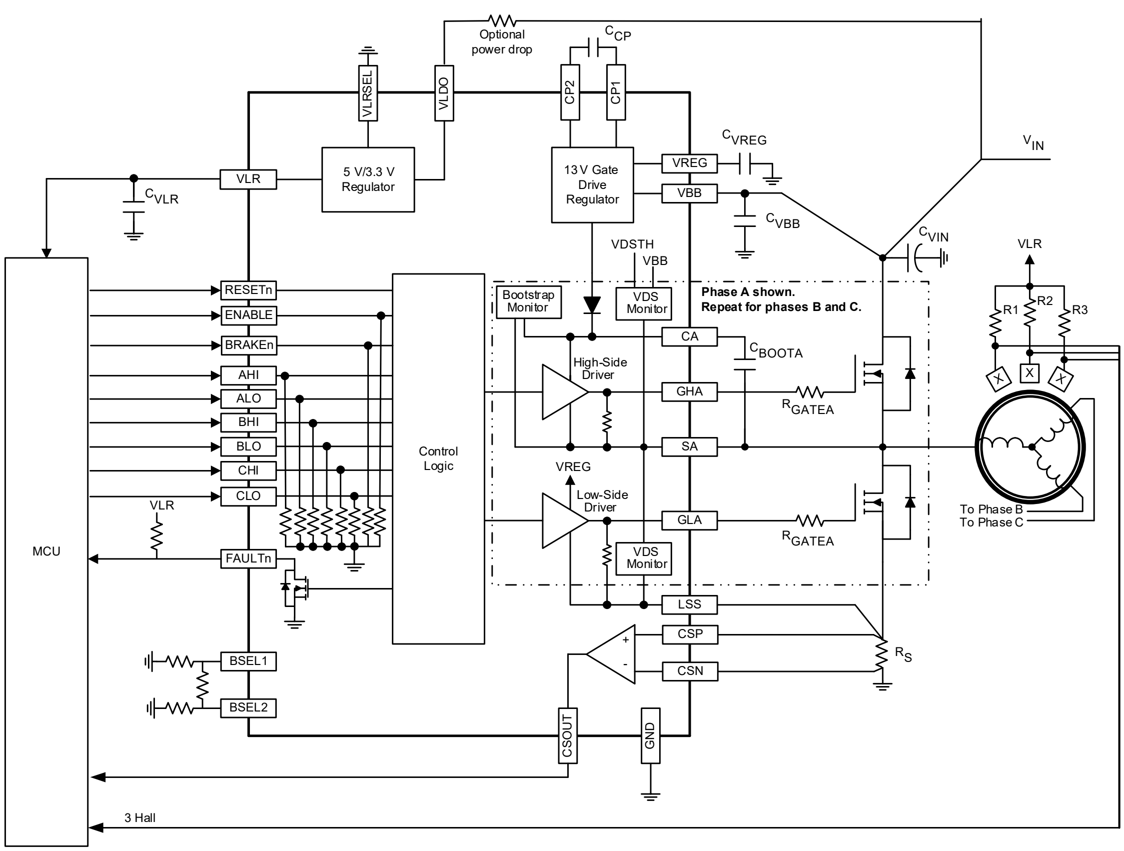
TYPICAL APPLICATIONS

- Cordless power tools
- Optimized for 12 V to 24 V-battery BLDC motor modules
- 24 V e-bikes



Block Diagram

FEATURES AND BENEFITS (continued)

- Differential current-sense amplifier
  - □ Adjustable gain and offset
  - □ 1 microsecond settling time
- Drain-to-source voltage (V_{DS}), undervoltage lockout (UVLO), and thermal shutdown diagnostic
- Latched thermal shutdown (TSD) with fault output

DESCRIPTION (continued)

voltage greater than the source voltage of the high-side MOSFET. Internal circuit protection includes latched thermal shutdown, crossover current protection, undervoltage lockout, and short-circuit protection. Full control is provided over all six power MOSFETs in the three-phase bridge, allowing motors to be driven with block commutation or sinusoidal excitation.

Bridge current can be measured using an integrated current-sense amplifier with a below-ground common-mode range that allows it to be used in low-side current-sense applications. Gain and offset are defined by external resistors.

The device includes an efficient low-dropout (LDO) regulator to provide 3.3 V or 5 V to external circuitry.

The A89120 is supplied in a leadless 6 mm × 6 mm × 0.9 mm, 36-pin quad-flat no-lead (QFN) package (suffix EV) with exposed power tab for enhanced thermal performance. The package is lead (Pb) free, with 100% matte-tin leadframe plating.

SELECTION GUIDE

Part Number	Rated Voltage	Packing	Package
A89120GEVSR	58	1500 pieces per 13-in. reel	6 mm × 6 mm; 0.9 mm nominal height 36-lead QFN with exposed thermal pad

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS: With respect to GND

Characteristic	Symbol	Notes	Rating	Unit
Load Supply Voltage	V_{VBBMAX}		–0.3 to 60	V
Analog Output	V_{VLR}		–0.3 to 6	V
Terminal VREG	V_{VREG}		–0.3 to 18	V
Terminal CP1	V_{CP1}		–0.3 to 16	V
Terminal CP2	V_{CP2}		$(V_{CP1}$ – 0.3) to $(V_{VREG}$ + 0.3)	V
Logic Inputs	V_{IN}		–0.3 to 6	V
FAULTn Output	V_{FAULTn}		–0.3 to 6	V
Sense Amplifier Inputs	V_{CSP}/V_{CSN}		–4 to 6.5	V
Sense Amplifier Outputs	V_{CSO}		–0.3 to 6.5	V
Terminals CA, CB, CC	V_{CX}		–0.3 to $(V_{VREG} + V_{VBBMAX})$	V
Terminals GHA, GHB, GHC	V_{GHX}		$(V_C$ – 16) to $(V_C$ +.3)	V
		Transient [1]	–18 to $(V_C$ +.3)	V
Terminals SA, SB, SC	V_{SX}		$(V_C$ – 16) to V_{VBBMAX}	V
		Transient [1]	–18 to $(V_C$ +.3)	V
Terminals GLA, GLB, GLC	V_{GLX}		$(V_{VREG}$ – 16) to 18	V
		Transient [1]	–8 to 18	V
Terminal LSS	V_{LSS}		$(V_{VREG}$ – 16) to 18	V
		Transient [1]	–8 to 18	V
Terminal VLDO	V_{LDO}		–0.3 to V_{VBBMAX}	V
Terminal VLRSEL	V_{VLRSEL}		–0.3 to 6	V
Maximum Continuous Junction Temperature	T_J		≤150	°C
Storage Temperature Range	T_s		–55 to 150	°C
Operating Temperature Range	T_A	Range G	–40 to 125	°C

[1] Duration less than 1 µs

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	EV package, 4-layer PCB based on JEDEC standard	27	°C/W

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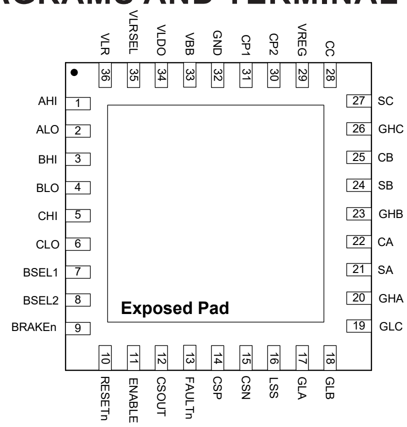
PINOUT DIAGRAMS AND TERMINAL LIST TABLE



EV Package Pinouts

Terminal List Table

Number	Name	Function
–	PAD	Thermal pad; connect to GND.
1	AHI	Logic input: Direct control for high-side output A. Refer to logic decode table in Functional Description.
2	ALO	Logic input: Direct control for low-side output A. Refer to logic decode table in Functional Description.
3	BHI	Logic input: Direct control for high-side output B. Refer to logic decode table in Functional Description.
4	BLO	Logic input: Direct control for low-side output B. Refer to logic decode table in Functional Description.
5	CHI	Logic input: Direct control for high-side output C. Refer to logic decode table in Functional Description.
6	CLO	Logic input: Direct control for low-side output C. Refer to logic decode table in Functional Description.
7	BSEL1	Used in association with BSEL2 by detection circuitry to determine the values for the V_{DS} threshold, offset, and gain of the current-sense amplifier.
8	BSEL2	Used in association with BSEL1 by the detection circuitry to determine the values for the V_{DS} threshold, offset, and gain of current-sense amplifier.
9	BRAKEn	Active low braking input; turns all low sides ON.
10	RESETn	Logic input to assert sleep mode.
11	ENABLE	Active high logic input, enables output drivers.
12	CSOUT	Current-sense amplifier output.
13	FAULTn	Active low fault output. Open drain; requires external pull up resistor.
14	CSP	Current-sense amplifier input.
15	CSN	Current-sense amplifier input.
16	LSS	Low-side source: low-side return path for discharge of the capacitance of the MOSFET gates, connected to the common sources of the low-side external MOSFETs through a low-impedance PCB trace.
17	GLA	Gate drive for external low-side MOSFET connected to phase A.
18	GLB	Gate drive for external low-side MOSFET connected to phase B
19	GLC	Gate drive for external low-side MOSFET connected to phase C.

Number	Name	Function
20	GHA	Gate drive for external high-side MOSFET connected to phase A.
21	SA	Negative supply for high-side gate drive. Connect to motor for phase A.
22	CA	Positive supply for high-side drive. Connect ceramic capacitor from CA to SA.
23	GHB	Gate drive for external high-side MOSFET connected to phase B.
24	SB	Negative supply for high-side gate drive. Connect to motor for phase B.
25	CB	Positive supply for high-side drive. Connect ceramic capacitor from CB to SB.
26	GHC	Gate drive for external high-side MOSFET connected to phase C.
27	SC	Negative supply for high-side gate drive. Connect to motor for phase C.
28	CC	Positive supply for high-side drive. Connect ceramic capacitor from CC to SC.
29	VREG	13 V gate-drive supply regulator output. when the motor phase outputs are driven low, the high-side bootstrap capacitors are charged from VREG. VREG also directly powers low-side gate drive circuits. A sufficiently large storage capacitor must be connected between this terminal and the GND terminal to provide the transient charging current.
30	CP2	Charge-pump capacitor terminal.
31	CP1	Charge-pump capacitor terminal.
32	GND	Ground.
33	VBB	Supply voltage input: Connect 0.22 µF (CVB2) X5R or X7R ceramic capacitor locally between VBB and GND, as close to the IC as practical.
34	VLDO	LDO supply input.
35	VLRSEL	Select VLR regulator output: for 3.3 V, connect to GND; for 5 V, connect to VLR.
36	VLR	5 V or 3.3 V/30 mA regulator output used to power external microprocessor. Stabilize with typical 4.7 µF X5R or X7R ceramic capacitor.

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CHARACTERISTIC PERFORMANCE

ELECTRICAL CHARACTERISTICS: Valid for T_A = –40°C to 125°C V_{VBB} = 5.5 V to 58 V (unless noted otherwise)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY AND REFERENCE						
Operating Voltage Range	V_{VBB}	Operating, outputs active	5.5	–	58	V
Motor Supply Current [2]	I_{VBB}	V_{VBB} = 24 V, f_{PWM} = 20 kHz, C_{LOAD} = 10 nF	–	24	28	mA
		V_{VBB} = 24 V, outputs disabled	–	7.5	10	mA
LDO Ground Current During SLEEP Mode [2]	I_{SLEEP}	V_{VBB} = 24 V, I_{VLR} = 100 µA, V_{RESETn} < 0.3 V, T_J = 25°C [1]	–	8.5	11	µA
		V_{VBB} = 24 V, I_{VLR} = 100 µA, V_{RESETn} < 0.3 V, –40°C ≤ T_J ≤ 125°C	–	–	15	µA
VREG Output Voltage	V_{VREG}	V_{VBB} > 6.5 V, 0 mA ≤ I_{VREG} ≤ 33 mA	9	13	14	V
		6 V < V_{VBB} ≤ 6.5 V, 0 mA ≤ I_{VREG} ≤ 20 mA	9	–	14	V
		6 V < V_{VBB} ≤ 6.5 V, 0 mA ≤ I_{VREG} ≤ 15 mA	9	–	14	V
VREG Output Capacitance [1]	C_{VREG}		2	–	22	µF
VLR Output Capacitance [1]	C_{VLR}		2.3	4.7	7	µF
Output Voltage	V_{VLR}	5.5 V ≤ V_{VBB} ≤ 58 V, V_{VLRSEL} = GND, 0 mA ≤ I_{OUT} ≤ 40 mA	3.135	3.3	3.465	V
		6.5 V ≤ V_{VBB} ≤ 58 V, V_{VLRSEL} = V_{VLR}, 0 mA ≤ I_{OUT} ≤ 40 mA	4.75	5	5.25	V
Output Overcurrent Limit [2]	I_{OCL}	V_{VLR} = 0 V	60	–	120	mA

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GATE DRIVE						
Bootstrap Diode Forward Voltage	V_{fBOOT}	I_D = 1 mA	0.4	0.7	1	V
		I_D = 100 mA	1.5	2.2	3.3	V
Bootstrap Diode Resistance	R_D	$R_{D(100mA)} = (V_{fBOOT(150\ mA)} - V_{fBOOT(50mA)})/100$ mA	6	11	25	Ω
Bootstrap Diode Current Limit [2]	I_{DBOOT}		250	500	750	mA
High-Side Gate Drive Output	$V_{GSH(H)}$	Bootstrap fully charged, C_{LOAD} = 10 nF	V_{CX} – 0.2	–	–	V
	$V_{GSH(L)}$	I_{GATE} < 10 μA	–	–	V_{SX} + 0.3	V
Low-Side Gate Drive Output	$V_{GSL(H)}$	V_{VREG} = 13 V, C_{LOAD} = 10 nF	V_{VREG} – 0.2	–	–	V
	$V_{GSL(L)}$	I_{GATE} < 10 μA	–	–	0.3	V
Gate Drive Pull-Up Resistance	$R_{GATE(ON)UP}$	I_{GHX} = –150 mA, T_J = 25°C [1]	–	6.8	–	Ω
		I_{GHX} = –150 mA, T_J = 125°C	5.5	9.75	14.5	Ω
Pull-Up Peak Source Current [1][2]	I_{PUPK}		–	0.9	–	A
Gate Drive Pull-Down Resistance	$R_{GATE(ON)DOWN}$	I_{GLX} = 150 mA, T_J = 25°C [1]	–	1.8	–	Ω
		I_{GLX} = 150 mA, T_J = 125°C	2	3	4	Ω
Pull-Down Peak Source Current [1][2]	I_{PDPK}		–	1.75	–	A
Output Switching Time	t_{rGX}	2 V to 10 V, V_{VREG} = 13 V, C_{LOAD} = 10 nF,	–	137	–	ns
	t_{fGX}	10 V to 2 V, V_{VREG} = 13 V, C_{LOAD} = 10 nF	–	62	–	ns
Turn-Off Propagation Delay	$t_{P(OFF)}$	Input change to unloaded gate-output change	–	50	–	ns
Turn-On Propagation Delay	$t_{P(On)}$	Input change to unloaded gate-output change	–	50	–	ns
Propagation Delay Matching (On to Off)	t_{OO}		–	–	20	ns
GHx Passive Pull-Down	R_{GHPD}	$V_{GHx} - V_{Sx}$ < 0.3 V	–	950	–	kΩ
GLx Passive Pull-Down	R_{GLPD}	$V_{GLx} - V_{LSS}$ < 0.3 V	–	950	–	kΩ
Dead Time	t_{DEAD}	BSEL1 = 100 ns	40	120	200	ns
		BSEL1 = 500 ns	325	500	675	ns
		BSEL1 = 1000 ns	675	1000	1325	ns
		BSEL1 = 1500 ns	1050	1500	1950	ns

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
PROTECTION						
Thermal Shutdown Temperature [1]	T_{TSD}	T_J increasing	–	170	–	ºC
Thermal Shutdown Hysteresis [1]	$T_{TSD(HYS)}$		–	15	–	ºC
VREG Undervoltage	$V_{VREG(UV)}$	V_{VREG} rising	7.4	7.95	8.5	V
VREG Undervoltage Hysteresis	$V_{VREG(HYS)}$		–	770	–	mV
Bootstrap Undervoltage	$V_{BOOT(UV)}$	V_{BOOT} rising, $V_C – V_S$	6.2	7	7.8	V
Bootstrap Hysteresis	$V_{BOOT(HYS)}$		–	1	–	V
VLR Undervoltage Threshold	$V_{VLRUV(3p3)}$	Voltage falling, V_{VLRSEL} = GND	2.4	2.7	2.85	V
	$V_{VLRUV(5)}$	Voltage falling, V_{VLRSEL} = V_{VLR}	3.87	4.1	4.33	V
VLR Undervoltage Hysteresis	$V_{VLR(HYS)}$		–	100	–	mV
VDS Threshold Range	V_{DSTH}	Programmable through BSEL1, BSEL2	0.3	–	1.2	V
VDS Fault Blank Time	t_{BL}		1.3	2	3	µs
VDS Short-to-Ground Threshold Offset	V_{STGO}	V_{DSTH} ≥ 900 mV	–200	±100	200	mV
		V_{DSTH} < 900 mV	–150	±50	150	mV
VDS Short-to-Battery Threshold Offset	V_{STBO}	V_{DSTH} ≥ 900 mV	–200	±100	200	mV
		V_{DSTH} < 900 mV	–150	±50	150	mV
LOGIC I/O						
Logic Input Voltage	$V_{IN(H)}$	AHI, ALO, BHI, BLO, CHI, CLO, ENABLE, RESETn, BRAKEn	2	–	–	V
	$V_{IN(L)}$		–	–	0.8	V
Input Hysteresis	$V_{IN(HYS)}$		–	500	–	mV
Logic Input Current [2]	$I_{IN(H)}$	V_{IN} = 5 V	–	100	–	µA
	$I_{IN(L)}$	V_{IN} = 0 V	–1	0	1	µA
Logic Input Pull-Down Resistor	R_{LPD}	AHI, ALO, BHI, BLO, CHI, CLO, ENABLE, BRAKEn	–	50	–	kΩ
FAULTn Pull-Down Voltage	V_{FAULT}	Fault present; I_{SINK} = 1 mA	–	–	0.3	V
Reset Pulse Width	t_{RST}		0.2	–	4.5	µs
Reset Shutdown Time	t_{SLEEP}	RESETn high-to-low transition	10	–	–	µs
Input Pin Glitch Reject [1]	t_{GLITCH}	ENABLE, BRAKEn	200	–	500	ns
Power-Up Time from Sleep	t_{PU}	RESETn low-to-high, C_{VREG} = 22 µF	–	–	3	ms

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Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
CURRENT-SENSE AMPLIFIER						
Input Offset Voltage [1]	V_{IOS}		–	±10	–	mV
Input Offset Voltage Drift [1]	dV_{IOS}		–	±4	–	µV/°C
Input Bias Current [2]	I_{BIAS}	V_{ID} = 0, V_{CM} in range	–50	–	5	µA
Input Offset Current [2]	I_{OS}	V_{ID} = 0, V_{CM} in range	–1.5	–	1.5	µA
Input Common-Mode Range (DC)	V_{CM}	V_{ID} = 0	–1.3	–	2	V
Gain	A_V	Programmable through BSEL1, BSEL2	10	–	40	V/V
Gain Error	E_A	V_{CM} in range	–1.6	–	1.6	%
Pedestal Voltage	V_{OOS}	Programmable through BSEL1, BSEL2	0.2	–	1.6	V
Pedestal Voltage Error	E_{VO}	V_{CM} in range, V_{OOS} > 0	–10	±2	10	%
Small Signal –3 dB Bandwidth Gain = 20 [1]	BW	V_{IN} = 10 mV_{PP}	2	–	–	MHz
Output Settling Time (to within 40 mV) [1]	t_{SET}	V_{CSO} = 1 V_{PP} square wave, gain = 20, C_{OUT} = 50 pF	0.2	–	1	µs
Output Dynamic Range	V_{CSOUT}	–100 µA < I_{CSO} < 100 µA	0.45	–	4.8	V
Output Voltage Clamp [1]	V_{CSC}	I_{CSO} = –2mA	3.7	4.2	5.1	V
Output Current Sink [2]	$I_{CS(SINK)}$	V_{ID} = 0 V, V_{CSO} = 0.8 V, gain = 20	230	–	490	µA
Output Current Sink (Boosted) [1][2]	$I_{CS(SINKB)}$	V_{OOS} = 0.8 V, V_{ID} = –50 mV, V_{CSO} = 1.5 V, gain = 20	1.8	–	4.4	mA
Output Current Source [2]	$I_{CS(SOURCE)}$	V_{OOS} = 0.8 V, V_{ID} = 200 mV, gain = 20, V_{CSO} = 1.5 V	–4.5	–	–1.7	mA
VBB Supply-Ripple Rejection Ratio [1]	$PSRR_{AC}$	V_{ID} = 0 V, 100 kHz, gain = 20	–	65	–	dB
	$PSRR_{DC}$	V_{CSP} = V_{CSM} = 0 V, DC, gain = 20	77	–	–	dB
DC Common-Mode Rejection Ratio [1]	$CMRR_{DC}$	V_{CM} step from 0 V to 200 mV, gain = 20	52	100	–	dB
AC Common-Mode Rejection Ratio [1]	$CMRR_{AC}$	V_{CM} = 200 mV_{PP}, 100 kHz, gain = 20	–	62	–	dB
		V_{CM} = 200 mV_{PP}, 1 MHz, gain = 20	–	43	–	dB
		V_{CM} = 200 mV_{PP}, 10 MHz, gain = 20	–	25	–	dB
Common-Mode Recovery Time (to within 100 mV) [1]	$t_{CM(REC)}$	V_{CM} step from –1.5 V to 1 V, gain = 20, C_{OUT} = 50 pF	–	< 2.1	–	µs
Output Slew Rate 10% to 90% [1]	SR	V_{ID} step from 0 V to 175 mV, gain = 20, C_{OUT} = 50pF	1.8	–	7.5	V/µs
Input Overload Recovery (to within 40 mV) [1]	$t_{ID(REC)}$	V_{ID} step from 250 mV to 0 V, gain = 20, C_{OUT} = 50 pF	0.4	–	2.1	µs

[1] Not production tested; assured by design and characterization.
[2] For input and output current specifications, negative current is defined as coming out of (sourcing from) the specified device terminal.

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FUNCTIONAL DESCRIPTION

Basic Operation

The A89120 provides six high-current gate drives capable of driving a wide range of N-channel power MOSFETs. The gate drives are configured as three half bridges, each with a high-side drive and a low-side drive. Direct control pins enable independent operation of the three half bridges in BLDC motors or permanent-magnet synchronous motors (PMSMs). Independent control over each MOSFET allows each driver to be driven with an independent PWM signal for full sinusoidal excitation.

The VBB input terminal powers an internal charge pump that generates a regulated supply (V_{VREG}) to provide all the current necessary to drive the low-side gate drive outputs directly plus the high-side drive via the bootstrap capacitors. This architecture ensures that all external MOSFETs are fully enhanced at battery voltages down to 5.5 V.

The A89120 is designed for use in battery-operated equipment where low-current operation is critical. An internal 3.3 V or 5 V LDO regulator provides the supply for an external microcontroller and/or external circuitry. A low-power sleep and standby mode allows the A89120, the power bridge, and the load to remain connected to a battery supply without the need for an additional supply switch.

The A89120 includes also a programmable amplifier designed for low-side current sensing in the presence of high current and voltage transients.

VLR Regulator

An integrated regulator controller is provided for external logic level circuits such as a microcontroller or an interface circuit. The regulator includes current limit, undervoltage, and short protection.

An overcurrent circuit limits the output of the regulator in the event of an excessively high load demand (load current > I_{OCL}). If the output voltage falls below the regulator undervoltage threshold (V_{VLRUV}), a fault state is flagged on the FAULTn output to provide an external warning, and the gate drive outputs are disabled.

Sleep Mode

Input terminal RESETn controls the low-power mode of operation of the A89120.

Low-power sleep mode is activated when RESETn is held low for longer than t_{SLEEP}. Sleep mode disables all the internal circuitry, excluding the VLR regulator.

In sleep mode, the ground current consumption from VBB is less than I_{SLEEP} (typically 8.5 µA) when the external load is less than 100 µA.

Gate Drivers

The A89120 is designed to drive external, low on-resistance, power N-channel MOSFETs. It supplies the large transient currents necessary to quickly charge and discharge the external MOSFET gate capacitance in order to reduce dissipation in the external MOSFET during switching. The charge current for the low-side drives and the main recharge current for the bootstrap capacitors are provided by the capacitor on the VREG terminal. The charge current for the high-side drives is provided by the bootstrap capacitors connected between the Cx and Sx terminals, one for each phase.

Bootstrap Supply

When the high-side drivers are active, the reference voltage (Sx) for the driver rises close to the bridge supply voltage. At that time, to ensure that the driver remains active, the supply to the driver must exceed the bridge supply voltage. This temporary high-side supply is provided by bootstrap capacitors, one for each high-side driver. These three bootstrap capacitors are connected between the bootstrap supply terminals, CA, CB, CC, and the corresponding high-side reference terminal, SA, SB, SC.

The bootstrap capacitors are independently charged to approximately V_{VREG} when the associated reference Sx terminal is low. When the output swings high, the voltage on the bootstrap supply terminal rises with the output to provide the boosted gate voltage needed for the high-side N-channel power MOSFETs.

It is necessary to charge the bootstrap capacitors by turning on the low-side drive (GLx) prior to attempting to turn on the complementary high-side (GHx). To protect the external MOSFETs from insufficient gate drive, the bootstrap capacitor voltage is monitored. Each bootstrap undervoltage monitor circuit prevents the high side from turning on if the bootstrap capacitor is not changed.

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VREG Charge-Pump Regulator

The gate drivers are powered by an internal voltage regulator that generates a voltage, V_{VREG}, at the VREG terminal. It limits the supply voltage to the drivers and, therefore, the maximum gate voltage. At low supply voltage, the regulated supply is maintained by a charge-pump boost converter. A sufficiently large storage capacitor must be connected between this terminal and the GND terminal to provide the transient charging current.

The decoupling capacitance is based on the bootstrap capacitor, which is dependent on the MOSFET selection. For details about the correct sizing of the VREG and bootstrap capacitors, refer to the Application Information section.

The regulated supply is maintained by a charge-pump buck-boost converter with a switching frequency of 62.5 kHz. The pump capacitor, C_{CP}, should have a nominal value of 0.47 µF and should be connected between the CP1 and CP2 terminals.

Dead Time

To prevent cross-conduction (shoot-through) in any phase of the power MOSFET bridge, it is necessary to have a dead-time delay between a high-side or low-side turn off and the next complementary turn-on event. The potential for cross-conduction occurs when any complementary high-side and low-side pair of MOSFETs are switched at the same time, for example, at the PWM switch point.

The dead time is generally set by the external controller driving the inputs; however, the A89120 has several options for dead time that can be selected via the configuration resistors connected to the BSEL1 and BSEL2 pins.

Gate Drive Control

Six logic-level digital inputs—AHI, ALO, BHI, BLO, CHI, and CLO—provide direct control for the gate drives, one for each drive. The xHI inputs correspond to the high-side drives, and the xLO inputs correspond to the low-side drives. Logic inputs have a typical hysteresis of 500 mV to improve noise performance. The operation of the inputs is shown Table 1. A pull-down resistor is connected to each input to ensure a safe state if the control becomes disconnected.

Table 1: Control Logic

Input		Output		Phase	Comment
xHI	xLO	GHx	GLx	Sx	
0	0	L	L	Z	Phase disabled
0	1	L	H	LO	Low-side active
1	0	H	L	HI	High-side active
1	1	L	L	Z	Phase disabled

The ENABLE input is connected directly to the gate-drive-output command signal, bypassing the main synchronous logic block on the chip (including all phase-control logic). This input can be used to provide a fast output disable (emergency cut-off) or to provide nonsynchronous fast decay PWM.

The BRAKEn input overrides the direct-control inputs and enables all low-side drivers. If a high-side driver is already enabled, the respective low-side driver become enabled after a dead time. BRAKEn input overrides the ENABLE input except when in sleep mode.

Three-Wire Drive Option

The A89120 provides an option to drive the six external MOSFETS using three lines from the microcontroller instead of six. This option is chosen via the configuration resistor selection. For the three-wire drive option, the high-side inputs are used and the low-side gates are driven in a complementary fashion, turning on after the selected dead time. The xLO inputs are ignored and can be left in the open circuit state.

Table 2: Control Logic—Three-Wire

Input		Output		Phase	Comment
xHI	xLO	GHx	GLx	Sx	
0	X	L	H	LO	Low-side active
1	X	H	L	HI	High-side active

Diagnostic

The A89120 includes many diagnostic features to provide indication of and/or protection against undervoltage, overvoltage, overtemperature, and power bridge faults (VDS monitor and bootstrap undervoltage).

When RESETn is high, the FAULTn pin can be used to communicate the failure condition. During typical operation, the open drain is pulled high externally, through a resistor. When a fault occurs, the open drain output is enabled and the FAULTn output is pulled low according to Table 3.

Table 3: Fault Logic

Event	Fault Pin	Outputs Disabled	Latched
TSD	Low	Y	Y
VREG	Low	Y	N
Boot UVLO	Low	Y(Note)	N
VLR UVLO	Low	Y	N
VDS	Low	Y	Y

NOTE: Upon detection of the boot UVLO condition, only the appropriate high side is disabled.

Latched faults that result in disabled outputs can be reset in two

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ways. Putting the device into sleep mode (RESETn low) resets the latch. RESETn can also be used to clear any fault conditions without entering sleep mode by pulsing low for 1 µs (within the range of the reset pulse width specification, t_{RST}).

Overtemperature (TSD)

If the die temperature exceeds T_{TSD}, FAULTn is pulled low and the outputs are disabled. Thermal shutdown is a latched fault.

Bootstrap UVLO Fault

Before a high-side switch is allowed to turn on and when a high side is on, it must have sufficient charge on the bootstrap capacitor. If a high side is instructed to turn on and the voltage on the appropriate bootstrap capacitor is less than the bootstrap threshold, the A89120 triggers a fault (FAULTn goes low) and does not allow the high-side gate to turn on. After a high-side gate drive has been successfully turned on, the appropriate bootstrap capacitor voltage must continue to exceed the bootstrap undervoltage threshold, $V_{BOOT(UV)}$. If the bootstrap capacitor voltage drops below $V_{BOOT(UV)}$, the high-side driver in question is switched off and FAULT goes low. The driver remains off until the bootstrap capacitor is charged to ($V_{BOOT(UV)}$ + $V_{BOOT(HYS)}$) and the gate xHI input is active high.

If a bootstrap capacitor fault condition is detected, only the driver in question is disabled. All other gate drives continue to respond to control inputs on xHI and xLO.

VDS Overvoltage Fault

Faults on any external MOSFETs are determined by monitoring the drain-to-source voltage of the MOSFET and comparing it to the drain-to-source overvoltage threshold. for the available threshold voltages, refer to Table 4.

If the measured voltage exceeds the configurable threshold value of the pin, the FAULTn output is set low and the gate drive outputs are disabled. A VDS fault is latched.

At every external MOSFET turn-on event, the output of all VDS comparators is ignored for the duration of the VDS fault blank time (t_{BL}); this prevents the reporting of spurious faults in response to switching transients.

Current-Sense Amplifier

A configurable-gain, differential, sense amplifier is provided to allow the use of low-value sense resistors or a current shunt as a low-side current-sensing element. The input common-mode range of the CSP and CSM inputs and programmable output offset allow below-ground current sensing—typically required for low-side current sense in PWM control of motors or other inductive loads—during switching transients. The output of the sense amplifier is available at the CSO output and can be used in peak-current or average-current control systems. The output can drive up to 4.8 V to permit maximized dynamic range with greater input-voltage analog-to-digital converters (ADCs).

The gain and offset of the sense amplifier are defined by the configuration of the pin-detect comparator, and shown in Table 4.

Pin-Detect Comparator

The A89120 is equipped with a pin-detect comparator on the BSEL1 and BSEL2 pins. This function allows the user to program 5 bits of digital features with three external E96 1% resistors. The pin-detect comparator requires a 51.1 kΩ resistor between BSEL1 and BSEL2, and the bit selections are determined by resistor values placed from BSEL1 to AGND and BSEL2 to AGND. The resistor values used for programming range from 511 Ω to 750 kΩ. The resistor from BSEL2 to GND programs the current-sense offset and gain. The resistor from BSEL1 to GND programs the VDS levels for short-to-ground and short-to-battery protection, dead time, and gate-drive logic mode.

The pin-detect circuitry is designed to be robust to ground differentials of ±20 mV, pin leakages of ±500 nA, and capacitances of up to 50 pF. These criteria allow for robust performance in all PCB layouts. For the configurable variables, refer to Table 4.

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Current Amplifier

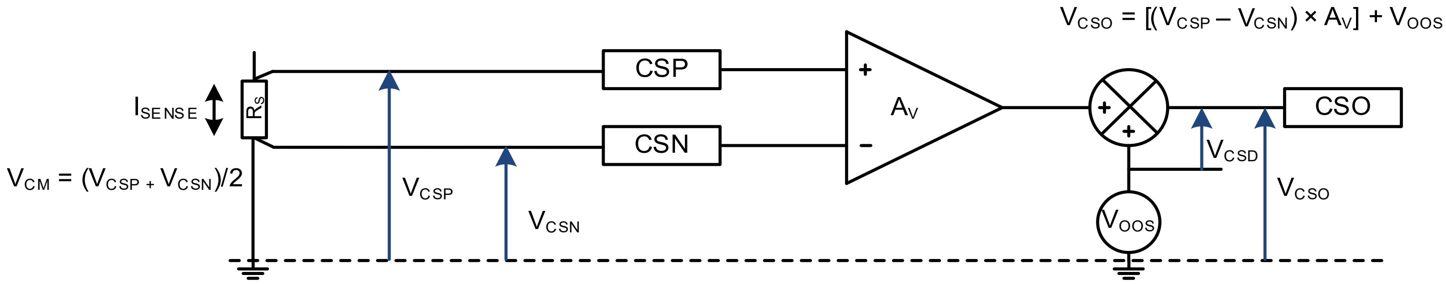

Table 4: BSEL1 and BSEL2

BSEL1			
	4 3	2 1	0
RBSEL1	**Dead Time (ns)**	**VDS Threshold (mv)**	**Inputs (#)**
511		300	6
1620			3
3480		600	6
5360			3
7150	100	900	6
9530			3
11500		1200	6
14000			3
16900		300	6
19600			3
23700		600	6
26100			3
30100	500	900	6
34800			3
40200		1200	6
44200			3
51100		300	6
59000			3
64900		600	6
75000			3
86600	1000	900	6
95300			3
110000		1200	6
133000			3
154000		300	6
187000			3
226000		600	6
274000			3
365000	1500	900	6
487000			3
750000		1200	6
Float			3

BSEL2		
	4 3	2 1 0
RBSEL2	**Gain (V/V)**	**Pedestal (mv)**
511		200
1620		400
3480		600
5360		800
7150	10	1000
9530		1200
11500		1400
14000		1600
16900		200
19600		400
23700		600
26100		800
30100	20	1000
34800		1200
40200		1400
44200		1600
51100		200
59000		400
64900		600
75000		800
86600	30	1000
95300		1200
110000		1400
133000		1600
154000		200
187000		400
226000		600
274000		800
365000	40	1000
487000		1200
750000		1400
Float		1600

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APPLICATION INFORMATION

Bootstrap Capacitor Selection

To properly size the capacitor, C_{BOOT}, the total gate charge must be known:

- If the bootstrap capacitor is too large, the charge time will be long, resulting in limits to the maximum duty cycle.
- If the bootstrap capacitor is too small, the voltage ripple will be large when charging the gate.

Size the C_{BOOT} capacitor such that the charge, Q_{BOOT}, is 20 times larger than the required charge for the gate of the MOSFET, Q_{GATE}, using:

$$C_{BOOT} = [Q_{GATE} \times 20]/[V_{BOOT}],$$

where V_{BOOT} is the voltage across the bootstrap capacitor.

The voltage drop, ΔV, across the bootstrap capacitor as the MOSFET gate is being charged can be approximated by:

$$\Delta V = [Q_{GATE}]/[C_{BOOT}].$$

For the bootstrap capacitor, a ceramic type rated at 16 V or larger should be used.

VREG Capacitor Selection

VREG is responsible for providing all the gate charge for the low-side MOSFETs and for providing all the charge current for the three bootstrap capacitors. For this purpose, the VREG capacitor should be 20 times the value of C_{BOOT}:

$$C_{VREG} = 20 \times C_{BOOT}$$

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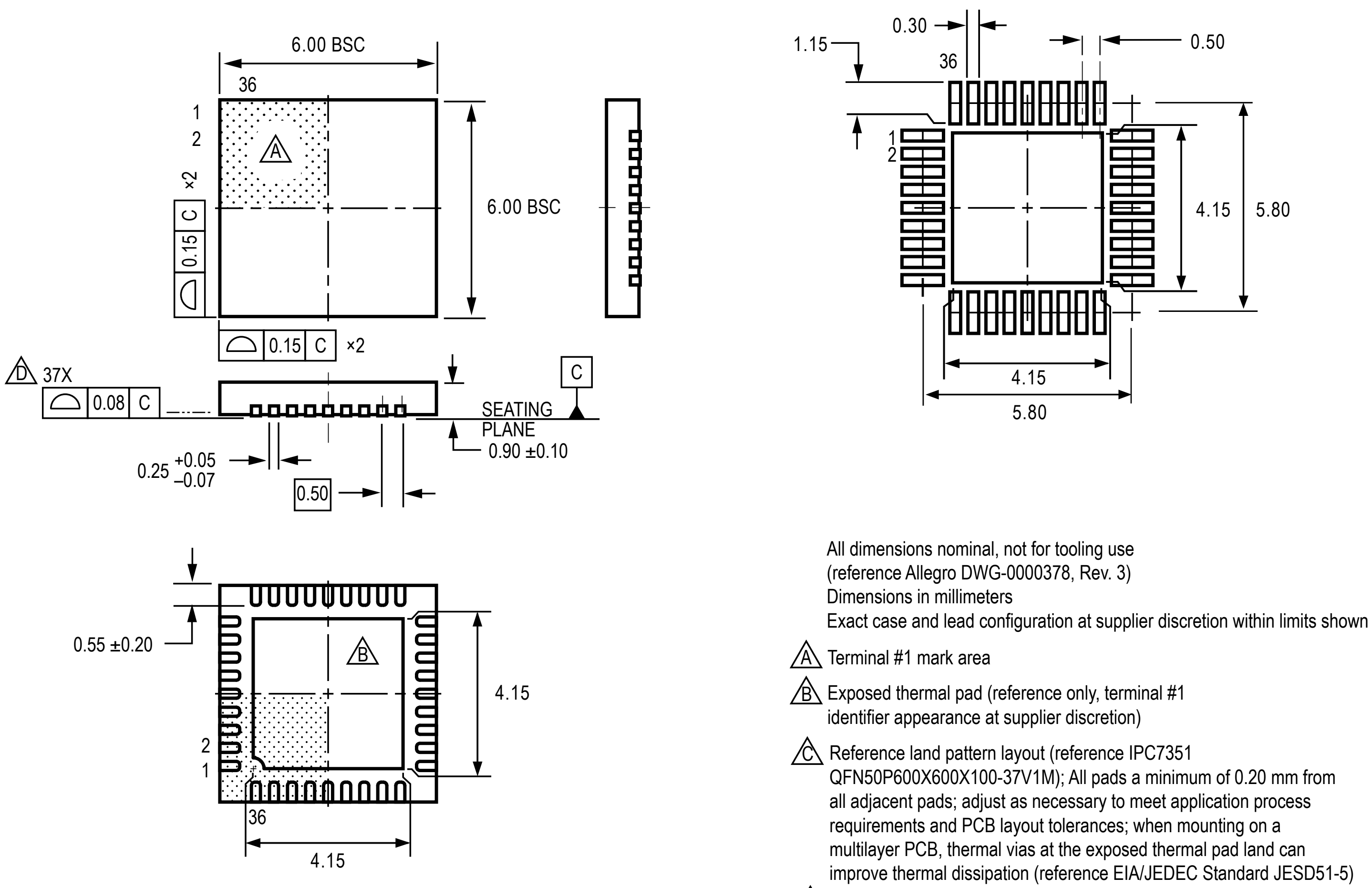
PACKAGE OUTLINE DRAWING



All dimensions nominal, not for tooling use
(reference Allegro DWG-0000378, Rev. 3)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P600X600X100-37V1M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

Figure 1: 36-Lead QFN with Exposed Pad (Suffix EV)

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Revision History

Number	Date	Description
–	March 11, 2024	Initial release

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