A89199

Automotive Three-Phase MOSFET Driver

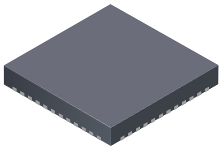
FEATURES AND BENEFITS

- 3-phase bridge MOSFET driver
- Bootstrap gate drive for N-channel MOSFET bridge
- Cross-conduction protection with adjustable dead time
- Charge pump for low-supply-voltage operation
- Strong pumped regulator terminal voltage (V_{REG}) charge pump supports up to 50 mA average gate-switching current and enables 410 nC external MOSFETs to be driven at 20 kHz
- Top-off charge pump for 100% pulse-width modulation (PWM)
- Programmable gate-drive voltage and strength
- 4.5 to 50 V supply-voltage operating range
- Integrated logic supply
- Three programmable current-sense amplifiers
- SPI-compatible serial interface
- ASIL Compliant: ASIL D safety element out-of-context (SEooC) developed in accordance with ISO 26262, when used as specified in the safety manual

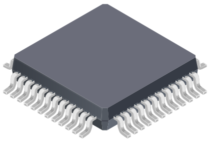
A2 SiL ISO 26262 ASIL Compliant

PACKAGES

48-pin QFN with exposed thermal pad and wettable flank (suffix EV)



48-pin LQFP with exposed thermal pad (suffix JP)



Not to scale

DESCRIPTION

The A89199 is the next-generation revision of the popular A4918. It is an N-channel power MOSFET driver capable of controlling MOSFETs connected in a three-phase bridge arrangement and is specifically designed for automotive applications with high-power inductive loads, such as brushless direct-current (BLDC) motors.

A unique charge pump regulator provides the supply for the MOSFET gate drive for battery voltages down to 7 V and allows the A89199 to operate with a reduced gate drive down to 4.5 V. Gate drive voltage and strength are programmable to help reduce electromagnetic compatibility (EMC) issues. A bootstrap capacitor is used to provide the above-battery supply voltage required for N-channel MOSFETs with an additional above-battery charge pump to ensure that the bootstrap capacitors remain charged when held in the on-state.

Full control is provided over all six power MOSFETs in the three-phase bridge. This allows motors to be driven with block commutation or sinusoidal excitation. The power MOSFETs are protected from shoot-through by integrated crossover control and optional programmable dead time.

Integrated diagnostics provide indication of multiple internal faults, system faults, and power bridge faults, and can be configured to protect the power MOSFETs under most short-circuit conditions. For safety-critical systems, the integrated diagnostic operation can be verified under control of the serial interface.

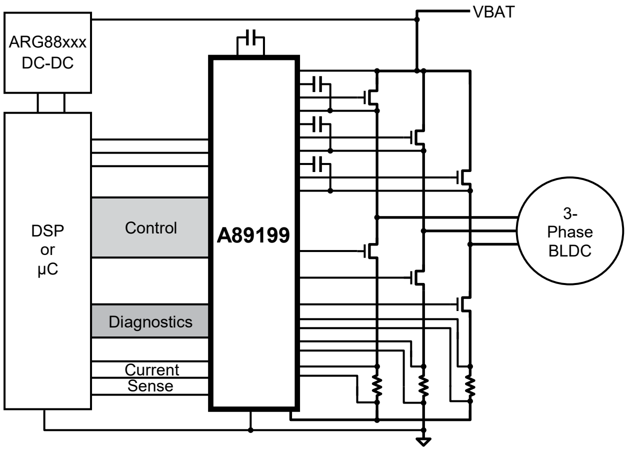


Figure 1: Typical Application

FEATURES AND BENEFITS (continued)

- Bridge control by direct logic inputs or serial interface
- Extensive programmable diagnostics
- Diagnostic verification
- Safety assist features
- Automotive AEC-Q100 qualified
- A^2-SIL™ product—device features for safety-critical systems

DESCRIPTION (continued)

The serial interface is provided to alter programmable settings and read back detailed diagnostic information.

The A89199 was developed in accordance with ISO 26262 as a hardware safety element out-of-context with ASIL D capability for use in automotive safety-related systems when integrated and used in the manner prescribed in the applicable safety manual and datasheet.

The A89199 is supplied in a 48-terminal wettable-flank quad-flat no-lead (QFN) package (suffix EV) and a 48-pin quad-flat package (QFP) (suffix JP), both with exposed thermal pad. These packages are lead (Pb) free with 100% matte tin leadframe plating.

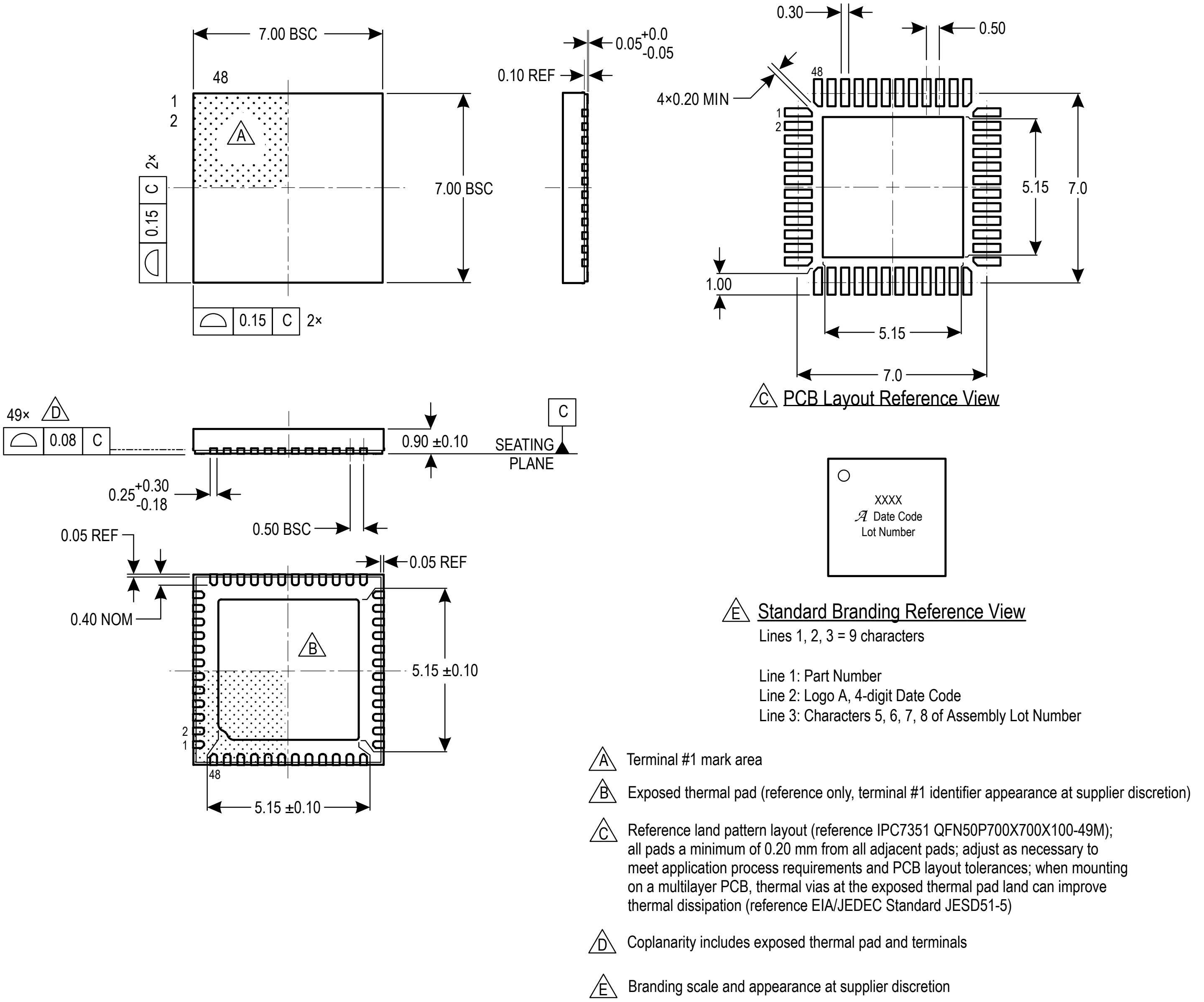
SELECTION GUIDE

Part Number	I/O Logic	Packing	Package
A89199KEVSR-3-T	3.3 V	4000 pieces per 13-inch reel	7 mm × 7 mm, 0.9 mm nominal height 48-terminal QFN with exposed thermal pad and wettable flank
A89199KEVSR-5-T	5 V		
A89199KJPTR-3-T	3.3 V	1500 pieces per 13-inch reel	7 mm × 7 mm, 1.6 mm nominal height 48-lead QFP with exposed thermal pad
A89199KJPTR-5-T	5 V		

PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use

(Reference DWG-0000378, Rev. 3)
Dimensions in millimeters
NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



Lines 1, 2, 3 = 9 characters

Line 1: Part Number
Line 2: Logo A, 4-digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P700X700X100-49M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

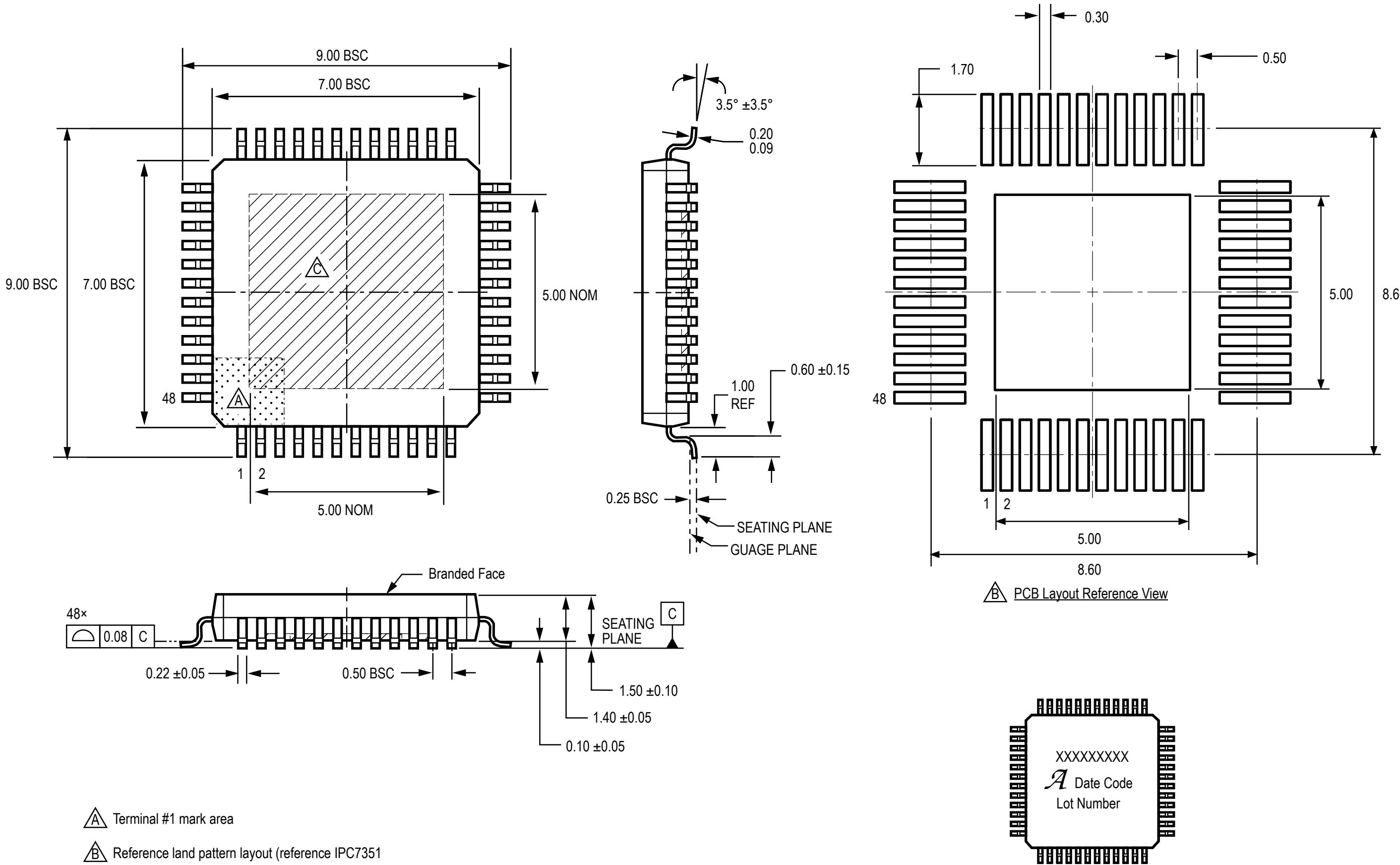
D Coplanarity includes exposed thermal pad and terminals

E Branding scale and appearance at supplier discretion

Figure 2: EV Package, 48-Pin QFN with Exposed Thermal Pad and Wettable Flank

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000386, Rev. 5 or JEDEC MS-026 BBCHD)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



B PCB Layout Reference View

A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 QFP50P900X900X160-48M); adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Exposed thermal pad (bottom surface); exact dimensions may vary with device

D Branding scale and appearance at supplier discretion

D Standard Branding Reference View
Line 1, 2, 3: Maximum 9 characters per line

Line 1: Part Number
Line 2: Logo A, 4-digit Date Code
Line 3: Assembly Lot Number

Figure 3: JP Package, 48-Pin LQFP with Exposed Thermal Pad

Revision History

Number	Date	Description
–	November 13, 2024	Initial release
1	July 21, 2025	Modified ASIL branding and text (pages 1, 2, and 17), regenerated table of contents (page 3), modified gate drive control description (page 22), and made minor formatting modifications throughout
2	August 11, 2025	Modified Gate-Drive Control section (page 22)
3	September 15, 2025	Modified Gate-Drive Control section (page 23)

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