Automotive MCU with 90 V MOSFET Driver

FEATURES AND BENEFITS

- 5.5 to 90 V supply voltage operating range
- 32-bit ARM cortex M4 CPU core
  - □ Up to 40 MHz clock frequency
  - □ On-chip ±1% accurate oscillator
  - □ Programmable clock generator
  - □ One-clock-per-machine cycle architecture
  - □ DMA
  - □ 16-level interrupt handler
  - □ SW-DP tw-wire debug
- On-chip memory
  - □ up to 248 kB flash
  - □ 32 kB DRAM
  - □ 8 kB IRAM
  - □ 32 kB boot ROM

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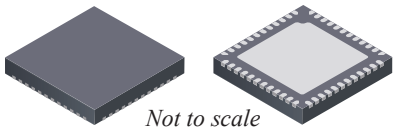
PACKAGE



Not to scale

48-pin 7 mm × 7 mm QFN with exposed thermal pad and wettable flank (suffix EV)

DESCRIPTION

The A89224 is a high-performance processor with integrated three-phase gate drive and precision current sense capability. It is designed for use with advanced standalone three-phase brushless DC (BLDC) motor and permanent magnet synchronous motor (PMSM) control applications.

The processor uses the ARM cortex M4 CPU core running at 40 MHz, giving up to 50 million instructions per second (mips) performance. The processor capability is further enhanced by peripheral functions specifically designed for motor control applications. These include a pulse-width modulation (PWM) generator and sense-current capture systems capable of providing up to 12-bit control precision at up to 20 kHz PWM frequency.

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APPLICATIONS

- HVAC
- Pump
- Cooling fan
- Seating moving

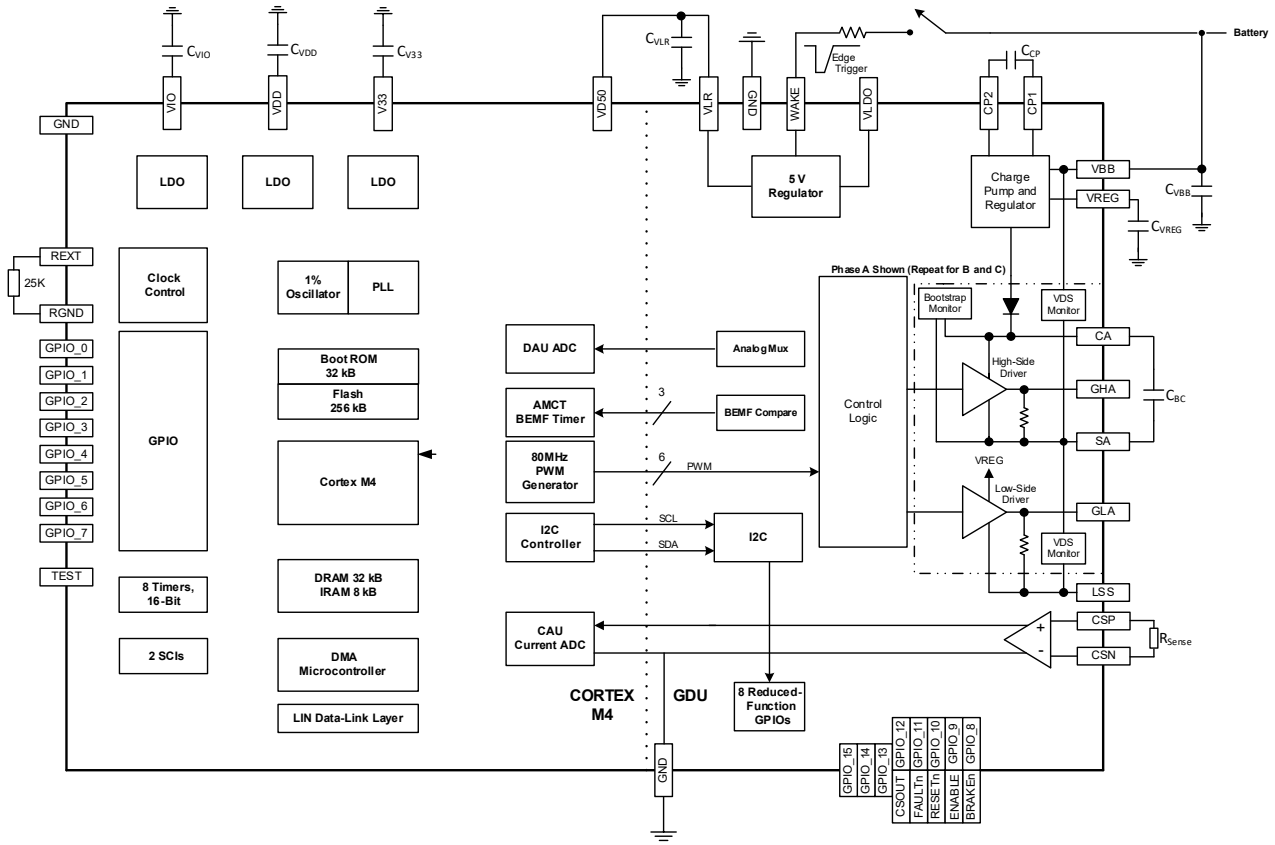

Figure 1: A89224 Block Diagram

FEATURES AND BENEFITS (continued)

- Three-phase bridge MOSFET driver with bootstrap gate drive for N-channel MOSFET bridge
- Charge pump for low supply voltage operation
- 5 V CMOS-compatible logic I/O
- 80 MHz PWM generator
  - □ 12-bit PWM at 20 kHz
  - □ Programmable back electromagnetic force (bemf) and current-sample control
- Programmable high-performance current-sense amplifier
  - □ 3 x 11 bit, 1 µs analog-to-digital converter (ADC) for current measurement
- 12-bit 1 µs data acquisition ADC with 16-channel multiplexer (mux)
- 8 general-purpose I/O (GPIO) ports
- 8 general-purpose timers
- 2 serial communication interfaces (SCIs)
- Local-interconnect network (LIN) datalink layer
- 1-phase bemf detector
- Integrated power management
- VDS, UVLO, and thermal shutdown diagnostic
- Latched TSD with fault output
- Automotive AEC-Q100 Grade 1 qualified

DESCRIPTION (continued)

16 general-purpose input and output (I/O) ports provide access to programmable serial communication interfaces and analog and digital inputs and outputs.

The gate driver is an N-channel power MOSFET driver capable of controlling MOSFETs connected in a three-phase bridge arrangement and is specifically designed for power applications with high-power inductive loads, such as BLDC motors.

A unique charge-pump regulator provides the supply for the MOSFET gate drive for battery voltages as low as 7 V and allows the A89224 to operate with a reduced gate drive voltage as low as 5.5 V. A bootstrap capacitor is used to provide the greater-than-battery supply voltage required for the N-channel MOSFETs.

The power supply unit provides and manages all internal supplies from a single 5.5 to 90 V supply. The microcontroller unit (MCU) section can also operate with an independent single 5 V supply.

Integrated programmable diagnostics provide indication of multiple internal faults, system faults, and power-bridge faults, and can be configured to protect the power MOSFETs under most short-circuit conditions.

The A89224 is supplied in a 48-lead quad-flat no-lead (QFN) package with exposed thermal pad. This package is lead (Pb) free with 100% matte tin leadframe plating.

SELECTION GUIDE

Part Number	Flash Memory (kB)	GPIO Voltage (V)	Package
A89224KEVSR-A	248	5	7 mm × 7 mm, 0.9 mm nominal height 48-terminal QFN with exposed thermal pad and wettable flank
A89224KEVSR-B	128	5	7 mm × 7 mm, 0.9 mm nominal height 48-terminal QFN with exposed thermal pad and wettable flank

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

NOTE: This is a short-form datasheet for preview purposes. Pages 4-27 have been removed. Contact Allegro MicroSystems to request complete datasheet.

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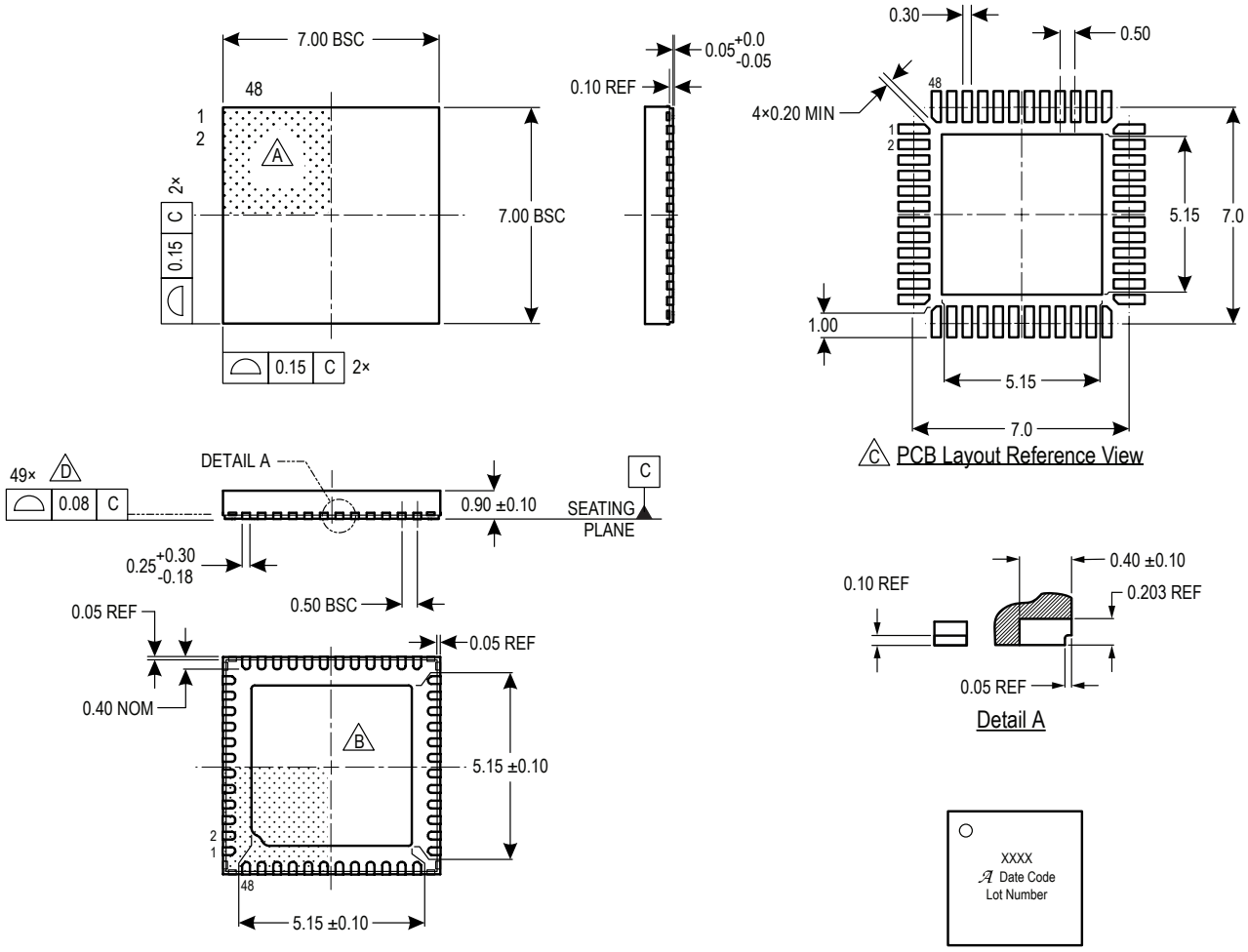
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference DWG-0000378, Rev. 3)
Dimensions in millimeters
NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P700X700X100-49M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Branding scale and appearance at supplier discretion

E Standard Branding Reference View
Line 1: Part Number
Line 2: Logo A, 4-digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Figure 2: 48-Pin QFN with Exposed Pad (Suffix -EV)

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Revision History

Number	Date	Description
–	February 18, 2025	Initial release
1	March 25, 2025	Updated block diagram (page 1); updated Terminal CP value (page 4); updated VREG Output Voltage value and VLR Output Overcurrent Limit, Core Voltage, Analog Voltage, Program Cycle, and Data Retention test conditions (page 7); updated Gate Drive Pull-Up Resistance (150°C) maximum value (page 11); updated VLR Undervoltage minimum value (page 12); updated Boot ROM section (page 14); and minor editorial updates

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