

80 V Automotive Half-Bridge MOSFET Driver

FEATURES AND BENEFITS

- Half-bridge MOSFET driver
- Bootstrap gate drive for N-channel MOSFET bridge
- Independent control of high-side and low-side gate drives with cross-conduction capability
- Charge pump regulator for low supply voltage operation
- 5.5 to 80 V supply voltage operating range
- Integrated logic I/O supply
- SPI-compatible serial interface
- Bridge control by direct logic inputs or serial interface
- Programmable gate drive
- Current sense amplifier
- Programmable diagnostics
- A²SIL™ product—device features for safety-critical systems
- AEC-Q100 Grade 0 qualified

DESCRIPTION

The A89503 is an N-channel power MOSFET driver capable of controlling MOSFETs connected in a half-bridge arrangement and is specifically designed for automotive applications with high-power inductive loads, such as brush DC motors, BLDC motors, VR/SR motors, solenoids, and actuators.

A unique charge pump regulator provides full gate drive over the full supply voltage range from 5.5 to 80 V for most applications. A bootstrap capacitor is used to provide the above-battery supply voltage required for N-channel MOSFETs.

Each MOSFET can be independently controlled by logic-level inputs or through the SPI-compatible serial interface. Fully independent control allows both external FETs to be turned on at the same time.

Integrated diagnostics provide indication of multiple internal faults, system faults, and power bridge faults, and can be configured to protect the power MOSFETs under most short circuit conditions.

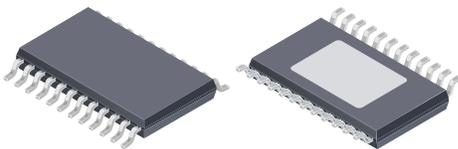
In addition to providing full access to the bridge control, the serial interface is also used to alter programmable settings such as VDS threshold and fault blank time. Detailed diagnostic information can be read through the serial interface.

The A89503 was developed in accordance with ISO 26262 as a hardware safety element out of context with ASIL B capability (pending assessment) for use in automotive safety-related systems when integrated and used in the manner prescribed in the applicable safety application note and datasheet.

The A89503 is supplied in a 24-lead eTSSOP (suffix LP). This package is lead (Pb) free, with 100% matte-tin leadframe plating (suffix -T).

PACKAGE:

24-lead TSSOP with exposed pad (suffix LP)



Not to scale

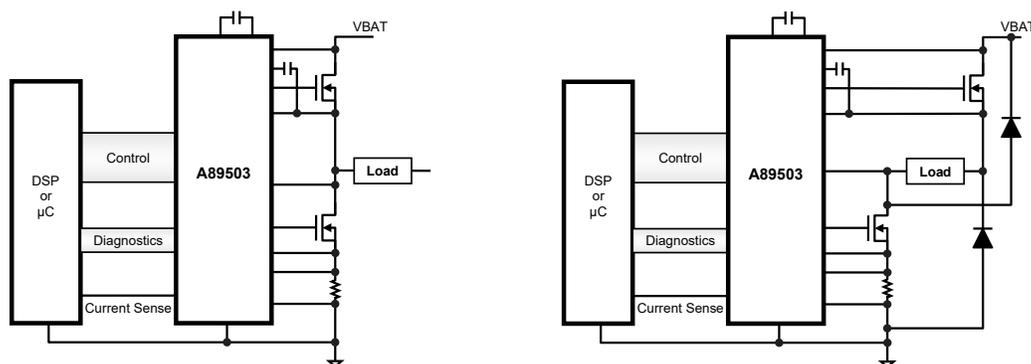


Figure 1: Typical Applications

SELECTION GUIDE

Part Number	I/O Logic	Packing	Package
A89503KLPTR-3-1	3.3 V	4000 pieces per reel	7.8 mm × 4.4 mm, 1.2 mm max height 24-lead TSSOP with exposed thermal pad
A89503KLPTR-5-1	5 V		

ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
Load Supply Voltage	V_{BB}		-0.3 to 80	V
Regulator Output	V_{REG}	VREG	-0.3 to 16	V
Charge Pump Capacitor Terminal	V_{CP1}	CP1	-0.3 to 16	V
Charge Pump Capacitor Terminal	V_{CP2}	CP2	$V_{CP1} - 0.3$ to $V_{REG} + 0.3$	V
Battery-Compliant Logic Input Terminals	V_{IB}	HS, LS _n , RESET _n , ENABLE	-0.3 to 80	V
Logic Input Terminals	V_I	STR _n , SCK, SDI	-0.3 to 6	V
Logic Output Terminal	V_O	SDO	-0.3 to 6	V
Diagnostics Output	V_{DIAG}	DIAG	-0.3 to 80	V
Sense Amplifier Inputs	V_{CSI}	CSP, CSM	-4 to 6.5	V
Sense Amplifier Output	V_{CSO}	CSO	-0.3 to 6	V
Bridge Drain Monitor Terminal	V_{BRG}	VBRG	-5 to 85	V
Bootstrap Supply Terminal	V_C	C	-0.3 to $V_{REG} + 80$	V
High-Side Gate Drive Output Terminal	V_{GH}	GH	$V_C - 16$ to $V_C + 0.3$	V
		GH (transient)	-18 to $V_C + 0.3$	V
High-Side Source (Load) Terminal	V_S	S	$V_C - 16$ to $V_C + 0.3$	V
		S (transient)	-18 to $V_C + 0.3$	V
Low-Side Drain (Load) Terminal	V_D	D	-16 to V_S	V
Low-Side Gate Drive Output Terminal	V_{GL}	GL	$V_{REG} - 16$ to 18	V
		GL (transient)	-8 to 18	V
Bridge Low-Side Source Terminal	V_{LSS}	LSS	$V_{REG} - 16$ to 18	V
		LSS (transient)	-8 to 18	V
Ambient Operating Temperature Range	T_A	Limited by power dissipation	-40 to 150	°C
Maximum Continuous Junction Temperature	$T_{J(max)}$		165	°C
Transient Junction Temperature	T_{Jt}	Overtemperature event not exceeding 10 seconds, lifetime duration not exceeding 10 hours, guaranteed by design characterization.	180	°C
Storage Temperature Range	T_{stg}		-55 to 150	°C

[1] With respect to GND. Ratings apply when no other circuit operating constraints are present.

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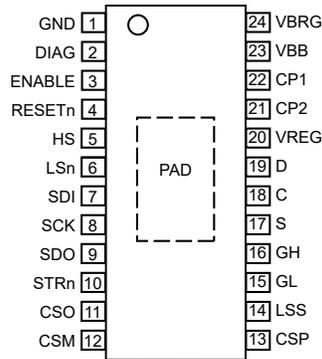
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Thermal Characteristics: May require derating at maximum conditions

Characteristic	Symbol	Test Conditions [2]	Value	Unit
Package Thermal Resistance	R _{θJA}	4-layer PCB based on JEDEC standard	28	°C/W
		2-layer PCB with 3.8 in. ² copper each side	38	°C/W
	R _{θJP}		2	°C/W

[2] Additional thermal information available on the Allegro website.

PINOUT DIAGRAM AND TERMINAL LIST TABLE



24-Lead eTSSOP (suffix LP)
Pinout Diagram

Terminal List Table

Name	Number	Function
C	18	Bootstrap Capacitor
CP1	22	Pump Capacitor CCP Connection
CP2	21	Pump Capacitor CCP Connection
CSM	12	Current Sense Amp -Input
CSO	11	Current Sense Amp Output
CSP	13	Current Sense Amp +Input
DIAG	2	Diagnostic Output
ENABLE	3	Gate drive output control Input
GH	16	High-side Gate Drive Output
GL	15	Low-side Gate Drive Output
GND	1	Power Ground
HS	5	High-side control Input
LSn	6	Low-side control Input
LSS	14	Low-side Source
D	19	Low-side Drain Connection
RESETn	4	Standby Mode Control Input
S	17	Load Connection
SCK	8	Serial Clock Input
SDI	7	Serial Data Input
SDO	9	Serial Data Output
STRn	10	Serial Strobe (chip select) Input
VBB	23	Main Power Supply
VBRG	24	High-side Drain voltage sense
VREG	20	Regulated gate drive supply
PAD	-	Thermal pad; connect to GND

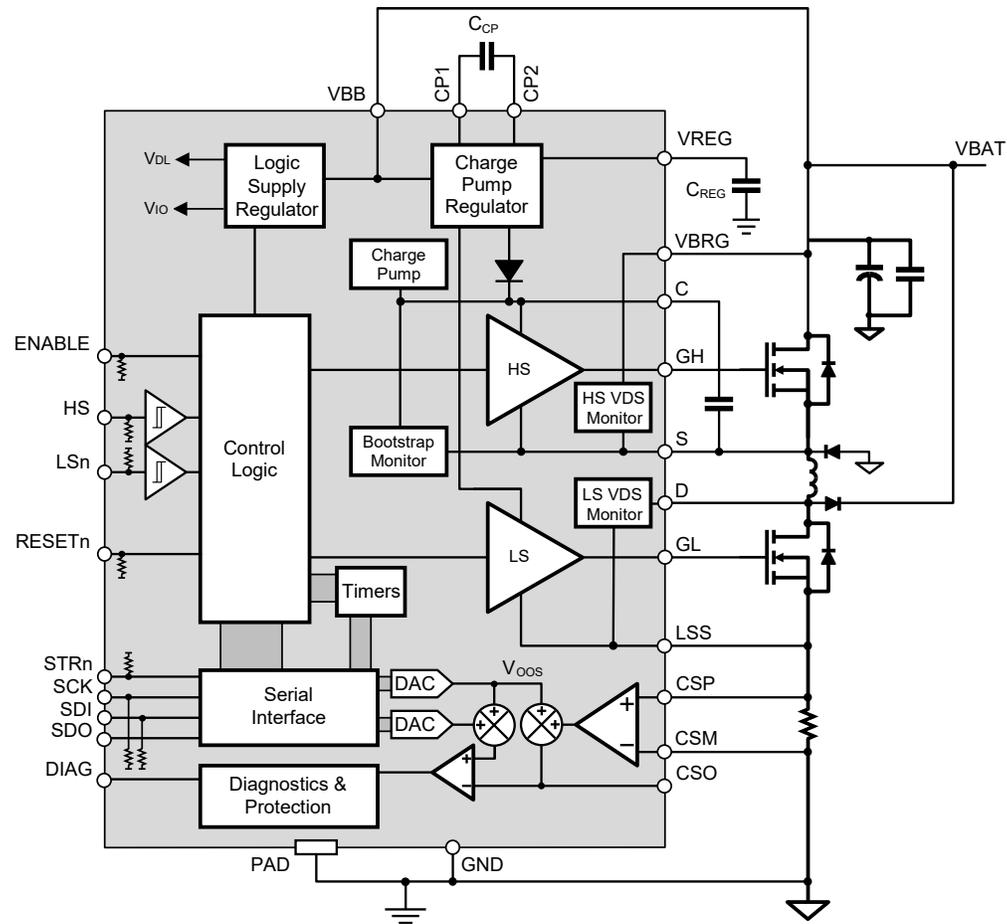


Figure 2: Functional Block Diagram

ELECTRICAL CHARACTERISTICS: Valid for $T_J = -40$ to 150°C , $V_{BB} = 5.5$ to 80 V, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY AND REFERENCE						
VBB Functional Operating Range	V_{BB}	Operating; outputs active	5.5	–	80	V
		Operating; outputs disabled	5	–	80	V
		No unsafe states	0	–	80	V
VBB Quiescent Current	I_{BBQ}	RESETn = high, $V_{BB} = 48$ V, All gate drive outputs low	–	8	20	mA
	I_{BBS}	RESETn ≤ 300 mV, sleep mode, $V_{BB} < 70$ V	–	–	30	μA
Internal Logic Supply Regulator Voltage ^{[3][4]}	V_{DL}		3.1	3.3	3.5	V
Logic I/O Regulator Voltage ^{[3][4]}	V_{IO}	A89503KLPTR-3	3	3.3	3.6	V
		A89503KLPTR-5; $V_{BB} > 6$ V	4.5	5	5.5	V
VREG Output Voltage	V_{REG}	$6.5 \text{ V} < V_{BB}$, $I_{VREG} = 0$ to 33 mA	9	11	11.7	V
		$6 \text{ V} < V_{BB} \leq 6.5 \text{ V}$, $I_{VREG} = 0$ to 20 mA	9	11	11.7	V
		$5.5 \text{ V} < V_{BB} \leq 6 \text{ V}$, $I_{VREG} = 0$ to 15 mA	9	11	11.7	V
Bootstrap Diode Forward Voltage	V_{fBOOT}	$I_D = 10$ mA	0.4	0.7	1.0	V
		$I_D = 100$ mA	1.35	2.2	2.8	V
Bootstrap Diode Current Limit	I_{DBOOT}		250	500	750	mA
Top-Off Charge Pump Current Limit	I_{TOCPM}		43	100	–	μA
High-Side Gate Drive Static Load Resistance	R_{GSH}		250	–	–	k Ω
System Clock Period	t_{OSC}		45	50	55	ns

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ELECTRICAL CHARACTERISTICS (continued): Valid for $T_J = -40$ to 150°C , $V_{BB} = 5.5$ to 80 V, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GATE OUTPUT DRIVE						
Turn-On Time (High-Side)	$t_{r(HS)}$	$C_{LOAD} = 15$ nF, 2 V to 8 V, $V_C - V_S = 11$ V	86	235	434	ns
Turn-On Time (Low-Side)	$t_{r(LS)}$	$C_{LOAD} = 15$ nF, 2 V to 8 V, $V_{REG} - V_{LSS} = 11$ V	86	235	434	ns
Turn-Off Time (High-Side)	$t_{f(HS)}$	$C_{LOAD} = 15$ nF, 8 V to 2 V, $V_C - V_S = 11$ V	44	97	205	ns
Turn-Off Time (Low-Side)	$t_{f(LS)}$	$C_{LOAD} = 15$ nF, 8 V to 2 V, $V_{REG} - V_{LSS} = 11$ V	44	97	205	ns
Pull-Up Peak Source Current (High-Side)	$I_{PUPK(HS)}$	$V_C - V_S = 11$ V	-1150	-	-250	mA
Pull-Up Peak Source Current (Low-Side)	$I_{PUPK(LS)}$	$V_{REG} - V_{LSS} = 11$ V	-1150	-	-250	mA
Pull-Up On Resistance	$R_{DS(on)UP}$	$T_J = 25^\circ\text{C}$, $I_{GH} = -150$ mA ^[1]	5.6	-	15.6	Ω
		$T_J = 150^\circ\text{C}$, $I_{GH} = -150$ mA ^[1]	9.1	-	23.9	Ω
Pull-Down Peak Sink Current (High-Side)	$I_{PDPK(HS)}$	$V_C - V_S = 11$ V	570	-	2100	mA
Pull-Down Peak Sink Current (Low-Side)	$I_{PDPK(LS)}$	$V_{REG} - V_{LSS} = 11$ V	570	-	2100	mA
Pull-Down On Resistance	$R_{DS(on)DN}$	$T_J = 25^\circ\text{C}$, $I_{GL} = 150$ mA	1.25	-	2.8	Ω
		$T_J = 150^\circ\text{C}$, $I_{GL} = 150$ mA	2.1	-	4.7	Ω
Turn-On Time Set Point Range	t_R		60	-	300	ns
Minimum Turn-On Time	t_{RM}	TR = 0	45	60	75	ns
Turn-On Time Mean Step Size	t_{RS}	TR > 0	12	16	22	ns
Turn-On Current I1	I_{R1}	$V_{GS} = 0$ V, IR1 = 15	-511	-120	-86	mA
		Programmable set point range	-8	-	-120	mA
Turn-On Current I2	I_{R2}	$V_{GS} = 0$ V, IR2 = 15	-511	-120	-86	mA
		Programmable set point range	-8	-	-120	mA
Turn-Off Time Set Point Range	t_F		60	-	300	ns
Minimum Turn-Off Time	t_{FM}	TF = 0	45	60	75	ns
Turn-Off Time Mean Step Size	t_{FS}	TF > 0	12	16	22	ns
Turn-Off Current I1	I_{F1}	$V_{GS} = 9$ V, IF1 = 15	84	120	148	mA
		Programmable set point range	8	-	120	mA
Turn-Off Current I2	I_{F2}	$V_{GS} = 9$ V, IF2 = 15	84	120	148	mA
		Programmable set point range	8	-	120	mA
GH Output Voltage High	V_{GHH}	Bootstrap capacitor fully charged	$V_C - 0.02$	-	-	V
GH Output Voltage Low	V_{GHL}	$-10 \mu\text{A} < I_{GH} < 10 \mu\text{A}$	-	-	$V_S + 0.02$	V
GL Output Voltage High	V_{GLH}		$V_{REG} - 0.02$	-	-	V
GL Output Voltage Low	V_{GLL}	$-10 \mu\text{A} < I_{GL} < 10 \mu\text{A}$	-	-	$V_{LSS} + 0.02$	V
GH Passive Pull-Down	R_{GHPD}	$V_{GH} - V_S = 0.1$ V	0.25	-	1.8	M Ω
GL Passive Pull-Down	R_{GLPD}	$V_{GL} - V_{LSS} = 0.1$ V	0.25	-	1.8	M Ω
GH Active Pull-Down	R_{GHPA}	$V_{C-S} > 4$ V	0.7	-	20	Ω
GL Active Pull-Down	R_{GLPA}	$V_{VREG-LSS} > 4$ V	0.7	-	20	Ω
Turn-Off Propagation Delay	$t_{P(off)}$	Input Change to unloaded Gate output change (Figure 5)	30	-	103	ns
Turn-On Propagation Delay	$t_{P(on)}$	Input Change to unloaded Gate output change (Figure 5)	30	-	103	ns
Propagation Delay Matching (On-to-Off)	Δt_{OO}		-	-	25	ns
Propagation Delay Matching (GH-to-GL)	Δt_{HL}	Same state change	-	-	25	ns

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ELECTRICAL CHARACTERISTICS (continued): Valid for $T_J = -40$ to 150°C , $V_{BB} = 5.5$ to 80 V, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
LOGIC INPUT AND OUTPUTS						
Input Low Voltage	V_{IL}	Except RESETh	–	–	$0.3 \times V_{IO}$	V
		RESETh	–	–	0.8	V
Input High Voltage	V_{IH}	Except RESETh	$0.7 \times V_{IO}$	–	–	V
		RESETh	2.4	–	–	V
Input Hysteresis	V_{Ihys}	Except RESETh	250	550	–	mV
		RESETh	200	500	–	mV
Input Pull-Down HS, ENABLE, RESETh	R_{PD}	$0 < V_{IN} < V_{IO}$	–	50	–	k Ω
	I_{PD}	$V_{IO} < V_{IN} < 80$ V	–	100	–	μA
Input Pull-Up LSn	R_{PD}	$0 < V_{IN} < V_{IO}$	–	50	–	k Ω
	I_{PD}	$V_{IO} < V_{IN} < 80$ V	–	100	–	μA
Input Pull-Down SDI, SCK	R_{PDS}	$0 < V_{IN} < V_{IO}$	–	50	–	k Ω
Input Pull-Up STRn (to V_{IO})	R_{PUS}		–	50	–	k Ω
Output Low Voltage	V_{OL}	$I_{OL} = 1$ mA	–	0.2	0.4	V
Output High Voltage	V_{OHS}	$I_{OS} = -1$ mA ^[1]	$V_{IO} - 0.4$	–	–	V
Output Leakage SDO ^[1]	I_{OS}	$0 \text{ V} < V_{OS} < V_{IO}$, STRn = 1	–1	–	1	μA
Output Current Limit (DIAG)	I_{OLDLIM}	$0 \text{ V} < V_{OD} < 12$ V, DIAG active	–	10	17	mA
		$18 \text{ V} \leq V_{OD} < 80$ V, DIAG active	–	–	2.5	mA
Output Leakage ^[1] (DIAG)	I_{OD}	$0 \text{ V} < V_{OD} < 12$ V, DIAG inactive	–1	–	1	μA
		$18 \text{ V} \leq V_{OD} < 80$ V, DIAG inactive	–	–	2.5	mA
LOGIC I/O – DYNAMIC PARAMETERS						
Reset Pulse Width	t_{RST}		0.5	–	4.5	μs
Reset Shutdown Time	t_{RSD}		30	–	–	μs
Input Pulse Filter Time	t_{PIN}	HS, LSn	–	35	–	ns
Clock High Time	t_{SCKH}	A in Figure 4	50	–	–	ns
Clock Low Time	t_{SCKL}	B in Figure 4	50	–	–	ns
Strobe Lead Time	t_{STLD}	C in Figure 4	100	–	–	ns
Strobe Lag Time	t_{STLG}	D in Figure 4	30	–	–	ns
Strobe High Time	t_{STRH}	E in Figure 4	350	–	–	ns
Data Out Enable Time	t_{SDOE}	F in Figure 4, $C_{LOAD} = 10$ pF	–	–	40	ns
Data Out Disable Time	t_{SDOD}	G in Figure 4	–	–	30	ns
Data Out Valid Time From Clock Falling	t_{SDOV}	H in Figure 4, $C_{LOAD} = 10$ pF	–	–	40	ns
Data Out Hold Time From Clock Falling	t_{SDOH}	I in Figure 4	5	–	–	ns
Data In Set-Up Time To Clock Rising	t_{SDIS}	J in Figure 4	15	–	–	ns
Data In Hold Time From Clock Rising	t_{SDIH}	K in Figure 4	10	–	–	ns
Wake Up From Sleep	t_{EN}	$C_{CP} = 2.2$ μF , $C_{REG} = 10$ μF	–	–	3	ms

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ELECTRICAL CHARACTERISTICS (continued): Valid for $T_J = -40$ to 150°C , $V_{BB} = 5.5$ to 80 V, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
CURRENT SENSE AMPLIFIER						
Input Offset Voltage	V_{IOS}	$-1.5\text{ V} < V_{CM} < 2\text{ V}$	-10	-	10	mV
Input Offset Voltage Drift Over Temperature	ΔV_{IOS}		-	± 4	-	$\mu\text{V}/^\circ\text{C}$
Input Bias Current [1]	I_{BIAS}	$V_{ID} = 0\text{ V}$, V_{CM} in range	-50	-	5	μA
Input Offset Current [1]	I_{OS}	$V_{ID} = 0\text{ V}$, V_{CM} in range	-1.5	-	+1.5	μA
Input Common-Mode Range (DC)	V_{CM}	$V_{ID} = 0\text{ V}$	-1.5	-	+2	V
Gain	A_V	Default power-up value	-	35	-	V/V
		Programmable range, SAG[2:0], nominal	10	-	50	V/V
Gain Error	E_A	V_{CM} in range	-1.6	-	+1.6	%
Output Offset	V_{OOS}	Default power-up value	-	2.5	-	V
		Programmable range, SAO[3:0], nominal	0	-	2.5	V
Output Offset Error	E_{VO}	V_{CM} in range, $V_{OOS} > 0\text{ V}$	-10	± 2	+10	%
Small Signal -3 dB Bandwidth at Gain = 25	BW	$V_{IN} = 10\text{ mV}_{pp}$	2	-	-	MHz
Output Settling Time (to within 40 mV)	t_{SET}	$V_{CSO} = 1\text{ V}_{pp}$ square wave, Gain = 20, $C_{OUT} = 50\text{ pF}$	-	-	1	μs
Output Dynamic Range	V_{CSOUT}	$-100\text{ }\mu\text{A} < I_{CSO} < 100\text{ }\mu\text{A}$	0.3	-	4.8	V
Output Voltage Clamp	V_{CSC}	$I_{CSO} = -2\text{ mA}$	4.9	5.2	5.7	V
Output Current Sink [1]	I_{CSsink}	$V_{ID} = 0\text{ V}$, $V_{CSO} = 1.5\text{ V}$, Gain = 20	230	-	470	μA
Output Current Sink (Boosted) [1][5]	$I_{CSsinkb}$	$V_{OOS} = 1.5\text{ V}$, $V_{ID} = -50\text{ mV}$, $V_{CSO} = 1.5\text{ V}$, Gain = 20	1.8	-	4.4	mA
Output Current Source [1]	$I_{CSsource}$	$V_{OOS} = 0\text{ V}$, $V_{ID} = 200\text{ mV}$, $V_{CSO} = 1.5\text{ V}$, Gain = 20	-5.5	-	-1.8	mA
		$V_{ID} = 0\text{ V}$, 100 kHz, Gain = 20	56	65	-	dB
VBB Supply Ripple Rejection Ratio	PSRR	$V_{CSP} = V_{CSM} = 0\text{ V}$, DC, Gain = 20	77	-	-	dB
DC Common-Mode Rejection Ratio	CMRR	V_{CM} step from 0 to 200 mV, Gain = 20	52	100	-	dB
AC Common-Mode Rejection Ratio	CMRR	$V_{CM} = 200\text{ mV}_{pp}$, 100 kHz, Gain = 20	-	62	-	dB
		$V_{CM} = 200\text{ mV}_{pp}$, 1 MHz, Gain = 20	-	43	-	dB
		$V_{CM} = 200\text{ mV}_{pp}$, 10 MHz, Gain = 20	-	25	-	dB
Common Mode Recovery Time (to within 100 mV)	t_{CMrec}	V_{CM} step from -4 V to +1 V, Gain = 20, $C_{OUT} = 50\text{ pF}$	-	-	2.1	μs
Output Slew Rate 10% to 90%	SR	V_{ID} step from 0 to 175 mV, Gain = 20, $C_{OUT} = 50\text{ pF}$	1.8	-	-	V/ μs
Input Overload Recovery (to within 40 mV)	t_{IDrec}	V_{ID} step from 250 mV to 0 V, Gain = 20, $C_{OUT} = 50\text{ pF}$	-	-	2.1	μs

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ELECTRICAL CHARACTERISTICS (continued): Valid for $T_J = -40$ to 150°C , $V_{BB} = 5.5$ to 80 V, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
DIAGNOSTICS AND PROTECTION						
VREG Undervoltage	V_{RON}	V_{REG} rising	7.6	7.95	8.3	V
	V_{ROFF}	V_{REG} falling	6.9	7.2	7.5	V
VREG Overvoltage Warning	V_{ROV}	V_{REG} rising	15.2	15.9	16.6	V
VREG Overvoltage Hysteresis	V_{ROVHys}		1130	1500	1850	mV
VBRG Overvoltage Warning Threshold	V_{BRGOV}	VPO = 0, V_{BRG} rising	52	54	58	V
		VPO = 1, V_{BRG} rising	57	60	63	V
VBRG Overvoltage Hysteresis	$V_{BRGOVHys}$		1.9	2.8	3.6	V
VBRG Undervoltage Threshold	V_{BRGUV}	VPU = 0, V_{BRG} falling	18	19	20	V
		VPU = 1, V_{BRG} falling	32	34	36	V
VBRG Undervoltage Hysteresis	$V_{BRGUVHys}$		1.2	1.6	1.9	V
VBB POR Voltage	V_{BBR}	V_{BB}	–	–	3.8	V
Bootstrap Undervoltage	V_{BCUV}	V_{BOOT} rising, $V_{BOOT} = V_C - V_S$	6.2	7	8.5	V
		V_{BOOT} falling, $V_{BOOT} = V_C - V_S$	5.15	6	7.1	V
Gate Drive Undervoltage Warning HS	V_{GSHUV}	V_{GSH} falling	$V_{BOOT} - 1.35$	$V_{BOOT} - 1$	$V_{BOOT} - 0.85$	V
Gate Drive Undervoltage Warning LS	V_{GSLUV}	V_{GSL} falling	$V_{REG} - 1.35$	$V_{REG} - 1$	$V_{REG} - 0.85$	V
Off-State Gate Drive Overvoltage Warning HS	V_{GSHOV}	V_{GSH} rising	$V_S + 0.85$	$V_S + 1.2$	$V_S + 1.8$	V
Off-State Gate Drive Overvoltage Warning LS	V_{GSLOV}	V_{GSL} rising	$V_{LSS} + 0.85$	$V_{LSS} + 1.2$	$V_{LSS} + 1.8$	V
VIO Undervoltage Threshold	V_{IOON}	A89503KLPTTR-3, V_{IO} rising	2.8	2.9	3.1	V
	V_{IOOFF}	A89503KLPTTR-3, V_{IO} falling	2.4	2.6	2.8	V
	V_{IOON}	A89503KLPTTR-5, V_{IO} rising	4.3	4.5	4.7	V
	V_{IOOFF}	A89503KLPTTR-5, V_{IO} falling	3.7	3.9	4.1	V
VBRG Input Voltage	V_{BRG}	When VDS monitor is active	5.5	V_{BB}	80	V
VBRG Input Current	I_{VBRG}	$V_{DSTH} = \text{default}$, $V_{BB} = 12$ V	–	–	5	mA
	I_{VBRGQ}	Sleep mode $V_{BB} < 70$ V	–	–	5	μA
VDS Threshold – High Side	V_{DSTH}	Default power-up value	–	1.2	–	V
		Programmable range, 7 V $\leq V_{BRG} < 80$ V	0	–	3.15	V
		Programmable range VT[5:0] 5.5 V $\leq V_{BRG} < 7$ V ^[6]	0	–	2.5	V
High-Side VDS Threshold Offset ^[2]	V_{DSTHO}	High-side on, $V_{DSTH} \geq 1$ V, $V_{BRG} > 7$ V	–200	± 100	200	mV
		High-side on, $V_{DSTH} < 1$ V	–150	± 50	150	mV
VDS Threshold – Low Side	V_{DSTL}	Default power-up value	–	1.2	–	V
		Programmable range, $V_{BB} \geq 5.5$ V ^[6]	0	–	3.15	V
Low-Side VDS Threshold Offset ^[2]	V_{DSTLO}	Low-side on, $V_{DSTL} \geq 1$ V, $V_{BRG} > 7$ V	–200	± 100	200	mV
		Low-side on, $V_{DSTL} < 1$ V	–150	± 50	150	mV

Continued on the next page...

ELECTRICAL CHARACTERISTICS (continued): Valid for $T_J = -40$ to 150°C , $V_{BB} = 5.5$ to 80 V, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
DIAGNOSTICS AND PROTECTION (CONTINUED)						
VDS and VGS Qualify Time	t_{VDQ}	Default power-up value (Figure 6)	86.96	102.3	117.65	μs
		Programmable range TVD[9:0], nominal	0	–	102.3	μs
Overcurrent Voltage	V_{OCT}	Default power-up value	0.45	0.6	0.75	V
		Programmable range, OCT[3:0], nominal	0.3	–	4.8	V
Overcurrent Qualify Time	t_{OCQ}		6.75	8.6	9.45	μs
Temperature Warning Threshold [7]	T_{JWH}	Temperature increasing	125	135	145	$^\circ\text{C}$
Temperature Warning Hysteresis [7]	T_{JWHhys}	Recovery = $T_{JWH} - T_{JWHhys}$	–	15	–	$^\circ\text{C}$
Overtemperature Threshold [7]	T_{JF}	Temperature increasing	165	175	185	$^\circ\text{C}$
Overtemperature Hysteresis [7]	T_{JHys}	Recovery = $T_{JF} - T_{JHys}$	–	15	–	$^\circ\text{C}$

[1] For input and output current specifications, negative current is defined as coming out of (being sourced by) the specified device terminal.

[2] VDS offset is the difference between the programmed threshold, V_{DSTH} or V_{DSTL} and the actual trip voltage.

[3] VIO, VDL derived from V_{BB} for internal use only. VDL not accessible on any device terminal.

[4] Verified by design and characterization. Not production tested.

[5] If the amplifier output voltage (V_{CSO}) is more positive than the value demanded by the applied differential input (V_{ID}) and output offset (V_{OOS}) conditions, then output current sink capability is boosted to enhance negative-going transient response.

[6] Maximum value of VDS threshold that should be set in the configuration registers for correct operation when V_{BRG} is within the stated range.

[7] Stated values confirmed by design and characterization (not production tested). Associated function production tested.

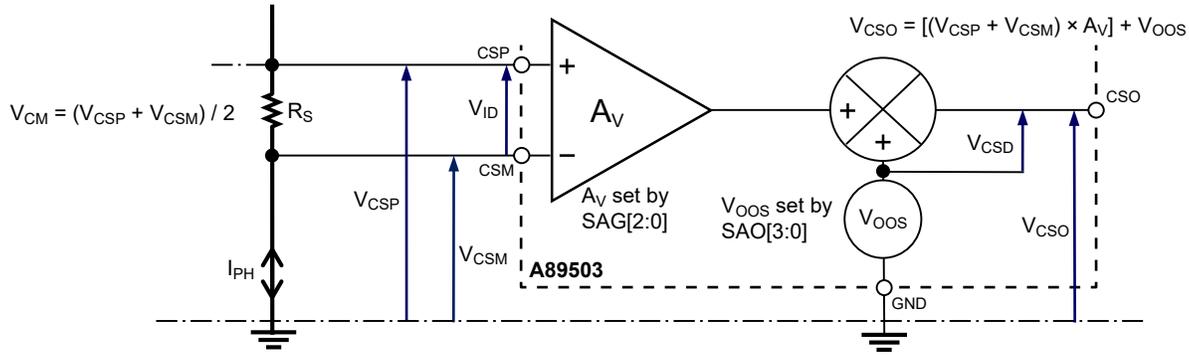


Figure 3: Sense Amplifier Voltage Definitions

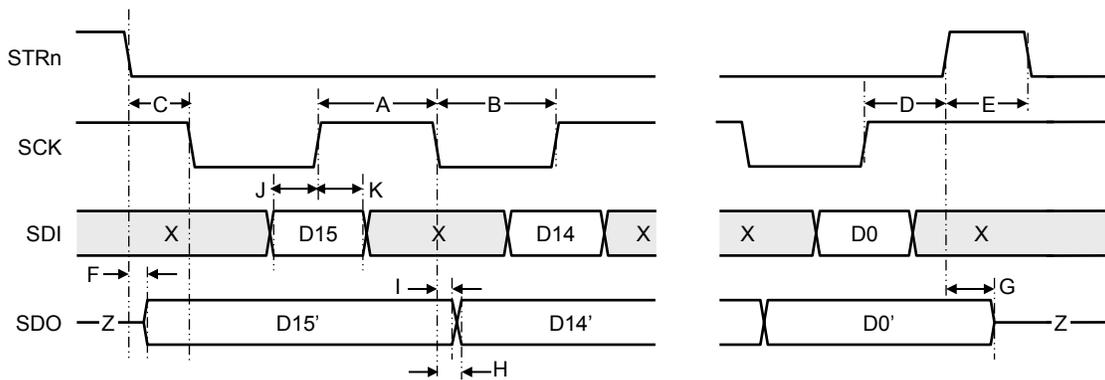


Figure 4: Serial Interface Timing (X = don't care, Z = high impedance (tri-state))

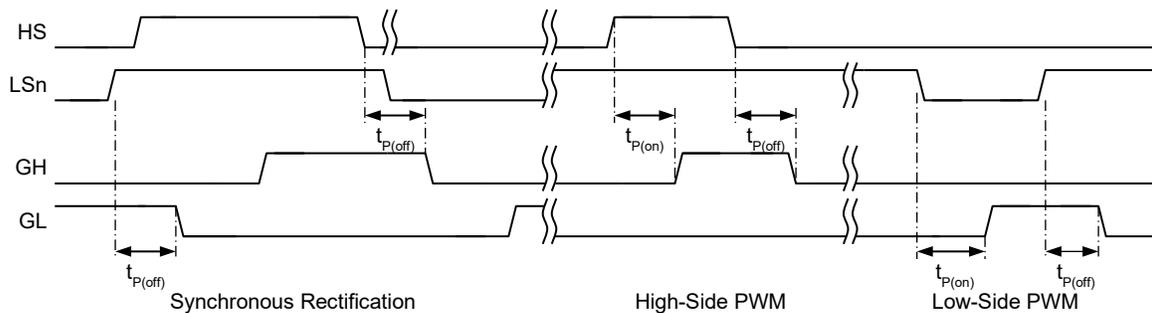


Figure 5: Gate Drive Timing – Control Inputs

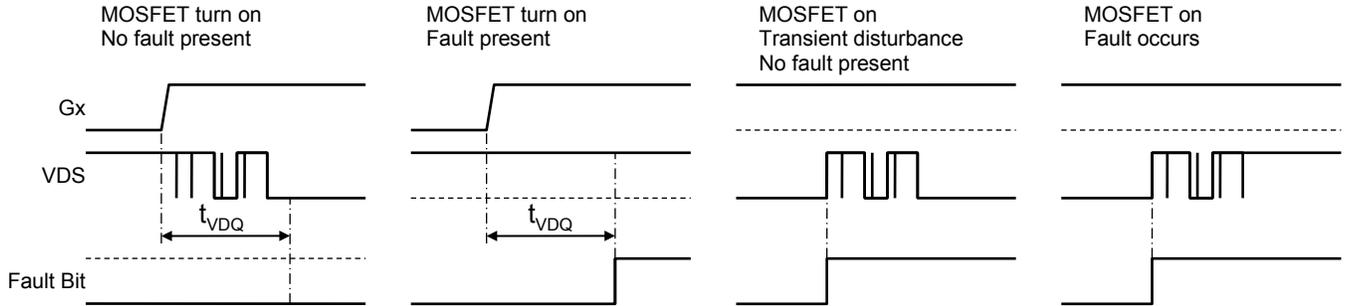


Figure 6a: VDS Fault Monitor – Blank Mode Timing (VDQ = 1)

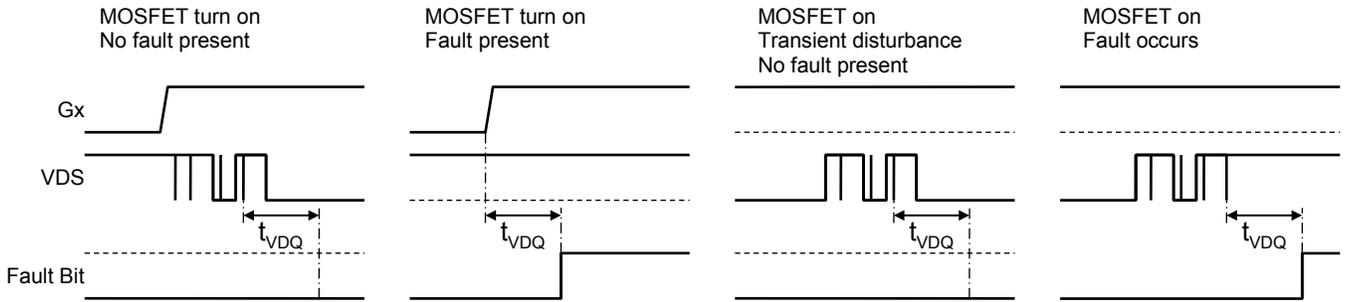


Figure 6b: VDS Fault Monitor – Debounce Mode Timing (VDQ = 0)

LOGIC TRUTH TABLES

Table 1: Control Logic (Control by Logic Inputs)

HS	LSn	GH	GL	S
0	1	LO	LO	Z
0	0	LO	HI	LO
1	1	HI	LO	HI
1	0	HI	HI	HI ^[1]

HI = high-side FET active
 LO = low-side FET active
 Z = high impedance, both FETs off
 All control register bits set to 0, RESETn = 1, ENABLE = 1

^[1] Load connection assumed between S terminal and drain of low-side MOSFET.

Table 2: Control Logic (Control by Serial Register)

HSR	LSR	GH	GL	S
0	0	LO	LO	Z
0	1	LO	HI	LO
1	0	HI	LO	HI
1	1	HI	HI	HI ^[1]

HI = high-side FET active
 LO = low-side FET active
 Z = high impedance, both FETs off
 HS = 0, LSn = 1, RESETn = 1, ENABLE = 1

^[1] Load connection assumed between S terminal and drain of low-side MOSFET.

Table 3: Control combination logic table – Logic Inputs and Serial Register

Terminal	Register	Internal
HS	HSR	HI
0	0	0
0	1	1
1	0	1
1	1	1

Terminal	Register	Internal
LSn	LSR	LO
1	0	0
1	1	1
0	0	1
0	1	1

Internal control signals (HI, LO) are derived by combining the logic states applied to the control input terminals (HS, LSn) with the bit patterns held in the Control register (HSR, LSR).

Normally the input terminals or the Control register method is used for control with the other being held inactive (all terminals or bits at logic 0).

ENABLE	HI	LO	GH	GL	S	Comment
1	0	0	L	L	Z	Bridge Disabled
1	0	1	L	H	LO	Bridge Sinking
1	1	0	H	L	HI	Bridge Sourcing
1	1	1	H	H	U ^[1]	Cross-Conduction
0	X	X	L	L	Z	Bridge Disabled

RESETn = 1
 HI = high-side FET active
 LO = low-side FET active
 X = don't care
 Z = high impedance, both FETs off
 U = undefined, both FETs on

^[1] If the MOSFETs are configured as a half bridge the state of S will be undefined.
 If the load is connected between the S terminal and drain of low-side MOSFET then S will be HI

FUNCTIONAL DESCRIPTION

The A89503 is a half-bridge (H-bridge) MOSFET driver (pre-driver) requiring a single unregulated supply of 5.5 to 80 V. It includes an integrated linear regulator to supply the internal logic. All logic inputs are compatible with 3.3 V logic (A89503KLPTR-3) or 5 V logic (A89503KLPTR-5) depending on part number selection.

The two high-current gate drives are capable of driving a wide range of N-channel power MOSFETs, and are configured as a half-bridge driver with one high-side drive and one low-side drive. The A89503 provides all necessary circuits to ensure that the gate-source voltage of both high-side and low-side external FETs are above 10 V, at supply voltages down to 7 V. For extreme battery voltage drop conditions, correct functional operation is guaranteed at supply voltages down to 5.5 V, but with a reduced gate drive voltage.

Gate drives can be controlled directly through the logic input terminals or through an SPI-compatible serial interface. Fully independent control allows both external FETs to be turned on at the same time. All logic inputs, except RESETn, are standard CMOS levels and can be compatible with 3.3 V (A89503KLPTR-3) or 5 V (A89503KLPTR-5) logic outputs depending on part number selection. The logic inputs are battery voltage compliant, meaning they can be shorted to ground or supply without damage, up to the maximum battery voltage of 80 V.

A low-power sleep mode allows the A89503, the power bridge, and the load to remain connected to a vehicle battery supply without the need for an additional supply switch.

The A89503 includes several diagnostic features to provide indication and/or protection against undervoltage, overtemperature, and power bridge faults. A single diagnostic output provides basic fault indication and detailed diagnostic information is available through the serial interface. The serial interface also provides access to programmable fault blanking time and programmable VDS threshold for short detection.

The A89503 includes a low-side current sense amplifier with programmable gain and offset. The amplifier is specifically designed for current sensing in the presence of high voltage and current transients.

Input and Output Terminal Functions

VBB: Main power supply for internal regulators and charge pump. The main power supply should be connected to VBB through a reverse voltage protection circuit and should be decoupled with ceramic capacitors connected close to the supply and ground terminals.

VBRG: Sense input to the top of the external MOSFET bridge. Allows accurate measurement of the voltage at the drain of the high-side MOSFET in the bridge.

CP1, CP2: Pump capacitor connection for charge pump. Connect a ceramic capacitor with a recommended nominal value of 2.2 μ F between CP1 and CP2. This should have a rated working voltage of at least 25 V and a tolerance of $\pm 20\%$ or better.

VREG: Regulated voltage, 11 V, used to supply the low-side gate drivers and to provide current for the above supply charge pump. A sufficiently large storage capacitor must be connected to this terminal to provide the required transient charging current.

GND: Analog, digital, and power ground. Connect to supply ground—see Layout Recommendations.

C: High-side connection for the bootstrap capacitor and positive supply for the high-side gate driver.

GH: High-side, gate-drive output for an external N-channel MOSFET.

S: Source connection for high-side MOSFET providing the negative supply connections for the floating high-side driver.

GL: Low-side gate-drive output for an external N-channel MOSFET.

LSS: Low-side return path for discharge of the capacitance on the low-side MOSFET gate, connected to the source of the low-side external MOSFET independently through a low-impedance track.

HS: Logic inputs with pull-down to control the high-side gate drive. Battery voltage compliant terminal.

LSn: Logic input with pull-up to control the low-side gate drive. Active-low input. Battery voltage compliant terminal.

ENABLE: Logic input to enable the gate drive outputs. Battery voltage compliant terminal.

RESETn: Clears latched fault states that may have disabled the outputs when taken low for the reset pulse width, t_{RST} . Forces low-power shutdown (sleep) when held low for more than the RESET shutdown time, t_{RSD} . Battery voltage compliant terminal.

SDI: Serial data logic input with pull-down. 16-bit serial word input msb first.

SDO: Serial data output. High impedance when STRn is high. Outputs bit 15 of the diagnostic register, the fault flag, as soon as STRn goes low.

SCK: Serial clock logic input with pull-down. Data is latched in from SDI on the rising edge of SCK. There must be 16 rising edges per write and SCK must be held high when STRn changes.

STRn: Serial data strobe and serial access enable logic input with pull-up. When STRn is high, any activity on SCK or SDI is ignored and SDO is high impedance, allowing multiple SDI slaves to have common SDI, SCK, and SDO connections.

CSP, CSM: Current sense amplifier inputs.

CSO: Current sense amplifier output.

D: Drain connection for low-side MOSFET.

DIAG: Diagnostic output. Provides general fault flag output.

Power Supplies

A single power supply voltage is required. The main power supply, V_{BB} , should be connected to VBB through a reverse voltage protection circuit. A 100 nF ceramic decoupling capacitor must be connected close to the supply and ground terminals.

A low power independent internal regulator provides the supply voltage, V_{DL} , to the internal logic. A second integrated linear regulator provides the supply voltage, V_{IO} , to all logic inputs and push-pull outputs. This digital I/O is set to 3.3 V (A89503KLPTR-3) or 5 V (A89503KLPTR-5).

All internal logic is guaranteed to operate correctly to below the regulator undervoltage levels, ensuring that the A89503 will continue to operate safely until all logic is reset when a power-on-reset state is present.

The A89503 will operate within specified parameters with V_{BB} from 7 to 80 V and will function correctly with a supply down to 5.5 V. This provides a rugged solution for use in the harsh automotive environment.

Pump Regulator

The gate drivers are powered by an internal regulator which limits the supply to the drivers and therefore the maximum gate voltage. This regulator uses a charge pump scheme with switching frequency of 62.5 kHz. At low supply voltage, the regulated supply is maintained by a charge pump boost converter which requires a pump capacitor connected between the CP1 and CP2 terminals. This capacitor should have a nominal value of 2.2 μ F, rated working voltage of at least 25 V, and a tolerance of $\pm 20\%$

or better. At supply voltage greater than 14 V, the pump regulator stops boosting and becomes a linear regulator.

The regulated voltage, V_{REG} , is available on the VREG terminal. A sufficiently large storage capacitor (see Applications section) must be connected to this terminal to provide the transient charging current to the low side drivers and the bootstrap capacitors.

Gate Drives

The A89503 is designed to drive external, low on-resistance, power N-channel MOSFETs. It will supply the large transient currents necessary to quickly charge and discharge the external MOSFET gate capacitance in order to reduce dissipation in the external MOSFET during switching. The charge current for the low-side drive is provided by the capacitor on the VREG terminal. The charge current for the high-side drives is provided by the bootstrap capacitor connected between the C and S terminals. MOSFET gate charge and discharge rates may be controlled by setting a group of parameters via the serial interface or by using an external gate resistor between the gate drive output and the gate terminal of the MOSFET.

Operational Configurations

The high-side and low-side gate drives are completely independent. The A89503 permits any combination of active high-side and low-side MOSFETs and does not provide any lockout or internally generated dead time. This allows the A89503 to be used in a complementary half-bridge configuration or to drive independent high-side and low-side MOSFETs.

In a simple half-bridge configuration, this allows more precise control of the timing of the MOSFET switching. In some circumstances, simultaneous activation of both high-side and low-side MOSFETs can be used to reduce diode conduction during synchronous rectification, which improves overall efficiency and reduces electromagnetic emissions. The precise timing and any required dead time must be provided by the external controller.

An example of independent driving is to use one gate drive output as a PWM control and the other as an on-off control. For example, the low-side drive can be used to enable current flow through the load and the high-side drive can be used to provide PWM current control. This example is shown in Figure 7. The low-side MOSFET enables or disables the flow of current, and the high-side MOSFET is used with the low-side recirculation diode to provide PWM current control.

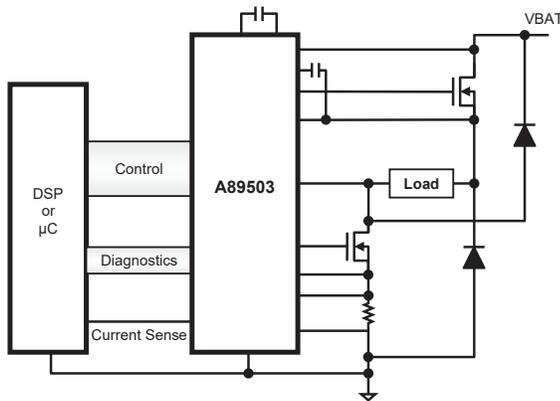


Figure 7: PWM Load current control

Bootstrap Supply

When the high-side drivers are active, the reference voltage for the driver will rise to close to the bridge supply voltage. The supply to the driver will then have to be above the bridge supply voltage to ensure that the driver remains active. This temporary high-side supply is provided by a bootstrap capacitor connected between the bootstrap supply terminal, C, and the high-side reference terminal, S.

The bootstrap capacitor is independently charged to approximately V_{REG} when the associated reference S terminal is low. When the output swings high, the voltage on the bootstrap supply terminal rises with the output to provide the boosted gate voltage needed for the high-side N-channel power MOSFETs.

Bootstrap Charge Cycle Considerations

The user must ensure that the bootstrap capacitor does not become discharged below the bootstrap undervoltage threshold, V_{BCUV} , or a bootstrap fault will be indicated and the outputs disabled. This can happen if the S terminal is not low enough for a long enough period to charge the bootstrap capacitor—for example, when the PWM duty cycles is very high and the charge time for the bootstrap capacitor is insufficient to ensure a sufficient recharge to match the MOSFET gate charge transfer during turn on.

If for any reason the bootstrap capacitor cannot be sufficiently charged, a bootstrap fault will occur—see Diagnostics section for further details.

Note that when the A89503 is used in the configuration shown in Figure 7 with an inductive load, the bootstrap capacitor is

charged in two ways depending on the current flowing in the load.

When no current is flowing in the load, the high-side MOSFET will be off and the bootstrap capacitor can be charged directly through the load by turning on the low-side MOSFET. This procedure should be followed before the first attempt to turn on the high-side MOSFET.

When current is flowing in the load and is controlled by PWM switching the high-side MOSFET, the bootstrap capacitor is charged through the load during a PWM off time. During the PWM off time, the current will continue to flow through the load inductance, pulling the voltage at the S terminal to a negative value in order to forward bias the recirculation diode.

Top-Off Charge Pump

If the high-side MOSFET is used as an enabling switch—for example, with a simple resistive load or when using low-side PWM switching—then once the MOSFET has been switched on, it will be held in the on state by an additional charge pump in the A89503 referred to as the “top-off” charge pump.

The top-off charge pump will allow the high-side drive to maintain the gate voltage on the external MOSFET indefinitely if required. This is a low current trickle charge pump and is only operated after a high side has been turned on. A small amount of bias current is drawn from the C terminal to operate the floating high-side circuit and the charge pump simply provides enough drive to ensure the bootstrap voltage, and hence the gate voltage, will not droop due to this bias current.

In some applications, a safety resistor is added between the gate and source of each MOSFET in the bridge. When a high-side MOSFET is held in the on state, the current through the associated high-side gate-source resistor (R_{GSH}) is provided by the high side driver and therefore appears as a static resistive load on the top-off charge pump. The minimum value of R_{GSH} for which the top-off charge pump can provide current, without dropping below the bootstrap undervoltage threshold, is defined in the Electrical Characteristics table.

In all cases, the charge required for initial turn-on of the high-side gate is always supplied by the bootstrap capacitor. If the bootstrap capacitor becomes discharged, the top-off charge pump alone will not provide sufficient current to allow the MOSFET to turn on.

High-Side Gate Drive

A high-side gate-drive output for external N-channel MOSFETs is provided on the GH terminal. GH = 1 (or “high”) means that

the upper half of the driver is turned on and its drain will source current to the gate of the high-side MOSFET in the external load-driving bridge, turning it on. $GH = 0$ (or “low”) means that the lower half of the driver is turned on and its drain will sink current from the external MOSFET’s gate circuit to the S terminal, turning it off.

The reference point for the high-side drive is the load connections, S. This terminal senses the voltage at the load connections. This terminal is also connected to the negative side of the bootstrap capacitor and is the negative supply reference connections for the floating high-side driver. The discharge current from the high-side MOSFET gate capacitance flows through these connections which should have low-impedance traces to the MOSFET bridge.

Low-Side Gate Drive

The low-side gate-drive output on GL is referenced to the LSS terminal. This output is designed to drive an external N-channel power MOSFET. $GL = 1$ (or “high”) means that the upper half of the driver is turned on and its drain will source current to the gate of the low-side MOSFET in the external power bridge, turning it on. $GL = 0$ (or “low”) means that the lower half of the driver is turned on and its drain will sink current from the external MOSFET’s gate circuit to the LSS terminal, turning it off.

The LSS terminal provides the return path for discharge of the capacitance on the low-side MOSFET gate. This terminal is connected independently to the source of the low-side external MOSFETs through a low-impedance track.

An integrated slew control feature allows the MOSFET gate charge and discharge rates to be controlled via the serial interface as detailed in the Gate Drive Control section.

Either the internal slew control or an external resistor between the gate drive output and the gate connection to the MOSFET (as close as possible to the MOSFET) can be used to control the slew rate seen at the gate, thereby controlling the di/dt and dv/dt of the voltage at the S terminal.

Gate Drive Passive Pull-Down

Each gate drive output includes a discharge circuit to ensure that any external MOSFET connected to the gate drive output is held off when the power is removed. This discharge circuit appears as 950 k Ω between the gate drive and the source connections for each MOSFET. It is only active when the A89503 is not driving the output to ensure that any charge accumulated on the MOSFET gate has a discharge path even when the power is not connected.

Gate Drive Control

MOSFET gate drives are controlled according to the values set in Config 6, 7, and 8 registers.

MOSFET off-to-on transitions are controlled as detailed in Figure 8a. When a gate drive is commanded to turn on a current, I_1 (as defined by $IR1[3:0]$), is sourced on the GH or GL terminal for a duration, t_1 (defined by $TR[3:0]$). These parameters should typically be set to quickly charge the MOSFET input capacitance to the start of the Miller region as drain-source voltage does not change during this period. Thereafter the current sourced on GH or GL is set to a value of I_2 (as defined by $IR2[3:0]$) and remains at this value while the MOSFET transitions through the Miller region and reaches the fully on state. For low-side gate drives, the MOSFET fully on state is defined as the voltage on GL gate drive output rising to a value within 1 V(typ) of V_{REG} . For the high-side gate drives the MOSFET fully on state is defined as the voltage on GH gate drive output rising to a value within 1 V(typ) of the C terminal. I_2 should be set to achieve the required input capacitance charge time. Once in the fully on state, the GH or GL output switches from current to voltage drive to hold the MOSFET in the on state.

If the values of $IR1[3:0]$ and $IR2[3:0]$ are set to 0, GH or GL produces maximum drive to turn on the MOSFET as quickly as possible without attempting to control the MOSFET input capacitance charge time (Figure 8b). The value of $TR[3:0]$ has no effect on switching speed.

MOSFET on-to-off transitions are controlled as detailed in Figure 8c. When a gate drive is commanded to turn off a current, I_1 (as defined by $IF1[3:0]$), is sunk by the GH or GL terminal for a duration, t_1 (defined by $TF[3:0]$). These parameters should typically be set to quickly discharge the MOSFET input capacitance to the start of the Miller region as drain-source voltage does not change during this period. Thereafter, the current sunk by GH or GL is set to a value of I_2 (as defined by $IF2[3:0]$) and remains at this value while the MOSFET transitions through the Miller region and reaches the fully off state. For the low-side gate drives, the MOSFET fully off state is defined as the voltage on the GL gate drive output falling to a value within 1 V(typ) of LSS. For the high-side gate drives, the MOSFET fully off is defined as the voltage on the GH gate drive output falling to a value within 1 V(typ) of the S terminal. I_2 should be set to achieve the required MOSFET input capacitance discharge time. Once in the fully off condition, the GH or GL output switches from current to voltage drive to hold the MOSFET in the off state. If the values of $IF1[3:0]$ and $IF2[3:0]$ are set to 0, GH or GL produces maximum drive to turn off the MOSFET as quickly

as possible without attempting to control the MOSFET input capacitance discharge time (Figure 8d). The value of TF[3:0] has no effect on switching speed.

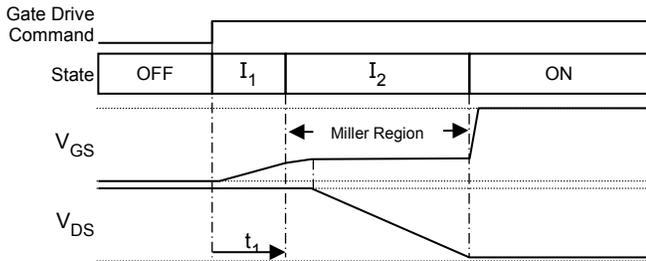


Figure 8a: Off-to-On Transition (Gate Drive)

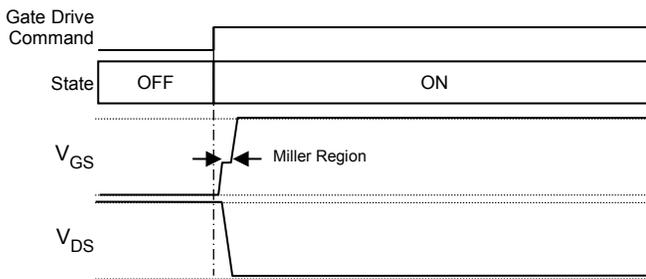


Figure 8b: Off-to-On Transition (Switched)

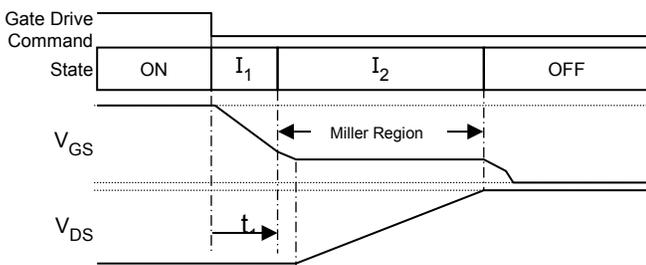


Figure 8c: On-to-Off Transition (Gate Drive)

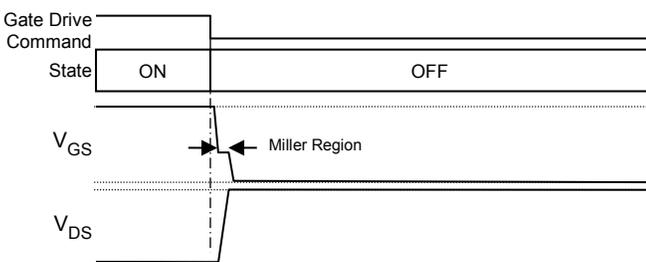


Figure 8d: On-to-Off Transition (Switched)

Logic Control Inputs

Two logic level digital inputs provide direct control for the gate drives, one for each drive. These are standard CMOS levels referenced to the voltage of the logic I/O regulator. All have a typical hysteresis of 500 mV to improve noise performance. Each input can be shorted to the VBB supply, up to the absolute maximum supply voltage, without damage to the input.

Input HS is active high and controls the high-side drive. LSn is active low and controls the low-side drive. HS has a pull-down resistor and LSn has a pull-up resistor to ensure an off state should the control signal become disconnected. The logical relationship between the inputs and the gate drive outputs is defined in Table 1.

The gate drive outputs can also be controlled through the serial interface by setting the appropriate bit in the control register. In the control register, all bits are active high. The logical relationship between the register bit setting and the gate drive outputs is defined in Table 2.

The logic inputs are combined, using logical OR, with the corresponding bits in the serial interface control register to determine the state of the gate drive. The logical relationship between the combination of logic input and register bit setting and the gate drive outputs is defined in Table 3. In most applications, either the logic inputs or the serial control will be used. When using only the logic inputs to control the bridge, the serial register should be left in the reset condition with all control bits set to 0. When using only the serial interface to control the bridge, the inputs should be tied such that the active low inputs are pulled high and the active high inputs connected to GND, i.e., HS tied to GND and LSn tied high.

Output Disable

The ENABLE input is connected directly to the gate drive output command signal, bypassing all gate drive control logic. This can be used to provide a fast output disable (emergency cutoff).

Sleep Mode

RESETn is an active-low input which allows the A89503 to enter sleep mode, in which the current consumption from the VBB supply and internal logic regulator is reduced to its minimum level. When RESETn is held low for longer than the reset shutdown time, t_{RSD} , the regulator and all internal circuitry is disabled and the A89503 enters sleep mode. In sleep mode, the latched faults and corresponding fault flags are cleared. When coming out of sleep mode, the protection logic ensures that the gate drive

outputs are off until the charge pump reaches its correct operating condition. The charge pump will stabilize in less than 3 ms under nominal conditions.

To allow the A89503 to start up without the need for an external logic input, the RESETn terminal can be pulled to VBB with an external pull-up resistor.

RESETn can also be used to clear any fault conditions without entering sleep mode by taking it low for the reset pulse width, t_{RST} . Any latched short detection fault, which disables the outputs, will be cleared, as will the serial fault register.

Current Sense Amplifier

A programmable gain, differential sense amplifier is provided to allow the use of low-value sense resistors or current shunt as a low-side current sensing element. The input common mode range of the CSP and CSM inputs and programmable output offset allow below ground current sensing typically required for low-side current sense in PWM control of motors, or other inductive loads, during switching transients. The output of the sense amplifier is available at the CSO output and can be used in peak or average current control systems. The output can drive up to 4.8 V to permit maximum dynamic range with higher input voltage A-to-D converters.

The gain of the sense amplifier is defined by the contents of the SAG[2:0] variable as:

SAG	Gain
0	10
1	15
2	20
3	25

SAG	Gain
4	30
5	35
6	40
7	50

The output offset, V_{OOS} , of the sense amplifier is defined by the contents of the SAO[3:0] variable as:

SAO	V_{OOS}
0	0
1	0
2	100 mV
3	100 mV
4	200 mV
5	300 mV
6	400 mV
7	500 mV

SAO	V_{OOS}
8	750 mV
9	1 V
10	1.25 V
11	1.5 V
12	1.75 V
13	2 V
14	2.25 V
15	2.5 V

The state of the SAT bit in the Config 5 register determines the voltage available on the CSO terminal. If SAT = 0, CSO carries the ground referenced V_{CSO} voltage, and if SAT = 1, CSO carries the output offset voltage V_{OOS} .

Diagnostic Monitors

Multiple diagnostic features provide three levels of fault monitoring. These include critical protection for the A89503, monitors for operational voltages and states, and detection of the power bridge and load fault conditions. All diagnostics, except for POR, serial transfer error, EEPROM fault, and overtemperature, can be masked by setting the appropriate bit in the mask registers.

Table 4: Diagnostic Functions

Name	Diagnostic	Level
POR	Internal logic supply undervoltage causing power-on reset	Chip
SE	Serial transmission error	Chip
EE	EEPROM error	Chip
OT	Chip junction over temperature	Chip
TW	High chip junction temperature warning	Monitor
VSO	VBRG supply overvoltage (Load dump detection)	Monitor
VSU	VBRG supply Undervoltage	Monitor
VRO	VREG output overvoltage	Monitor
VRU	VREG output undervoltage	Monitor
VLU	Logic I/O regulator undervoltage	Monitor
OC	Over current	Bridge
VBS	Bootstrap undervoltage	Bridge
HU	High-side VGS undervoltage	Bridge
LU	Low-side VGS undervoltage	Bridge
HO	High-side VDS overvoltage	Bridge
LO	Low-side VDS overvoltage	Bridge
HGO	High-side off-state VGS overvoltage	Bridge
LGO	Low-side off-sate VGS overvoltage	Bridge

The fault status is available from the status and diagnostic registers accessed through the serial interface.

DIAG Output

The DIAG terminal provides a single diagnostic output signal that outputs a general logic-level fault flag. DIAG remains low while any fault except SE or OC is present or if one of the latched faults has been detected and the general fault flag has not been reset since then. When the general fault flag is reset, the DIAG output will be high.

Status and Diagnostic Registers

The serial interface allows detailed diagnostic information to be read from the diagnostic registers on the SDO output terminal at any time.

A system status register provides a summary of all faults in a single read transaction. The status register is always output on SDO when any register is written.

The first bit (bit 15) of the status register contains a common fault flag, FF, which will be high if any of the fault bits in the status register have been set. This allows fault condition to be detected using the serial interface by simply taking STRn low. As soon as STRn goes low, the first bit in the status register can be read on SDO to determine if a fault has been detected at any time since the last fault register reset. In all cases the fault bits in the diagnostic registers are latched and only cleared after a fault register reset.

FF provides an indication that a fault has occurred since the last fault reset and one or more fault bits have been set.

Note that FF (bit 15) does not provide the same function as the general fault flag output on the DIAG terminal. The fault flag output on the DIAG terminal provides an indication that either a fault is present or the outputs have been disabled due to a latched fault state. FF provides an indication that a fault has occurred since the last fault reset and one or more fault bits have been set.

Chip-Level Protection

Chip-wide parameters critical for correct operation of the A89503 are monitored. These include maximum chip temperature, minimum internal logic supply voltage, and the serial interface transmission. These three monitors are necessary to ensure that the A89503 is able to respond as specified.

CHIP FAULT STATE: INTERNAL LOGIC UNDERVOLTAGE

The A89503 has an independent internal logic regulator to supply the internal logic. This is to ensure that external events, other than loss of supply, do not prevent the A89503 from operating correctly. The internal logic supply regulator will continue to operate with a low supply voltage, for example, if the main supply voltage drops to a very low value during a severe cold crank event. In extreme low supply circumstances, or during power-up or power-down, an undervoltage detector ensures that the A89503 operates correctly. The logic supply undervoltage lockout cannot be masked as it is essential to guarantee correct operation over the full supply range.

When power is first applied to the A89503, the internal logic is prevented from operating, and all gate drive outputs are held in the off state until the internal regulator voltage, V_{DL} , exceeds the logic supply undervoltage lockout rising (turn-on) threshold. At this point, all serial control registers will be reset to their power-on state and all fault states will be reset. The FF bit and the POR bit in the status register will be set to one to indicate that a power-on-reset has taken place. Other Diagnostic and Status register bits including V_{IO} , V_{REG} , and V_{BB} undervoltages may immediately then be set as a result of startup conditions within the part. It is recommended that the Diagnostic and Status registers are read after V_{IO} , V_{REG} , and V_{BB} have settled within their respective operating ranges to clear any fault indications of this type. The A89503 then goes into its fully operational state and begins operating as specified.

Once the A89503 is operational, the internal logic supply continues to be monitored. If, during the operational state, V_{DL} drops below logic supply undervoltage lockout falling (turn-off) threshold, derived from V_{BBR} , then the logical function of the A89503 cannot be guaranteed and the outputs will be immediately disabled. The A89503 will enter a power-down state and all internal activity, other than the logic regulator voltage monitor will be suspended. If the logic supply undervoltage is a transient event, then the A89503 will follow the power-up sequence above as the voltage rises. As long as V_{BB} remains above the POR voltage, V_{BBRmax} , the logic within the A89503 will remain active.

CHIP FAULT STATE: OVERTEMPERATURE

If the chip temperature rises above the over temperature threshold, T_{JF} , the over temperature bit, OT, will be set in the status register. If FOT = 1 when an overtemperature is detected, all gate drive outputs will be disabled automatically. If FOT = 0, then no circuitry will be disabled and action must be taken by the user to limit the power dissipation in some way so as to prevent overtemperature damage to the chip and unpredictable device operation. When the temperature drops below T_{JF} by more than the hysteresis value, T_{JFHys} , the fault state is cleared, and when FOT = 1, the outputs re-enabled. The overtemperature bit remains in the status register until reset.

CHIP FAULT STATE: SERIAL ERROR

If there are more than 16 rising edges on SCK or if STRn goes high and there are fewer than 16 rising edges on SCK or the parity is not odd, then the write will be cancelled without writing data to the registers and the SE bit will be set to indicate a data transfer error. If the transfer is a write, then the status register will not be reset. If the transfer is a diagnostic register read, then the addressed register will not be reset.

If a serial error is detected and $FSE = 1$, then all gate drive outputs will be driven low (disabled) until the next valid frame is sent to the A89503. If $FSE = 0$, then no further action will be taken.

CHIP FAULT STATE: EEPROM

Configuration and calibration information is stored within internal EEPROM and loaded into working registers to configure the device at power up. As part of this process, a data integrity check is carried out. If the check returns a single bit error, automatic error correction is applied and the part starts up. If the check returns a multiple bit error, all gate drives are disabled, the general fault flag is set low, and the EEPROM error bit, EE, is set in the Status register. EEPROM faults can only be cleared by a power-on-reset (POR).

Operational Monitors

Parameters related to the safe operation of the A89503 in a system are monitored. These include parameters associated with external active and passive components, power supplies, and interaction with external controllers.

Voltages relating to driving the external power MOSFETs are monitored, specifically V_{REG} , the bootstrap capacitor voltage, and the V_{GS} of each gate drive output. The bridge supply voltage, V_{BRG} , is monitored for both overvoltage and undervoltage events.

MONITOR: VREG VOLTAGE (VR: VRO, VRU)

The internal charge-pump regulator supplies the low-side gate driver and the bootstrap charge current. It is critical to ensure that the regulated voltage, V_{REG} , at the VREG terminal is sufficiently high before enabling any of the outputs.

If V_{REG} goes below the VREG undervoltage threshold, V_{ROFF} , the VREG undervoltage bit, VRU, will be set in the diagnostic register.

If a VREG undervoltage state is present and $FVRU = 1$, all gate drive outputs go low. When V_{REG} rises above the rising threshold, V_{RUON} , the fault is cleared and, if $FVRU = 1$, the gate drive outputs are re-enabled. The VRU bit remains in the diagnostic register until cleared. If $FVRU = 0$, fault reporting will be the same but the gate drive outputs are not disabled and appropriate action to avoid potential misoperation or damage to the A89503 and/or bridge MOSFETs must be taken by the external controller.

The VREG undervoltage monitor circuit is active during power up. If $FVRU = 1$, all gate drives will be low until V_{REG} is greater than the rising threshold, V_{RON} . If $FVRU = 0$, the gate drive out-

puts will be active as soon as there is sufficient voltage on VREG to activate the gate drive outputs.

Note that this is sufficient to turn on standard threshold external power MOSFETs at a battery voltage as low as 5.5 V, but the on-resistance of the MOSFET may be higher than its specified maximum.

The VREG undervoltage monitor can be disabled by setting the VRU bit in the mask register. Although not recommended, setting VRU to 1 or FVRU to 0 can allow the A89503 to operate below its minimum specified supply voltage level with a severely impaired gate drive. The specified electrical parameters will not be valid in this condition.

The output of the VREG regulator is also monitored to detect any overvoltage applied to the VREG terminal.

If V_{REG} goes above the VREG overvoltage threshold, V_{ROV} , the VREG overvoltage bit, VRO, will be set in the diagnostic register. If $FVRO = 1$, all gate drive outputs go low, the motor drive is disabled, and the motor coasts. If $FVRO = 0$, no action is taken and the outputs are protected from overvoltage by independent Zener clamps. When V_{REG} falls below V_{ROV} by more than the hysteresis voltage, V_{ROVHys} , the fault state is cleared but the VRO bit remains in the diagnostic register until cleared.

MONITOR: TEMPERATURE WARNING

If the chip temperature rises above the temperature warning threshold, T_{JW} , the hot warning bit, TW, will be set in the status register and if $FTW = 1$, all gate drives will be low. If $FTW = 0$, gate drives will remain active. When the temperature drops below T_{JW} by more than the hysteresis value, T_{JWHys} , the fault state is cleared and the TW bit remains in the status register until reset.

MONITOR: VBRG SUPPLY OVERVOLTAGE AND UNDERVOLTAGE

The main battery voltage supply to the bridge, V_{BRG} , is monitored by the A89503 on the VBRG terminal to indicate if the supply voltage has exceeded its normal operating range (for example, during a load dump transient). If V_{BRG} rises above the VBRG overvoltage warning threshold, V_{BRGOV} , then the general fault flag will be set, the VSO bit will be set in Diagnostic 2 register, the VS bit (which indicates the logical OR of the VSO and VSU bits) will be set in the Status register. When V_{BRG} drops below the falling VBRG overvoltage falling threshold, $V_{BRGOV} - V_{BRGOVHys}$, the general fault flag will be cleared but the VSO and VS bits will remain set until the Diagnostic 2 register is read. The VBRG overvoltage warning threshold can be set to one of two levels using the VPO bit.

If V_{BRG} falls below the VBRG undervoltage warning threshold, V_{BRGUV} , then the VSU bit will be set in the Diagnostic 2 register and the VS bit (which indicates the logical OR of the VSO and VSU bits) will be set in the Status register. If $FVSU = 1$, the general fault flag will be set and all the drive outputs will be driven low (disabled) causing the motor to coast. When VBRG moves above the rising VBRG undervoltage threshold, $V_{BRGUV} + V_{BRGUVHys}$, the general fault flag will be cleared and the gate drive outputs will be re-enabled but the VSU and VS bits will remain set until the Diagnostic 2 register is read. If $FVSU = 0$, fault reporting will be the same but the gate drive outputs will not be disabled. The VBRG undervoltage warning threshold can be set to one of two level using the VPU bit.

MONITOR: VIO UNDERVOLTAGE

The logic I/O voltage, V_{IO} , is monitored to ensure that the logic interface voltage is high enough to permit correct operation of the logic input buffers. If V_{IO} drops below the falling undervoltage threshold, V_{IOOFF} , the regulator undervoltage bit, VLU, will be set in the status register, the general fault flag will be set low, and all gate drive outputs will be disabled. When V_{IO} rises above the rising threshold, V_{IOON} , the gate drive outputs will revert to the commanded state and the general fault flag will be reset. The VLU fault bit remains in the status register until cleared.

Power Bridge and Load Faults

BRIDGE: OVERCURRENT DETECT

The output from the sense amplifier can be compared to an overcurrent threshold voltage, V_{OCT} , to provide indication of overcurrent events. V_{OCT} is generated by a 4-bit DAC with a resolution of 300 mV and defined by the contents of the OC[3:0] variable and the contents of the SAO[3:0] variable. V_{OCT} is approximately defined as:

$$V_{OCT} = [(n + 1) \times 300 \text{ mV}]$$

where n is a positive integer defined by OCT[3:0]

Any offset programmed on SAO[3:0] is applied to both the current sense amplifier output, V_{CSO} , and the Overcurrent threshold, V_{OCT} , and has no effect on the overcurrent threshold, I_{OCT} . The relationship between the threshold voltage and the threshold current is approximately defined as:

$$I_{OCT} = V_{OCT} / (R_S \times A_V)$$

where V_{OCT} is the overcurrent threshold voltage programmed by OCT[3:0], R_S is the sense resistor value in Ω and A_V is the sense amp gain defined by SAG[2:0].

The output from the overcurrent comparator is filtered by an overcurrent qualifier circuit. This circuit uses a timer to verify that the output from the comparator is indicating a valid overcurrent event. The qualifier can operate in one of two ways, debounce or blanking, selected by the OCQ bit.

In the default debounce mode, a timer is started each time the comparator output indicates an overcurrent. This timer is reset when the comparator changes back to indicate normal operation. If the debounce timer reaches the end of the timeout period, set by t_{OCQ} , then the overcurrent event is considered valid and the overcurrent bit, OC, will be set in the Diag 2 register.

In the optional blanking mode, a timer is started when a low-side gate drive is turned on. The output from the comparator is ignored (blanked) for the duration of the timeout period, set by t_{OCQ} . If a comparator output indicates an overcurrent event when the blanking timer is not active then the overcurrent event is considered valid and the overcurrent bit, OC, will be set in the Diag 2 register.

When a valid overcurrent is detected with $FOC = 1$, the general fault flag is not affected, all gate drive outputs are driven inactive (low), and the OC bit is set. If $FOC = 0$, and an overcurrent is detected, the general fault flag is not affected, the outputs remain active, and only the OC bit is set.

BRIDGE: BOOTSTRAP CAPACITOR UNDERVOLTAGE FAULT

The A89503 monitors the bootstrap capacitor charge voltage to ensure sufficient high-side drive. The user must ensure that the bootstrap capacitor does not become discharged below the bootstrap undervoltage threshold, V_{BCUV} , or a bootstrap fault will be indicated and the outputs disabled. This can happen with very high PWM duty cycles when the charge time for the bootstrap capacitor is insufficient to ensure a sufficient recharge to match the MOSFET gate charge transfer during turn on. The user must also ensure that the bootstrap capacitor is sufficiently charged before attempting to turn on the high-side MOSFET. If the bootstrap voltage is below the undervoltage threshold when the high-side MOSFET is being switched on, then the bootstrap undervoltage is immediately detected.

The action taken when a valid bootstrap undervoltage fault is detected and the fault reset conditions depend on the state of the FVBU bit.

If $FVBU = 0$, the fault state will be latched, the bootstrap undervoltage fault bit in the status register, V_{BS} , will be set, and the high-side MOSFET will be disabled. The fault state, but not the

bootstrap undervoltage fault bit, will be reset by a low pulse on the RESETn input or the next time the MOSFET is commanded to switch on. If the MOSFET is being driven with a PWM signal, then this will usually mean that the MOSFET will be turned on again each PWM cycle. If this is the case, and the fault condition remains, then a valid fault will again be detected and the sequence will repeat. The fault state will be reset by a low pulse on the RESETn input, by a serial read of the diagnostic or status register, or by a power-on reset.

If FVBU = 1, the fault will be latched, the associated bootstrap undervoltage fault bit will be set, and all MOSFETs will be disabled. The fault state will be reset by a low pulse on the RESETn input, by a serial read of the Diagnostic 2 register, or by a power-on reset.

The bootstrap undervoltage monitor can be disabled by setting the VBS bit in the mask register. Although not recommended, this can allow the A89503 to operate below its minimum specified supply voltage level with a severely impaired gate drive. The specified electrical parameters may not be valid in this condition.

BRIDGE: MOSFET VDS OVERVOLTAGE FAULT

Faults on the external MOSFETs are determined by monitoring the drain-source voltage of the MOSFET and comparing it to a drain-source overvoltage threshold. There are two thresholds: V_{DSTH} for the high-side MOSFET and V_{DSTL} for the low-side MOSFET. V_{DSTH} and V_{DSTL} are generated by internal DACs and are defined by the values in the VTH[5:0] and the VTL[5:0] variables respectively. These variables provide the input to two 6-bit DACs with a least significant bit value of typically 50 mV. The output of the DAC produces the threshold voltage approximately defined as:

$$V_{DSTH} = n \times 50 \text{ mV}$$

where n is a positive integer defined by VT[5:0]

or:

$$V_{DSTL} = n \times 50 \text{ mV}$$

where n is a positive integer defined by VT[5:0].

The drain-source voltage for the low-side MOSFET is measured between the D terminal and the LSS terminal. Using the LSS terminal rather than the ground connection avoids adding any low-side current sense voltage to the real low-side drain-source voltage and avoids false VDS fault detection.

When the A89503 is used in applications where the load is connected between the source of the high-side MOSFET and the drain of the low-side MOSFET, as shown in Figure 6, the low-

side VDS monitor should be disabled by setting the LO bit to 1 in the Mask 1 register. This is necessary as the reference voltage for the drain of the low-side MOSFET is the S terminal which will be pulled to the supply when the high-side MOSFET is on and will cause a false low-side VDS fault if the low-side VDS monitor is active.

The drain-source voltage for the high-side MOSFET is measured between the S terminal and the VBRG terminal. Using the VBRG terminal rather than the VBB avoids adding any reverse diode voltage or high-side current sense voltage to the real high-side drain-source voltage and avoids false VDS fault detection.

The VBRG terminal is an independent sense input to the top of the MOSFET bridge. It should be connected independently and directly to the common connection point for the drain of the power bridge MOSFET at the positive supply connection point in the bridge. The input current to the VBRG terminal is proportional to the drain-source threshold voltage, V_{DST} , and is approximately:

$$I_{VBRG} = 72 \times V_{DSTH} + 52$$

where I_{VBRG} is the current into the VBRG terminal in μA and V_{DSTH} is the drain-source threshold voltage described above.

Note that the VBRG terminal can withstand a negative voltage up to -5 V . This allows the terminal to remain connected directly to the top of the power bridge during reverse battery conditions where the body diodes of the power MOSFETs are used to clamp the negative voltage.

The output from each VDS overvoltage comparator is filtered by a VDS fault qualifier circuit. This circuit uses a timer to verify that the output from the comparator is indicating a valid VDS fault. The duration of the VDS fault qualifying timer, t_{VDQ} , is determined by the contents of the TVD[9:0] variable. t_{VDQ} is approximately defined as:

$$t_{VDQ} = n \times 100 \text{ ns}$$

where n is a positive integer defined by TVD[9:0].

The qualifier can operate in one of two ways: debounce mode or blanking mode, selected by the VDQ bit.

In the default debounce mode, a timer is started each time the comparator output indicates a VDS fault detection when the corresponding MOSFET is active. This timer is reset when the comparator changes back to indicate normal operation. If the debounce timer reaches the end of the timeout period, set by t_{VDQ} , then the VDS fault is considered valid and the corresponding VDS fault bit, LO or HO, will be set in the diagnostic register.

In the optional blanking mode, a timer is started when a gate drive is turned on. The output from the VDS overvoltage comparator for the MOSFET being switched on is ignored (blanked) for the duration of the timeout period, set by t_{VDQ} . If the comparator output indicates an overvoltage event when the MOSFET is switched on and the blanking timer is not active, then the VDS fault is considered valid and the corresponding VDS fault bit, LO or HO, will be set in the diagnostic register.

The VDQ and TVD[9:0] qualifier parameters apply to the VDS overvoltage, VGS undervoltage and the off-state VGS overvoltage monitors.

If a valid VDS fault is detected, the fault will be latched and the associated MOSFET will be disabled. This state will remain until reset depending on the value set in the FDSO bit.

If FDSO = 1, the fault state will only be reset by a low pulse on the RESETn input, by a serial read of the diagnostic register, or by a power-on reset.

If FDSO = 0, the fault state, but not the VDS fault bit, will be reset the next time the MOSFET is commanded to switch on. If the MOSFET is being driven with a PWM signal, then this will usually mean that the MOSFET will be turned on again each PWM cycle. If this is the case, and the fault conditions remains, then a valid fault will again be detected after the timeout period and the sequence will repeat. The fault state will be reset by a low pulse on the RESETn input, by a serial read of the diagnostic register, or by a power-on reset.

If FDSO = 0, care must be taken to avoid damage to the MOSFET where the VDS fault is detected. Although the MOSFET will be switched off as soon as the fault is detected at the end of the fault validation timeout, it is possible that it could still be damaged by excessive power dissipation and heating. To limit any damage to the external MOSFETs or the load, the MOSFET should be fully disabled by logic inputs from the external controller.

BRIDGE: VGS UNDERVOLTAGE

To ensure that the gate drive output is operating correctly, each gate drive output voltage is independently monitored, when active, to ensure the drive voltage, V_{GS} , is sufficient to fully enhance the power MOSFET in the external bridge.

If V_{GS} on any active gate drive output goes below the gate drive undervoltage warning, V_{GSUV} , the general fault flag will be active and the corresponding gate drive undervoltage bit, HU or LU, will be set in the diagnostic register. If FGSU = 1, all gate drive outputs will be inactive (low). If FGSU = 0, no other action will be taken. When V_{GS} rises above V_{GSUV} by more than the hysteresis

voltage, $V_{GSUVHys}$, the general fault flags go inactive. The fault bits remain in the diagnostic register until cleared.

For the high-side VGS comparator, the VGSUV threshold is set 1 V(typ) below the voltage on the C terminal, and for the low-side gate comparator, the V_{GSUV} threshold is set 1 V(typ) below V_{REG} .

The output from each VGS undervoltage comparator is filtered by a VGS fault qualifier circuit. This circuit uses a timer to verify that the output from the comparator is indicating a valid VGS fault. The duration of the VGS fault qualifying timer, t_{VDQ} , is determined by the contents of the TVD[9:0] variable. t_{VDQ} is approximately defined as:

$$t_{VDQ} = n \times 100 \text{ ns}$$

where n is a positive integer defined by TVD[9:0].

The qualifier can operate in one of two ways: debounce mode or blanking mode, selected by the VDQ bit.

In debounce mode (the default setting), a timer is started each time the comparator output indicates a VGS fault detection when the corresponding MOSFET is active. This timer is reset when the comparator changes back to indicate V_{GS} is within 1 V of the voltage on the C terminal (high-side gate drive) or V_{REG} (low-side gate drive). If the debounce timer reaches the end of the timeout period, set by t_{VDQ} , then the VGS fault is considered valid.

In blanking mode (optional), a timer is started when any gate drive is turned on. The outputs from the VGS undervoltage comparators for all MOSFETs are ignored (blanked) for the duration of the timer's active period, set by t_{VDQ} . If any comparator output indicates a VGS fault and the blanking timer is not active, then the VGS fault is considered valid.

The VDQ and TVD[9:0] qualifier parameters apply to the VDS overvoltage, VGS undervoltage, and the off-state VGS overvoltage monitors.

BRIDGE: OFF-STATE VGS OVERVOLTAGE

To ensure that the gate drives are successfully driven low when requested by the microcontroller, each gate drive output voltage is independently monitored, when commanded off, to ensure the voltage, V_{GS} , is below the overvoltage threshold and it is not sufficient to start conduction in the MOSFET.

If V_{GS} on any inactive gate drive output does not fall below the off-state VGS overvoltage warning, V_{GSOV} , the general fault flag will be active and the corresponding bit, HGO or LGO, will be set in Diagnostic 0 register. In addition, the FF and GSO bits will be set in the Status register. No further action will be taken. The

fault bits remain set in the diagnostic register until cleared.

For the high-side VGS comparator, the V_{GSOV} threshold is set 1 V(typ) above the voltage on the S terminal, and for the low-side VGS comparator, the V_{GSOV} is set 1 V(typ) above the voltage on LSS terminal.

The output from each off-state VGS overvoltage comparator is filtered by a VGS fault qualifier circuit. This circuit uses a timer to verify that the output from the comparator is indicating a valid off-state VGS fault. The duration of the VGS fault qualifying timer, t_{VDQ} , is determined by the contents of the TVD[9:0] variable. t_{VDQ} is approximately defined as:

$$t_{VDQ} = n \times 100 \text{ ns}$$

where n is a positive integer defined by TVD[9:0].

The qualifier can operate in one of two ways: debounce mode or blanking mode, selected by the VDQ bit.

In debounce mode (the default setting), a timer is started each time the comparator output indicates a VGS fault detection when the corresponding MOSFET is commanded off. This timer is reset when the comparator changes back to indicate VGS is within 1 V(typ) of the voltage on the S terminal (high-side) or LSS terminal (low-side). If the debounce timer reaches the end of the timeout period, set by t_{VDQ} , then the VGS fault is considered valid.

In blanking mode (optional), a timer is started when any gate drive is turned off. The outputs from the off-state VGS overvoltage comparators for both MOSFETs are ignored (blanked) for the duration of the timer's active period, set by t_{VDQ} . If any comparator output indicates a VGS fault and the blanking time is not active, then the VGS fault is considered valid.

The VDQ and TVD[9:0] qualifier parameters apply to the VGS undervoltage, VDS overvoltage, and the off-state VGS overvoltage monitors.

MOSFET FAULT STATE: SHORT TO SUPPLY

A short from the load connections to the battery or VBB connection is detected by monitoring the voltage across the low-side MOSFET using the S terminal and the LSS terminal. This drain-source voltage is then compared to the low-side Drain-Source Threshold Voltage, V_{DSTL} . If the blanking timer is active, the output from the VDS overvoltage comparator will be ignored for t_{VDQ} . While the low-side VDS fault is detected, the VDS fault bit, LO, will be set in the diagnostic register and the low-side MOSFET will be disabled. When FDSO is set to 1, both MOSFETs will be disabled.

MOSFET FAULT STATE: SHORT TO GROUND

A short from the load connection to ground is detected by monitoring the voltage across the high-side MOSFET using the S terminal and the voltage at VBRG. This drain-source voltage is then compared to the high-side Drain-Source Threshold Voltage, V_{DSTH} . If the blanking timer is active, the output from the VDS overvoltage comparator will be ignored for t_{VDQ} . While the high-side VDS fault is detected, the VDS fault bit, HO, will be set in the diagnostic register and the high-side MOSFET will be disabled. When FDSO is set to 1, both MOSFETs will be disabled.

Fault Action

The action taken when one of the diagnostic functions indicates a fault is listed in Table 5.

When a fault is detected a corresponding fault state is considered to exist. In some cases, the fault state only exists during the time the fault is detected. In other cases, when the fault is only detected for a short time, the fault state is latched (stored) until reset. The faults that are latched are indicated in table 5. Latched fault states are always reset when RESETn is taken low, a power-on-reset state is present or when the associated fault bit is read through the serial interface. Any fault bits that have been set in the status or diagnostic register are only reset when a power-on-reset state is present or when the associated fault bit is read through the serial interface. RESETn low will not reset the fault bits in the status or diagnostic registers.

For most of the diagnostic functions, the action taken when a fault state is detected can be programmed to force the gate drive outputs into the inactive (low) state or to leave them active. The action is selected by a 1 or a 0 in specific stop on fault (SoF) bit associated with the diagnostic. The specific SoF bits for each diagnostic and the action taken for each setting are listed in Table 5.

The fault condition power-on-reset is considered critical to the safe operation of the A89503 and the system. If this fault is detected, then the gate drive outputs are automatically driven low and both MOSFETs in the bridge held in the off state. This state will remain until the fault is removed.

Setting any of the FVRU, FVRO, FVSU, FOT, FTW, FSE, FVBU, FOC, FDSO, or FGSU bits in the Stop-on-Fault register to 0 such that the gate drive outputs are not disabled in the event of the corresponding fault being detected means that the A89503 will not take any action to protect itself or the external bridge MOSFETs and damage may occur. Appropriate action must be taken by the external controller.

Fault Masks

Individual diagnostics—except power-on reset, EEPROM error, serial transmission error and over temperature—can be disabled by setting the corresponding bit in the mask register. Power-on-reset cannot be disabled because the diagnostics and the output control depend on the logic regulator to operate correctly. If a bit is set to one in the mask register, then the corresponding diagnostic will be completely disabled. No fault states for the disabled diagnostic will be generated and no fault flags or diagnostic bits will be set. See Mask Register definition for bit allocation. Care must be taken when diagnostics are disabled to avoid potentially damaging conditions.

Table 5: Fault Actions

Fault Description	SoF Bit Name	Disable Outputs		Fault State Latched
		SoF Bit = 0	SoF Bit = 1	
No Fault	–	No	No	–
Power-on-Reset	–	Yes ^[1]	Yes ^[1]	No
VREG Undervoltage	FVRU	No ^[3]	Yes ^[1]	No
VREG Overvoltage	FVRO	No	Yes ^[1]	No
VIO Undervoltage	–	Yes ^[1]	Yes ^[1]	No
VBRG Overvoltage	–	No	No	No
VBRG Undervoltage	FVSU	No ^[3]	Yes ^[1]	No
Overtemperature	FOT	No ^[3]	Yes ^[1]	No
Temperature Warning	FTW	No	Yes ^[1]	No
Serial Transmission Error	FSE	No	Yes ^[1]	No
Bootstrap Undervoltage	FVBU	Yes ^[2]	Yes ^[1]	Yes
Overcurrent	FOC	No	Yes ^[1]	Yes
VDS Overvoltage	FDSO	Yes ^[2]	Yes ^[1]	Yes
VGS Undervoltage	FGSU	No ^[3]	Yes ^[1]	Yes
Off-State VGS Overvoltage	–	No	No	No
EEPROM	–	Yes ^[1]	Yes ^[1]	Yes

^[1] Both gate drives low, both MOSFETs off.

^[2] Gate drive to the affected MOSFET low, only the affected MOSFET off.

^[3] Stated fault condition may damage the A89503 and/or bridge MOSFETs unless appropriate action taken by the external controller.

SERIAL INTERFACE

Table 6: Serial Register Definition*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0: Not Used	0	0	0	0	WR	0	0	0	0	0	0	0	0	0	0	P
1: Config 1	0	0	0	1	WR	OCT3	OCT2	OCT1	OCT0	VTH5	VTH4	VTH3	VTH2	VTH1	VTH0	P
2: Config 2	0	0	1	0	WR	OCQ	VDQ			VTL5	VTL4	VTL3	VTL2	VTL1	VTL0	P
3: Config 3	0	0	1	1	WR	TVD9	TVD8	TVD7	TVD6	TVD5	TVD4	TVD3	TVD2	TVD1	TVD0	P
4: Config 4	0	1	0	0	WR	VPO	VPU									P
5: Config 5	0	1	0	1	WR	SAT		SAO3	SAO2	SAO1	SAO0		SAG2	SAG1	SAG0	P
6: Config 6	0	1	1	0	WR			TR3	TR2	TR1	TR0	TF3	TF2	TF1	TF0	P
7: Config 7	0	1	1	1	WR			IR13	IR12	IR11	IR10	IF13	IF12	IF11	IF10	P
8: Config 8	1	0	0	0	WR			IR23	IR22	IR21	IR20	IF23	IF22	IF21	IF20	P
9: Stop on Fault	1	0	0	1	WR	FVRU	FVRO	FVSU	FOT	FTW	FSE	FVBU	FOC	FDSO	FGSU	P
10: Mask 0	1	0	1	0	WR			VBS	TW			HGO	LGO	HU	LU	P
11: Mask 1	1	0	1	1	WR	VRO	VRU	VSO	VSU		VLU			HO	LO	P
12: Diag 0	1	1	0	0	0							HGO	LGO	HU	LU	P
13: Diag 1	1	1	0	1	0	VRO	VRU							HO	LO	P
14: Diag 2	1	1	1	0	0	VSO	VSU			VBS				OC		P

*Power-on reset value shown below each input register bit.

Continued on the next page...

Table 6: Serial Register Definition (continued)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
15: Control	1	1	1	1	WR									HSR	LSR	P
						0	0	0	0	0	0	0	0	0	0	
Status	FF	POR	SE	EE	OT	TW	VS	GSO		VR	VLU	OC	VBS	GSU	DSO	P
	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

A three-wire synchronous serial interface, compatible with SPI, is used to control the features of the A89503. The SDO terminal can be used during a serial transfer to provide diagnostic feedback and readback of the register contents.

The A89503 can be operated without the serial interface using the default settings and the logic control inputs; however, application-specific configurations are only possible by setting the appropriate register bits through the serial interface. In addition to setting the configuration bits, the serial interface can also be used to control the bridge MOSFETs directly.

The serial interface timing requirements are specified in the Electrical Characteristics table and illustrated in Figure 4. Data is received on the SDI terminal and clocked through a shift register on the rising edge of the clock signal input on the SCK terminal. STRn is normally held high, and is only brought low to initiate a serial transfer. No data is clocked through the shift register when STRn is high, allowing multiple slave units to use common SDI and SCK connections. Each slave then requires an independent STRn connection. The SDO output assumes a high-impedance state when STRn is high, allowing a common data readback connection.

When 16 data bits have been clocked into the shift register, STRn must be taken high to latch the data into the selected register. When this occurs, the internal control circuits act on the new data and the registers are reset depending on the type of transfer.

If there are more than 16 rising edges on SCK, or if STRn goes high and there are fewer than 16 rising edges on SCK—either being described as a framing error—the write will be cancelled without latching data to the register. The Status register will not be reset.

The first four bits, D[15:12], in a serial word are the register address bits, giving the possibility of 16 register addresses. The

fifth bit, WR (D[11]), is the write/read bit. When WR is 1, the following 10 bits, D[10:1], clocked in from the SDI terminal are written to the addressed register. When WR is 0, then no data is written to the serial registers and the contents of the addressed register are clocked out on the SDO terminal.

The last bit in any serial transfer, D[0], is a parity bit (P) that is set to ensure odd parity in the complete 16-bit word. Odd parity means that the total number of 1s in any transfer should always be an odd number. This ensures that there is always at least one bit set to 1 and one bit set to 0 and allows detection of stuck-at faults on the serial input and output data connections. The parity bit is not stored but generated on each transfer.

In addition to the addressable registers, a read-only status register is output on SDO for all register addresses when WR is set to 1. For all serial transfers, the five bits output on SDO will always be the first five bits from the status register. Register data is output on the SDO terminal msb first while STRn is low and changes to the next bit on each falling edge of SCK. The first bit, which is always the FF bit from the status register, is output as soon as STRn goes low.

Registers 12, 13, and 14 contain diagnostic fault indicators and are read-only. If the WR bit for these registers is set to 1, then the data input through SDI is ignored and the contents of the status register are clocked out on the SDO terminal then reset as for a normal write. No other action is taken. If the WR bit for these registers is set to 0, then the data input through SDI is ignored and the contents of the addressed register are clocked out on the SDO terminal and the addressed register is reset.

If a framing or parity error is detected, the SE bit is set in the Status register to indicate a data transfer error. This fault condition can be cleared by a subsequent valid serial write or by a power-on-reset.

Configuration Registers

Eight registers are used to configure the operating parameters of the A89503.

Config 1: Bridge monitor setting:

- OCT[3:0], a 4-bit integer to set the overcurrent threshold voltage, V_{OCT} , in 300 mV increments.
- VTH[5:0], a 6-bit integer to set the drain-source threshold voltage, V_{DSTH} , in 50 mV increments.

Config 2: Bridge monitor setting:

- OCQ, selects the overcurrent qualifier mode, blank or debounce.
- VDQ, selects the VDS and VGS qualifier mode, blank or debounce.
- VTL[5:0], a 6-bit integer to set the low-side drain-source threshold voltage, V_{DSTL} , in 50 mV increments.

Config 3: Bridge monitor setting:

- TVD[9:0], a 10-bit integer to set the VDS and VGS fault verification time, t_{VDQ} , in 100 ns increments.

Config 4: Regulator configuration:

- VPO, selects the VBRG overvoltage warning threshold.
- VPU, selects the VBRG undervoltage threshold.

Config 5: Sense amplifier setting:

- SAO[3:0], a 4-bit integer to set the sense amplifier offset up between 0 and 2.5 V.
- SAG[2:0], a 3-bit integer to set the sense amplifier gain between 10 and 50 V/V.
- SAT, outputs the output offset on the CSO terminal.

Config 6: Gate drive time setting:

- TR[3:0], a 4-bit integer to set the high-side and low-side I_1 time in 16 ns increments.
- TF[3:0], a 4-bit integer to set the high-side and low-side I_1 time in 16 ns increments.

Config 7: Gate drive current setting:

- IR1[3:0], a 4-bit integer to set the MOSFET turn-on I_1 current in 8 mA increments.
- IF1[3:0], a 4-bit integer to set the MOSFET turn-off I_1 current in 8 mA increments.

Config 8: Gate drive current setting:

- IR2[3:0], a 4-bit integer to set the MOSFET turn-on I_2 current

in 8 mA increments.

- IF2[3:0], a 4-bit integer to set the MOSFET turn-off I_2 current in 8 mA increments.

Stop On Fault Register

A register to control whether the gate drive outputs are to remain enabled or disabled in response to faults. One bit per fault type defines stop on fault behavior for VRU, VRO, VSU, OT, TW, SE, VBS, OC, DSO, and GSU diagnostics.

Diagnostic Registers

In addition to the read-only status register, five registers provide detailed diagnostic management and reporting. Two mask registers allow individual diagnostics to be disabled and three read-only diagnostic registers provide fault bits for individual diagnostic tests and monitors. If a bit is set to one in the mask register, then the corresponding diagnostic will be completely disabled. No fault states for the disabled diagnostic will be generated and no fault flags or diagnostic bits will be set. These bits in the diagnostic registers are reset on completion of a successful read of the register.

Mask 0:

Individual bits to disable bootstrap undervoltage (VBS), temperature warning (TW), the VGS undervoltage diagnostic monitors (HU and LU), and the off-state VGS overvoltage monitors (HGO and LGO).

Mask 1:

Individual bits to disable the voltage regulator (VRO, VRU, VSO, VSU, and VIO) and the VDS overvoltage diagnostic monitors (HO and LO).

Diagnostic 0 (read only):

Individual bits indicating faults detected in VGS undervoltage diagnostic monitors (HU and LU) and off-state VGS overvoltage monitors (HGO and LGO).

Diagnostic 1 (read only):

Individual bits indicating faults detected in voltage regulator (VRO and VRU) and VDS overvoltage diagnostic monitors (HO and LO).

Diagnostic 2 (read only):

Individual bits indicating faults detected in the VBRG supply voltage (VSO and VSU), bootstrap undervoltage (VBS), and overcurrent (OC).

Control Register

The Control register contains one control bit for each MOSFET:

- HSR and LSR, MOSFET Control bits.

Status Register

There is one status register in addition to the 16 addressable registers. When any register transfer takes place, the first five bits output on SDO are always the most significant five bits of the status register regardless of whether the addressed register is being read or written (see serial timing diagram).

The content of the remaining eleven bits will depend on the state of the WR bit input on SDI. When WR is 1, the addressed register will be written and the remaining eleven bits output on SDO will be the least significant ten bits of the status register followed by a parity bit. When WR is 0, the addressed register will be read and the remaining eleven bits will be the contents of the addressed register followed by a parity bit.

The read-only status register provides a summary of the chip status by indicating if any diagnostic monitors have detected a fault. The most significant three bits of the status register (FF, POR, SE, and EE) indicate critical system faults. Bits OT and TW provide indicators for specific individual monitors and the remaining bits are derived from the contents of the three diagnostic registers. The contents and mapping to the diagnostic registers are listed in Table 7.

Table 7: Status Register Mapping

Status Register Bit	Diagnostic	Related Diagnostic Register Bits
FF	Status Flag	None
POR	Power-On-Reset	None
SE	Serial Error	None
EE	EEPROM Error	None
OT	Overtemperature	None
TW	Temperature Warning	None
VS	VBRG Monitor	VSO, VSU
GSO	Off-State VGS OV	HGO, LGO
VR	VREG Monitor	VRU, VRO
VLU	Logic I/O Regulator UV	None
OC	Overcurrent	OC
VBS	Bootstrap UV	VBS
GSU	VGS UV	HU, LU
DSO	VDS OV	HO, LO

UV = Undervoltage, OV = Overvoltage

The first most significant bit in the register is the diagnostic status flag, FF. This is high if any bits in the status register are set. When STRn goes low to start a serial write, the SDO outputs the diagnostic status flag. This allows the main controller to poll the A89503 through the serial interface to determine if a fault has been detected. If no faults have been detected, then the serial transfer may be terminated without generating a serial read fault by ensuring that SCK remains high while STRn is low. When STRn goes high, the transfer will be terminated and SDO will go into its high-impedance state.

The second most significant bit is the POR bit. At power-up or after a power-on-reset, the FF bit and the POR bit are set, indicating to the external controller that a power-on-reset has taken place. All other diagnostic bits are reset and all other registers are returned to their default state. Note that a power-on-reset only occurs when the output of the internal logic regulator rises above its undervoltage threshold. Power-on-reset is not affected by the state of the VBB supply or the VREG regulator output. In general, V_{IO} , V_{REG} , and V_{BB} undervoltages may immediately be set as a result of startup conditions within the part.

The third bit in the status register is the SE bit, which indicates that the previous serial transfer was not completed successfully.

The fourth bit in the Status register is the EE bit, which indicates that an EEPROM error was detected at device power-up.

Bits OT, TW, and VLU are the fault bits for the two temperature monitors and the logic I/O regulator monitor, respectively. If one or more of these faults, along with the POR and SE faults, are no longer present, then the corresponding fault bits will be reset following a successful read of the status register. Resetting only affects latched fault bits for faults that are no longer present. For any static faults that are still present, for example overtemperature, the fault flag will remain set after the reset.

The remaining bits, GSO, VS, VR, OC, VBS, GSU, and DSO, are all derived from the contents of the diagnostic registers and are only cleared when the corresponding contents of the diagnostic register are read; they cannot be reset by reading the Status register. A fault indicated on any of the related diagnostic register bits will set the corresponding status bit to 1. The related diagnostic register must be read to determine the exact fault and clear the fault if the fault condition has cleared.

SERIAL REGISTER REFERENCE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
----	----	----	----	----	----	---	---	---	---	---	---	---	---	---	---

1: Config 1	0	0	0	1	WR	OCT3	OCT2	OCT1	OCT0	VTH5	VTH4	VTH3	VTH2	VTH1	VTH0	P
						0	0	0	1	0	1	1	0	0	0	
2: Config 2	0	0	1	0	WR	OCQ	VDQ			VTL5	VTL4	VTL3	VTL2	VTL1	VTL0	P
						0	0	0	0	0	1	1	0	0	0	
3: Config 3	0	0	1	1	WR	TVD9	TVD8	TVD7	TVD6	TVD5	TVD4	TVD3	TVD2	TVD1	TVD0	P
						1	1	1	1	1	1	1	1	1	1	
4: Config 4	0	1	0	0	WR	VPO	VPU									P
						1	0	0	0	0	0	0	0	0	0	

Config 1

OCT[3:0] Overcurrent threshold.

$$V_{OCT} = (n + 1) \times 300 \text{ mV}$$

where n is a positive integer defined by OCT[3:0]
e.g. for the power-on-reset condition.
OCT[3:0] = [0001] then $V_{OCT} = 0.6 \text{ V}$.
The range of V_{OCT} is 0.3 to 4.8 V.

VTH[5:0] High-side VDS overvoltage threshold.

$$V_{DSTH} = n \times 50 \text{ mV}$$

where n is a positive integer defined by VTH[5:0],
e.g. for the power-on-reset condition.
VTH[5:0] = [01 1000] then $V_{DST} = 1.2 \text{ V}$.
The range of V_{DST} is 0 to 3.15 V.

Config 2

OCQ Overcurrent time qualifier mode.

OCQ	Qualifier	Default
0	Debounce	D
1	Blank	

VDQ VDS and VGS Fault qualifier mode.

VDQ	VDS Fault Qualifier	Default
0	Debounce	D
1	Blank	

VTL[5:0] Low-side VDS overvoltage threshold.

$$V_{DSTL} = n \times 50 \text{ mV}$$

where n is a positive integer defined by VTL[5:0],
e.g. for the power-on-reset condition.
VTL[5:0] = [01 1000] then $V_{DSTL} = 1.2 \text{ V}$.
The range of V_{DSTL} is 0 to 3.15 V.

Config 3

TVD[9:0] VDS and VGS verification time.

$$t_{VDQ} = n \times 100 \text{ ns}$$

where n is a positive integer defined by TVD[9:0],
e.g. for the power-on-reset condition.
TVD[9:0] = [11 1111 1111] then $t_{VDQ} = 102.3 \mu\text{s}$.
The range of t_{VDQ} is 0 to 102.3 μs .

Config 4

VPO V_{BRG} overvoltage warning threshold.

VPO	V_{BRG} Overvoltage	Default
0	52 V	
1	58 V	D

VPU V_{BRG} undervoltage threshold.

VPU	V_{BRG} Undervoltage	Default
0	20 V	D
1	36 V	

SERIAL REGISTER REFERENCE (continued)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
----	----	----	----	----	----	---	---	---	---	---	---	---	---	---	---

5: Config 5	0	1	0	1	WR	SAT		SAO3	SAO2	SAO1	SAO0		SAG2	SAG1	SAG0	P
						0	0	1	1	1	1	0	1	0	1	

Config 2

SAO[3:0] Sense Amp Offset.

Where SAO is a positive integer defined by SAO[3:0].

SAO	Offset	Default
0	0 mV	
1	0 mV	
2	100 mV	
3	100 mV	
4	200 mV	
5	300 mV	
6	400 mV	
7	500 mV	
8	750 mV	
9	1.0 V	
10	1.25 V	
11	1.5 V	
12	1.75 V	
13	2.0 V	
14	2.25 V	
15	2.5 V	D

SAG[2:0] Sense Amp Offset.

Where SAG is a positive integer defined by SAG[2:0].

SAG	Gain	Default
0	10	
1	15	
2	20	
3	25	
4	30	
5	35	D
6	40	
7	50	

SAT Sense Amp Test.

SAT	CSO terminal	Default
0	Current sense amp output	D
1	Output offset	

SERIAL REGISTER REFERENCE (continued)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
----	----	----	----	----	----	---	---	---	---	---	---	---	---	---	---

6: Config 6	0	1	1	0	WR			TR3	TR2	TR1	TR0	TF3	TF2	TF1	TF0	P
						0	0	0	0	0	1	0	0	0	1	

7: Config 7	0	1	1	1	WR			IR13	IR12	IR11	IR10	IF13	IF12	IF11	IF10	P
						0	0	0	0	0	0	0	0	0	0	

8: Config 8	1	0	0	0	WR			IR23	IR22	IR21	IR20	IF23	IF22	IF21	IF20	P
						0	0	0	0	0	0	0	0	0	0	

Config 6

TR[3:0] MOSFET turn-on t_1 time.

$$t_1 = (n \times 16 \text{ ns}) + 60 \text{ ns}$$

where n is a positive integer defined by TR[3:0],
e.g. if TR[3:0] = [0001] then $t_1 = 76 \text{ ns}$.

The range of t_1 is 60 to 300 ns.

TF[3:0] MOSFET turn-off t_1 time.

$$t_1 = (n \times 16 \text{ ns}) + 60 \text{ ns}$$

where n is a positive integer defined by TF[3:0],
e.g. for the power-on-reset condition.

TF[3:0] = [0001] then $t_1 = 76 \text{ ns}$.

The range of t_1 is 60 to 300 ns.

Config 7

IR1[3:0] MOSFET turn-on I_1 current.

$$I_1 = n \times -8 \text{ mA}$$

where n is a positive integer defined by IR1[3:0],
e.g. if IR1[3:0] = [1000] then $I_1 = -64 \text{ mA}$

The range of I_1 is -8 mA to -120 mA.

Selecting a value of 0 will set maximum gate drive to turn on the MOSFET as quickly as possible.

IF1[3:0] MOSFET turn-off I_1 current.

$$I_1 = n \times 8 \text{ mA}$$

where n is a positive integer defined by IF1[3:0],
e.g. if IF1[3:0] = [1000] then $I_1 = 64 \text{ mA}$.

The range of I_1 is 8 to 120 mA.

Selecting a value of 0 will set maximum gate drive to turn on the MOSFET as quickly as possible.

Config 8

IR2[3:0] MOSFET turn-on I_2 current.

$$I_2 = n \times -8 \text{ mA}$$

where n is a positive integer defined by IR2[3:0],
e.g. if IR2[3:0] = [1000] then $I_2 = -64 \text{ mA}$.

The range of I_2 is -8 to -120 mA.

Selecting a value of 0 will set maximum gate drive to turn on the MOSFET as quickly as possible.

IF2[3:0] MOSFET turn-off I_2 current.

$$I_2 = n \times 8 \text{ mA}$$

where n is a positive integer defined by IF2[3:0],
e.g. if IF2[3:0] = [1000] then $I_2 = 64 \text{ mA}$.

The range of I_2 is 8 to 120 mA.

Selecting a value of 0 will set maximum gate drive to turn on the MOSFET as quickly as possible.

SERIAL REGISTER REFERENCE (continued)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
----	----	----	----	----	----	---	---	---	---	---	---	---	---	---	---

9: Stop On Fault	1	0	1	1	WR	FVRU	FVRO	FVSU	FOT	FTW	FSE	FVBU	FOC	FDSO	FGSU	P
						1	1	1	1	1	1	1	1	1	1	

Stop On Fault

- FVRU VREG Undervoltage
- FVRO VREG Overvoltage
- FVSU VBRG Undervoltage
- FOT Overtemperature
- FTW Temperature Warning
- FSE Serial Error
- FVBU Bootstrap Undervoltage
- FOC Overcurrent
- FDSO VDS Overvoltage
- FGSU VGS Undervoltage

SERIAL REGISTER REFERENCE (continued)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
----	----	----	----	----	----	---	---	---	---	---	---	---	---	---	---

10: Mask 0	1	0	1	0	WR			VBS	TW			HGO	LGO	HU	LU	P
	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

11: Mask 1	1	0	1	1	WR	VRO	VRU	VSO	VSU		VLU			HO	LO	P
	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Mask 0

- VBS Bootstrap Undervoltage
- TW Temperature Warning
- HGO High-Side Off-State VGS Overvoltage
- LGO Low-Side Of-State VGS Overvoltage
- HU High-Side VGS Undervoltage
- LU Low-Side VGS Undervoltage

Mask 1

- VRO VREG Overvoltage
- VRU VREG Undervoltage
- VSO VBRG Overvoltage
- VSU VBRG Undervoltage
- VLU Logic I/O Undervoltage
- HO High-Side VDS Overvoltage
- LO Low-Side VDS Overvoltage

xxx	Fault Mask	Default
0	Fault detection permitted	D
1	Fault detection disabled	

SERIAL REGISTER REFERENCE (continued)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
12: Diag 0	1	1	0	0	0							HGO	LGO	HU	LU	P
						0	0	0	0	0	0	0	0	0	0	
13: Diag 1	1	1	0	1	0	VRO	VRU							HO	LO	P
						0	0	0	0	0	0	0	0	0	0	
14: Diag 2	1	1	1	0	0	VSO	VSU			VBS				OC		P
						0	0	0	0	0	0	0	0	0	0	

Diag 0 (read only)

HGO High-Side Off-State VGS Overvoltage

LGO Low-Side Off-State VGS Overvoltage

HU High-Side VGS Undervoltage

LU Low-Side VGS Undervoltage

Diag 1 (read only)

VRO VREG Overvoltage

VRU VREG Undervoltage

HO High-Side VDS Overvoltage

LO Low-Side VDS Overvoltage

Diag 2 (read only)

VSO VBRG Overvoltage

VSU VBRG Undervoltage

VBS Bootstrap Undervoltage

OC Overcurrent On Sense Amp

xxx	Status
0	No fault detected
1	Fault detected

SERIAL REGISTER REFERENCE (continued)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
----	----	----	----	----	----	---	---	---	---	---	---	---	---	---	---

15: Control	1	1	1	1	WR									HSR	LSR	P
	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Control

HSR High-side gate drive

LSR Low-side gate drive

See Table 2 and Table 3 for control logic operation.

SERIAL REGISTER REFERENCE (continued)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Status (read only)	FF	POR	SE	EE	OT	TW	VS	GSO		VR	VLU	OC	VBS	GSU	DSO	P
	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	

Status (read only)

FF	Diagnostic Register Flag
POR	Power-On-Reset
SE	Serial Error
EE	EEPROM Fault
OT	Overtemperature
TW	High Temperature Warning
VS	VBRG Faults
GSO	Off-State VGS Overvoltage
VR	VREG Out Of Range
VLU	Logic I/O Regulator Undervoltage
OC	Overcurrent
VBS	Bootstrap Undervoltage
GSU	VGS Undervoltage
DSO	VDS Overvoltage

Status Register Bit Mapping

Status Register Bit	Related Diagnostic Register Bits
FF	None
POR	None
SE	None
EE	None
OT	None
TW	None
VS	VSO, VSU
GSO	HGO, LGO
VR	VRU, VRO
VLU	None
OC	OC
VBS	VBS
GSU	HU, LU
DSO	HO, LO

U = Undervoltage, O = Overvoltage

xxx	Status
0	No fault detected
1	Fault detected

APPLICATION INFORMATION

Bootstrap Capacitor Selection

The A89503 requires a bootstrap capacitor C . To simplify this description of the bootstrap capacitor selection criteria, generic naming is used here. So, for example, C_{BOOT} , Q_{BOOT} , and V_{BOOT} refer to the bootstrap capacitor, and Q_{GATE} refers to the high-side MOSFET. C_{BOOT} must be correctly selected to ensure proper operation of the device—too large and time will be wasted charging the capacitor, resulting in a limit on the maximum duty cycle and PWM frequency; too small and there can be a large voltage drop at the time the charge is transferred from C_{BOOT} to the MOSFET gate.

To keep the voltage drop due to charge sharing small, the charge in the bootstrap capacitor, Q_{BOOT} , should be much larger than Q_{GATE} , the charge required by the gate:

$$Q_{BOOT} \gg Q_{GATE}$$

A factor of 20 is a reasonable value, so

$$Q_{BOOT} = C_{BOOT} \times V_{BOOT} = Q_{GATE} \times 20$$

or

$$C_{BOOT} = \frac{Q_{GATE} \times 20}{V_{BOOT}}$$

where V_{BOOT} is the voltage across the bootstrap capacitor.

The voltage drop, ΔV , across the bootstrap capacitor as the MOSFET is being turned on, can be approximated by:

$$\Delta V = \frac{Q_{GATE}}{C_{BOOT}}$$

so for a factor of 20, ΔV will be 5% of V_{BOOT} .

The maximum voltage across the bootstrap capacitor under normal operating conditions is $V_{REG}(\max)$. However, in some circumstances the voltage may transiently reach a maximum of 18 V, which is the clamp voltage of the Zener diode between the C terminal and the S terminal. In most applications with a good ceramic capacitor, the working voltage can be limited to 16 V.

Bootstrap Charging

It is necessary to ensure the high-side bootstrap capacitor is completely charged before a high-side PWM cycle is requested. The time required to charge the capacitor, t_{CHARGE} , in μs , is approximated by:

$$t_{CHARGE} = \frac{C_{BOOT} \times \Delta V}{100}$$

where C_{BOOT} is the value of the bootstrap capacitor in nF and ΔV is the required voltage of the bootstrap capacitor. At power up and when the drivers have been disabled for a long time, the bootstrap capacitor can be completely discharged. In this case, ΔV can be considered to be the full high-side drive voltage, 12 V. Otherwise, ΔV is the amount of voltage dropped during the charge transfer, which should be 400 mV or less. The capacitor is charged whenever the S terminal is pulled low and current flows from the capacitor connected to the VREG terminal through the internal bootstrap diode circuit to C_{BOOT} .

VREG Capacitor Selection

The internal reference, V_{REG} , supplies current for the low-side gate-drive circuits and the charging current for the bootstrap capacitors. When a low-side MOSFET is turned on, the gate-drive circuit will provide the high transient current to the gate that is necessary to turn the MOSFET on quickly. This current, which can be several hundred milliamperes, cannot be provided directly by the limited output of the VREG regulator but must be supplied by an external capacitor, C_{REG} , connected between the VREG terminal and GND.

The turn-on current for the high-side MOSFET is similar in value but is mainly supplied by the bootstrap capacitor. However, the bootstrap capacitor must then be recharged from C_{REG} through the VREG terminal. Unfortunately, the bootstrap recharge can occur a very short time after the low-side turn on occurs. This means that the value of C_{REG} between VREG and GND should be high enough to minimize the transient voltage drop on VREG for the combination of a low-side MOSFET turn on and a bootstrap capacitor recharge. For block commutation control (trapezoidal drive), where only one high side and one low side are switching during each PWM period, a minimum value of $20 \times C_{BOOT}$ is reasonable. For sinusoidal control schemes, a minimum value of $40 \times C_{BOOT}$ is recommended. As the maximum working voltage of C_{REG} will never exceed V_{REG} , the part's voltage rating can be as low as 15 V. However, it is recommended that a capacitor rated to at least twice the maximum working voltage should be used to reduce any impact operating voltage may have on capacitance value. For best performance, C_{REG} should be ceramic rather than electrolytic. C_{REG} should be mounted as close to the VREG terminal as possible.

Current Sense Amplifier Configuration

Amplifier gain, A_V , and output offset zero point voltage, V_{OOS} , may be set to a range of values by the SAG[2:0] and SAO[3:0] variables respectively as defined in the Current Sense Amplifiers section above. It is important that both values are selected to ensure the absolute voltage at the CSO output, V_{CSO} , remains within the amplifier's dynamic range, V_{CSOUT} , and the dynamic range of any downstream signal processing circuitry. Allowance must be made for both positive and negative current flows within the sense resistor.

With reference to Figure 3, the relationship between phase current I_{PH} , sense resistor value, R_S , and differential amplifier input voltage, V_{ID} is given by:

$$V_{ID} = V_{CSP} - V_{CSM} = I_{PH} \times R_S$$

The current sense amplifier's output voltage on CSO with respect to the programmed value of output offset is:

$$V_{CSD} = (V_{CSP} - V_{CSM}) \times A_V$$

The absolute voltage on CSO when SAT = 1 with respect to ground is therefore:

$$V_{CSO} = [(V_{CSP} - V_{CSM}) \times A_V] + V_{OOS}$$

If, for example, the following parameter values are assumed:

- $R_S = 1 \text{ m}\Omega$
- $I_{PH} = -20\text{A to } +40\text{A}$

- $A_V = 20$ (SAG[2:0] = 0b010)
- $V_{OOS} = 1 \text{ V}$ (SAO[3:0] = 0b1001)

V_{ID} ranges between -20 mV and $+40 \text{ mV}$ and V_{CSO} between 0.6 V and 1.8 V . V_{CSO} remains within the amplifier dynamic range, V_{CSOUT} , of 0.3 V to 4.8 V . However, if A_V is increased to 50, V_{CSO} attempts to drive to 0 V and 3.0 V , the amplifier dynamic range limits are not complied with, and the amplifier output saturates at its negative limit. This situation could be remedied by reducing A_V to 30 ($0.4 \text{ V} < V_{CSO} < 2.2 \text{ V}$) or increasing V_{OOS} to 1.5 V ($0.5 \text{ V} < V_{CSO} < 3.5 \text{ V}$).

Current Sense Amplifier Output Signals

As defined in Figure 3, the current sense amplifier output signals on the CSO pin is internally referenced to the output offset which can be made available on the CSO terminal by setting the SAT bit to 1. The sense amp output voltage and the output offset voltage may be measured consecutively with respect to ground, and the values subtracted to give the required output signal voltages as $V_{CSD} = V_{CSO} - V_{OOS}$.

The Input Offset Voltage, V_{IOS} , and the associated drift, ΔV_{IOS} , multiplied by the selected amplifier gain, A_V , represent the offset and offset drift limits that apply to V_{CSD} . The Output Offset Error limits, E_{VO} , and Output Offset Drift limits, V_{OOSD} , apply directly to V_{OOS} . E_{VO} and V_{OOSD} do not affect current sense output accuracy.

INPUT/OUTPUT STRUCTURES

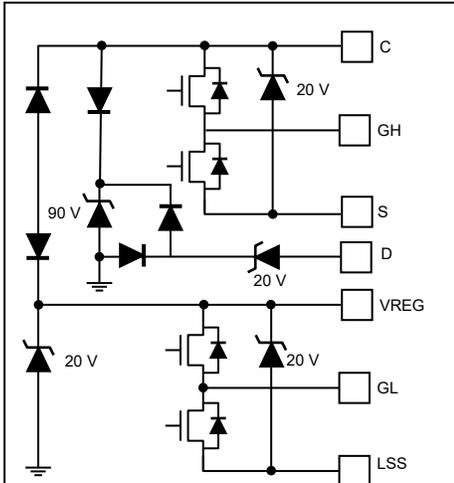


Figure 9a: Gate Drive Outputs

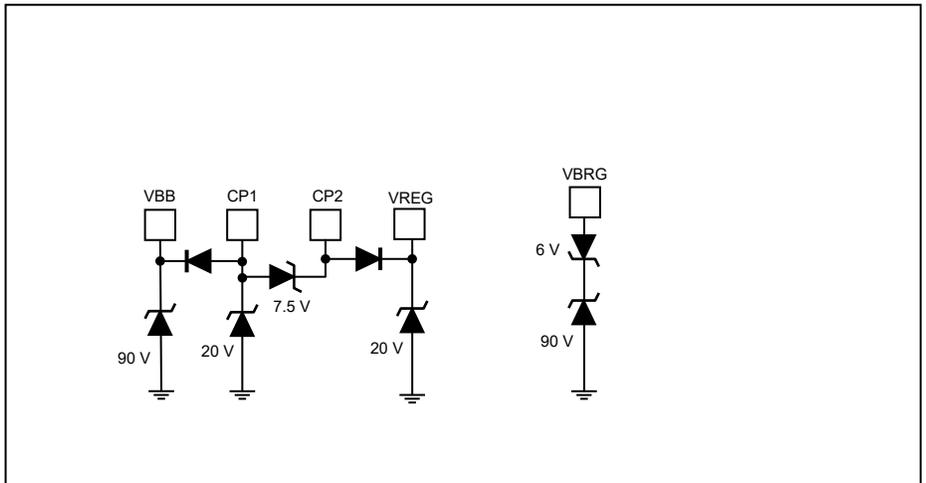


Figure 9b: Supplies

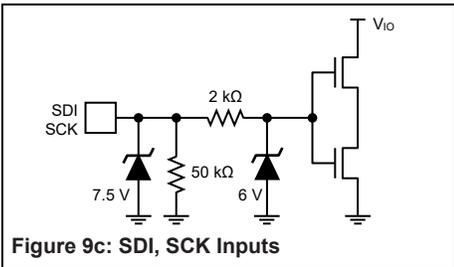


Figure 9c: SDI, SCK Inputs

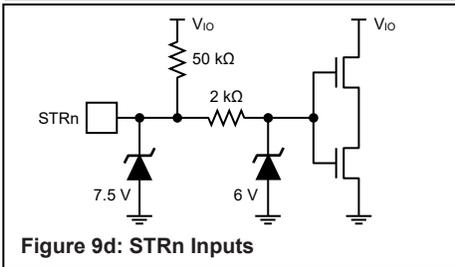


Figure 9d: STRn Inputs

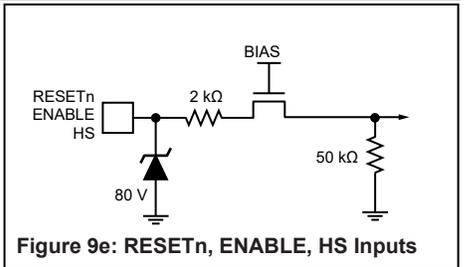


Figure 9e: RESETn, ENABLE, HS Inputs

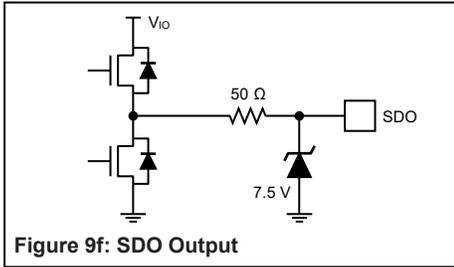


Figure 9f: SDO Output

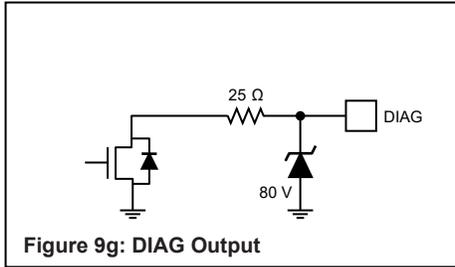


Figure 9g: DIAG Output

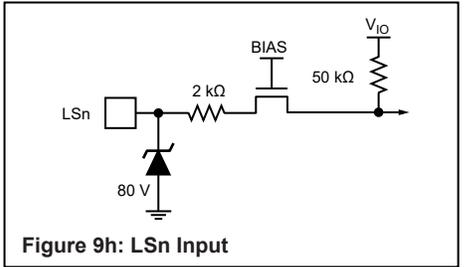


Figure 9h: LSn Input

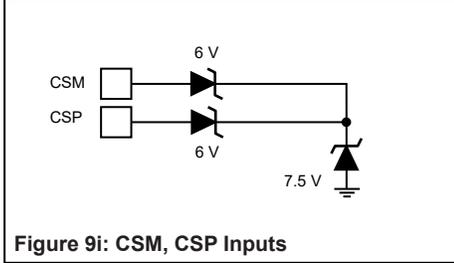


Figure 9i: CSM, CSP Inputs

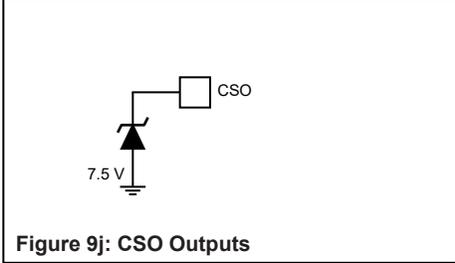


Figure 9j: CSO Outputs

LAYOUT RECOMMENDATIONS

Careful consideration must be given to PCB layout when designing high-frequency, fast-switching, high-current circuits:

- The exposed thermal pad should be connected to the GND terminal.
- Minimize stray inductance by using short, wide copper tracks at the drain and source terminals of all power MOSFETs. This includes load lead connections and the input power bus. This will minimize voltages induced by fast switching of large load currents.
- Consider the addition of small (100 nF) ceramic decoupling capacitor across the source and drain of the power MOSFETs to limit fast transient voltage spikes caused by track inductance.
- Keep the gate discharge return connections S and LSS as short as possible. Any inductance on these tracks will cause negative transitions on the corresponding A89503 terminals, which may exceed the absolute maximum ratings. If this is likely, consider the use of clamping diodes to limit the negative excursion on these terminals with respect to the GND terminal.
- Supply decoupling, typically a 100 nF ceramic capacitor, should be connected between VBB and GND as close to the A89503 terminals as possible.
- Supply decoupling should be connected between VREG and GND as close to the A89503 terminals as possible.
- Check the pick voltage excursion of the transients on the LSS terminal with reference to the GND terminal using a close-grounded ("tip & barrel") probe. If the voltage at any LSS terminal exceeds the absolute maximum in the datasheet, add additional clamping and/or capacitance between the LSS terminal and the GND terminal.
- Gate charge drive paths and gate discharge return paths may carry a large transient current pulse. Therefore, the traces from GH, GL, S, and LSS should be as short as possible to reduce the track inductance.
- Provide an independent connection between the LSS terminal to the source of the low-side MOSFET in the power bridge. Connection of the LSS terminal directly to the GND terminal is not recommended as this may inject noise into sensitive functions such as the various voltage monitors.
- A low-cost diode can be placed in the connection to VBB to provide reverse battery protection. In reverse battery conditions, it is possible to use the body diodes of the power MOSFETs to clamp the reverse voltage to approximately 4 V. In this case, the additional diode in the VBB connection will prevent damage to the A89503 and the VBRG input will survive the reverse voltage.

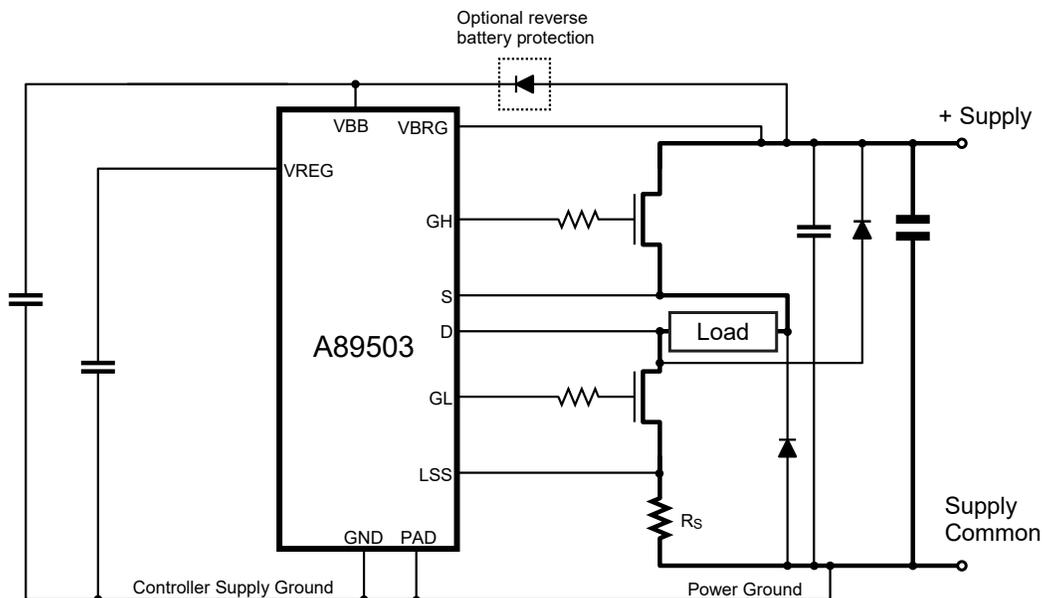


Figure 10: Supply Routing Suggestions

PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000379, Rev. 3 and JEDEC MO-153ADT)

NOT TO SCALE

Dimensions in millimeters

Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

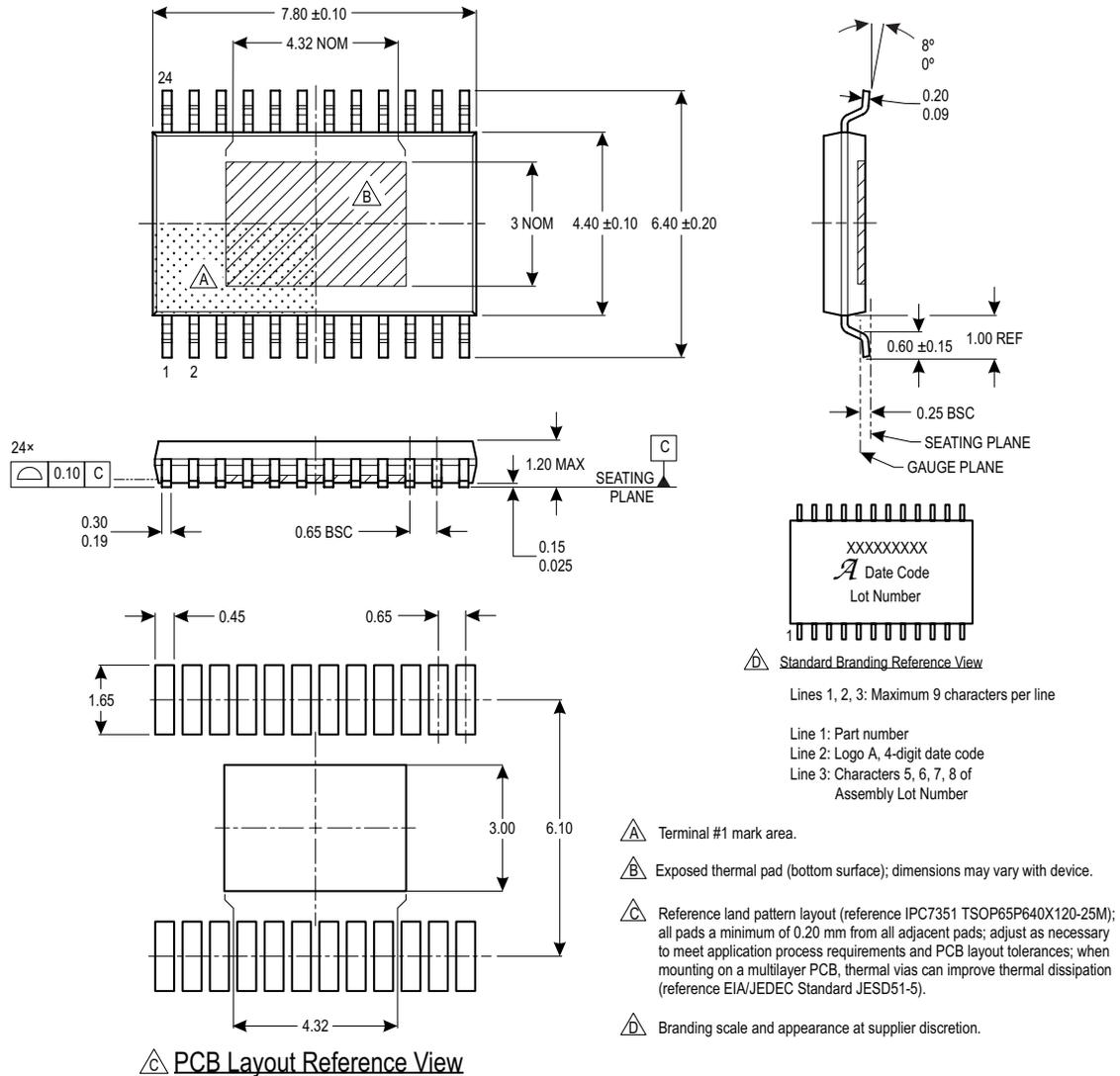


Figure 11: Package LP, 24-Lead TSSOP with Exposed Pad

Revision History

Number	Date	Description
–	March 23, 2020	Initial release
1	June 15, 2020	Added AEC-Q100 qualification to Features and Benefits (page 1)
2	March 12, 2021	Updated Pull-Up On Resistance maximum values, GH Active Pull-Down and GL Active Pull-Down test conditions, typical, and maximum values (page 7), Input Offset Voltage test conditions and values (page 9), VDS Threshold – High Side and Low Side default power-up minimum and maximum values (page 10), Pump Regulator section (page 16), and Sleep Mode section (page 20); added footnote 7 to Temperature Warning Threshold, Temperature Warning Hysteresis, Overtemperature Threshold, and Overtemperature Hysteresis (page 11).
3	November 15, 2021	Updated Bootstrap Undervoltage maximum values (page 10).
4	March 25, 2022	Updated package drawing (page 44) and minor editorial updates.
5	May 10, 2023	Updated Selection Guide (page 2).
6	March 11, 2024	Part variant A89503KLPTR-3-1 status changed to Last-Time Buy (page 2).
7	March 18, 2025	Part variant A89503KLPTR-3-1 status changed to Active (page 2)

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