ACS37030 and ACS37032

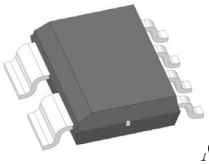
DC to 5 MHz Bandwidth, Galvanically Isolated, High-Accuracy Current Sensor IC with Reference Output (ACS37030) or Fault (ACS37032)

FEATURES AND BENEFITS

- High operating bandwidth for fast control loops or where high-speed switching currents are monitored
  - □ DC to 5 MHz bandwidth
  - □ 40 ns typical response time
- High accuracy and low noise
  - □ ±2% sensitivity error over temperature
  - □ ±10 mV maximum offset voltage over temperature
  - □ 50 mA_{RMS} input referred noise
  - □ 3.3 V non-ratiometric supply operation
  - □ Differential sensing immune to external magnetic fields
- VREF output voltage for differential routing in noisy application environments (ACS37030)
- FAULT output for fast open drain overcurrent detection (ACS37032)
- Highly isolated compact surface-mount packages
- Available in two packages
- Wide operating temperature, –40°C to 150°C
- Grade 0, AEC-Q100 automotive qualified (MY pending)

PACKAGE:

6-pin Fused-Lead SOIC (suffix LZ)



6-pin Fused-Lead Wide Body SOIC (suffix MY)

Not to scale

DESCRIPTION

The ACS37030/2 is a fully integrated current sensor IC that senses current flowing through the primary conductor. Two signal paths are used: a Hall-effect element path to capture DC and low-frequency current information, and an inductive coil path to capture high-frequency current information. These two paths are summed to allow for sensing of a wide frequency band with a single device. The properties of the coil increase SNR as frequency increases, minimizing noise seen at the output.

The internal construction provides high isolation by magnetically coupling the field generated by current flow in the conductor to the fully monolithic Hall and coil IC. The current is sensed differentially by two Hall plates and two coils that subtract out interfering common-mode magnetic fields. The IC has no physical connection to the integrated current conductor and provides a 3500 V_{RMS} (LZ) and 4242 V_{RMS} (MY) isolation voltage between the primary signal leads. These high ratings provide a basic working voltage of 905 V_{RMS} (LZ) and 1000 V_{RMS} (MY) isolation voltage between the primary and secondary signal leads of the package.

Both zero current reference (ACS37030) and overcurrent fault with internal pull up (ACS37032) options are available.

The ACS37030/32 is provided in two six-lead custom SOIC surface mount packages; these packages are low resistance, <1 mΩ with fuse-lead current conductors. The LZ package has a resistance of 0.6 mΩ with a creepage/clearance of 4.1 mm, while the MY package has a resistance of 0.9 mΩ with a creepage/clearance of 8.5 mm. The leadframe is plated with 100% matte tin, which is compatible with standard lead (Pb) free printed circuit board assembly processes. Internally, the device is Pb-free.

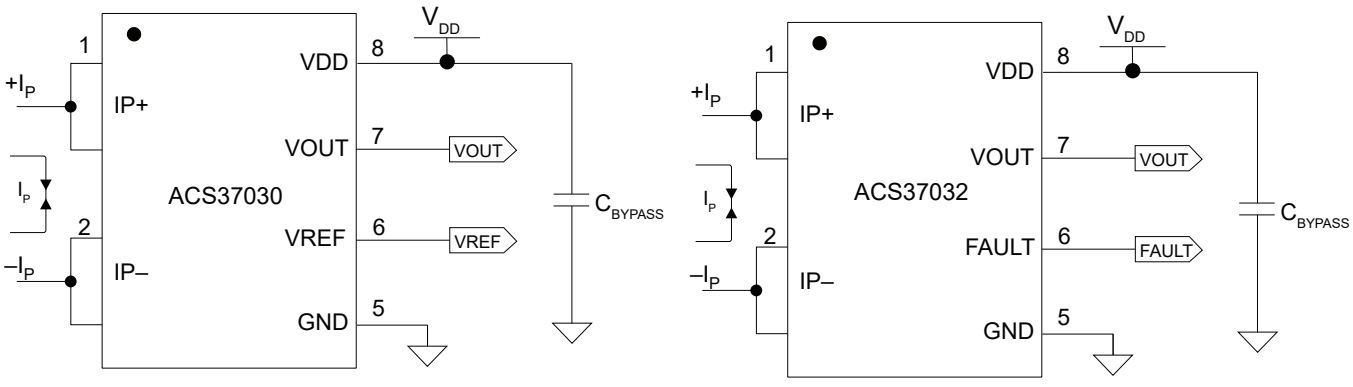


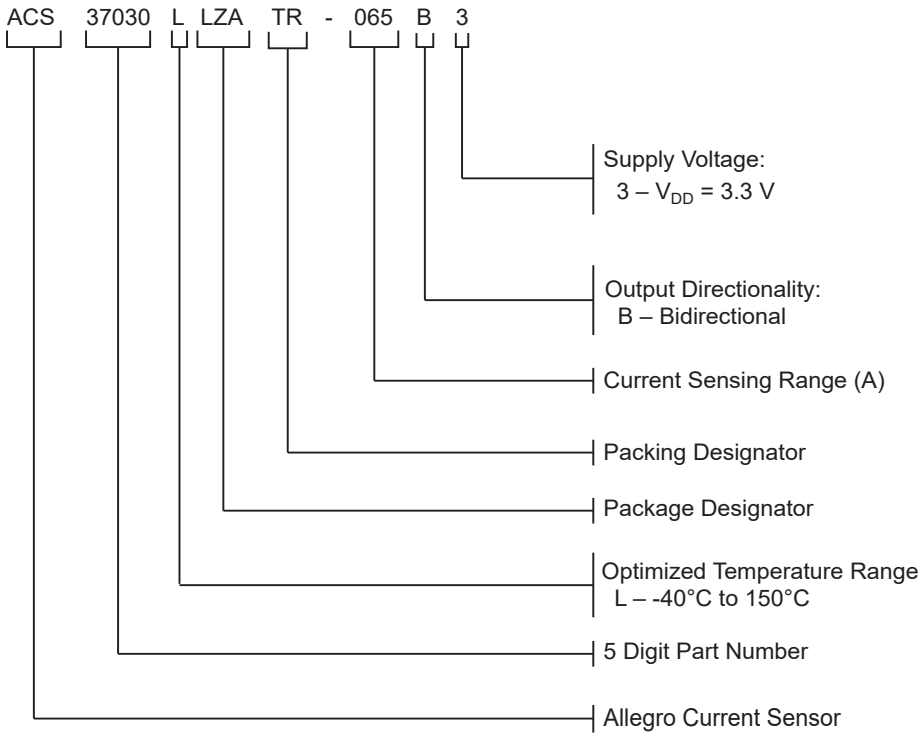
Figure 1: Typical Application Circuit

The device outputs an analog signal, V_{OUT}, that varies linearly with the bidirectional AC or DC primary current, I_P, within the ranges specified.

SELECTION GUIDE

Part Number	Current Sensing Range, I_{PR} (A)	Sensitivity (mV/A)	V_{DD} (V)	V_{QVO} (V)	Feature	Optimized Temperature Range T_A (°C)	Packing
LZ Package							
ACS37030LLZATR-020B3	±20	66	3.3	1.65	VREF	–40 to 150	Tape and reel, 3000 pieces per reel
ACS37030LLZATR-040B3	±40	33					
ACS37030LLZATR-065B3	±65	20.3					
ACS37032LLZATR-020B3	±20	66			FAULT		
ACS37032LLZATR-040B3	±40	33					
ACS37032LLZATR-065B3	±65	20.3					
MY Package (Wide Body)							
ACS37030LMYATR-025B3	±25	52.8	3.3	1.65	VREF	–40 to 150	Tape and reel, 3000 pieces per reel
ACS37030LMYATR-040B3	±40	33					
ACS37030LMYATR-065B3	±65	20.3					
ACS37032LMYATR-025B3	±25	52.8			FAULT		
ACS37032LMYATR-040B3	±40	33					
ACS37032LMYATR-065B3	±65	20.3					

PART NAMING SPECIFICATION



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ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{DD}		–0.5 to 4	V
Forward Output Voltage	V_O	Applies to V_{OUT}, V_{REF}, and FAULT	–0.5 to V_{DD} + 0.5 (< 3.8)	V
Operating Ambient Temperature	T_A	L temperature range	–40 to 150	°C
Storage Temperature	T_{stg}		–65 to 165	°C
Maximum Junction Temperature	T_{JMAX}	Sensing range of sensor is limited by T_{JMAX} = 165°C	165	°C

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

LZ PACKAGE ISOLATION CHARACTERISTICS

Characteristic	Symbol	Notes	Value	Units
Withstand Strength [1][2]	V_{ISO}	Agency rated for 60 seconds per UL 62368-1 (edition 3)	3500	V_{RMS}
Working Voltage for Basic Isolation [2]	V_{WVBI}	Maximum approved working voltage for basic (single) isolation according to UL 62368-1 (edition 3)	1280	V_{PK} or V_{DC}
			905	V_{RMS}
Working Voltage for Reinforced Isolation [2]	V_{WVRI}	Maximum approved working voltage for reinforced isolation according to UL 62368-1 (edition 3)	717	V_{PK} or V_{DC}
			507	V_{RMS}
Surge Voltage	V_{SURGE}	1.2/50 µs waveform, tested in dielectric fluid to determine the intrinsic surge immunity of the isolation barrier	13000	V_{PK}
Impulse Withstand	$V_{IMPULSE}$	1.2/50µs waveform, tested in air	5000	V_{RMS}
Clearance	D_{CL}	Minimum distance through air from IP leads to signal leads	4.1	mm
Creepage	D_{CR}	Minimum distance along package body from IP leads to signal leads	4.1	mm
Distance Through Insulation	DTI	Minimum internal distance through insulation	54	µm
Comparative Tracking Index	CTI	Material Group I	>600	V

[1] Production tested in accordance UL 62368-1 (edition 3).
[2] Certification pending.

MY PACKAGE ISOLATION CHARACTERISTICS

Characteristic	Symbol	Notes	Value	Units
Withstand Strength [1][2]	V_{ISO}	Agency rated for 60 seconds per UL 62368-1 (edition 3)	4242	V_{RMS}
Working Voltage for Basic Isolation [2]	V_{WVBI}	Maximum approved working voltage for basic (single) isolation according to UL 62368-1 (edition 3)	1414	V_{PK} or V_{DC}
			1000	V_{RMS}
Working Voltage for Reinforced Isolation [2]	V_{WVRI}	Maximum approved working voltage for reinforced isolation according to UL 62368-1 (edition 3)	707	V_{PK} or V_{DC}
			500	V_{RMS}
Surge Voltage	V_{SURGE}	1.2/50 µs waveform, tested in dielectric fluid to determine the intrinsic surge immunity of the isolation barrier	10000	V_{PK}
Impulse Withstand	$V_{IMPULSE}$	1.2/50µs waveform, tested in air	6000	V_{RMS}
Clearance	D_{CL}	Minimum distance through air from IP leads to signal leads	8.5	mm
Creepage	D_{CR}	Minimum distance along package body from IP leads to signal leads	8.5	mm
Distance Through Insulation	DTI	Minimum internal distance through insulation	54	µm
Comparative Tracking Index	CTI	Material Group II	400 to 599	V

[1] Production tested in accordance UL 62368-1 (edition 3).
[2] Certification pending.

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THERMAL CHARACTERISTICS

Characteristic	Symbol	Notes	Value	Unit
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	LZ package; mounted on the standard LZ Current Sensor Evaluation Board (ACSEVB-LC8-LZ6)	16	°C/W
		MY package; mounted on the standard MY Current Sensor Evaluation Board (ACSEVB-MZ6-MY6)	17	°C/W
Package Thermal Metric (Junction to Top)	Ψ_{JT}	LZ package; mounted on the standard LZ Current Sensor Evaluation Board (ACSEVB-LC8-LZ6)	0	°C/W
		MY package; mounted on the standard MY Current Sensor Evaluation Board (ACSEVB-MZ6-MY6)	–3	°C/W
Package Thermal Resistance (Junction to Case)	$R_{\theta JC}$	LZ package; simulated per the methods in JESD51-1	23	°C/W
		MY package; simulated per the methods in JESD51-1	26	°C/W
Package Thermal Resistance (Junction to Board)	$R_{\theta JB}$	LZ package; simulated per the methods in JESD51-8	12	°C/W
		MY package; simulated per the methods in JESD51-8	7	°C/W

PACKAGE CHARACTERISTICS

Characteristic	Symbol	Notes	Min.	Typ.	Max.	Unit
Internal Conductor Resistance	R_{IC}	T_A = 25°C, LZ	–	0.68	–	mΩ
		T_A = 25°C, MY	–	0.9	–	mΩ
Internal Conductor Inductance	L_{IC}	T_A = 25°C, LZ	–	2.2	–	nH
		T_A = 25°C, MY	–	4.4	–	nH
Moisture Sensitivity Level	MSL	Per IPC/JEDEC J-STD-020	–	2	–	–

PINOUT DIAGRAM AND TERMINAL LIST TABLE

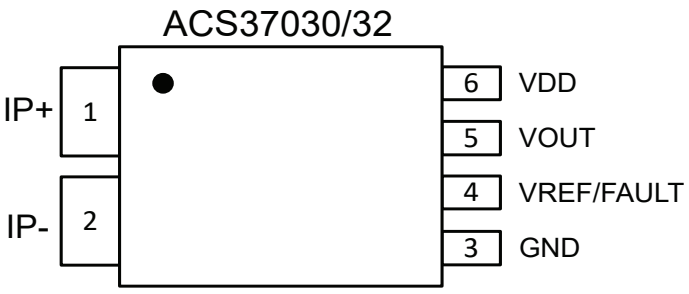

Figure 2: Package Pinout Diagram

Terminal List

Number	Name	Description
1	IP+	Positive terminal for current being sensed
2	IP–	Negative terminal for current being sensed
3	GND	Device ground terminal
4	VREF/FAULT	Reference or overcurrent fault output
5	VOUT	Analog output signal
6	VDD	Device power supply terminal

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FUNCTIONAL BLOCK DIAGRAM

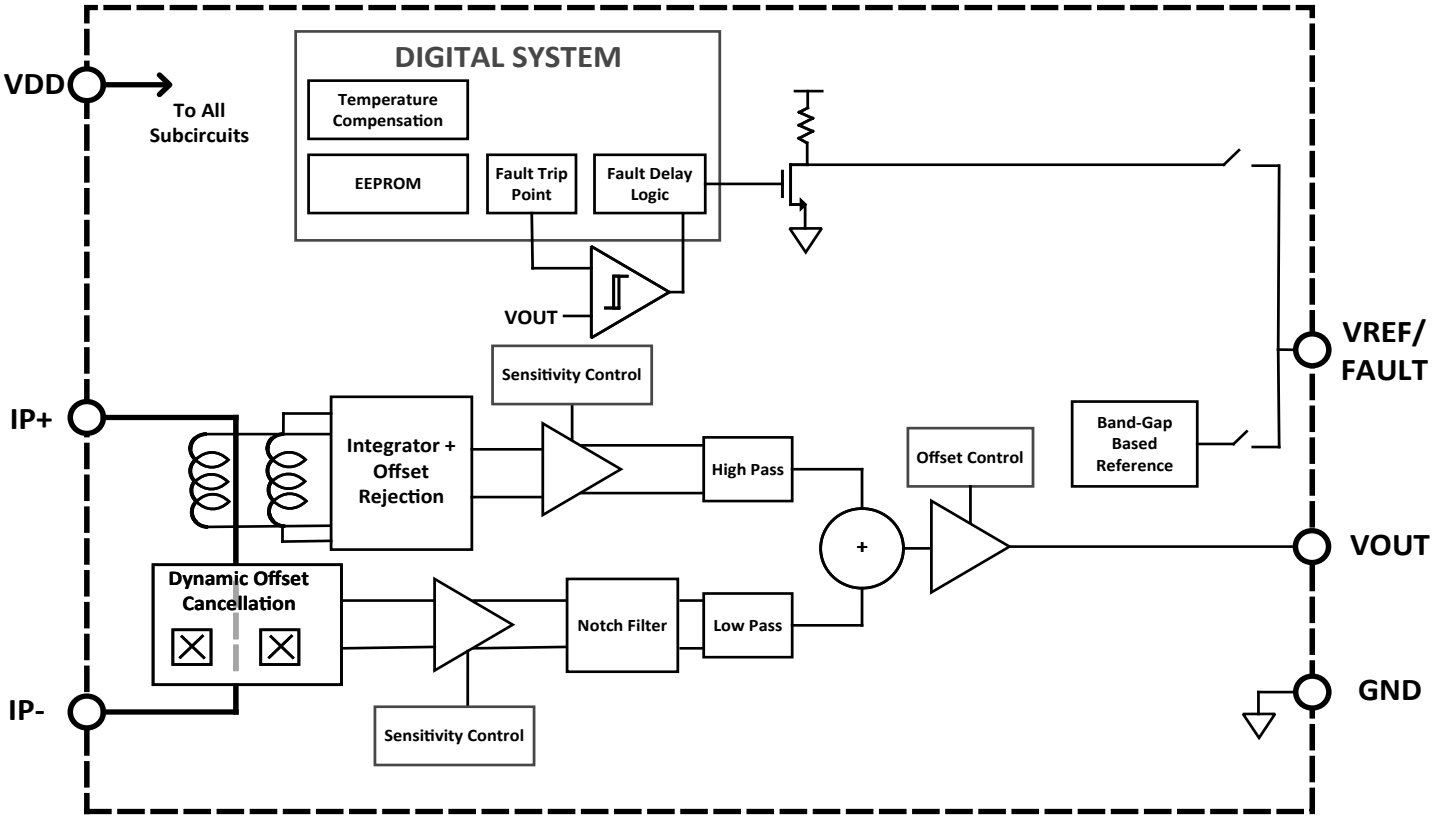

Figure 3: Functional Block Diagram

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NOTE: This is a short-form datasheet for preview purposes. Pages 6–26 have been removed. Contact Allegro MicroSystems to request a complete datasheet.

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PACKAGE OUTLINE DRAWING

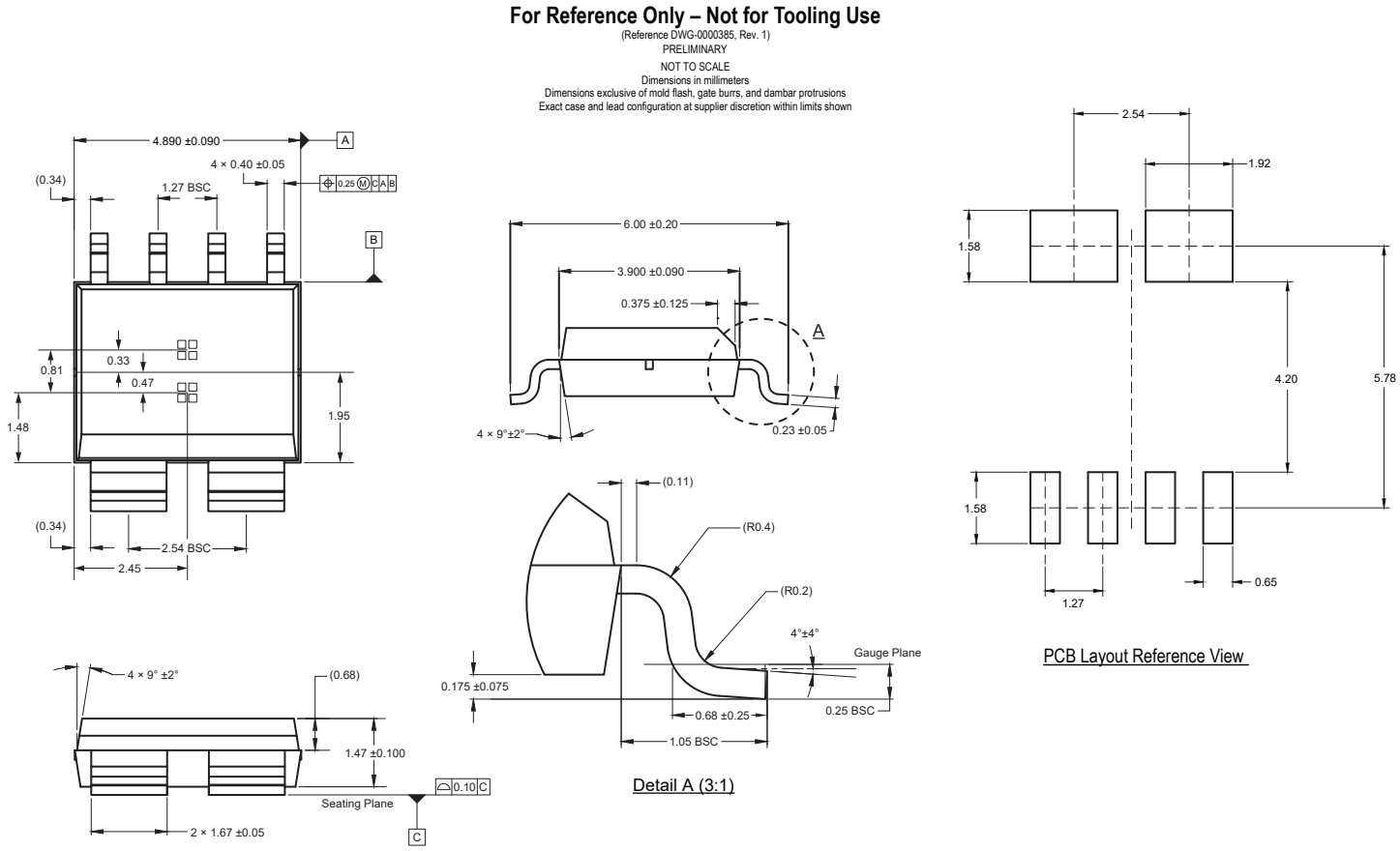
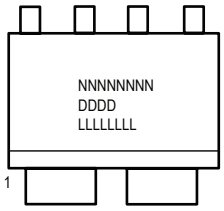


Figure 16: Custom 6-Pin SOIC (Suffix LZ)



Standard Branding Reference View

N = Device Part Number
D = Date Code
L = Assembly Lot Number

Figure 17: LZ Package Branding

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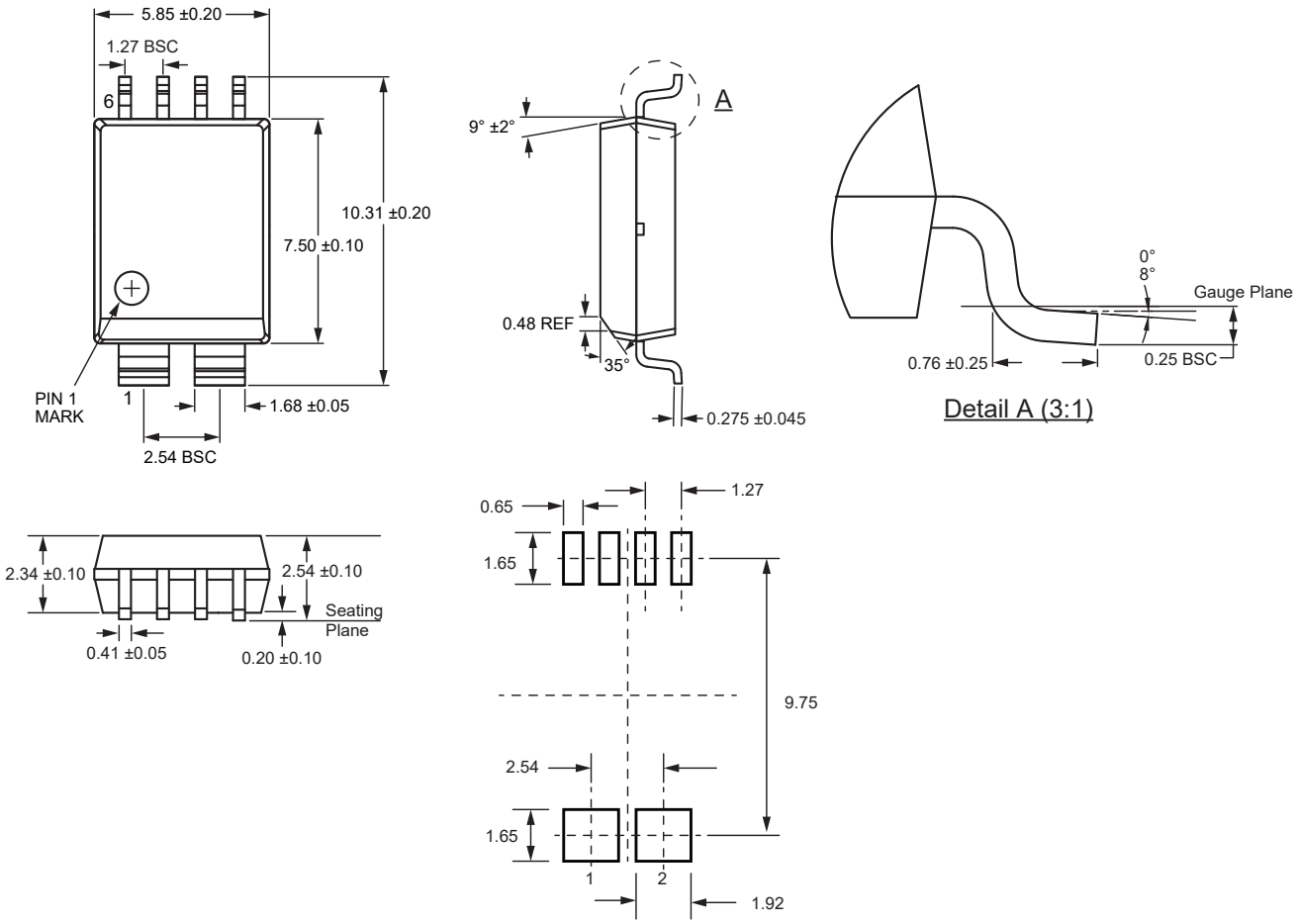
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000388, Rev. 2)

NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



PCB Layout Reference View

All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

Figure 18: Custom 6-Pin SOIC (Suffix MY)

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Revision History

Number	Date	Description
–	November 29, 2023	Initial release
1	January 18, 2024	Added UL Number (page 1); removed "certification pending" footnote from Isolation Characteristics table (page 3); updated Sensitivity Error and Coil Path Sensitivity Error test conditions (pages 6-11); updated Thermal Performance section (pages 18-19)
2	June 12, 2024	Added output resistive load characteristic (page 5)
3	March 14, 2025	Added MY package variants and overhauled datasheet for MY package variants (all pages)

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