ACS37100

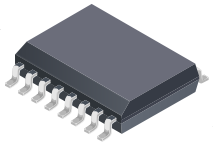
10 MHz TMR Current Sensor with Overcurrent FAULT Detection and Output Voltage Reference

FEATURES AND BENEFITS

- Tunneling magnetoresistance (TMR) sensing element
- High operating bandwidth for fast control loops or where high-speed switching currents are monitored
  - □ DC to 10 MHz bandwidth
  - □ 50 ns typical response time
- High accuracy and low noise
  - □ ±2% sensitivity error over temperature
  - □ ±8 mV maximum offset voltage over temperature
  - □ 26 mA_{RMS} input referred noise
  - □ 3.3 V non-ratiometric supply operation
  - □ Multiple gain options available
  - □ Differential sensing immune to external magnetic fields
- VREF output voltage for differential routing in noisy application environments
- Overcurrent FAULT output with adjustable FAULT threshold for fast open-drain overcurrent detection
- UL-certified, highly isolated compact surface-mount packages
- Available in 16-pin SOICW package: MA (8 mm creepage)
- Wide operating temperature, –40°C to 150°C
- Grade 0, AEC-Q100 automotive qualified

PACKAGE: 16-Pin SOICW

Suffix MA



Not to scale

DESCRIPTION

The ACS37100 is a fully integrated TMR current sensor in an SOICW-16 package that is factory-trimmed to provide high accuracy over the entire operating range without the need for customer programming.

The internal construction provides high isolation by magnetically coupling the field generated by current flow in the conductor to the monolithic TMR IC. The current is sensed differentially by two TMR bridges that subtract out interfering common-mode magnetic fields. The IC has no physical connection to the integrated current conductor and provides a 5000 V_{RMS} isolation voltage between the primary signal leads. This high rating provides a basic working voltage of 1097 V_{RMS} (MA package) between the primary and secondary signal leads of the package. The SOICW-16 MA package has 1.2 mΩ conductor resistance.

The ACS37100 integrates a fast adjustable overcurrent fault feature, which provides hardware short-circuit detection for system protection. The device also integrates a voltage reference output (VREF) that provides a stable voltage that corresponds to the 0 A output voltage, allowing for differential measurements of the output.

The leadframe is plated with 100% matte tin, which is compatible with standard lead (Pb) free printed circuit board assembly processes. Internally, the device is Pb-free.

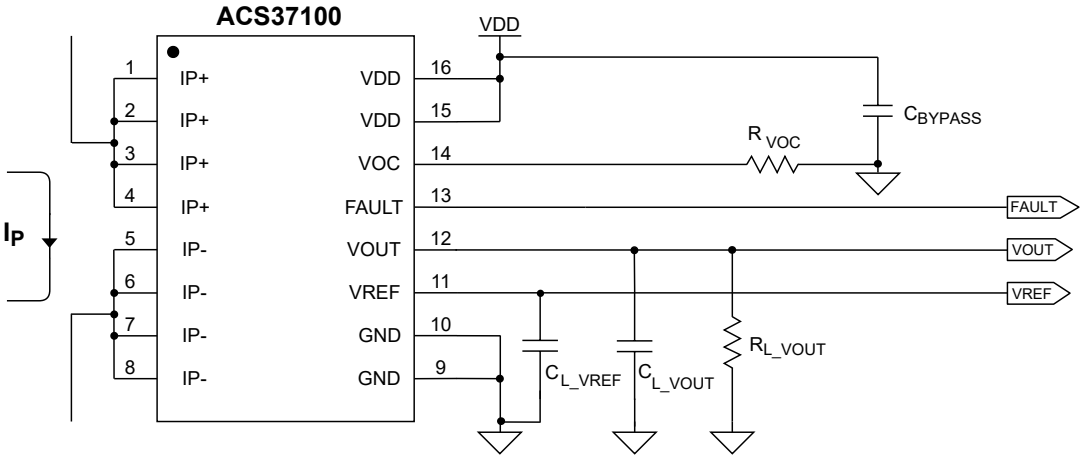


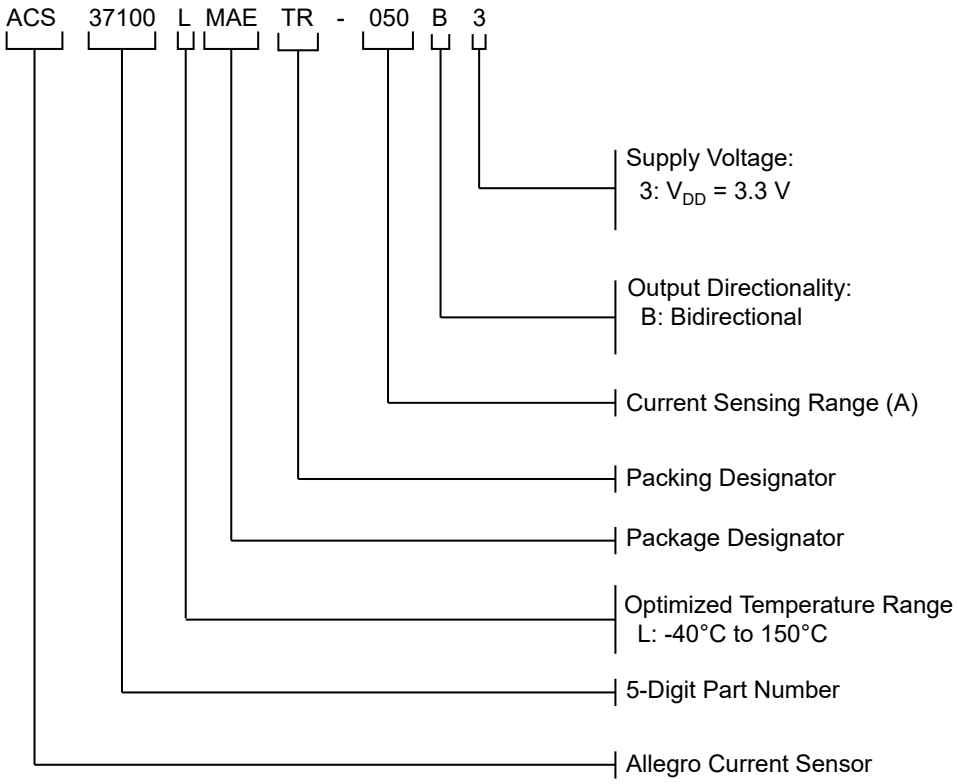
Figure 1: Typical Application Circuit

The device outputs an analog signal, V_{OUT}, that varies linearly with the bidirectional AC or DC primary current, I_P, within the ranges specified.

SELECTION GUIDE

Part Number	Current Sensing Range, I_{PR} (A)	Sensitivity (mV/A)	Nominal V_{DD} (V)	Optimized Temp. Range T_A (°C)	Packing
ACS37100LMAETR-025B3	±25	52.8	3.3	–40 to 150	1000 pieces per 13-inch reel
ACS37100LMAETR-050B3	±50	26.4	3.3		

PART NAMING SPECIFICATION



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ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Min.	Max.	Unit
Supply Voltage	V_{DD}		–0.5	4	V
Output Voltage	V_O	Applies to V_{OUT}, FAULT, and V_{REF}	–0.5	$(V_{DD} + 0.5) \leq 3.8$	V
Input Voltage	V_I	Applies to VOC	–0.5	$(V_{DD} + 0.5) \leq 3.8$	V
Input Current	I_P	Current above this value can cause a permanent change in performance	–150	150	A
Operating Ambient Temperature	T_A	L temperature range	–40	150	°C
Storage Temperature	T_{stg}		–65	165	°C
Maximum Junction Temperature	$T_{J(MAX)}$		–	165	°C

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

ISOLATION CHARACTERISTICS

Characteristic	Symbol	Notes	Rating	Unit
Withstand Voltage [1]	V_{ISO}	Agency rated for 60 seconds per UL 62368-1 (edition 3)	5000	V_{RMS}
Working Voltage for Basic Insulation	V_{WVBI}	Maximum approved working voltage for basic (single) isolation according to UL 62368-1 (edition 3)	1550	V_{PK} or V_{DC}
			1097	V_{RMS}
Working Voltage for Reinforced Insulation	V_{WVRI}	Maximum approved working voltage for reinforced insulation according to UL 62368-1 (edition 3)	800	V_{PK} or V_{DC}
			565	V_{RMS}
Surge Voltage	V_{SURGE}	1.2/50 µs waveform, tested in dielectric fluid to determine the intrinsic surge immunity of the isolation barrier	10000	V_{PK}
Impulse Withstand	$V_{IMPULSE}$	1.2/50 µs waveform, tested in air	7071	V_{RMS}
Clearance	D_{CL}	Minimum distance through air from IP leads to signal leads	8	mm
Creepage	D_{CR}	Minimum distance along package body from IP leads to signal leads	8	mm
Distance Through Insulation	DTI	Minimum internal distance through insulation	105	µm
Comparative Track Index	CTI	Material Group II	400 to 599	V

[1] Production tested in accordance with UL 62368-1 (edition 3).

THERMAL CHARACTERISTICS

Characteristic	Symbol	Notes	Value	Unit
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	Mounted on the standard MA/LA Current Sensor Evaluation Board (ACSEVB-MA16-LA16)	20	°C/W
Package Thermal Metric (Junction to Top)	Ψ_{JT}		2.4	°C/W
Package Thermal Resistance (Junction to Case)	$R_{\theta JC}$	Simulated per the methods in JESD51-1	14	°C/W
Package Thermal Resistance (Junction to Board)	$R_{\theta JB}$	Simulated per the methods in JESD51-8	14	°C/W

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PINOUT DIAGRAM AND TERMINAL LIST TABLE

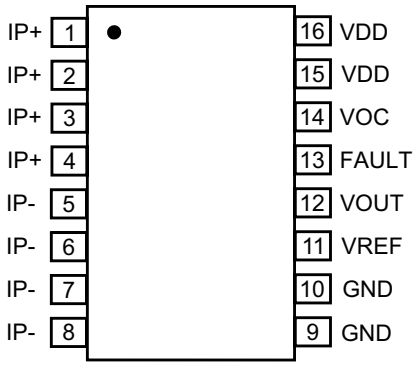

Figure 2: MA Pinout Diagram

Terminal List Table

Number	Name	Description
1, 2, 3, 4	IP+	Positive terminals for current being sensed; fused internally
5, 6, 7, 8	IP-	Negative terminals for current being sensed; fused internally
9	GND	Device ground terminal
10		
11	VREF	Zero current voltage reference
12	VOUT	Analog output representing the current flowing through I_P
13	FAULT	Overcurrent fault, open-drain
14	VOC	Sets the overcurrent FAULT threshold via external resistor divider; if not using VOC, connect to GND for 100% overcurrent FAULT operating threshold
15	VDD	Device power supply terminal
16		

PACKAGE CHARACTERISTICS

Characteristic	Symbol	Notes	Min.	Typ.	Max.	Unit
Internal Conductor Resistance	R_{IC}	T_A = 25°C	–	1.2	–	mΩ
Internal Conductor Inductance	L_{IC}	T_A = 25°C	–	4.2	–	nH
Moisture Sensitivity Level	MSL	Per IPC/JEDEC J-STD-020	–	3	–	–

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FUNCTIONAL BLOCK DIAGRAM

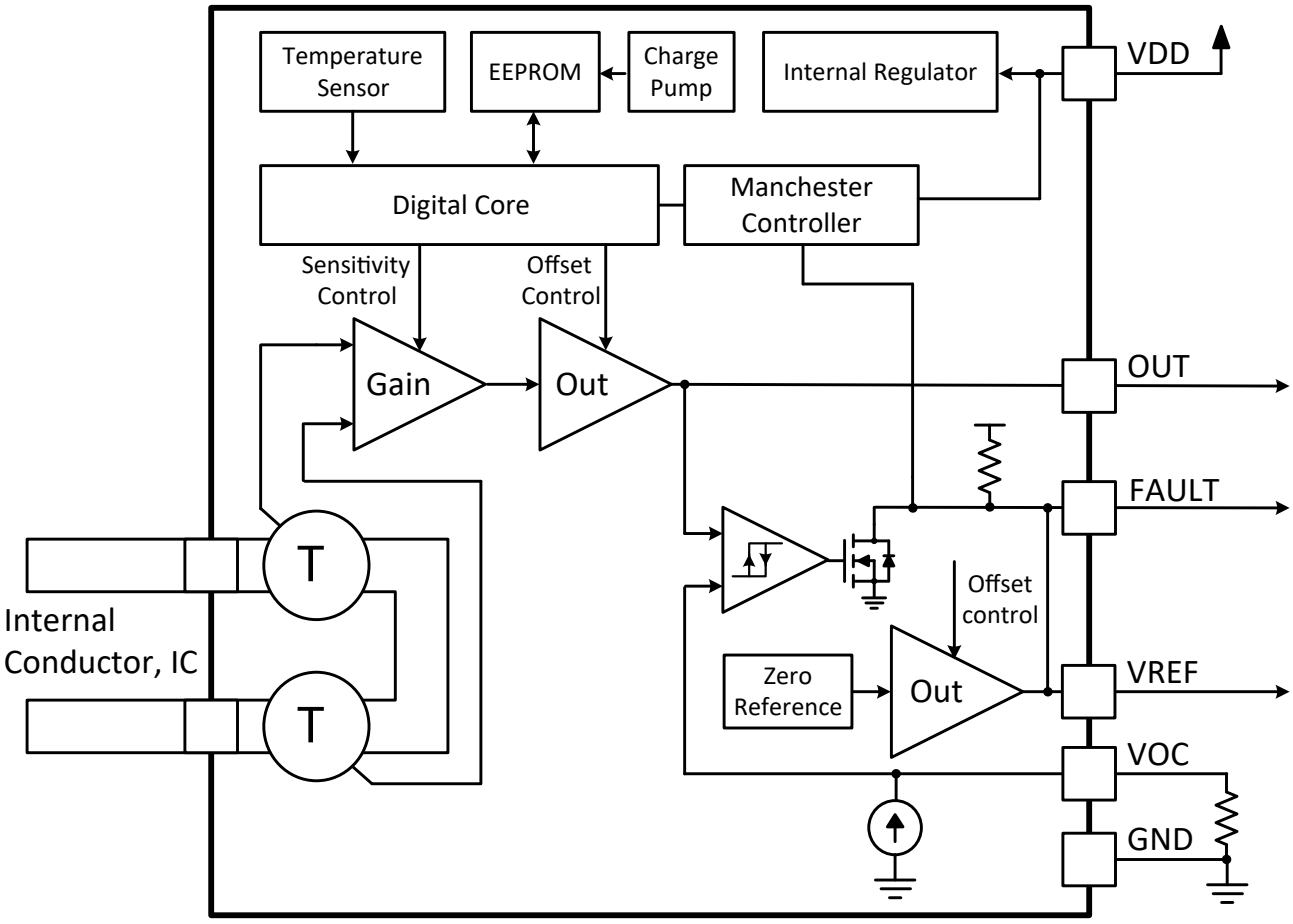

Figure 3: Functional Block Diagram

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COMMON ELECTRICAL CHARACTERISTICS: Valid through the full operating temperature range, T_A = –40°C to 150°C, C_{BYPASS} = 0.1µF, and V_{DD} = $V_{DD(TYP)}$, unless specified otherwise. Minimum and maximum values are tested in production or validated by design and characterization.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}		3.0	3.3	3.6	V
Supply Current	I_{DD}	No load on VOUT, FAULT, and VOC	–	10	20	mA
Supply Bypass Capacitor [1]	C_{BYPASS}		0.1	–	–	µF
VOUT Capacitive Load	C_{L_VOUT}		–	–	100	pF
VOUT Resistive Load	R_{L_VOUT}		50	–	–	kΩ
Power-On Reset Voltage	V_{POR}	T_A = 25°C, V_{DD} rising 1 V/ms	2.6	2.9	3	V
Power-On Reset Hysteresis	V_{POR_HYST}		200	–	600	mV
Power-on Time	t_{PO}		–	100	–	µs
OUTPUT SIGNAL CHARACTERISTICS (VOUT)						
Output Saturation Voltage	V_{SAT_H}	R_L = 50 kΩ to GND	V_{DD} – 0.2	–	–	V
	V_{SAT_L}	R_L = 50 kΩ to VDD	–	–	0.15	V
VOUT Short Circuit Current	I_{SC_VOUT}	T_A = 25°C, VOUT to GND	–	1.4	–	mA
		T_A = 25°C, VOUT to VDD	–	1.4	–	mA
Bandwidth	BW	Small signal –3 dB, C_L = 100 pF	–	10	–	MHz
Rise Time	t_R	T_A = 25°C, C_L = 100 pF	–	50	–	ns
Response Time	t_{RESP}	T_A = 25°C, C_L = 100 pF	–	50	–	ns
Propagation Delay	t_{PD}	T_A = 25°C, C_L = 100 pF	–	50	–	ns
Noise	I_N	BW = 10 MHz, T_A = 25°C, C_{L_VOUT} = 100 pF	–	26	–	mA_{RMS}
REFERENCE OUTPUT CHARACTERISTICS (VREF)						
VREF Capacitive Load	C_{L_VREF}	VREF to GND	–	–	100	pF
VREF Resistive Load	R_{L_VREF}	VREF to GND, VREF to VDD	50	–	–	kΩ
VREF Short Circuit Current	I_{SC_VREF}	T_A = 25°C, shorted to GND	–	1.4	–	mA
		T_A = 25°C, shorted to VDD	–	1.4	–	mA
FAULT OUTPUT CHARACTERISTICS (FAULT and VOC)						
Overcurrent Operating Range	I_{OCR}		50	–	200	$\%I_{PR}$
FAULT Internal Pull-Up Resistance	R_{L_IFAULT}	FAULT to VDD	–	10	–	kΩ
Overcurrent Error	E_{OC}	T_A = 25°C	–10	–	10	$\%I_{OCR}$ [2]
FAULT Output Low Voltage	V_{FAULT_L}	R_{L_FAULT} = 10 kΩ, fault condition present	–	–	0.4	V
FAULT Leakage Current	I_{FAULT_OFF}	R_{L_FAULT} = 10 kΩ, no fault condition present	–	1	–	µA
Overcurrent FAULT Hysteresis	I_{OC_HYST}	T_A = 25°C	–	6	–	$\%I_{PR}$
Overcurrent FAULT Response Time [1]	t_{OC_RESP}	T_A = 25°C	–	100	–	ns
Overcurrent FAULT Release Time [1]	t_{OC_HLD}	T_A = 25°C	–	2	–	µs
VOC Input Linear Operating Range	V_{OR_VOC}	T_A = 25°C	0.66	1.32	2.64	V

[1] Validated by design and characterization.
[2] Where I_{OCR} is the specific point at which the overcurrent FAULT trigger will occur.

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ACS37100LMAETR-025B3 PERFORMANCE CHARACTERISTICS: Valid through full operating temperature range, T_A = – 40°C to 150°C, C_{BYPASS} = 0.1 µF, and typical V_{DD}, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
NOMINAL PERFORMANCE						
Current Sensing Range	I_{PR}	Limited by T_{JMAX} = 165°C	–25	–	25	A
Sensitivity	Sens	$I_{PR(min)} < I_P < I_{PR(max)}$	–	52.8	–	mV/A
Quiescent Voltage Output	V_{QVO}	I_P = 0A	–	1.65	–	V
Reference Voltage Output	V_{REF}		–	1.65	–	V
Overcurrent FAULT Threshold	I_{OC}		–	±25	–	A
Overcurrent FAULT Hysteresis	I_{OC_HYST}		–	1.5	–	A
FAULT ERROR						
Overcurrent Error	I_{OC_E}		–2.5	–	2.5	A
ERROR COMPONENTS						
Sensitivity Error	E_{SENS}	$I_P = I_{PR(max)}$, T_A = –40°C to 150°C	–2	–	2	%
Offset Error	V_{OE}	I_P = 0 A, T_A = –40°C to 150°C	–8	–	8	mV
Reference Voltage Output Error	V_{REF_E}	I_P = 0 A, T_A = –40°C to 150°C	–10	–	10	mV
Quiescent Voltage Offset Error	V_{QVO_E}	I_P = 0 A, T_A = –40°C to 150°C	–10	–	10	mV
Noise	N	T_A = 25°C, C_L = 1 nF, BW = 10 MHz	–	1.4	–	mV_{RMS}
Power Supply Offset Error	V_{OE_PS}	$V_{DD(TYP)}$ ± 5%	–5	–	5	mV
Power Supply Sensitivity Error	E_{SENS_PS}	$V_{DD(TYP)}$ ± 5%	–1.1	–	1.1	%
ERROR INCLUDING LIFETIME DRIFT [2][3]						
Sensitivity Error Including Lifetime Drift	E_{SENS_LT}	$I_P = I_{PR(MAX)}$, T_A = –40°C to 150°C	–	±0.75	–	%
Offset Error Including Lifetime Drift	V_{OE_LT}	I_P = 0 A, T_A = –40°C to 150°C	–	±3.5	–	mV
Reference Voltage Error Including Lifetime Drift	V_{REF_LT}	T_A = –40°C to 150°C	–	±2.5	–	mV
Quiescent Voltage Error Including Lifetime Drift	V_{QVO_LT}	I_P = 0 A, T_A = –40°C to 150°C	–	±3	–	mV

[1] Absolute minimum (Min. or min) and absolute maximum (Max. or max) are the production limits that the device must not exceed.
[2] Validated by design and characterization
[3] Lifetime drift is the mean drift of worst-case distribution observed after AEC-Q100 qualification stresses.

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ACS37100LMAETR-050B3 PERFORMANCE CHARACTERISTICS: Valid through full operating temperature range, T_A = – 40°C to 150°C, C_{BYPASS} = 0.1 µF, and typical V_{DD}, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
NOMINAL PERFORMANCE						
Current Sensing Range	I_{PR}		–50	–	50	A
Sensitivity	Sens	$I_{PR(min)} < I_P < I_{PR(max)}$	–	26.4	–	mV/A
Quiescent Voltage Output	V_{QVO}	I_P = 0A	–	1.65	–	V
Reference Voltage Output	V_{REF}		–	1.65	–	V
Overcurrent FAULT Threshold	I_{OC}		–	±50	–	A
Overcurrent FAULT Hysteresis	I_{OC_HYST}		–	3	–	A
FAULT ERROR						
Overcurrent Error	I_{OC_E}		–5	–	5	A
ERROR COMPONENTS						
Sensitivity Error	E_{SENS}	$I_P = I_{PR(max)}$, T_A = –40°C to 150°C	–2	–	2	%
Offset Error	V_{OE}	I_P = 0 A, T_A = –40°C to 150°C	–8	–	8	mV
Reference Voltage Output Error	V_{REF_E}	I_P = 0 A, T_A = –40°C to 150°C	–10	–	10	mV
Quiescent Voltage Offset Error	V_{QVO_E}	I_P = 0 A, T_A = –40°C to 150°C	–10	–	10	mV
Noise	N	T_A = 25°C, C_L = 1 nF, BW = 10 MHz	–	0.7	–	mV_{RMS}
Power Supply Offset Error	V_{OE_PS}	$V_{DD(TYP)}$ ± 5%	–5	–	5	mV
Power Supply Sensitivity Error	E_{SENS_PS}	$V_{DD(TYP)}$ ± 5%	–1.1	–	1.1	%
ERROR INCLUDING LIFETIME DRIFT [2][3]						
Sensitivity Error Including Lifetime Drift	E_{SENS_LT}	$I_P = I_{PR(MAX)}$, T_A = –40°C to 150°C	–	±0.75	–	%
Offset Error Including Lifetime Drift	V_{OE_LT}	I_P = 0 A, T_A = –40°C to 150°C	–	±3.5	–	mV
Reference Voltage Error Including Lifetime Drift	V_{REF_LT}	T_A = –40°C to 150°C	–	±2.5	–	mV
Quiescent Voltage Error Including Lifetime Drift	V_{QVO_LT}	I_P = 0 A, T_A = –40°C to 150°C	–	±3	–	mV

[1] Absolute minimum (Min. or min) and absolute maximum (Max. or max) are the production limits that the device must not exceed.
[2] Validated by design and characterization
[3] Lifetime drift is the mean drift of worst-case distribution observed after AEC-Q100 qualification stresses.

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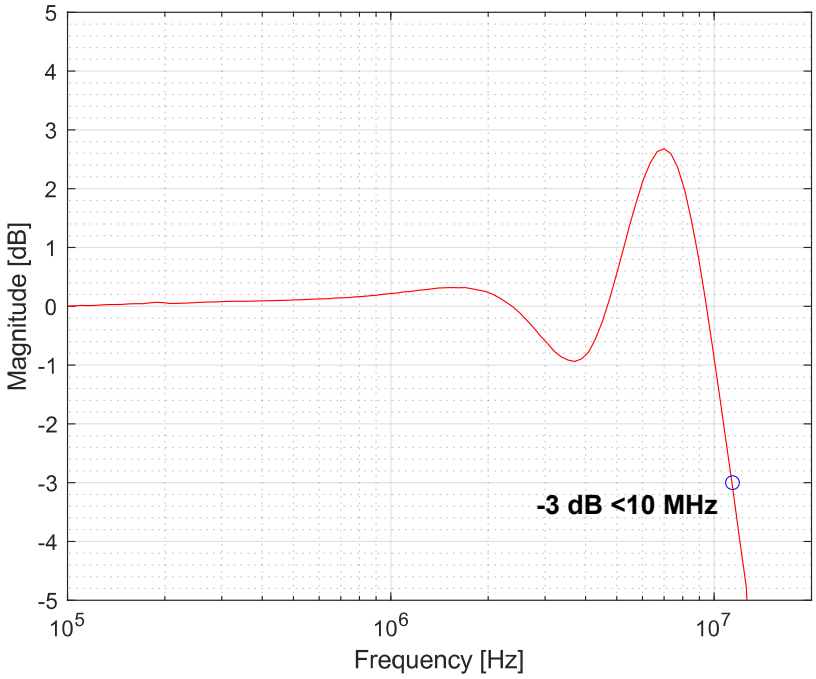
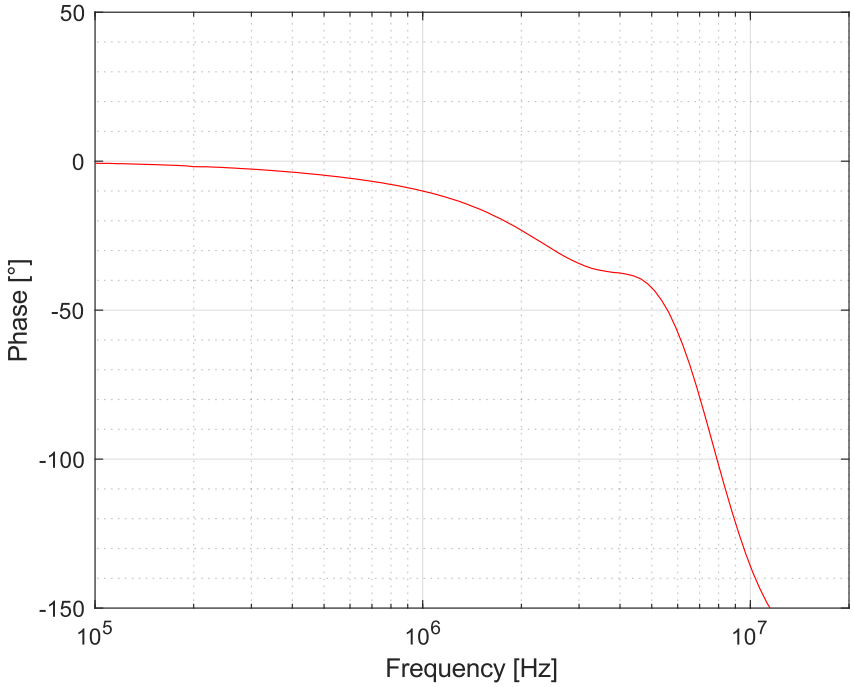
ACS37100 TYPICAL FREQUENCY RESPONSE





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RESPONSE CHARACTERISTICS DEFINITIONS

Response Time (t_{RESP})

The time interval between a) when the sensed input current reaches 90% of its full-scale value, and b) when the sensor output, V_{OUT}, reaches 90% of its full-scale output value.

Propagation Delay (t_{PD})

The time interval between a) when the sensed input current reaches 20% of its full-scale value, and b) when the sensor output, V_{OUT}, reaches 20% of its full-scale output value.

Rise Time (t_R)

The time interval between a) when the sensor output, V_{OUT}, reaches 10% of its full-scale value, and b) when the sensor output, V_{OUT}, reaches 90% of its full-scale value.

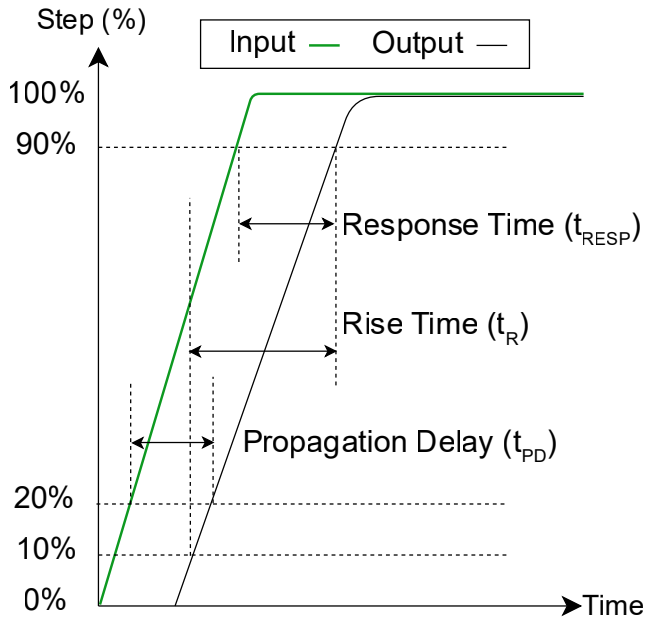

Figure 4: Step Response Characteristics

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FUNCTIONAL DESCRIPTION OF POWER ON/OFF OPERATION

Introduction

The graphs in this section show the behavior of V_{OUT} as V_{DD} increases to greater than or reduces to less than the required power-on voltage. The same labeling convention for different voltage thresholds is used in Figure 5 and Figure 6. References in brackets "[ ]" are valid for each of these graphs.

Power-On Operation

As the supply voltage, V_{DD}, ramps up, the VOUT pin is in a high-impedance state (high-Z) until V_{DD} reaches and passes V_{POR} [1]. Once V_{DD} has passed V_{POR} [1], VOUT enters typical operation and starts responding to applied current, I_P.

Power-Off Operation

As V_{DD} reduces to less than $V_{POR} - V_{POR\_HYST}$, the outputs enter a high-Z state. The hysteresis on the power-on voltage prevents noise on the supply line from causing V_{OUT} to repeatedly enter and exit the high-Z state at approximately the V_{POR} level.

NOTE: Because the device enters a high-Z state and does not drive the output in that state, the time it takes the output to reach a steady state depends on the external circuitry.

Voltage Thresholds

POWER-ON VOLTAGE (V_{POR})

The power-on voltage, V_{POR}, is the supply voltage at which the current sensor enters typical operation and the analog output pin VOUT starts to respond to the applied current, I_P.

POWER-ON RESET HYSTERESIS (V_{POR_HYST})

When the supply voltage reduces to less than $V_{POR} - V_{POR\_HYST}$ [2] while the sensor is in operation, the digital circuitry turns off and the analog output enters a high-Z state. After V_{DD} recovers and exceeds V_{POR} [1], the output enters typical operation after a delay of t_{PO}.

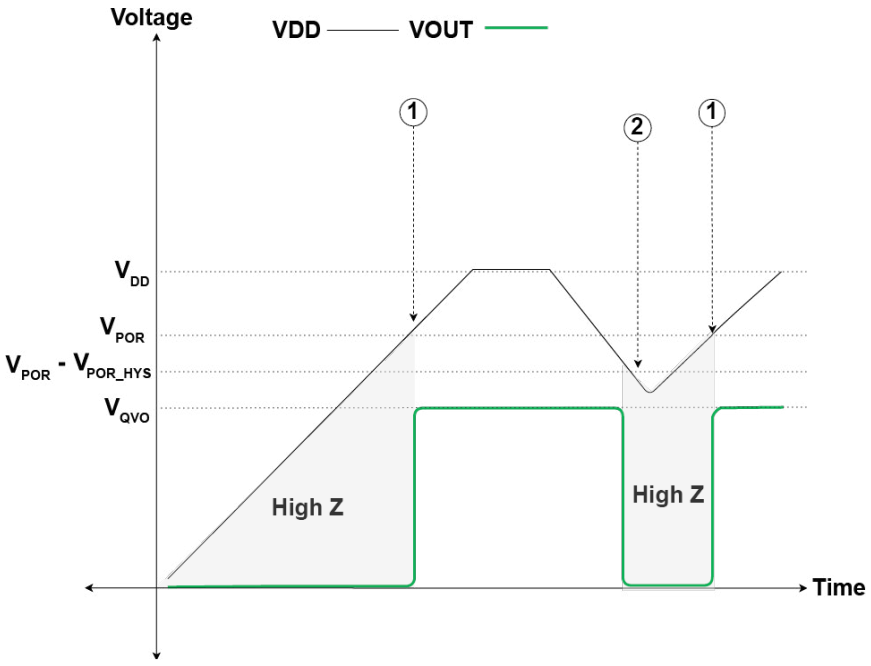

Figure 5: Power-On and Power-Off Operation

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Timing Thresholds

POWER-ON DELAY (t_{PO})

When the supply voltage reaches V_{POR} [1], the device requires a finite time to power its internal components before the outputs are released from the high-impedance state and start to respond to the measured current, I_P. Power-on time, t_{PO}, is defined as the time it takes for the output voltage to settle within ±10% of its steady-state value in the presence of an applied current, I_P, which can be observed as the time from [1] to [A] in Figure 6.

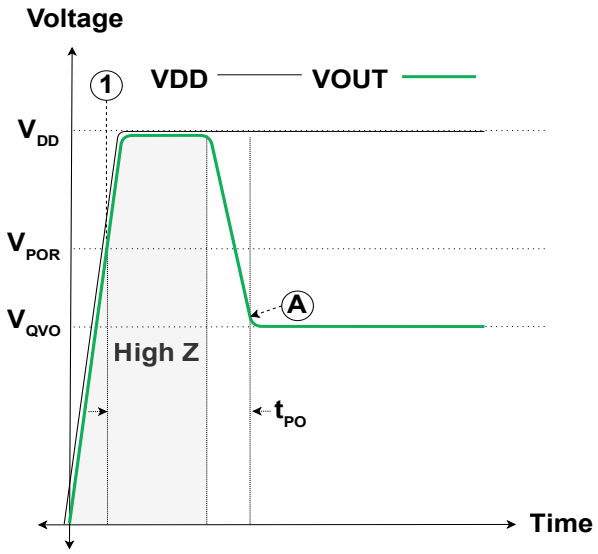

Figure 6: Power-On Delay, t_{PO}

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DEFINITIONS OF OPERATING AND PERFORMANCE CHARACTERISTICS

Quiescent Voltage Output (V_{QVO})

Quiescent voltage output, V_{QVO}, is defined as the voltage on the output, V_{OUT}, when no current is applied, $I_P = 0$.

$$V_{QVO} = V_{OUT\_@0A}\ [mV]$$

Quiescent Voltage Output Error (V_{QVO_E})

Quiescent voltage output error, V_{QVO_E}, is defined as the deviation of V_{QVO} from the nominal target value in production testing.

$$V_{QVO\_E} = V_{QVO\_MEASURED} - V_{QVO\_IDEAL}\ [mV]$$

Power Supply Offset Error (V_{OE_PS})

Power supply offset error, V_{OE_PS}, is defined as the change in V_{QVO} due to variations in the power supply voltage at a specific temperature. The power supply offset error is defined as the change in offset measured between the nominal supply voltage (V_{DD}) and V_{DD} ±E%, where E is the difference between V_{DD} and $V_{DD(MAX)}$ in percent. The error is expressed in mV to indicate how much the offset deviates from its ideal value due to changes in the supply voltage.

$$V_{OE\_PS} = V_{QVO_{@VDD\pm E\%,T_A}} - V_{QVO_{@VDD,T_A}}\ [mV]$$

Sensitivity (Sens)

Sensitivity, or Sens, is defined as the ratio of the V_{OUT} swing and the current through the primary conductor, I_P. The current causes a voltage change on V_{OUT} away from V_{QVO} until V_{SAT}. The magnitude and direction of the output voltage is proportional to the magnitude and direction of the current, I_P. The proportional relationship between output voltage and current is Sensitivity, defined as:

$$Sens = \frac{V_{OUT\_IP1} - V_{OUT\_IP2}}{I_{P1} - I_{P2}}\ [mV/A]$$

where I_{P1} and I_{P2} are two different currents, and $V_{OUT}(I_{P1})$ and $V_{OUT}(I_{P2})$ are the respective output voltages, at VOUT, at those currents.

Sensitivity Error (E_{SENS})

Sensitivity error, E_{SENS}, is the deviation of Sensitivity from the nominal sensitivity target value in production testing.

$$E_{SENS} = \frac{SENS_{MEASURED} - SENS_{IDEAL}}{SENS_{IDEAL}}\ x\ 100\ [\%]$$

Power Supply Sensitivity Error (E_{SENS_PS})

Power supply sensitivity error, E_{SENS_PS}, is a measure of the change in sensitivity due to variations in the power supply voltage at a specific temperature. The power supply sensitivity error is defined as the percentage change in sensitivity measured between the nominal supply voltage (V_{DD}) and V_{DD} ±E%, where E is the difference between V_{DD} and $V_{DD(MAX)}$ in percent. The error is expressed as a percentage to indicate how much the sensitivity deviates from its ideal value due to changes in the supply voltage.

$$E_{SENS\_PS} = \frac{SEN_{@VDD\pm E\%,T_A} - SENS_{@VDD,T_A}}{SENS_{@VDD,T_A}}$$

Output Saturation Voltage (V_{SAT_H} and V_{SAT_L})

Output saturation voltage, V_{SAT}, is defined as the minimum and maximum voltages the VOUT output buffer can drive. V_{SAT_H} is the highest voltage the output can reach, while V_{SAT_L} is the lowest. In other states, the VOUT pin may be pulled outside of V_{SAT_L} and V_{SAT_H}. Note that changing the sensitivity does not change the V_{SAT} points.

Error Including Lifetime Drift (E_{SENS_LT} and V_{QVO_LT})

Lifetime drift characteristics are based on the mean drift of the worst-case distribution observed during AEC-Q100 qualification stresses.

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DEFINITIONS OF OVERCURRENT FAULT CHARACTERISTICS AND PERFORMANCE

OVERCURRENT FAULT PIN ($\overline{FAULT}$)

As the output swings, if the sensed current exceeds its set threshold, the overcurrent FAULT pin triggers with an active low flag. This is internally compared with either the factory-programmed threshold or the VOC voltage. This flag trips symmetrically for the positive and negative overcurrent fault operating point.

VOLTAGE OVERCURRENT PIN (VOC)

The voltage overcurrent pin, or VOC, is a voltage input that is used to set the overcurrent FAULT threshold, I_{OCR}. There are two ways to set the threshold: 1) via a resistor, R_{VOC}, between VOC and GND, or 2) by an external low-impedance voltage source connected to VOC.

The sensor has an internal factory-calibrated current source at VOC. Connecting a resistor between VOC and GND sets the voltage at VOC. I_{OCR} is set as a percentage of the full-scale sensing range of the device, $I_{PR(MAX)}$, and can be between 50% $I_{PR(Max.)}$ and 200% $I_{PR(MAX)}$.

If VOC is connected to GND or if the voltage on VOC is less than 0.1 V, the overcurrent FAULT threshold is 100%.

Table 1: FAULT threshold, IOCR, as set by VVOC

R_{VOC} (kΩ)	V_{VOC} (V)	I_{OCR} (%$I_{PR(MAX)}$)
0	<0.1	100
33	0.66	50
46.6	0.932	75
66.1	1.322	100
86	1.72	125
99.1	1.982	150
115.6	2.312	175
132.1	2.642	200

The voltage at VOC can also be set using an external low-impedance voltage source that overdrives the internal current supply. If the application does not require the threshold to be adjusted once the sensor is in operation, it is recommended to use a low-tolerance resistor for fixing I_{OCR}.

If the VOC pin is being driven by a non-inverted buffered V_{REF}, it is important to consider that any error from the V_{REF} pin is gained as well. For instance, if V_{REF} error is +10 mV and the gain = 4 for the non-inverting operational amplifier, then the VOC pin is 40 mV from the expected target.

OVERCURRENT FAULT OUTPUT ERROR (E_{OC})

Overcurrent FAULT error, E_{OC}, is defined as the difference between the set current threshold, and the measured current at which the FAULT activates.

OVERCURRENT FAULT HYSTERESIS (I_{OC_HYST})

Overcurrent hysteresis, or I_{OC_HYST}, is defined as the magnitude of current in percentage of the FS that must drop before a fault assertion is cleared. This can be seen as the separation between the voltages [9] to [10] in Figure 7 and Figure 8.

VOC INPUT LINEAR OPERATING RANGE (V_{OR_VOC})

VOC input linear operating range, V_{OR_VOC}, is the voltage range for V_{VOC} in which the overcurrent FAULT threshold, I_{OCR}, varies linearly with V_{VOC}.

OVERCURRENT FAULT RESPONSE TIME (t_{OC_RESP})

Overcurrent response time, or t_{OC_RESP}, is defined as the time from when the input current reaches the operating point [9] until the FAULT pin falls below V_{FAULT_L} [G].

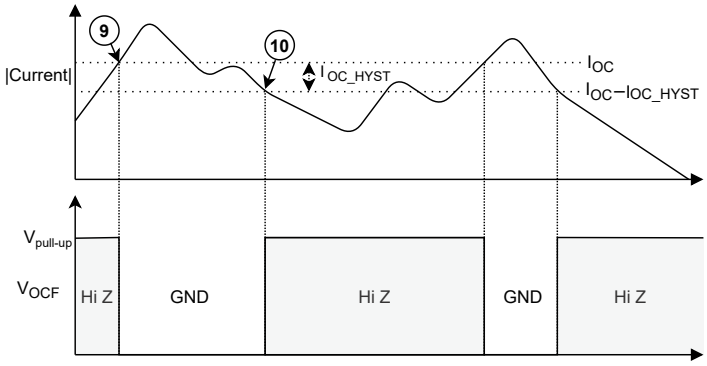

Figure 7: Fault Thresholds and Pin Functionality

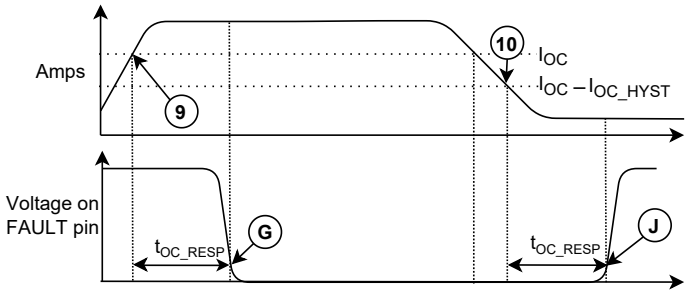

Figure 8: Fault Timing Diagram

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THERMAL PERFORMANCE

Resistive heating due to the flow of electrical current in the package should be considered during the thermal design of the application. The sensor, PCB, and PCB terminals generate heat and act as a heat sink.

The thermal response is highly dependent on the PCB layout, copper thickness, cooling method, and the profile of the injected current (including peak current, current on-time, and duty cycle).

In-pad vias help improve thermal performance. Placing vias under the copper pads of the board reduces electrical resistance and improves heat conduction to the PCB (Figure 9 and Figure 10). The ACSEVB-MA16-LA16 includes in-pad vias and is recommended to improve thermal performance.

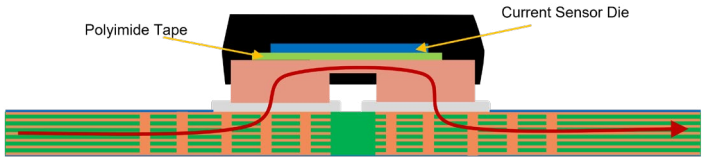

Figure 9: Vias Under Copper Pads (not to scale)

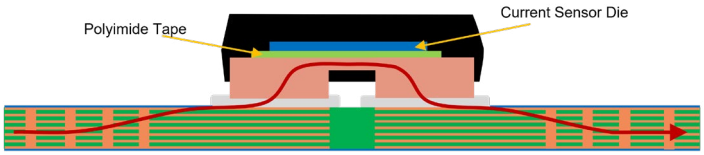

Figure 10: No Vias Under Copper Pads (not to scale)

Figure 11 shows the measured rise in steady-state die temperature of sensor versus DC continuous current at an ambient temperature T_A = 25°C for two board designs: with filled in-pad vias and without in-pad vias.

Figure 12 shows the measured rise in steady-state die temperature of sensor versus DC continuous current at ambient temperatures of 25°C and 125°C.

The thermal performance of the sensor must always be verified in the specific conditions of the application. The maximum junction temperature of the sensor, $T_{J(MAX)}$ = 165°C, must not be exceeded.

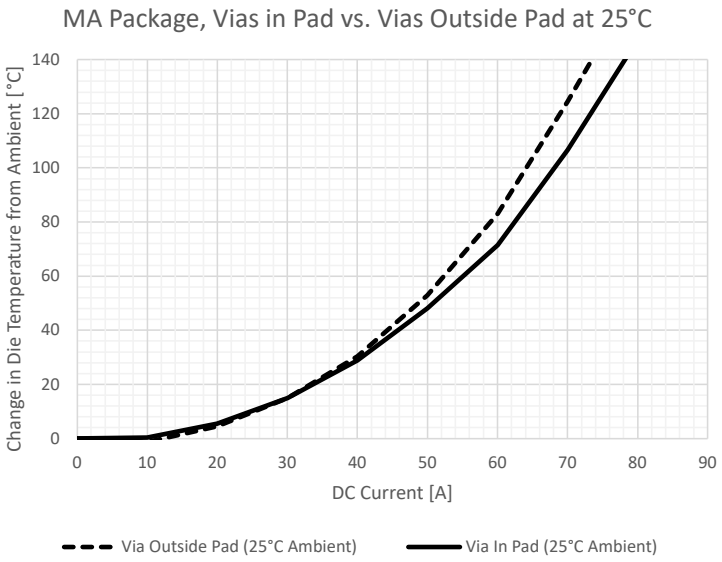

Figure 11: MA Package Performance with/without Vias

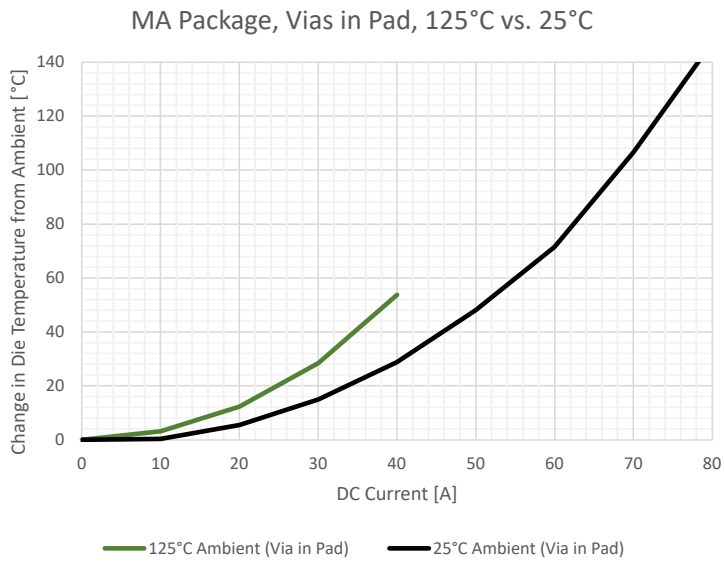

Figure 12: MA Package Performance at 25°C and 125°C

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Evaluation Board Layout

Thermal data shown was collected using the ACSEVB-MA16-LA16 Allegro evaluation board (TED-0004111). This board includes six layers of 2-ounce copper weight on all layers. The top and bottom layers of the PCB are shown in Figure 13.

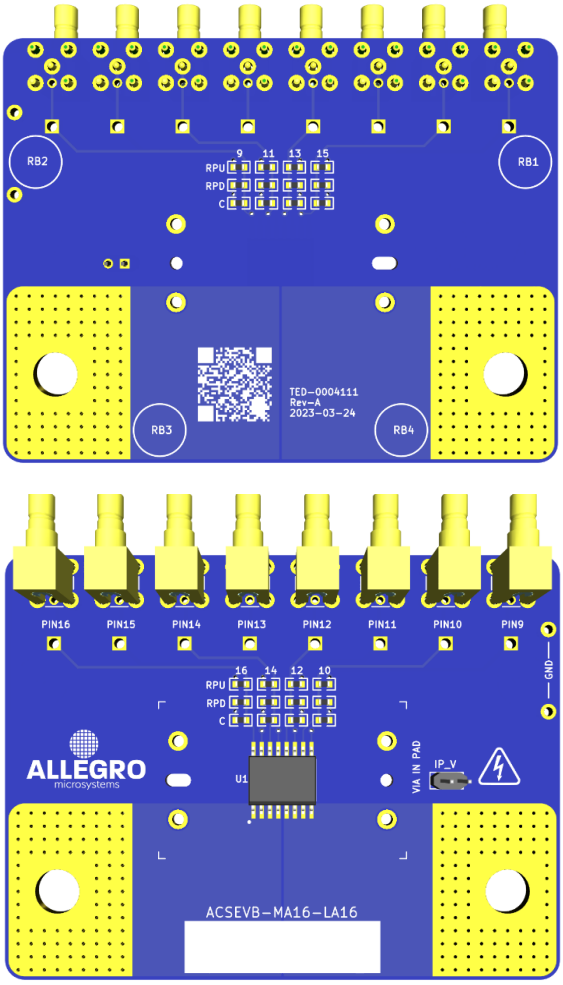

Figure 13: MA/LA Evaluation Board Top and Bottom Layers

Design support files for the ACSEVB-MA16-LA16 evaluation board are available for download from the Allegro website. See the technical documents section of the Allegro website for more information.

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PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000388, Rev. 1 and JEDEC MS-013AA)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

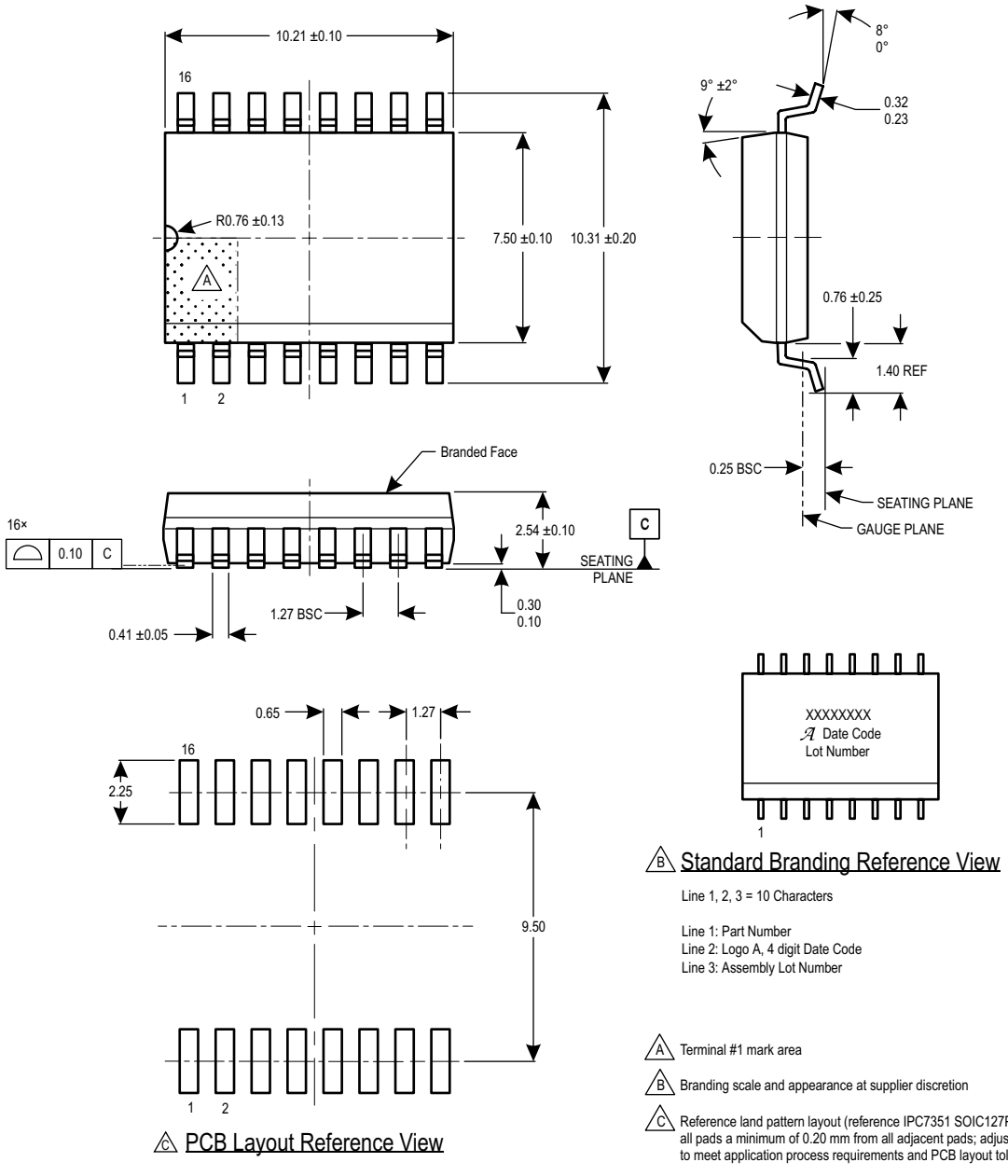

Figure 14: Package MA, 16-Pin SOICW

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Revision History

Number	Date	Description
–	August 28, 2025	Initial release
1	October 16, 2025	Updated Conductor Resistance value (page 1, page 4)
2	November 4, 2025	Updated Description (page 1), updated Input Current in Absolute Maximum Ratings table (page 3)
3	April 15, 2026	Updated Features and Benefits section and Typical Application Circuit diagram (page 1), updated selection guide and part naming specification (page 2), updated isolation characteristics table (page 3), updated Functional Block Diagram (page 5), updated Common Electrical Characteristics table (page 6), updated Performance Characteristics tables (pages 7, 8), editorial updates (pages 11, 12, 14, 16), updated Fault Timing Diagram and Voltage Overcurrent Pin application information (page 14)

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