ACS37503

Very High Precision, Programmable Linear Hall-Effect Sensor IC

High-Bandwidth (350 kHz) Analog Output for Core-Based Current Sensing

FEATURES AND BENEFITS

- Factory-programmed 4th order polynomial temperature compensation (TC) provides ultralow thermal drift
  - Sensitivity Error ±1%
  - Offset Error ±5 mV
- Very fast response time (1.7 µs)
- High operating bandwidth: DC to 350 kHz
- User programmable threshold for:
  - Overcurrent fault
  - Overtemperature fault
- AEC-Q100 Grade 0, automotive qualified
- Customer-programmable, high-resolution offset, and sensitivity trim
- Extremely low noise and high resolution achieved via proprietary Hall element and low-noise amplifier circuits

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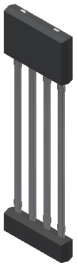
PACKAGE: 4-PIN SIP (SUFFIX KT AND OK)

TN Leadform



Contact Allegro about legacy leadform options

KT Package

Not to scale

DESCRIPTION

The Allegro ACS37503 IC incorporates a Hall element with BiCMOS integrated circuitry to provide a fully monolithic linear current sensor IC. The IC is sensitive to magnetic flux density orthogonal to the IC package surface and the output is an analog voltage proportional to the applied flux density. The ACS37503 is designed to be used in conjunction with a ferromagnetic core to provide highly accurate current sensing. The gain and offset drift over temperature is factory-programmed at Allegro and delivers a solution with 1% sensitivity error and 5 mV offset error from –40°C to 150°C

The ACS37503 is customer programmable. The absolute value of gain and offset can be programmed after manufacturing to provide customers industry-leading current sensor accuracy. The sensor has a high operating bandwidth from DC to 350 kHz and 1.7 µs fast response time. It is ideal for use in high-frequency automotive inverters and DC/DC converters where fast switching is required.

The ACS37503 offers features like undervoltage detection (UVD) as well as low-voltage programming that eliminates the need for voltages greater than VCC during user programming Broken ground wire detection, power-on reset, and under/overvoltage detection provide the required diagnostics for safety-critical automotive applications.

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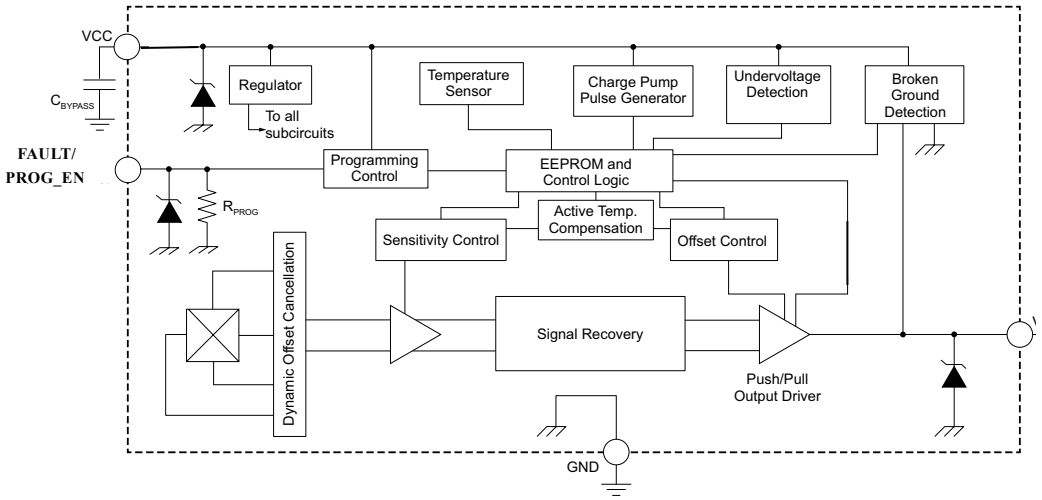

Figure 1: Functional Block Diagram

FEATURES AND BENEFITS (CONTINUED)

- Wide selectable sensitivity range between 0.5 and 11.5 mV/G
- Ratiometric output.
- Precise recoverability after temperature cycling
- Open circuit detection on ground pin (broken wire)
- Undervoltage detection (UVD)
- Low-voltage programming
- Wide ambient temperature range: –40°C to 150°C
- Immune to mechanical stress
- Extremely thin package: 1 mm case thickness, only for KT package.

DESCRIPTION (CONTINUED)

Device parameters are specified across an extended ambient automotive temperature range: –40°C to 150°C. The ACS37503 sensor IC is provided in an extremely thin case (1 mm thick), 4-pin SIP (single inline package, suffix KT) that is lead (Pb) free, with 100% matte-tin leadframe plating.

Table of Contents

Allegro MicroSystems
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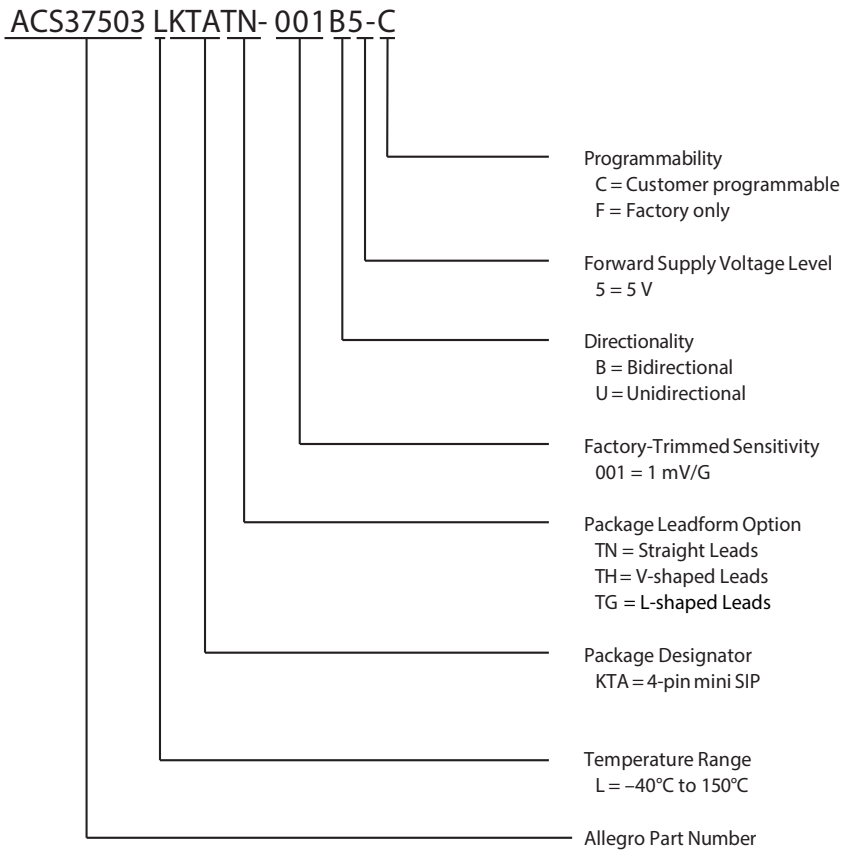
www.allegromicro.com

SELECTION GUIDE

Part Number [1]	Factory-Programmed Sensitivity (mV/G)	Programmable Sens Range (mV/G)	Low-Voltage Programming/ UVD Capable	Package	T_A (°C)	Packing
ACS37503LKTATN-001B5-C	1	0.5 – 1.10	Yes	4-pin SIP (suffix KT) TN leadform	–40 to 150	4000 pieces per 13-inch reel
ACS37503LKTATN-002B5-C	2	1.10 – 2.42				

[1] Characteristics are guaranteed within the sense programmable range of the corresponding part number.



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ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		6.5	V
Reverse Supply Voltage	V_{RCC}	$T_{J(max)}$ should not be exceeded	–0.5	V
Forward Output Voltage	V_{FOUT}	Applies to VOUT, FAULT,	V_{FOUT} ≤ (Vcc+0.7) ≤ 6.5	V
Reverse Output Voltage	V_{ROUT}	Applies to VOUT, FAULT	–0.5	V
Output Current	I_{OUT}	Maximum survivable sink or source current on the output	10	mA
Operating Ambient Temperature	T_A	L, temperature range	–40 to 150	°C
Storage Temperature	T_{stg}		–65 to 165	°C
Maximum Junction Temperature	$T_{J(max)}$		165	°C

ESD RATINGS

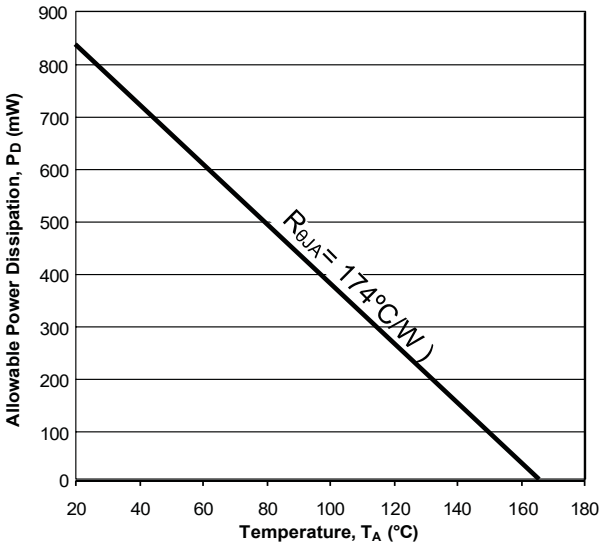
Characteristic	Symbol	Test Conditions	Value	Unit
Human Body Model	V_{HBM}	Per AEC-Q100	±5	kV
Charged Device Model	V_{CDM}	Per AEC-Q100	±1	kV

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions [1]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Package KT, on 1-layer PCB with exposed copper limited to solder pads	174	°C/W

[1] Additional thermal information available on the Allegro website

Allowable Power Dissipation versus Ambient Temperature



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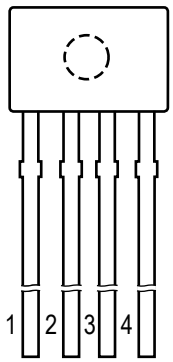
PINOUT DIAGRAM AND TERMINAL LIST TABLE



ACS37503 Terminal List Table

Number	Name	Function
1	VCC	Input Power Supply; also used for programming
2	VOUT	Output Signal, also used for programming
3	FAULT/PROG_EN	Overcurrent fault and overtemperature fault; Low-Voltage Programming Enable pin
4	GND	Ground

Figure 2: KT Package Pinout Diagram (Ejector pin mark on opposite side)

TYPICAL APPLICATION DRAWING

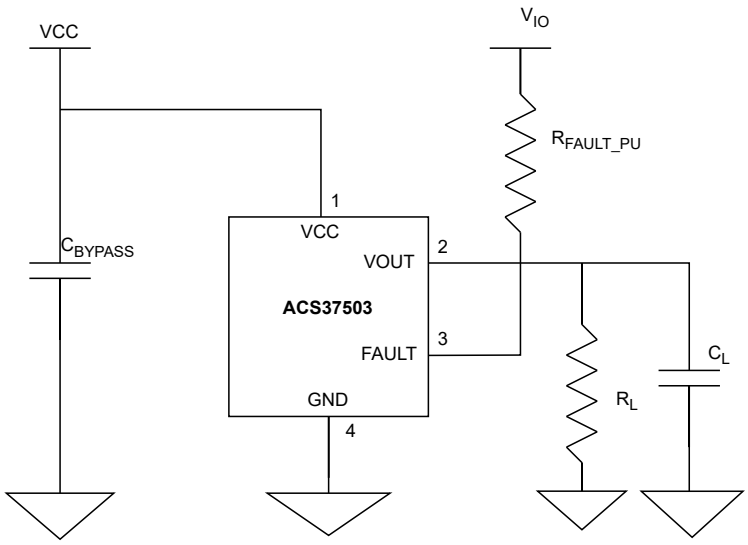


Figure 3: Typical Application Drawing

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OPERATING CHARACTERISTICS: Valid over full operating temperature range of T_A, C_{BYPASS} = 0.1 µF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
ELECTRICAL CHARACTERISTICS							
Supply Voltage	V_{CC}	5 V variant		4.5	5	5.5	V
		3.3 V variant		3.135	3.3	3.465	V
Supply Current	I_{CC}	No load on VOUT; $V_{CC(min)} \le V_{CC} \le V_{CC(max)}$	5 V variant	–	8.5	10	mA
			3.3 V variant	–	8.5	10	mA
Power-On Reset Voltage	V_{POR_H}	T_A = 25°C, V_{CC} rising,		2.6	2.75	2.9	V
	V_{POR_L}	T_A = 25°C, V_{CC} falling		2.3	2.45	2.6	V
	V_{POR_HYS}	T_A = 25°C		200	300	400	mV
Power-On Delay Time[8]	t_{PO}	T_A = 25°C, C_{BYPASS} = open, C_L = 1 nF		–	65	–	µs
Overvoltage Detection [2]	V_{OVD_H}	T_A = 25°C, VCC rising		6.1	6.25	6.4	V
	V_{OVD_L}	T_A = 25°C, VCC falling		5.7	–	6.05	V
	V_{OVD_HYS}	T_A = 25°C		0.3	–	–	V
Overvoltage Detection Enable/Disable Delay Time	t_{OVD_EN}	T_A = 25°C		60	65	70	µs
	t_{OVD_DIS}	T_A = 25°C		–	14	20	µs
Undervoltage Detection [2]	V_{UVD_H}	T_A = 25°C, V_{CC} rising		4.15	–	4.45	V
	V_{UVD_L}	T_A = 25°C, V_{CC} falling		3.9	–	4.2	V
	V_{UVD_HYS}	T_A = 25°C		200	275	350	mV
UVD Enable/Disable Delay Time [2]	t_{UVD_EN}	T_A = 25°C		60	65	70	µs
	t_{UVD_DIS}	T_A = 25°C		–	14	20	µs
Maximum Field Range	B	Maximum input field range to which the part will respond		–	±4000	–	G
OUTPUT CHARACTERISTICS							
DC Output Resistance	R_{OUT}	T_A = 25°C		0	4	8	Ω
Output Load Resistance [1]	R_L	VOUT to GND or VCC		4.7	10	–	kΩ
Output Load Capacitance	C_L	VOUT to GND		–	1	5	nF
Output Full-Scale Range	$V_{OUT\_FS\_RAT}$	Ratiometric		0.1 × V_{CC}	–	0.9 × V_{CC}	
	$V_{OUT(FSR)}$	Full-scale output for V_{CC} = 5 V, Bidirectional		–	±2	–	V
		Full-scale output for V_{CC} = 3.3 V, Bidirectional		–	±1.32	–	V
		Full-scale output for V_{CC} = 5 V, Unidirectional		–	4	–	V
Output Voltage Saturation	V_{SAT_H}	T_A = 25°C, R_L = 10 kΩ to GND		V_{CC} – 0.2	–	–	V
	V_{SAT_L}	T_A = 25°C, R_L = 10 kΩ to V_{CC}		–	–	0.25	V
Output Voltage with Broken GND	V_{BRK_L}	T_A = 25°C, R_L = 10 kΩ to GND, V_{CC} = 5 V		0	14	200	mV
		T_A = 25°C, R_L = 10 kΩ to GND, V_{CC} = 3.3 V		0	14	150	
	V_{BRK_H}	T_A = 25°C, R_L = 10 kΩ to VCC, Pin 3 = open		V_{CC} – 0.2	V_{CC} – 0.1	V_{CC}	V

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Noise	V_{IN}	TA = 25°C, CL = 1 nF, Sens = 1 mV/G	–	1.36	–	mG/√(Hz)
		TA = 25°C, CL = 1 nF, Sens = 2 mV/G	–	1.08	–	mG/√(Hz)
		TA = 25°C, CL = 1 nF, Sens = 4 mV/G	–	0.7	–	mG/√(Hz)
		TA = 25°C, CL = 1 nF, Sens = 5 mV/G	–	0.69	-	mG/√(Hz)
		TA = 25°C, CL = 1 nF, Sens = 8 mV/G	–	0.55	–	mG/√(Hz)
	V_{ON}	TA = 25°C, CL = 1 nF, BW= 350 kHz, Sens = 1 mV/G	–	1.12	–	mV_{RMS}
		TA = 25°C, CL = 1 nF, BW= 350 kHz, Sens = 5 mV/G	–	2.73	–	mV_{RMS}
		TA = 25°C, CL = 1 nF, BW= 350 kHz, Sens = 8 mV/G	–	3.48	–	mV_{RMS}
Propagation Delay Time	t_{pd}	T_A = 25°C, C_L = 1 nF, R_L= 10 kΩ, BW_LO = 0	–	1	1.4	µs
Response Time	$t_{RESPONSE}$	T_A = 25°C, C_L = 1 nF, R_L= 10 kΩ, BW_LO = 0	–	1.7	2.7	µs
Rise Time	t_r	T_A = 25°C, C_L = 1 nF, R_L= 10 kΩ, BW_LO = 0	–	1.5	2.5	µs
Bandwidth	BW	Small signal –3 dB, C_L = 1 nF, T_A = 25°C; Sens = 10 mV/G, BW_LO = 0	–	350	–	kHz
	BW_{LOW}	Small signal –3 dB, C_L = 1 nF, T_A = 25°C; Sens = 10 mV/G, BW_LO = 1	–	30	–	kHz
QUIESCENT OUTPUT VOLTAGE ($V_{OUT(Q)}$)						
Number of Fine QVO Programming Bits	QVO_FINE		–	8	–	bit
Quiescent Voltage Output [3]	$V_{OUT(QU)}$	Unidirectional, T_A = 25°C , V_{CC} = 5 V	0.495	0.5	0.505	V
		Unidirectional, T_A = 25°C , V_{CC} = 3.3 V	0.3267	0.33	0.333	V
	$V_{OUT(QBI)}$	Bidirectional, T_A = 25°C, V_{CC} = 5 V	2.495	2.5	2.505	V
		Bidirectional, T_A = 25°C, V_{CC} = 3.3 V	1.646	1.65	1.654	V
Average Quiescent Voltage Output Programming Step Size [4]	$V_{OUT(Q)Step}$	T_A = 25°C	–	1.05	–	mV
Average Quiescent Voltage Output Temperature Compensation Step Size	$V_{OUT(Q)TCStep}$		–	$V_{OUT(Q)Step}$	1.18	mV
SENSITIVITY (Sens)						
Coarse Sensitivity Programming Bits [5]	SENS_COARSE		–	2	–	bit
Fine Sensitivity Programming Bits	SENS_FINE		–	11	–	bit
Sensitivity Programming Range [6]	$Sens_{PR}$	VCC = 5 V, SENS_COARSE = 0	0.5	–	1.10	mV
		VCC = 5 V, SENS_COARSE = 1	1.10	–	2.42	mV
		VCC = 5 V, SENS_COARSE = 2	2.42	–	5.32	mV
		VCC = 5 V, SENS_COARSE = 3	5.32	–	11.5	mV
		VCC = 3.3 V, SENS_COARSE = 0	0.33	–	0.73	mV
		VCC = 3.3 V, SENS_COARSE = 1	0.73	–	1.6	mV
		VCC = 3.3 V, SENS_COARSE = 2	1.6	–	3.5	mV
		VCC = 3.3 V, SENS_COARSE = 3	3.5	–	7.7	mV

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OPERATING CHARACTERISTICS (continued): Valid over full operating temperature range of T_A, C_{BYPASS} = 0.1 µF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Average Sensitivity Programming Step Size	$Step_{SENSE}$	VCC = 5 V, SENS_COARSE = 0	–	0.71	–	µV/G
		VCC = 5 V, SENS_COARSE = 1	–	1.54	–	µV/G
		VCC = 5 V, SENS_COARSE = 2	–	3.4	–	µV/G
		VCC = 5 V, SENS_COARSE = 3	–	7.45	–	µV/G
		VCC = 3.3 V, SENS_COARSE = 0	–	0.46	–	µV/G
		VCC = 3.3 V, SENS_COARSE = 1	–	1.02	–	µV/G
		VCC = 3.3 V, SENS_COARSE = 2	–	2.24	–	µV/G
		VCC = 3.3 V, SENS_COARSE = 3	–	4.92	–	µV/G
Average Sensitivity Temperature Compensation Step Size	$Step_{SENSETC}$	T_A = –40°C to 150°C	–	$Step_{SENS}$	–	µV/G
SENSITIVITY ERROR						
Sensitivity Error	$Sens_{ERR}$	T_A = 25°C, factory-programmed sensitivity	–1	–	1	%
Sensitivity Error Over Temperature	$\Delta Sens_{TC}$	–40°C ≤ T_A ≤ 150°C, relative to 25°C	–1	–	1	%
Sensitivity Linearity Error [7]	Lin_{ERR}	4.5 V ≤ VCC ≤ 5.5 V, below ±3 kG	–0.5	–	0.5	%
		4.5 V ≤ VCC ≤ 5.5 V, ±3 kG ≤ ±4 kG	–1	–	1	%
Sensitivity Ratiometry Error	$Rat_{ERRSENS}$	V_{CC} = 4.85 to 5.15 V	–0.3	–	0.3	%
QUIESCENT VOLTAGE OUTPUT ERROR						
Quiescent Voltage Output Error	$V_{OUT(Q)ERR}$	T_A = 25°C	–5	–	5	mV
Quiescent Voltage Output Drift Over Temperature	$\Delta V_{OUT(Q)TC}$	–40°C ≤ T_A ≤ 150°C, relative to 25°C	–5	–	5	mV
Quiescent Voltage Output Ratiometry Error	$V_{RatERRVOUT(Q)}$	V_{CC} = 4.85 to 5.15 V	–3	–	3	mV
LIFETIME [9]						
Sensitivity Lifetime Drift	$Sens_{ERR\_LIFE}$	T_A = 25°C	–	0.5	–	%

[1] Using small RL will increase output error; this error scales with output causing offset and symmetry error, i.e. using a RL = 4.7 kΩ will cause a 4 mV error due to the resistor divider between the R_L(pulldown) and the internal resistance of 4 Ω at 5 V output. Keep this in mind when sizing R_L.
[2] OVD/UVD was characterized on the bench. VCC ramp rate of 0.1 V/ms and 1000 V/µs for thresholds and timing respectively.
[3] Devices programmed to the typical values are guaranteed to meet the VOUT(Q)TC spec.
[4] This is an average and actual step can vary. For best results, check QVO after every retrim. Refer to the Quiescent Voltage Output Programming Resolution in the definition section.
[5] Allegro guarantees limits of devices that remain within their factory programmed SEN_COARSE and the corresponding $SENS_{PR}$ during customer programming.
[6] Device performance is guaranteed within these ranges.
[7] Validated by characterization and design.
[8] Power-on delay time includes Power on reset release time and Power on reset output settle time.
[9] Lifetime drift numbers represent the average parameter drift seen during qualification.

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FAULT CHARACTERISTICS : Valid over full operating temperature range of T_A, C_{BYPASS} = 0.1 µF, and V_{CC} = 5 V, 3.3 V unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
External Fault Pull-up Resistor	R_{FAULT_PU}	FAULT to VCC	4.7	10	44	kΩ
External Fault Capacitor	C_{FAULT}	FAULT to GND	–	–	0.5	nF
Fault Leakage Current	I_{LEAK}	RFAULT = 10 kΩ to VCC, FAULT in HiZ	–	–	4	µA
Fault Output Voltage	V_{FAULT_ON}	RFAULT = 4.7 kΩ to VCC; FAULT pin voltage when asserted	–	–	0.5	V
Fault Pull-up Voltage	V_{IO}	RFAULT connected between FAULT and VIO	3	–	V_{CC}	V
Fault Output Voltage when deasserted	V_{FAULT_OFF}	RFAULT = 44 kΩ to VCC; 6.5 V > VCC > 5.5 V	V_{CC} – 0.3	–	V_{CC}	V
OCF Response Time	t_{OCF}	Time from |Field| rising above OCF Threshold until assert, Field step from 0 to 1.2 OCF Threshold(OCF_THR) in 0.5 µs, BW=350 kHz	–	–	1.2	µs
OCF Error over Temperature		Temperature range from –40°C to 150°C, relative to 25°C	–	5	–	%FS
Overcurrent Fault Hysteresis	OCF_{HYST}	Bidirectional mode only	10	12.5	15	%FS
		Unidirectional mode only	5	6.25	7.5	%FS
Overcurrent Fault Customer programming range	OCF_THR	Bidirectional Output	50	–	125	%FS
		Unidirectional Output	50	–	100	%FS
Overcurrent Fault programming step size			–	5	–	%FS
Total Overcurrent Fault Error over temperature with blind-blow programming code		Error vs expected threshold (computed from nominal Code to Threshold transfer function) Temperature range from –40°C to 150°C.	–10	–	10	%FS
Overtemperature Fault Accuracy	T_{OTF_ACC}		–10	±3	10	°C
Overtemperature Fault Threshold Range	T_{OTF_THR}	Programmable using OTF_THR	95	155	165	°C
Overtemperature Fault Hysteresis	T_{OTF_HYST}		10	15	20	°C

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RESPONSE CHARACTERISTICS DEFINITIONS AND PERFORMANCE DATA

Response Time ($t_{RESPONSE}$)

The time interval between a) when the applied magnetic field reaches 90% of its final value, and b) when the sensor output reaches 90% of its full-scale value.

Propagation Delay (t_{pd})

The time interval between a) when the applied magnetic field reaches 20% of its full-scale value, and b) when the sensor output reaches 20% of its full-scale value.

Rise Time (t_r)

The time interval between a) when the sensor reaches 10% of its full-scale value, and b) when it reaches 90% of its full-scale value.

Output Slew Rate (SR)

The rate of change (V/µs) in the output voltage from a) when the sensor reaches 10% of its full-scale value, and b) when it reaches 90% of its full-scale value.

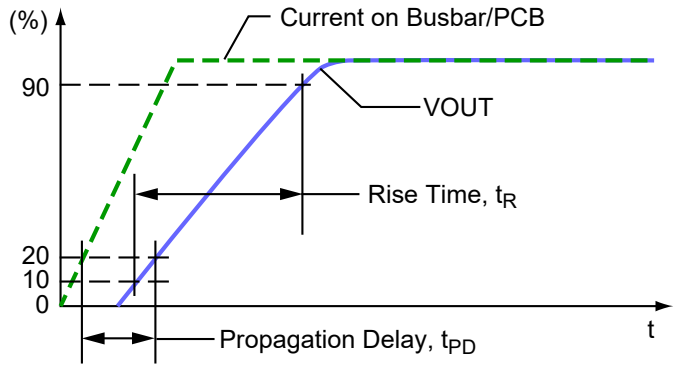

Figure 4: Propagation delay and rise time

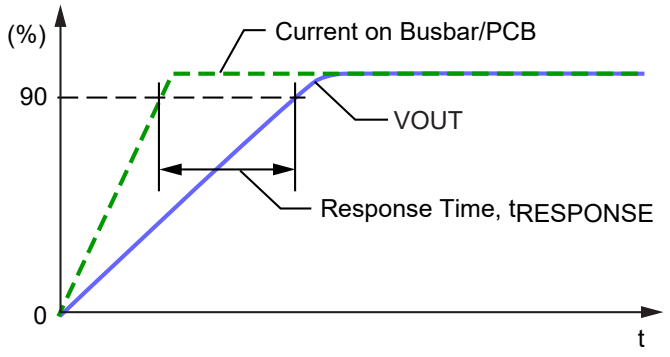

Figure 5: Response time

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Quiescent Voltage Output ($V_{OUT(Q)}$)

In the quiescent state (no significant magnetic field: B = 0 G), the output ($V_{OUT(Q)}$) has a constant ratio to the supply voltage (V_{CC}) throughout the entire operating ranges of V_{CC} and ambient temperature (T_A).

Before any programming, the Quiescent Voltage Output ($V_{OUT(Q)}$) has a nominal value of V_{CC} / 2 for a bidirectional device and 0.5 V for unidirectional parts with a V_{CC} of 5 V.

Quiescent Voltage Output Programming Range

The Quiescent Voltage Output ($V_{OUT(Q)}$) can be programmed within the Quiescent Voltage Output Programming Range limits. Exceeding the specified Quiescent Voltage Output Programming Range limits will cause Quiescent Voltage Output Drift Over Temperature ($\Delta V_{OUT(Q)TC}$) to deteriorate beyond the specified values.

Average Quiescent Voltage Output Programming Step Size ($Step_{VOUT(Q)}$)

The Average Quiescent Voltage Output Programming Step Size ($Step_{VOUT(Q)}$) is determined using the following calculation:

$$V_{OUT(Q)Step} = \frac{V_{OUT(Q)maxcode} - V_{OUT(Q)mincode}}{2^n - 1}, \quad (1)$$

where n is the number of available programming bits in the trim range, 9 bits, $V_{OUT(Q)maxcode}$ is at decimal code 255, and $V_{OUT(Q)mincode}$ is at decimal code 256.

Quiescent Voltage Output Programming Resolution

The programming resolution for any device is half of its programming step size.

The step size of each bit can vary. For best accuracy, check $V_{OUT(Q)}$ after every trim. The devices DAC performance is screened and accounted in the factory-standard trim but becomes a possible source of error if the device is reprogrammed beyond the Quiescent Voltage Output; programming beyond this range causes $\Delta V_{OUT(Q)TC}$ to be invalid.

Quiescent Voltage Output Drift Over Temperature ($\Delta V_{OUT(Q)TC}$)

The Quiescent Voltage Output ($V_{OUT(Q)}$) may drift from its nominal value through the operating ambient temperature (T_A). The Quiescent Voltage Output Drift Over Temperature ($\Delta_{VOUT(Q)TC}$) is defined as:

$$\Delta V_{OUT(Q)TC} = V_{OUT(Q)(TA)} - V_{OUT(Q)(25°C)} \quad (2)$$

$\Delta V_{OUT(Q)TC}$ should be calculated using the measured value of $V_{OUT(Q)}$ at the current temperature and at 25°C.

Sensitivity (Sens) and Sensitivity Error ($Sens_{ERR}$)

The presence of a south polarity magnetic field, perpendicular to the branded surface of the package face, increases the output voltage from its quiescent value toward the supply voltage rail. The amount of the output voltage increase is proportional to the magnitude of the magnetic field applied.

Conversely, the application of a north polarity field decreases the output voltage from its quiescent value. This proportionality is specified as the magnetic sensitivity, Sens (mV/G), of the device, and it is defined as:

$$Sens = \frac{V_{OUT(BPOS)} - V_{OUT(BNEG)}}{BPOS - BNEG}, \quad (3)$$

where BPOS and BNEG are two magnetic fields with opposite polarities.

Sensitivity error is the error in percent between the factory-programmed sensitivity and the measured sensitivity value.

Factory-Programmed Sensitivity

Before any programming, Sensitivity has a nominal value that depends on the SENS_COARSE bits setting. Each variant has a different SENS_COARSE setting. The TC performance is guaranteed if the SENS_COARSE bit is in its default factory value and within the Sensitivity Programming Range corresponding to the SENS_COARSE bit.

Sensitivity Programming Range ($Sens_{PR}$)

The magnetic sensitivity (Sens) can be programmed around its initial value within the sensitivity range limits: $Sens_{PR}$(min) and $Sens_{PR}$(max). Exceeding the specified Sensitivity Range will cause Sensitivity Drift Over Temperature ($\Delta Sens_{TC}$) to deteriorate beyond the specified values.

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Average Fine Sensitivity Programming Step-Size (StepSENS)

This is a change in the fine sensitivity parameter per code of sensf DAC. This value changes depending on SENS_COARSE. The over temperature performance of the device is guaranteed only for the factory programmed SENS_COARSE and its associated $Sens_{PR}$.

Sensitivity Programming Resolution

This resolution is equal to or less than 1/2 × $Step_{SENS}$. If the device is more than 1/2 × $Step_{SENS}$ but less than one $Step_{SENS}$ away from a desired trim, then an additional step in the correct direction will yield a resolution less than 1/2 × $Step_{SENS}$.

Sensitivity Drift Over Temperature ($\Delta Sens_{TC}$)

Sensitivity (sens) may drift from its expected value (Sens_EXPECTED) over the operating ambient temperature range (T_A). The Sensitivity Drift Over Temperature ($\Delta Sens_{TC}$) is defined as:

$$\Delta Sens_{TC} = \frac{Sens_{(TA)} - Sens_{(25°C)}}{Sens_{(25°C)}} \times 100\% \quad . \qquad (4)$$

Output Voltage Operating Range

The functional output voltage for optimal performance of the device is 0.5 V to 4.5 V output voltage where V_{CC} = 5 V. The device can respond to magnetic fields that cause the output to go beyond these voltages, but parameters may not meet datasheet limits.

NONLINEARITY (Lin_{ERR})

Nonlinearity is a measure of how linear the output of the sensor IC is over the full current measurement range. The nonlinearity E_{LIN} is calculated as:

$$E_{LIN} = \frac{\Delta V_{OUT}(B) - B \cdot Sens_{Fit}}{\Delta V_{OUT}(FS)} \qquad (5)$$

where SensFit is the best-fit sensitivity when the magnetic field intensity is swept from -FS to +FS, and ΔVOUT(B) is the change in output voltage relative to QVO with an applied field:

$$\Delta V_{OUT}(B) = V_{OUT(B)} - V_{OUT(Q)} \qquad (6)$$

Note FS is the field required to generate a full-scale output, at B = –FS, VOUT = 0.1×VCC, while at B = +FS, VOUT = 0.9×VCC. The specified ELIN is the worst-case linearity error over the entire field range.

Ratiometry Error (Rat_{ERR})

The ACS37503 device features a ratiometric output. This means that the Quiescent Voltage Output ($V_{OUT(Q)}$), Sensitivity (Sens) are proportional to the Supply Voltage (V_{CC}).When the supply voltage increases or decreases by a certain percentage, each characteristic also increases or decreases by the same percentage. Ratiometry Error is the difference between the measured change in the supply voltage relative to 5 V, and the measured change in each characteristic.

The Quiescent Voltage Output Ratiometry Error, $V_{RatERRVOUT(Q)}$ (mV), for a given supply voltage (V_{CC}) is defined as:

$$V_{RATERRVOUT(Q)} = \left[\left(V_{OUT(5V)} \times \frac{Vcc}{5V}\right) - V_{OUT(VCC)}\right] \qquad (7)$$

The Sensitivity Ratiometry Error, $Rat_{ERRSens}$ (%), for a given Supply Voltage (V_{CC}) is defined as:

$$Rat_{ERRSens} = \left(1 - \frac{Sens_{(VCC)} / Sens_{(5V)}}{V_{CC} / 5\ V}\right) \times 100\% \quad . \qquad (8)$$

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VOUT

When in mission mode, VOUT voltage is equal to
VOUT = Sens × B + QVO.

QVO is the output voltage in the absence of input magnetic field, in volts. Sens is the sensitivity of VOUT to the input magnetic field, in volts/gauss. B is the input magnetic field orthogonal to the marked face of the package, in gauss.

The sensor supports a wide range of sensitivities, from 0.5 mV/G to above 11.5 mV/G. This wide range of sensitivities is divided into 4 sub-ranges called coarse ranges. The coarse sensitivity range is set with SENS_COARSE register. Each device is production trimmed for a given coarse range and VCC mode (3.3 V/5 V) should not be changed by the customer, device performances are not guaranteed when changing those settings. Within each coarse range, the sensitivity can be trimmed accurately using the SENS_FINE register. Device performances are guaranteed when changing SENS_FINE over the range of sensitivities specified for the given part number. Refer to the selection guide for available options.

Settings impacting the QVO value are:

- Unidirectional/bidirectional mode: In unidirectional mode, the sensor can sense only unidirectional Field and QVO is set to the minimum value of the Output Full scale range. This setting depends on UNI_EN register.
- 3.3 V/5 V mode: QVO adapts to the changes in Output Full scale range occurring when changing VCC mode setting. This setting depends on VCC3V3_EN register.

The sensor bandwidth can be changed with the BW_LO register. Reducing the bandwidth of the sensor decreases the total integrated noise seen on VOUT. Performances of the sensor are guaranteed even when changing this setting versus the production trim. It is possible to select between the following bandwidth settings:

- 350 kHz / 30 kHz

Output Saturation Voltage (V_{SAT})

The output voltage can swing to a maximum of V_{SAT_H} and to a minimum of V_{SAT_L}.

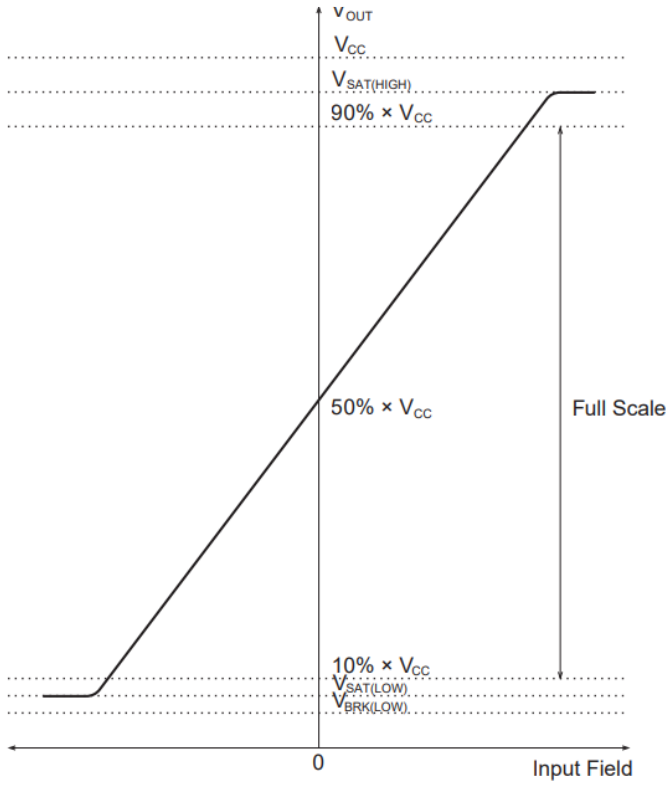

Figure 6: VOUT Characteristics of ratiometric device

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FAULT

FAULT pin driver has an open-drain output. The user shall connect externally a pull-up resistor between the FAULT pin and the V_{IO} voltage desired for communication. The driver supports V_{IO} voltages from 3 V to VCC.

FAULT status	V(FAULT)
Asserted fault	0 V
Non-asserted fault	VIO (10 kΩ external pull-up resistor)

Overcurrent Fault

This device has an overcurrent fault (OCF) comparator which trips when the current value goes above the EEPROM programmed threshold. The fault comparator operates on a signal farther in the signal path, resulting in a response time similar to the device bandwidth with high accuracy. Overcurrent fault events are reported by asserting the FAULT pin to 0. At startup, the OCF function is enabled after POT. The OCF Function is active only when the circuit is in mission mode.

OCF threshold can be programmed in EEPROM using following formula:

$$Code = \frac{OCFthreshold(\%FS) - 50}{1.25}$$

A code 0 corresponds to a 50% FS threshold and a code 15 to a

125% FS. Functionality for values above 15 is not guaranteed.

The OCF hysteresis can be set to either 6.25% FS or 12.5% FS in EEPROM. Positive and Negative OCF thresholds are symmetrically set using the same EEPROM register, OCF_THR.

OCF Mask time is configurable and is defined as the minimum duration for which an OCF event must be present before the OCF is asserted. The mask is also used when de-asserting OCF. This prevents short transient spikes from causing erroneous OCF flagging.

Possible OCF Mask settings are OFF or 5 µs.

OCF hold time is the minimum duration for which OCF is asserted, this value is configurable in EEPROM. The OCF Hold timer is started when the Fault pin is asserted due to an OCF event. This timer is not reset as long as the FAULT pin is asserted low. For example, if two consecutive OCF events of 100 µs duration separated by 500 µs occur and the hold time is set to be 1 ms, then the FAULT pin will be asserted for 1 ms (there will be no hold timer reset by the second OCF event).

Possible OCF Hold settings are OFF, 1 ms.

Overtemperature Fault

This device features a programmable overtemperature fault (OTF) detector. When the circuit internal temperature rises above the threshold defined in EEPROM, the FAULT pin is asserted. Once the temperature fall at least 10°C below the set threshold, the FAULT pin is de-asserted. It is possible to disable the OTF detection in EEPROM. When OTF Latch is configured, the device needs to be power-cycled to release the fault condition following an overtemperature event. This functionality is disabled by default.

Broken Wire Detection

If the GND pin is disconnected, node A becomes open, the VOUT pin and FAULT pin will go to a high-impedance state. The output voltage will go to V_{BRK_L} since a load resistor R_L is connected to GND and the user can detect the circuit is experiencing a failure. If the VCC pin is disconnected, node B becomes open, the VOUT pin and FAULT pin will go to a high-impedance state. The output voltage will go to V_{BRK_L} since a load resistor R_L is connected to GND and the user can detect the circuit is experiencing a failure.

Following such an event, the device will not respond to any applied magnetic field. FAULT pin is pulled to V_{CC} (or V_{IO} according to application) using load resistor R_{PU}.

If the disconnected wire is reconnected, the device will resume operation of performing a power-up sequence.

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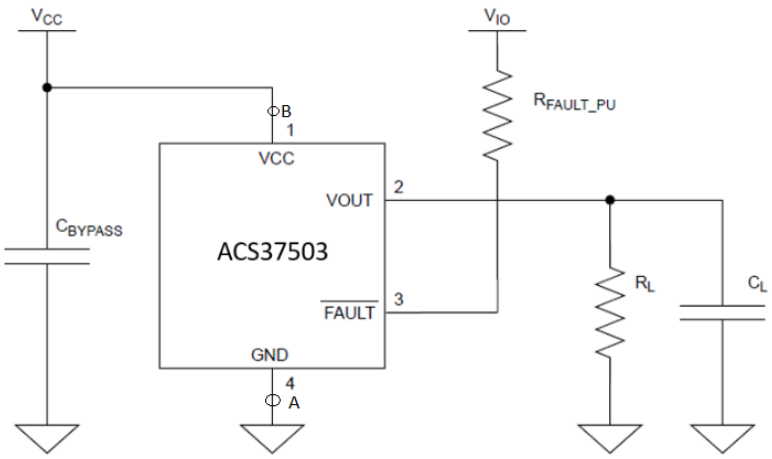

Figure 7: Connection for detecting broken wire

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Power-On Reset Voltage (V_{POR})

On power-up, to initialize to a known state and avoid current spikes, the ACS37503 is held in a reset state. The reset signal is disabled when VCC reaches V_{PORH} and time t_{PORR} has elapsed, allowing the output voltage to go from a high-impedance state into normal operation. During power-down, the reset signal is enabled when VCC reaches V_{PORL}, causing the output voltage to go into a high-impedance state. (Note that a detailed description of POR can be found in the Functional Description section).

Power-On Reset Release Time (t_{POR_R})

When V_{CC} rises to V_{POR_H}, the Power-On Reset counter starts. The ACS37503 output voltage will transition from a high-impedance state to normal operation only when the Power-On Reset Counter has reached t_{PORR} and V_{CC} has been maintained above V_{POR_H}.

Broken Wire Voltage (V_{BRK})

If the GND pin is disconnected (ACS37503 wire event), the output voltage will go to V_{BRK_H} (if a load resistor is connected to VCC) or to V_{BRK_L} (if a load resistor is connected to GND).

Note: No applied magnetic field should generate output deviation larger than Output Full Scale Range for valid Broken Ground detection.

Power-On Time (t_{PO})

When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field.

Power-On Time (t_{PO}) is defined as the time it takes for the output voltage to settle within ±10% of its steady-state value under an applied magnetic field, after the power supply has reached its minimum specified operating voltage ($V_{CC(min)}$) as shown in Figure 9.

Temperature Compensation Power-On Time (t_{TC})

After Power-On Time (t_{PO}) elapses, t_{TC} is required before a valid temperature compensated output.

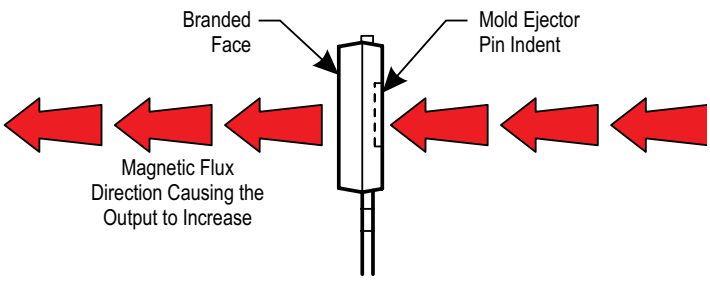

Figure 8: Magnetic Flux Polarity

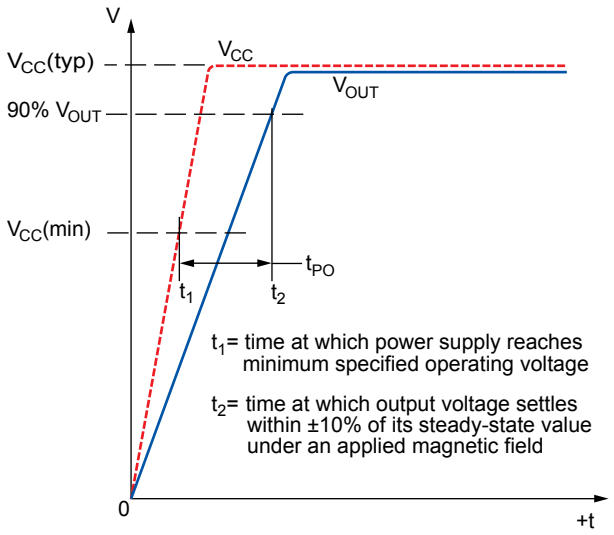

Figure 9: Power-On Time Definition

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FUNCTIONAL DESCRIPTION

Power-Up

The descriptions in this section assume TA = 25°C, no capacitive load at output, resistive load at output (pull-down) and no significant magnetic field is present.

At power-up, as VCC ramps up, the VOUT pin is tight to GND and FAULT pin is in a high impedance state. When VCC reaches and passes $V_{UVD(H)}$ [B] (or $V_{POR(H)}$ [A] if UVD is disabled), the device takes a time, t_{PO} to load the EEPROM parameters and settle down, initial temperature compensation and release outputs.

VOUT pin will become active when t_{PO} time expires [C] after VCC has reached $V_{UVD(H)}$ [B].

FAULT pin will become active when $t_{POR-OCF}$ time expires after VCC has reached $V_{UVD(H)}$.

If VCC does not exceed $V_{UVD(H)}$ [B], the VOUT pin is kept tight to GND and FAULT pin is kept in high impedance state.

Undervoltage Detection (UVD)

If VCC drops below $V_{UVD(L)}$ [H], VOUT will go to GND and FAULT pin to high impedance state after $t_{UVD(E)}$ [I]. The VOUT pin will stay at GND and FAULT pin at high impedance until VCC raises above $V_{UVD(H)}$ [J] or VCC falls below $V_{POR(L)}$ [L]. If VCC rises above $V_{UVD(H)}$ [J], outputs will resume operation. If VCC drops below $V_{POR(L)}$ [L], VOUT pin will stay at GND and FAULT pin at high impedance state.

While UVD is enabled [I], if VCC exceeds $V_{UVD(H)}$ [J] , UVD will be disabled after $t_{UVD(D)}$, and the outputs will resume normal operation [K].

Overvoltage Detection (OVD)

If VCC goes up above $V_{OVD(H)}$ [D], outputs will go to high impedance state after $t_{OVD(E)}$ [E].

While OVD is enabled [E], if VCC drops below $V_{OVD(L)}$ [F], OVD will be disabled after $t_{OVD(D)}$, and the outputs will return to normal operation [G].
When programming the ACS37503, Overvoltage Detection must be active for communication. The ACS37503 output will resume normal operation after VCC is below the Overvoltage Detection disable voltage, VOVD_L. Note that Supply Voltage limits still apply for all operating characteristics.

Power-Down

As VCC drops below $V_{UVD(L)}$ [H], VOUT will go to GND and FAULT pin to high impedance state after $t_{UVD(E)}$ [I]. As VCC drops below $V_{POR(L)}$ [L] outputs will remain in the state (VOUT at GND and FAULT in high impedance state).

The descriptions in this section assume: Temperature = 25°C, no output load (R_L, C_L), and no magnetic field is present.

Power-On Reset (POR)

When the device is off, the output will be in a high-impedance state.

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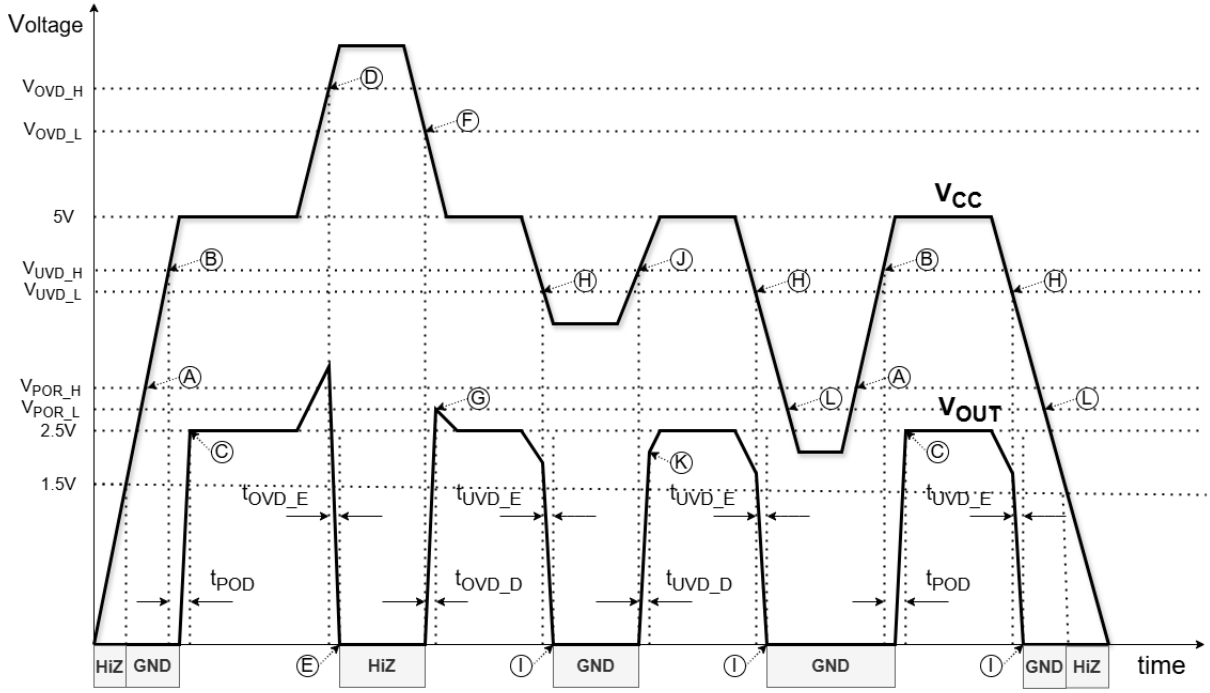

Figure 10: POR, UVD and OVD Operation – VOUT behavior of 5 V ratiometric device

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Output Pins Test Sequence

There is a possibility to trigger a test sequence on VOUT and FAULT pins. This feature is aimed at helping the user to verify the connectivity of the device in the system. During the sequence, Vout and Fault outputs are going through all their different states. There is a complete programmability of the sequence length, sequence trigger and pin checking.

Both VOUT and Fault test sequences can be run independently always at startup, only upon reception of a test sequence trigger pattern, both at startup and on reception of a test sequence trigger pattern or never (disabled).

External trigger of test sequence is possible when FAULT pin is externally pulled-down for 1ms ±10% preceding no fault assert at least for atleast 1 ms (trigger pattern). Notice that the FAULT pin should not be internally asserted during the whole duration of the unlock sequence (no OCF or OTF event), otherwise the pattern is considered as non-valid.

VOUT pin test sequence consists of 8 segments of same programmable length:

- 1QVO
- VOUT(SATL)
- QVO
- HiZ
- QVO
- Internal pull-down
- QVO
- V OUT(SATH)

FAULT pin test sequence consists of 4 segments of same programmable length:

- Fault not asserted
- OCF positive event (FAULT asserted)
- Fault not asserted
- OCF negative event (FAULT asserted)

Sequence timing is unchanged when fault_pd_dis is set. The value of FAULT is however affected by this setting. When fault_pd_dis=1, the voltage on FAULT pin will be the same for step 9 and 11 as it is for step 10.

VOUT and FAULT test sequences are run sequentially. Sequence segment length can be set to 0.1, 0.5, 1 or 2 ms.

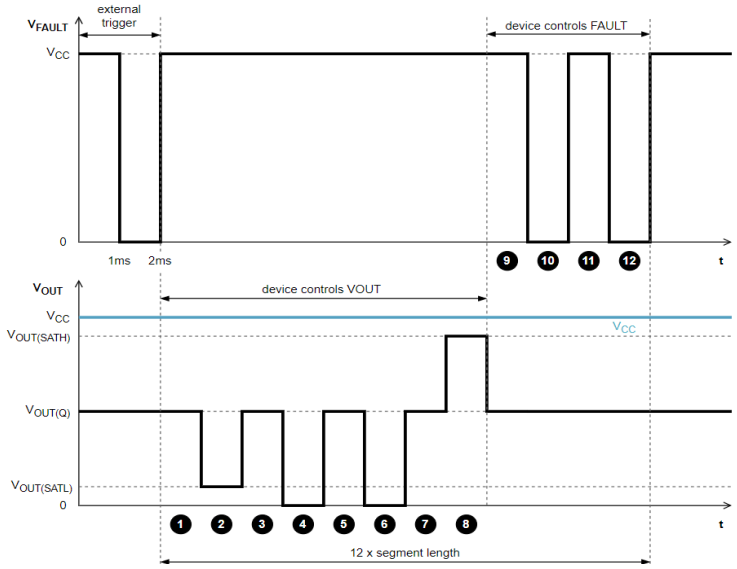

Figure 11: Output test sequence

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PROGRAMMING GUIDELINES

Device Programming

Device programming can be achieved with bidirectional communication on VOUT. Manchester encoding is used. The device has an internal charge pump to generate the EEPROM pulses.

The serial interface allows an external controller to read and write registers, including EEPROM, in the device using a point-topoint command/acknowledge protocol. The device does not initiate communication; it only responds to commands from the external controller. Each transaction consists of a command from the controller. If the command is a write, there is no acknowledging from the device. If the command is a read, the device responds by transmitting the requested data.

The controller must open serial communication with the ACS37503 by performing a memory unlock sequence. This sequence requires the writing of an access code 0x2C413736 to address 0x27. If UNLOCK_CODE bit is set the user unlock code 0xAFCF6C27 have to be applied first (by writing to address 0x27). This must be completed within 45 ms or the device will be disabled for read and write access. After three failed attempts to unlock the memory, the device is locked until next power-cycle.

When register ANALOG_LOCK_CFG > 0 (analog lock is enabled), the part is in analog mode; even if the memory has been unlocked, it is necessary to generate an analog lock override event in order to communicate with the device. The aim of this feature is to prevent unwanted programming when in analog mode.

The ACS37503 defaults with ANALOG_LOCK_CFG = 0 and UNLOCK_CODE = 0 to provide ease of programming at end-ofline calibration. Once calibration is complete, it is strongly recommended that ANALOG_LOCK_CFG and UNLOCK_CODE be set to lock the memory and ensure against accidental programming in the field.

Legacy Memory Unlock Method

VCC voltage is raised (OVD event) followed by transmission of the unlock code (optional) and the access code on VOUT before 45 ms elapses after power-up.

If timeout expires or incorrect access code is sent, VOUT remains in the normal analog mode and the device remains locked for communication on VOUT until a power reset occurs.

This method requires OVD functionality to be enabled in

EEPROM (OVD_DIS = 0x0, factory setting) and is applicable when register ANALOG_LOCK_CFG = 0x1 (or 0x2 or 0x3). Note that for 3.3 V V_{CC} mode it is recommended to have 1 ms time between OVD and sending the unlock code.

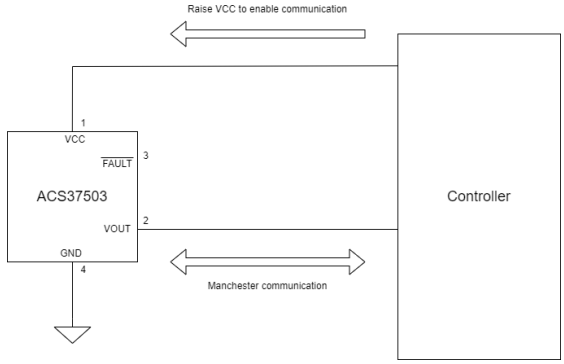

Figure 12: Programming Connection Using OVD

Low Voltage Unlock Pattern

The low voltage unlock pattern consists of externally pulling down the FAULT pin to ground for 2 ms ±10%. A no fault assert condition of at least 2 ms should precede the external pull-down.

This allow overriding the analog lock without OVD event generation. Notice that the FAULT pin has not to be internally asserted during the whole duration of the unlock sequence (no OCF or OTF event), otherwise the pattern is considered as nonvalid.

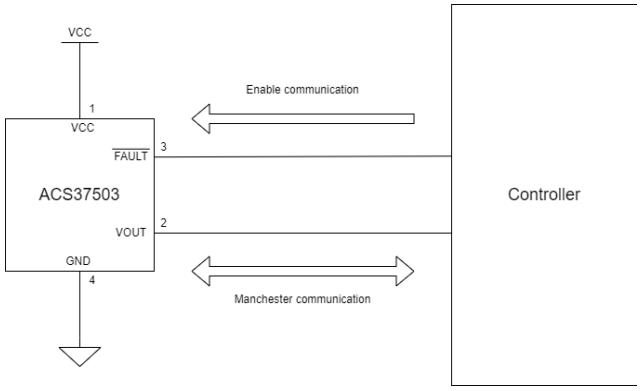

Figure 13: Low Voltage Programming Connection

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Low Voltage Startup Unlock Method

This method requires to apply the low voltage unlock pattern on FAULT pin before 45 ms elapses after startup.

When 45 ms timeout expires, VOUT resumes normal analog mode and the device remains locked for communication on VOUT until a power reset occurs.

When this unlock method is authorized in EEPROM (ANALOG_LOCK_CFG = 0x2), if the part is successfully unlocked, then applying the low voltage pattern will generate an analog_lock override event and put VOUT to high impedance for 45 ms. Otherwise, if the part is still locked after the initial timeout expires, the part will not generate an analog lock override event when a low-voltage pattern is applied on FAULT pin (and VOUT will not go to high-impedance).

Timeout 1 (TO1) Timer

The Timeout timer TO1 stops counting when a communication occurs so that it is possible to unlock the part even with the slowest possible Manchester communication speed. We consider that a communication is occurring after 2 synchorinzation bits are received. This applies to:

- TO1 expiration at startup with legacy memory unlock method
- TO1 expiration at startup with low-voltage startup unlock
- TO1 expiration after reception of low-voltage unlock pattern when low-voltage runtime unlock method is used
- TO1 duration after reception of low-voltage unlock pattern when analog_lock_cfg = 0

For the Low-voltage runtime unlock method and Low-voltage startup unlock where TO1 is used to place Vout in high impedance, the timer automatically expires if the user unset the communication dedicated mode (manch_comm_e=0). This allow to resume analog operation in a faster and more predictable way than waiting that the timer counts to TO1.

Timeout 2 (TO2) Timer

If Unlock code is required then Customer access code must be sent before Timeout 2 expires.

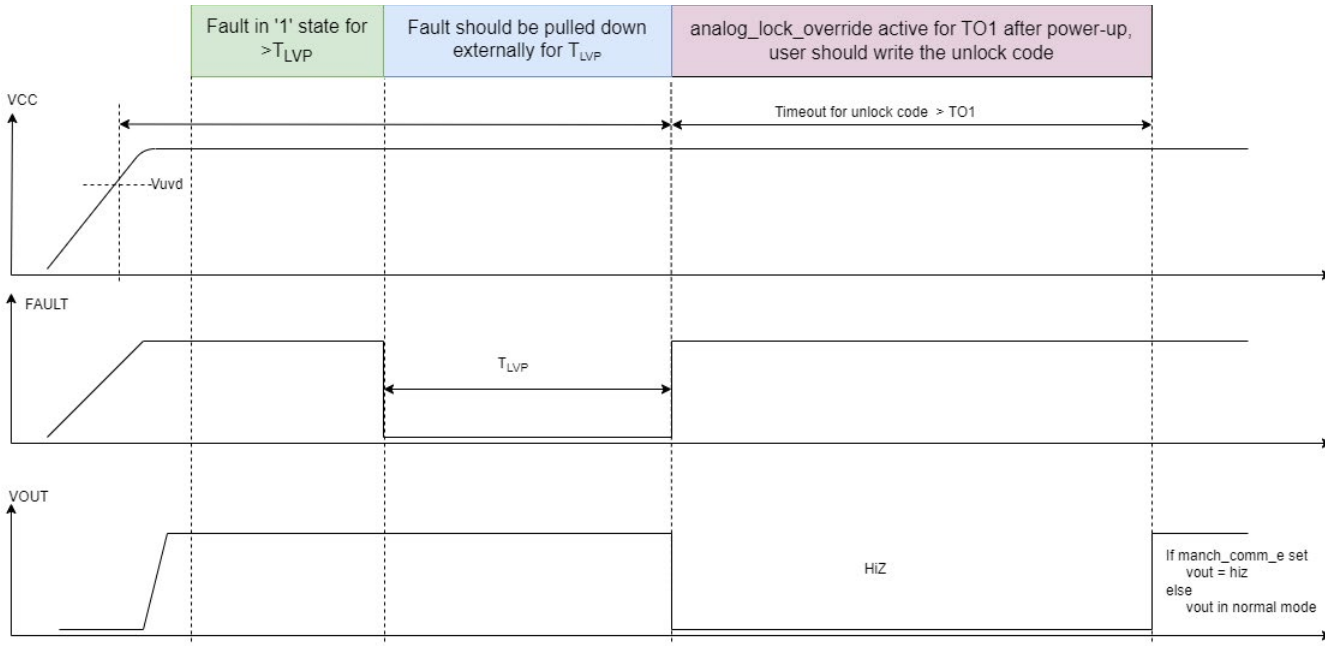

Figure 14: Low Voltage Startup Unlock Timing Diagram

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Low Voltage Runtime Unlock Method

This method requires to apply the low voltage unlock pattern on FAULT pin anytime during operation.When 45 ms time-out expires before a valid unlock sequence is received, VOUT resumes normal analog mode.

When this unlock method is authorized in EEPROM (ANALOG_LOCK_CFG = 0x3), applying the low voltage pattern will generate an analog lock override event and put VOUT to high impedance for 45 ms (even if the part is already unlocked), except if the maximum number of unlock attempts is reached.

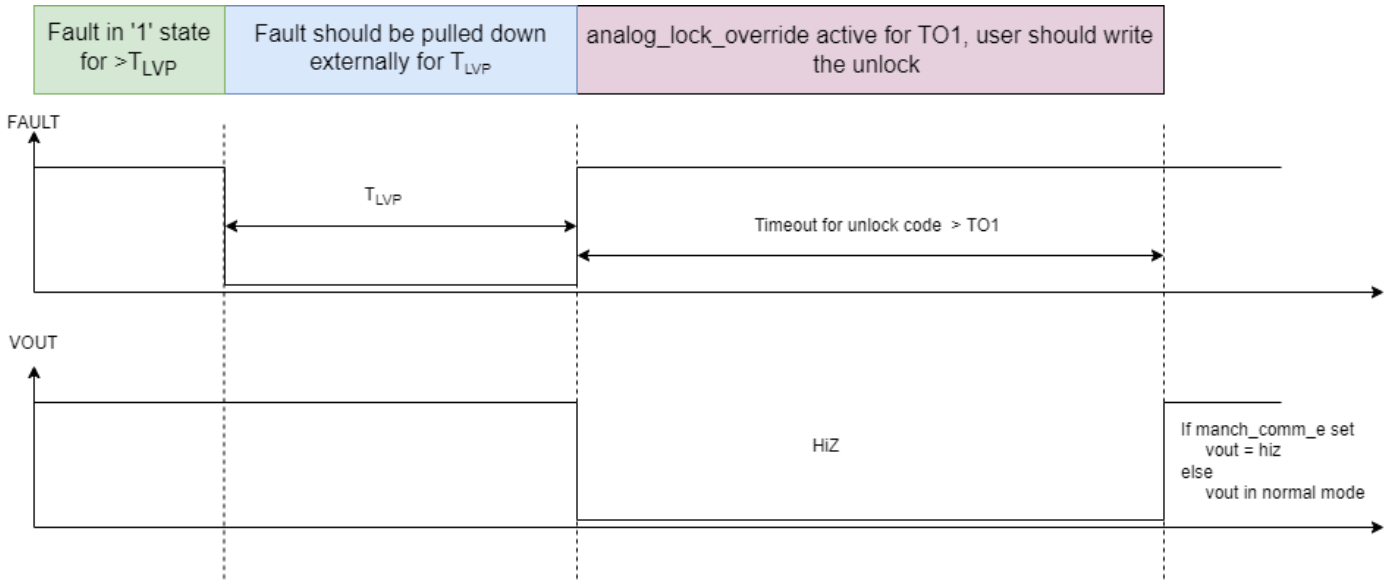

Figure 15: Low Voltage Runtime Unlock Timing Diagram

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Manchester Protocol

The serial interface uses a Manchester-encoding-based protocol (0 = rising edge, 1 = falling edge), with address and data transmitted MSB first. Four commands are recognized by the ACS37503: Write Access Code, Write to Volatile Memory, Write to Non-Volatile Memory (EEPROM) and Read. One frame type, Read Acknowledge, is sent by the ACS37503 in response to a Read command.

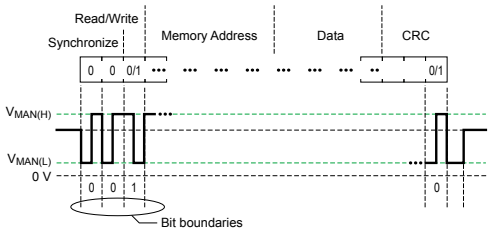

Figure 16: General Format For Serial Interface Commands

Read (Controller to ACS37503)

The fields for the Read command are:

- Sync (2 zero bits)
- Read/Write (1 bit, must be 1 for read)
- CRC (3 bits)

Figure 17 shows the sequence for a Read command.

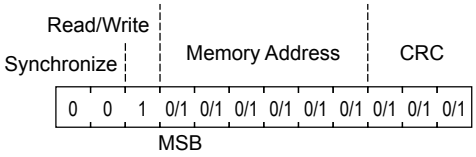

Figure 17: Read Sequence

Read Acknowledge (ACS37503 to Controller)

The fields for the data return frame are:

- Sync (2 zero bits)
- Data (32 bits):
  - □ [31:28] Irrelevant
  - □ [27:26] ECC Pass/Fail
  - □ [25:0] Data

Figure 18 shows the sequence for a Read Acknowledge. Refer to the Detecting ECC Error section for instructions on how to detect Read/Write Synchronize Memory Address Data (32 bits) and ECC failure.

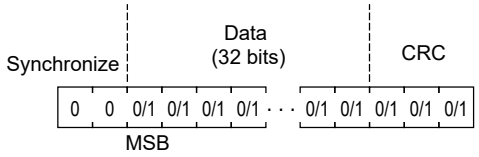

Figure 18: Read Acknowledgement Sequence

Write (Controller to ACS37503)

The fields for the Write command are:

- Sync (2 zero bits)
- Read/Write (1 bit, must be 0 for write)
- Address (6 bits)
- Data (32 bits):
- [31:26] Irrelevant
- [25:0] Data
- CRC (3 bits)

Figure 19 shows the sequence for a Write command. Bits [31:26] are Don't Care because the ACS37503 automatically generates 6 ECC bits based on the content of bits [25:0]. These ECC bits will be stored in EEPROM at locations [31:26].

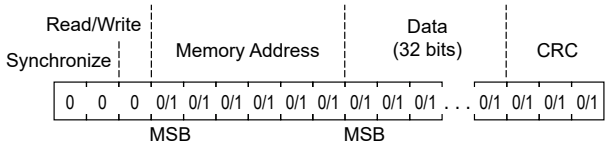

Figure 19: Write Sequence

Write Access Code (Controller to ACS37503)

The fields for the Access Code command are:

- Sync (2 zero bits)
- Read/Write (1 bit, must be 0 for write)
- Address (6 bits, address 0x27 for Customer Access)
- Data (32 bits, 0x2C413736 for Customer Access)
- CRC (3 bits)

Figure 20 shows the sequence for an Access Code command.

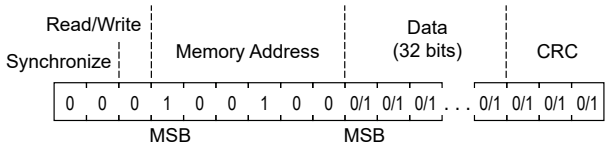

Figure 20: Write Access Code

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Access Codes Information

Name	Serial Interface Format	
	Register Address (Hex)	Data (Hex)
Unlock code	0x27	0xAFCF 6C27
Access code	0x27	0x2C41 3736

Programming Parameters

Characteristics	Symbol	Note	Min.	Typ.	Max.	Unit
Forward Program Enable Voltage	V_{PROG}	$V_{PROG} < V_{CC} + 2$ V	–	–	6.5	V
Program Enable Voltage High	V_{PROG_H}	Program enable signal high level on VCC	6.1	6.25	6.4	V
Program Enable Voltage Low	V_{PROG_L}	Program enable signal low level on VCC	5.7	5.9	6.04	V
Reverse Program Enable Voltage	V_{RPROG}		–	–	–0.5	V
Low-voltage unlock sequence: Fault input logic high		70% of VIO=3 V	2.0	–	–	V
Low-voltage unlock sequence: Fault input logic low		30% of VIO=3 V	–	–	0.8	V
Manchester High Voltage	V_{MAN_H}	Data pulse on VOUT	0.7 × VCC	–	VCC	V
Manchester Low Voltage	V_{MAN_L}	Data pulse on VOUT	0	–	0.3 × VCC	V
Program Write Delay	t_w	Delay between EEPROM writes	–	25	35	ms
Timeout 1	TO1		–	–	45	ms
Timeout 2	TO2			–	2	ms
Low voltage pattern trigger time	T_{LVP}		1.8	2	2.2	ms
Program time delay	t_d	Delay between consecutive read/writes during same Manchester event	–	74	–	µs
Output enable delay, legacy method	t_e	Time for Vout to go back to normal operation after VCC has crossed $V_{OVD(DIS)}$.	–	14	20	µs
Output enable delay, low voltage method		Time for Vout to go back to normal operation after communication is completed.	–	45	–	ms
Output enable delay, analog lock disable		VOUT goes back normal operations (analog mode) after Tbit/2 following the end of reading sequence.	–	16.5	–	µs
Bit rate	t_{BITR}	Communication rate	1	30	100	kbps

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Memory-Locking Mechanisms

The ACS37503 is equipped with two distinct memory-locking mechanisms:

- Default Lock: All registers of the ACS37503 are locked by default. EEPROM and volatile memory cannot be written. To disable the default lock, a specific 32-bit customer access code must be written to address 0x27 within access code timeout (either TO2 or TO1). After doing so, registers can be accessed. If VCC is power-cycled, the default lock automatically becomes re-enabled. This ensures that, during typical operation, memory content does not become altered due to unwanted glitches on VCC or the VOUT pin.
- Lock Bit: After EEPROM has been programmed by the user, the DEV_LOCK bit can be set high and VCC power-cycled to permanently disable the ability to read from or write to any register. This prevents the ability to use the previously described method to disable the default lock

NOTE: After the DEV_LOCK bit is set high and the VCC pin has been power-cycled, the DEV_LOCK bit can no longer be cleared and registers can no longer be written to.

Analog Lock Configuration

Analog Lock Configuration	Characteristic	Device Unlock	Communication Trigger
0	No comm lock	• Within TO1 at startup OR within TO1 after reception of a low-voltage pattern anytime • Access code • Unlock code if bit is set	Output placed in HiZ after reception of low-voltage pattern or OVD (if OVD_DIS = 0)
1	Legacy at startup	• Within TO1 at startup • Access code • Unlock code if bit is set	Requires OVD event
2	Low-voltage or legacy at startup	• Within TO1 at startup • Access code • Unlock code if bit is set	Requires OVD event or low-voltage unlock pattern
3	Low-voltage runtime or legacy at startup	• Within TO1 at startup when communication with OVD OR within TO1 after reception of a low-voltage pattern received anytime • Access code • Unlock code if bit is set	Requires OVD event or low-voltage unlock pattern

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MANCHESTER COMMUNICATIONS

Table 1: Customer Memory Map

Address	Parameter Name	Description	Read/ Write	Bits	Location
EEPROM: 0x00	Y_DIE_LOC	Y die location	R	8	21:14
	X_DIE_LOC	X die location	R	8	13:6
EEPROM: 0x01	FACTORY_LOT	Factory Probe Lot	R	16	21:6
	FACTORY_WAFER	Factory Wafer Number	R	6	5:0
EEPROM: 0x06 Shadow: 0x0E	ECC_6	Error correction code	R	6	31:26
	SPARE_REGS	Spare	RW	2	25:24
	BW_LO	Bandwidth limitation to 30 $kHz_{(TYP)}$ when set to 1.	RW	1	23
	UNI_EN [1]	Enables unidirectional output	RW	1	22
	UNLOCK_CODE	Bit to enable unlock code	R	1	21
	ANALOG_LOCK_CFG	Configures the lock or unlock	RW	2	20:19
	VCC_3V3_EN	Enables the 3.3 V V_{CC} mode	RW	1	18
	OVD_DIS	Disables overvoltage detection	RW	1	17
	UVD_DIS	Disables undervoltage detection	RW	1	16
	HP_POL [1]	Reverses output polarity	RW	1	15
	SENS_COARSE [1]	Coarse Sensitivity	RW	2	14:13
	OTF_THR	Overtemperature threshold, 0: 95°C, 1: 105°C, ..., 7: 165°C	RW	3	12:10
	OTF_DIS	Disables overtemperature fault	RW	1	9
	OCF_THR	Overcurrent fault threshold limits, 0: 50% FS, 1:55%....15:125%, Factory OCF_THR setting is 100%	RW	4	8:5
	OCF_HOLD	Minimum duration of Fault assertion in case OCF event: 0: 0 µs (disabled) 1: 1 ms	RW	1	4
	OCF_MASK	Minimum duration of OCF event before it is reported: 0: 0 µs (disabled) 1: 5 µs	RW	1	3
	OCF_HI	Increases Overcurrent Fault hysteresis	RW	1	2
	OCF_DIS	Disables OCF	RW	1	1
	DEV_LOCK	Bit to lock the serial interface from receiving data	RW	1	0
EEPROM: 0x07 Shadow: 0x0F	ECC_7	Error correction code	R	6	31:26
	FAULT_FRC	Pulls FAULT to ground	RW	1	25
	TEST_SEQ_LENGTH	Sets the length of the test sequence segments	RW	2	24:23
	FAULT_TEST_SEQ	Executes test sequence on FAULT pin	RW	2	22:21
	VOUT_TEST_SEQ	Executes test sequence on VOUT pin	RW	2	20:19
	SENS_FINE	Sensitivity, fine adjustment	RW	11	18:8
	QVO_FINE	Quiescent Output Voltage (QVO), fine adjustment	RW	8	7:0
Volatile: 0x26	DSC	Die source code	R	30	29:0
Volatile: 0x29	MANCH_COMM_E	Allows continues Manchester R/W commands with the analog output being disabled without overdriving the output pin nor OVD signaling	RW	1	0
Volatile: 0x2F	OTF_STATUS	OTF status bit. Cleared by reading	RW	1	2
	OCF_STATUS	OCF status bit. Cleared by reading	RW	1	1
	OVD_STATUS	Overvoltage detection flag based on OVD signal from Voltage Monitoring	RW	1	0

[1] Overtemperature performance is no longer valid if this register is changed from factory default

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PACKAGE OUTLINE DRAWINGS

For Reference Only - Not for Tooling Use

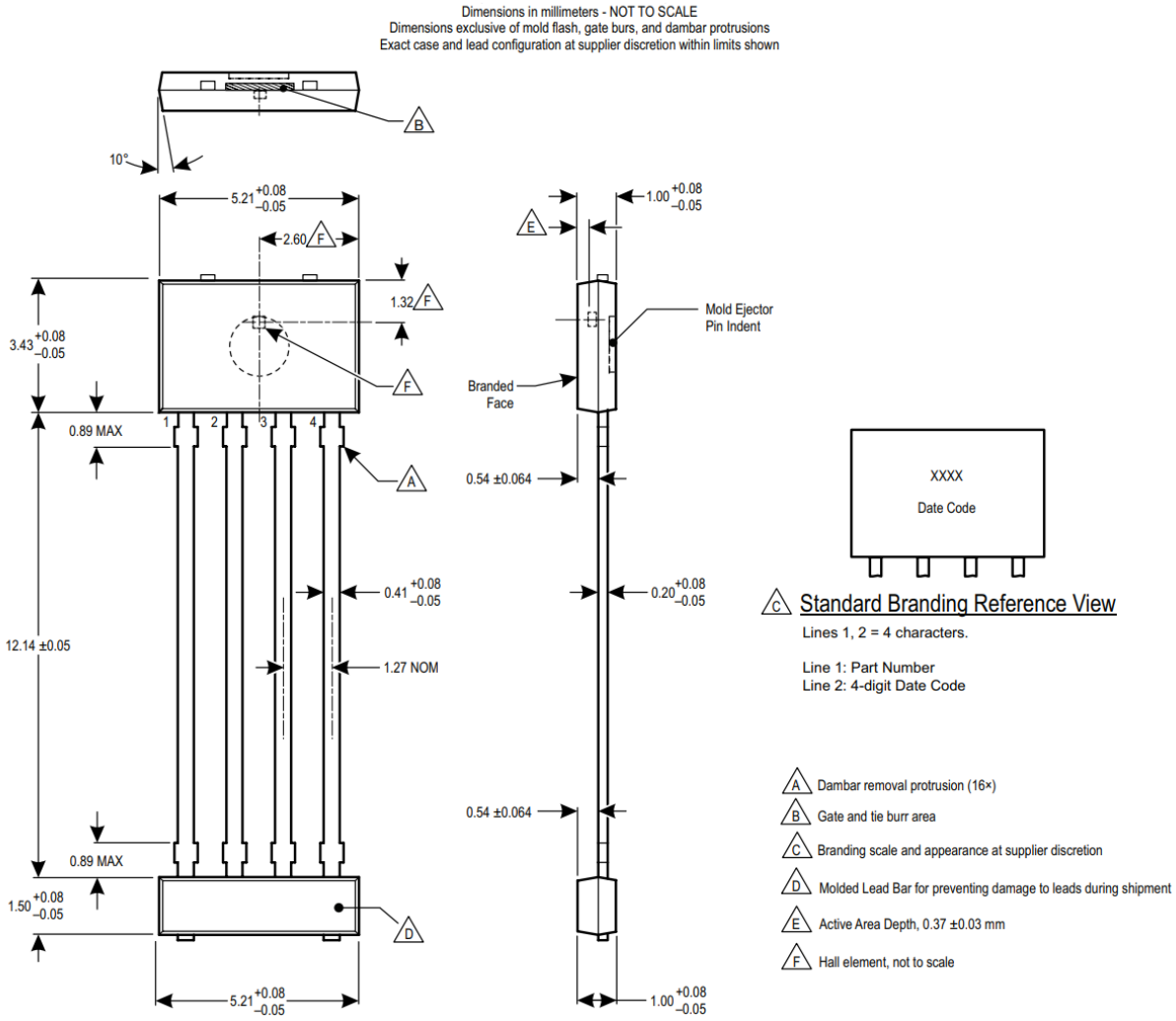

Figure 21: Package KT, 4-Pin SIP, TN Leadform (Straight Leads)

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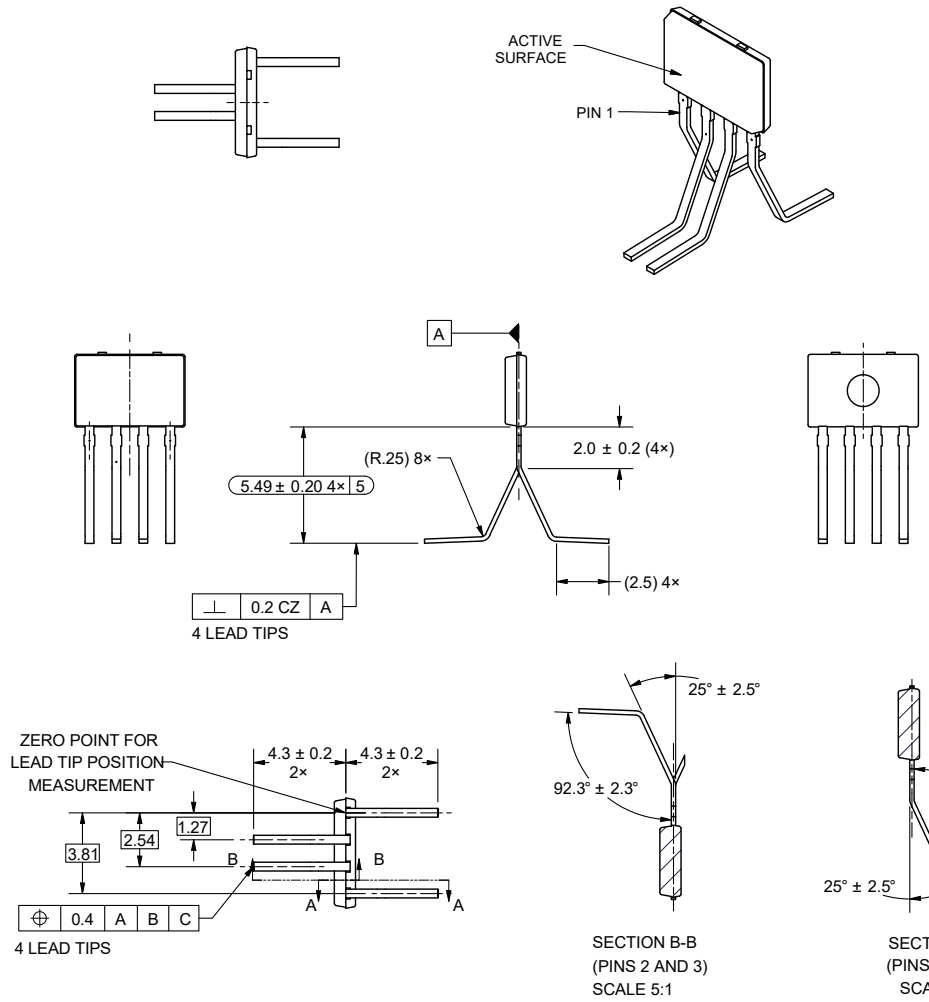

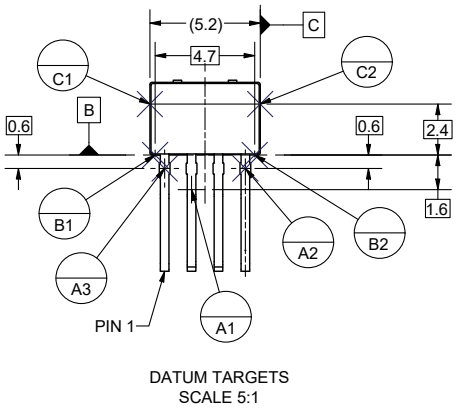

NOTES:

1) LEAD TRIM AND FORMING OPERATIONS PERFORMED ON ALLEGRO SUPPLIED MATERIAL.

2) FOR DIMENSIONS AND TOLERANCING ON SUPPLIED DEVICES, REFER TO ALLEGRO DWG-0000426, REV. 3.

3) TRUE POSITION AND PROFILE TOLERANCE APPLIES ALONG EACH LEAD IN A ZONE STARTING FROM THE LEAD TIP AND ENDING NO MORE THAN 10 mm IN FROM THE TIP.

METRIC TOLERANCES
X.X ± 0.2
X.XX ± 0.1
X.XXX ± 0.05
ANGULAR ± 1°

ALL SURFACES TO BE 0.80 µm OR BETTER
BREAK ALL SHARP EDGES
0.4 mm × 0.4 mm
HOLD ALL DIMS AFTER PLATING

REFERENCE DWG-0000776, Rev. 3

Figure 22: Package KT, 4-Pin SIP, TH Leadform (V-Shaped Leads)

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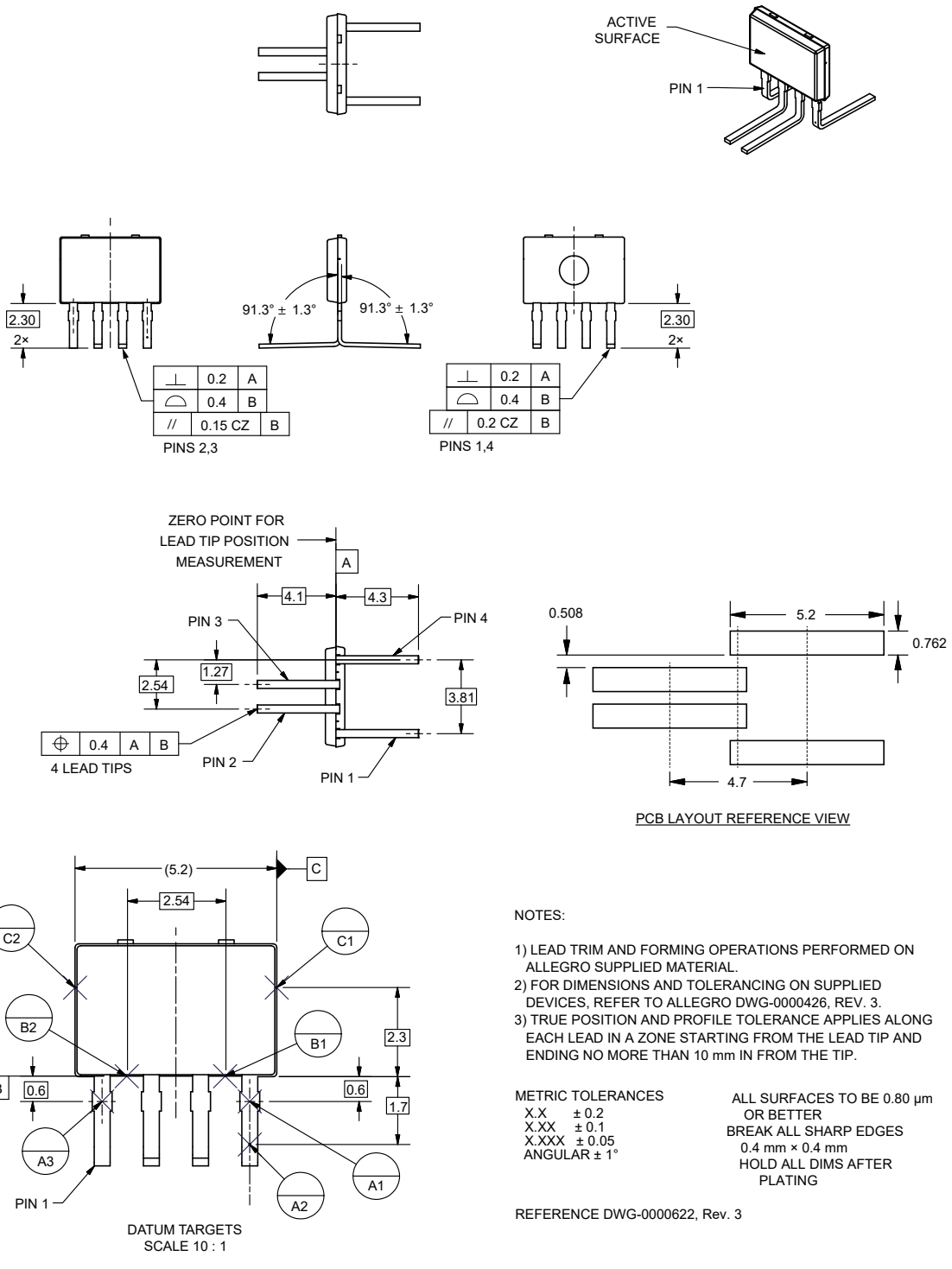

NOTES:

1) LEAD TRIM AND FORMING OPERATIONS PERFORMED ON ALLEGRO SUPPLIED MATERIAL.
2) FOR DIMENSIONS AND TOLERANCING ON SUPPLIED DEVICES, REFER TO ALLEGRO DWG-0000426, REV. 3.
3) TRUE POSITION AND PROFILE TOLERANCE APPLIES ALONG EACH LEAD IN A ZONE STARTING FROM THE LEAD TIP AND ENDING NO MORE THAN 10 mm IN FROM THE TIP.

METRIC TOLERANCES
X.X ± 0.2
X.XX ± 0.1
X.XXX ± 0.05
ANGULAR ± 1°

ALL SURFACES TO BE 0.80 µm OR BETTER
BREAK ALL SHARP EDGES
0.4 mm × 0.4 mm
HOLD ALL DIMS AFTER PLATING

REFERENCE DWG-0000622, Rev. 3

Figure 23: Package KT, 4-Pin SIP, TG Leadform (L-Shaped Leads)

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Revision History

Number	Date	Description
–	December 10, 2025	Initial release

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