

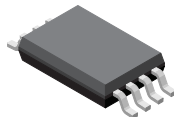
High-Precision, Programmable Linear Hall-Effect Sensor IC

with V_{REF} Overcurrent Fault, and High-Bandwidth (400 kHz) Analog Output for Core-Based Current Sensing

FEATURES AND BENEFITS

- Industry-leading noise performance
- User-programmable bandwidth (100 to 400 kHz) for easy tradeoff between speed and noise
- Very fast response time (<1.25 μ s typ.)
- Wide sensing range (0.8 to 18 mV/G)
- Factory-programmed sensitivity and offset over temperature
- User-programmable sensitivity and offset
- User-programmable sensitivity over temperature for ferromagnetic core drift compensation
- User-programmable overcurrent fault (OCF) pin
 - 1.5 μ s (typ) OCF response time
- User-programmable, bidirectional reference pin (V_{REF}) for full control over offset levels
- Non-ratiometric output for immunity to noisy supplies
- Undervoltage and overvoltage detection
- High output drive current (15 mA)
- Low power mode for reduced I_{CC}
- VCC pin survives exposure up to 15 V
- Monolithic Hall IC for high reliability
- Surface mount, small footprint, low-profile TSSOP8 package
- AEC-Q100 Grade 1, automotive qualified

PACKAGE: 8-pin TSSOP package (suffix LU)



Not to scale

DESCRIPTION

The Allegro ACS37600 is a linear sensor IC designed to be used in conjunction with a ferromagnetic core to provide a highly accurate current sensor suitable for industrial, commercial, and communications applications.

The device consists of a precise, low-offset, chopper-stabilized Hall-effect front end. Magnetic flux orthogonal to the IC package surface is sensed by the integrated Hall and converted into a proportional voltage. A very wide sensitivity range allows current sensor module makers to use this IC for a <20 A or a >1000 A module.

A selectable bandwidth from 100 kHz to >400 kHz makes the device ideal for fast switching applications and applications where low noise is required.

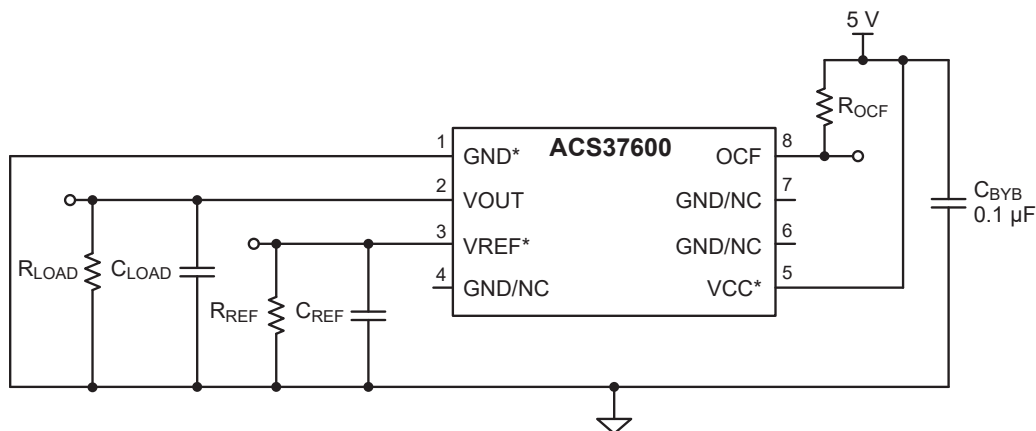
A user-programmable, bidirectional reference voltage pin (V_{REF}) enables constant monitoring of the zero-current voltage and easy interfacing with 3.3 V and 5 V ADCs.

The device includes a user-programmable overcurrent fault pin with a 1.5 μ s (typ) response time for fast short-circuit protection.

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TYPICAL APPLICATIONS

- Current sensing modules
- Solar (MPPT, combiner box)
- Motor control
- Uninterruptable power supplies (UPS)
- Smart fuse
- Overcurrent detection
- Power supplies



* Required for communication.

Figure 1: Typical Application Circuit for ACS37600

DESCRIPTION (continued)

The sensitivity and offset drift over temperature are factory programmed at Allegro to provide a highly accurate solution across the full temperature range.

The ACS37600 is customer programmable. The absolute value of sensitivity and offset can be programmed after manufacturing. Additionally, customers can program the sensitivity over temperature to compensate for ferromagnetic core drifts, enabling industry-leading current sensor accuracy.

A non-ratiometric output immune to supply noise, the ability to survive up to 15 V on the supply pin, and a stellar ESD performance make the ACS37600 ideal for applications where reliability and robustness are required.

The IC is offered in a low-profile 8-pin surface mount TSSOP package (thin-shrink small outline package, suffix LU) that is lead (Pb) free, with 100% matte tin leadframe plating.



SELECTION GUIDE

Part Number	Factory-Trimmed Sensitivity (mV/G)	Factory-Programmed Operating Range (G)		Programmable Sens Range (mV/G)	T_A (°C)	Packing ^[2]
		Bidirectional	Unidirectional ^[1]			
ACS37600KLUA-1P5B5-C	1.5	±1333	0 to 2667	0.8 ^[3] to 1.7	-40 to 125	4000 pieces per 13-inch reel
ACS37600KLUA-003B5-C	3	±667	0 to 1333	1.7 to 3.5		
ACS37600KLUA-006B5-C	6	±333	0 to 667	3.5 to 7.2		
ACS37600KLUA-013B5-C	13.5	±148	0 to 296	7.2 to 18		
ACS37600KLUA-1P5B5-CP	-1.5	±1333	0 to -2667	-0.8 ^[3] to -1.7		
ACS37600KLUA-003B5-CP	-3	±667	0 to -1333	-1.7 to -3.5		
ACS37600KLUA-006B5-CP	-6	±333	0 to -667	-3.5 to -7.2		
ACS37600KLUA-013B5-CP	-13.5	±148	0 to -296	-7.2 to -18		

^[1] This range applies if the VREF pin is overdriven to 0.5 V. If this range is desired without overdriving the VREF pin, contact an Allegro representative.

^[2] Contact an Allegro representative for additional packing options.

^[3] Refer to operating range table for high gauss performance.

Part Numbering Specification

ACS37600KLUATR-1P5B5-CP

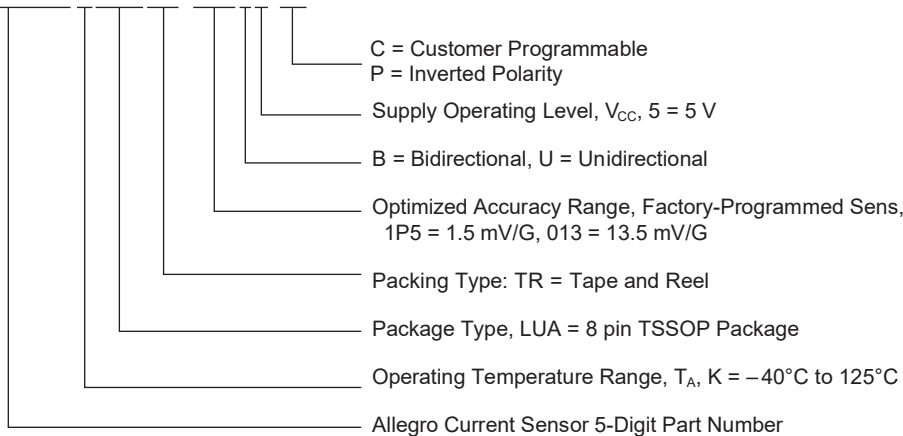


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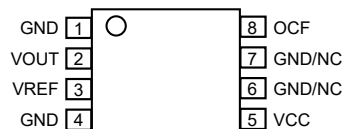
ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{CC}		15	V
Reverse Supply Voltage	V_{RCC}		-0.5	V
Output Voltage	V_{OUT}		$(V_{CC} + 0.5) \leq 15$	V
Reverse Output Voltage	V_{ROUT}		-0.5	V
Reference and OCF Voltage	V_{REF}, V_{OCF}		$(V_{CC} + 0.5) \leq 6.5$	V
Reverse Reference and OCF Voltage	V_{RREF}, V_{ROCF}		-0.5	V
Output Source	I_{OUT}	VOUT connected to GND	30	mA
Output Sink	I_{IN}	VOUT connected to VCC	-30	mA
Operating Ambient Temperature	T_A	Range L	-40 to 150	°C
Junction Temperature	$T_{J(MAX)}$		165	°C
Storage Temperature	T_{stg}		-65 to 165	°C
Maximum Field Range	B	Field of which the device will respond	± 3000	G

OPERATING PARAMETERS

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Operational Ambient Temperature Range	T_A	L temperature range	-40	-	150	°C
Optimal Ambient Temperature Range	T_A	K temperature range	-40	-	125	°C
Optimal Absolute Field Range	B_{OG}	Performance specifications are guaranteed at or within this limit of B	0	-	1625	G
Nominal Absolute Field Range	B_{NG}	Linearity degrades within this B range	1650	-	2500	G
Extended Absolute Field Range	B_{EG}	The output may still respond but linearity degrades significantly within this B range	2500	-	3000	G

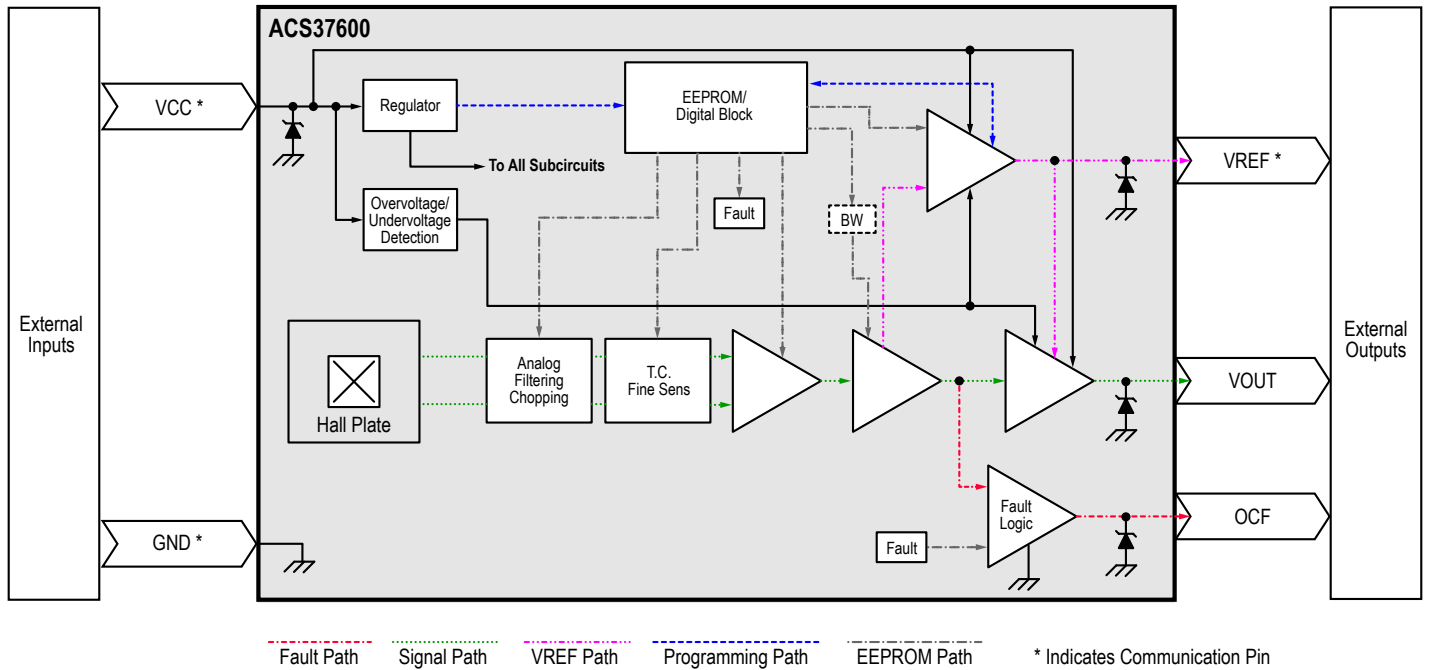
Pinout Diagram



Pinout List

Number	Name	Description
6, 7	GND/NC	No connect or Ground; connect to GND for optimal ESD performance
1, 4	GND	Device ground (Pin 1 is primary GND)
5	VCC	Device supply
2	VOUT	Device analog output
3	VREF	Reference voltage for output
8	OCF	Overcurrent fault (OCF) reporting pin (open drain)

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS: Valid through the full operating temperature range, T_A , $C_{BYP} = 0.1 \mu F$, $V_{CC} = 5 V$, $eco_mode = 0$, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	Standard operating voltage	4.5	5	5.5	V
Supply Current	I_{CC}	$V_{CC} = 4.5$ to 5.5 V, output open, factory default	–	16	23	mA
		$V_{CC} = 4.5$ to 5.5 V, output open, $eco_mode = 1$	–	14	23	mA
Output Capacitive Load	C_{LOAD}	VOOUT to GND	–	–	4.7	nF
Output Resistive Load	R_{LOAD}	VOOUT to GND or VOOUT to VCC	2	–	–	k Ω
Reference Resistive Load	R_{REF}	VREF to GND	200	–	–	k Ω
Reference Capacitive Load	C_{REF}	VREF in input/output mode, VREF to GND	0.5	–	47	nF
		VREF in output mode only, VREF to GND	0.5	–	4.7	nF
Overcurrent Fault Pull-Up Resistor	R_{OCF}	OCF to VCC or other pull-up node	10	–	–	k Ω
Power-On Reset Voltage [1]	$V_{POR(H)}$	Device powers on; V_{CC} ramp rate = +1 V/ms from GND	3.6	3.8	3.9	V
	$V_{POR(Hys)}$	$V_{POR(H)} - V_{POR(L)}$; $T_A = 25^\circ C$	0.25	0.4	0.56	V
	$V_{POR(L)}$	Device powers off; V_{CC} ramp rate = –1 V/ms from 5 V	3.2	3.4	3.5	V
Power-On Reset Release Time	t_{PORR}	Time from $V_{UVD(H)}$ [1] until output and reference is released	–	95	–	μs
Power-On Reset: Output Settle Time	$t_{POR(OUT)}$	Time from when t_{PORR} until 90% $V_{OUT} - V_{REF}$ stable state with 0 G applied; $C_{LOAD} = 4.7$ nF, no R_{LOAD}	–	8	–	μs
Power-On Reset: Reference Settle Time	$t_{POR(REF)}$	V_{REF} in output/input or output only mode; time from t_{PORR} until 90% reference steady state with 0 G applied; no R_{REF} , $C_{REF} = 4.7$ nF	–	17	–	μs
Power-On Delay	t_{POD}	$T_A = 25^\circ C$, V_{REF} in input only mode, driven to 2.5 V; time from $V_{UVD(H)}$ [1] until 90% V_{OUT} stable state with 0 G applied; $C_{LOAD} = 4.7$ nF, no R_{LOAD}	–	103	–	μs
		$T_A = 25^\circ C$, V_{REF} in input/output or output only mode, driving to 2.5 V; time from $V_{UVD(H)}$ [1] until 90% V_{OUT} stable state with 0 G applied; C_{LOAD} and $C_{REF} = 4.7$ nF, no R_{LOAD} or R_{REF}	–	112	–	μs
Overcurrent Fault Startup Time	$t_{POR(OCF)}$	Time from $V_{UVD(H)}$ [1] until fault is functional	–	105	–	μs
Temperature Compensation Update Rate	t_{UR}		–	8	–	ms
Undervoltage Detection	$V_{UVD(H)}$	$V_{OUT} =$ nominal operation; $T_A = 25^\circ C$; V_{CC} ramp rate = +1 V/ms from GND	4	–	4.4	V
	$V_{UVD(Hys)}$	$V_{UVD(H)} - V_{UVD(L)}$; $T_A = 25^\circ C$	–	0.4	–	V
	$V_{UVD(L)}$	$V_{OUT} = 0$ V; $T_A = 25^\circ C$; V_{CC} ramp rate = –1 V/ms from 5 V	3.6	–	4	V
UVD Enable Delay Time	$t_{UVD(E)}$	Time measured from falling $V_{CC} < V_{UVD(E)}$ to V_{OUT} pulled low	35	64	90	μs
UVD Disable Delay Time	$t_{UVD(D)}$	Time measured from rising $V_{CC} > V_{UVD(D)}$ to V_{OUT} is 90% V_{REF} stable state with 0 G applied	–	8	–	μs
Overvoltage Detection	$V_{OVD(H)}$	$V_{OUT} =$ high Z[2]; $T_A = 25^\circ C$; V_{CC} ramp rate = +1 V/ms from 5 V	7.2	7.6	8	V
	$V_{OVD(Hys)}$	$V_{UVD(H)} - V_{UVD(L)}$; $T_A = 25^\circ C$	–	1	–	V
	$V_{OVD(L)}$	$V_{OUT} =$ back to nominal operation; $T_A = 25^\circ C$; V_{CC} ramp rate = –1 V/ms from 8.1 V	6.1	6.6	7	V
OVD Enable Delay Time	$t_{OVD(E)}$	Time measured from falling $V_{CC} > V_{OVD(E)}$ to V_{OUT} becoming high Z	35	64	90	μs
OVD Disable Delay Time	$t_{OVD(D)}$	Time measured from rising $V_{CC} < V_{OVD(D)}$ to V_{OUT} is 90% V_{REF} stable state with 0 G applied	–	7	–	μs
Supply Zener Clamp Voltage	V_Z	$T_A = 25^\circ C$, $I_{CC} = 30$ mA	–	20	–	V

[1] POR release threshold is either $V_{POR(H)}$ if $uvd_dis = 1$ or $V_{UVD(H)}$ if $uvd_dis = 0$. Factory default setting is $uvd_dis = 0$.

[2] Reverse output voltage maximum can be exceeded if V_{OUT} is pulled down to –6 V.

ELECTRICAL CHARACTERISTICS (continued): Valid through the full operating temperature range, T_A , $C_{BYP} = 0.1 \mu F$, $V_{CC} = 5 V$, $eco_mode = 0$, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
VOUT OPERATING CHARACTERISTICS							
Output Voltage Operating Range	V_{OOR}	Linear operating range	0.5	–	4.5	V	
Output Saturation Voltage	$V_{SAT(HIGH)}$	$V_{CC} = 5 V$, $R_{LOAD} = 2 k\Omega$ pull-down	$V_{CC} - 0.3$	–	–	V	
	$V_{SAT(LOW)}$	$V_{CC} = 5 V$, $R_{LOAD} = 2 k\Omega$ pull-up	0	–	0.4	V	
Output Saturation @ 10 mA Current Load (Pull-Up Config.)	$V_{SAT(HIGH)}$	$V_{CC} = 5 V$, $I_L = -10 mA$, $T_A = 25^\circ C$	4.5	4.7	–	V	
	$V_{SAT(LOW)}$	$V_{CC} = 5 V$, $I_L = 10 mA$, $T_A = 25^\circ C$	–	0.2	0.4	V	
DC Output Resistance	R_{OUT}		–	2	5	Ω	
Output Maximum Drive Current	I_{OD}	Drive mode: Turbo	–	–	15	mA	
		Drive mode: Economy	–	–	7.5	mA	
Rise Time	t_{RISE}	$T_A = 25^\circ C$, $C_L = 1 nF$, 1 μs input step 1 V output swing 10% to 90% V_{OUT}	BW = 100 kHz	–	2.4	3.5	μs
			BW = 250 kHz	–	1.65	2.5	μs
			BW = 400 kHz	–	1.2	2	μs
			BW = 450 kHz	–	1.15	–	μs
Propagation Delay	t_{PD}	$T_A = 25^\circ C$, $C_L = 1 nF$, 1 μs input step 1 V output swing, 10% input to 10% output	BW = 100 kHz	–	0.9	1.5	μs
			BW = 250 kHz	–	0.85	1.4	μs
			BW = 400 kHz	–	0.75	1.3	μs
			BW = 450kHz	–	0.7	–	μs
Response Time	$t_{RESPONSE}$	$T_A = 25^\circ C$, $C_L = 1 nF$, 1 μs input step 1 V output swing 90% input to 90% output	BW = 100 kHz	–	3.5	6	μs
			BW = 250 kHz	–	2.4	3.5	μs
			BW = 400 kHz	–	1.25	2.5	μs
			BW = 450kHz	–	1.2	–	μs
Overshoot	V_{OS}	$T_A = 25^\circ C$, $C_L = 4.7 nF$, 1 μs input step 1 V output swing	$bw_sel = 0, 1, 2$	–	5	10	%
			$bw_sel = 3$	–	5	15	%
Settling Time	t_{SETTLE}	V_{OUT} within 3% V_{OUT} Step, $T_A = 25^\circ C$, $C_L = 1 nF$, 1 μs input step 1 V output swing	–	–	10	μs	
Input Referred Noise Density	B_{ND}	$V_{CC} = 5.0 V$, Input Referred, @ 400 kHz	$T_A = 25^\circ C$	–	1.21	1.64	mG/ \sqrt{Hz}
			$T_A = 125^\circ C$	–	1.69	2.25	mG/ \sqrt{Hz}
Output Noise	V_N	$V_{CC} = 5.0 V$, $C_L = 1 nF$, Sens = 3 mV/G, BW = 400kHz	$T_A = 25^\circ C$	–	2.83	–	mV _{RMS}
			$T_A = 125^\circ C$	–	3.61	–	mV _{RMS}
Sensitivity Symmetry Error	E_{SYM}		–1	0.25	1	%	
Nonlinearity	E_{LIN}	$T_A = -40^\circ C$ to $125^\circ C$, $ B \leq 1650 G$	–0.5	± 0.25	0.5	%	
		$T_A = -40^\circ C$ to $125^\circ C$, 2500 G > $ B $ > 1650 G	–1	–	1	%	
Offset Power Supply Rejection Ratio	$PSRR_O$	AC $V_{CC} = 5 V \pm 10\%$, $T_A = 25^\circ C$	DC to 1 kHz	–	40	–	dB
			1 to 20 kHz	–	30	–	dB
			20 to 60 kHz	–	20	–	dB
Sensitivity Power Supply Rejection Ratio	$PSRR_S$	AC $V_{CC} = 5 V \pm 10\%$, $T_A = 25^\circ C$	DC to 1 kHz	–	40	–	dB
			1 to 20 kHz	–	30	–	dB
			20 to 60 kHz	–	20	–	dB
Power Supply Offset Error	V_{PS}	DC $V_{CC} = 5.5 V$ and $4.5 V$	–5	± 0.25	5	mV	
Power Supply Sensitivity Error	EPS	DC $V_{CC} = 5.5 V$ and $4.5 V$	–0.5	–	0.5	%	

ELECTRICAL CHARACTERISTICS (continued): Valid through the full operating temperature range, T_A , $C_{BYP} = 0.1 \mu F$, $V_{CC} = 5 V$, $eco_mode = 0$, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
VREF OUTPUT CHARACTERISTICS							
Reference Output Noise	V_{NR}	$f > 100 \text{ Hz}$	–	0.5	–	$\mu V/\sqrt{\text{Hz}}$	
DC Internal Reference Output Resistance	R_{REF_INT}	Output/Input Mode	150	200	300	Ω	
		Output Mode Only	–	2	5	Ω	
		Input Mode Only	–	200	–	$k\Omega$	
Reference Voltage Input Range	$V_{REF(IN)}$	$T_A = 25^\circ\text{C}$, V_{REF} overdriven externally	0.5	–	2.65	V	
Reference Source Current	I_{SOURCE_REF}	V_{REF} to GND	0.5	0.7	1	mA	
Reference Sink Current	I_{SINK_REF}	V_{REF} to VCC	–	5	10	mA	
OCF OPERATING CHARACTERISTICS							
Overcurrent Fault Leakage Current	I_{LEAK}	$V_{CC} = 5 V$, $R_{FAULT} = 10 k\Omega$ to VCC, during non-fault condition	–	1	–	μA	
Overcurrent Fault On Internal Resistance	R_{OCF_Int}	Open drain; active low	105	140	200	Ω	
Overcurrent Fault Output Voltage	V_{OCF_ON}	OCF pin voltage during fault condition	–	–	0.3	V	
Overcurrent Fault Fall Time	$t_{OCF(FALL)}$	$R_{OCF} = 10 k\Omega$, 90% output to 10% output final voltage	–	1	–	μs	
Overcurrent Fault Response Time	t_{OCF}	Time from input rising above $ V_{OCF(OP)} $ until $OCF < V_{OCF_ON}$	BW = 100 kHz	–	2.7	7.5	μs
			BW = 250 kHz	–	2	5	μs
			BW = 400 kHz	–	1.5	4	μs
			BW = 450 kHz	–	1.4	–	μs
Overcurrent Fault Hysteresis	V_{OCF_Hyst}	Hysteresis below trip point before fault resets	ocf_hys = 0	–	120	–	mV
			ocf_hys = 1	–	240	–	mV

ELECTRICAL CHARACTERISTICS (continued): Valid through the full operating temperature range, T_A , $C_{BYP} = 0.1 \mu F$, $V_{CC} = 5 V$, $eco_mode = 0$, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
PROGRAMMABLE CHARACTERISTICS: QUIESCENT VOLTAGE AND REFERENCE VOLTAGE							
Reference Voltage Coarse	$BITS_{VREF_COARSE}$	vref_coarse	–	2	–	bit	
Reference Voltage Fine	$BITS_{VREF_FINE}$	voff_fine	–	9	–	bit	
Factory-Programmed Reference Voltage	V_{REF_FACT}		–	2.5	–	V	
Average VREF Programming Step Size	$STEP_{VREF}$	$T_A = 25^\circ C$	–	0.98	–	mV	
Reference Voltage Temperature Compensation Step Size	$STEP_{VREF_TC}$	Step size at each of TC point	–	$STEP_{VREF}$	–	mV	
Reference Voltage Output Programming Range	$V_{REF(OUT)}$	$T_A = 25^\circ C$; the vref_fine programming range for a given vref_coarse	vref_coarse = 11; factory default	2.35	2.5	2.65	V
			vref_coarse = 10	1.5	1.65	1.8	V
			vref_coarse = 01	1.35	1.5	1.65	V
			vref_coarse = 00	0.35	0.5	0.65	V
Offset Voltage Programming Bits	$BITS_{VOFF_FINE}$	voff_fine	–	9	–	bit	
Factory-Programmed Quiescent Voltage Output	$V_{OUT(Q)}$	$T_A = 25^\circ C$; 0 G	–	V_{REF}	–	V	
Offset Voltage Programming Step Size	$STEP_{VOFF}$	$V_{OFF} = V_{OUT(Q)} - V_{REF}$	–	1.15	–	mV	
Offset Voltage Temperature Compensation Step Size	$STEP_{VOFF_TC}$	Step size at each of TC point	–	$STEP_{VREF}$	–	mV	
Offset Voltage Programming Range	V_{OFF_PR}	$V_{OFF} = V_{OUT(Q)} - V_{REF}$	–200	–	200	mV	
PROGRAMMABLE CHARACTERISTICS: SENSITIVITY							
Coarse Sensitivity Programming Bits	$BITS_{SENS_C}$	sens_coarse	–	2	–	bit	
Sensitivity Programming Bits	$BITS_{SENS_FINE}$	sens_fine	–	9	–	bit	
Factory-Programmed Sensitivity	$Sens_{FACT}$	$T_A = 25^\circ C$	sens_coarse = 11; 013B5-C	–	13.5	–	mV/G
			sens_coarse = 10; 006B5-C	–	6	–	mV/G
			sens_coarse = 01; 003B5-C	–	3	–	mV/G
			sens_coarse = 00; 1P5B5-C	–	1.5	–	mV/G
Average Sensitivity Step Size	$STEP_{SENS}$	$T_A = 25^\circ C$; sens_fine programming step size for a given sens_coarse	sens_coarse = 11	29.57	34	40	$\mu V/G$
			sens_coarse = 10	13.14	15.11	17.78	$\mu V/G$
			sens_coarse = 01	6.57	7.56	8.89	$\mu V/G$
			sens_coarse = 00	3.29	3.78	3.44	$\mu V/G$
Sensitivity Temperature Compensation Step Size	$STEP_{SENS_TC}$	Step size at each of TC point	–	$STEP_{SENS}$	–	Sens	

ELECTRICAL CHARACTERISTICS (continued): Valid through the full operating temperature range, T_A , $C_{BYP} = 0.1 \mu F$, $V_{CC} = 5 V$, $eco_mode = 0$, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
PROGRAMMABLE CHARACTERISTICS: SENSITIVITY (CONTINUED)							
Sensitivity Programming Range	$Sens_{SPR}$	$T_A = 25^\circ C$; $sens_fine$ programming range for a given $sens_coarse$	$sens_coarse = 11$	7.2	–	18	mV/G
			$sens_coarse = 10$	3.5	–	7.2	mV/G
			$sens_coarse = 01$	1.7	–	3.5	mV/G
			$sens_coarse = 00$	0.8	–	1.7	mV/G
Sensitivity Slope Over Temperature Bits	$BITS_{SENS_SLOPE}$	$gain_tc$	–	6	–	bit	
Sensitivity Slope Temperature Coefficient Step Size	$STEP_{SENS_SLOPE}$		–	0.002	–	%/ $^\circ C$	
Sensitivity Slope Temperature Coefficient Programming Range	$Sens_{SLOPE_PR}$		–0.025	–	0.05	%/ $^\circ C$	
PROGRAMMABLE CHARACTERISTICS: OVERCURRENT FAULT							
Overcurrent Fault Step Bits	$BITS_{OCF}$	ocf_thr	–	9	–	bit	
Factory Overcurrent Fault Operating Point	$V_{OCF(fact)}$	Fault threshold in mV of equivalent output swing from V_{REF}	–	2000	–	mV	
Overcurrent Fault Step Size	$STEP_{OCF}$	V_{OCF} step size in mV of equivalent output swing	–	9	–	mV	
Overcurrent Fault Operating Point Range	V_{OCF_R}	Fault operating point range in mV of equivalent output swing from V_{REF}	500	–	5000	mV	
Overcurrent Fault Mask Time Range	$t_{OCF(MASK)}$	With $R_{FAULT} = 10 k\Omega$	0	–	3.5	μs	
Overcurrent Fault Hold Time	$t_{OCF(HOLD)}$	Minimum time after OCF flag before flag is released	0	–	5	ms	

ACS37600KLU DEVICE PERFORMANCE CHARACTERISTICS: Valid through the full operating temperature range, T_A , $C_{BYP} = 0.1 \mu F$, $V_{CC} = 5 V$, $eco_mode = 0$, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
QUIESCENT OUTPUT VOLTAGE AND REFERENCE OUTPUT VOLTAGE ERROR						
Factory QVO Error	$V_{OUT(Q)_ERR}$	$T_A = 25^\circ C$	-10	1±4	10	mV
QVO Temperature Drift	$V_{OUT(Q)_TC}$	$T_A = 25^\circ C$ to $125^\circ C$, $V_{OUT(Q)} - V_{OUT(Q)@25^\circ C}$	-10	2 ±6	10	mV
		$T_A = 25^\circ C$ to $-40^\circ C$, $V_{OUT(Q)} - V_{OUT(Q)@25^\circ C}$	-10	-1 ±4	10	mV
Factory Reference Output Voltage Error	V_{REF_ERR}	$T_A = 25^\circ C$	-10	±4	10	mV
Reference Voltage Temperature Drift	V_{REF_TC}	$T_A = 25^\circ C$ to $125^\circ C$, $V_{REF} - V_{REF@25^\circ C}$	-10	±4	10	mV
		$T_A = 25^\circ C$ to $-40^\circ C$, $V_{REF} - V_{REF@25^\circ C}$	-10	-1 ±2	10	mV
Factory Offset Output Voltage Error	V_{OE_ERR}	$T_A = 25^\circ C$, $V_{OUT(Q)} - V_{REF}$	-10	-1±3	10	mV
Offset Error Temperature Drift	V_{OE_TC}	$T_A = 25^\circ C$ to $125^\circ C$, $V_{OE} - V_{OE@25^\circ C}$	-10	-4 ±3	10	mV
		$T_A = 25^\circ C$ to $-40^\circ C$, $V_{OE} - V_{OE@25^\circ C}$	-10	-1 ±4	10	mV
SENSITIVITY ERROR						
Factory Sensitivity Error	E_{SENS_ERR}	$T_A = 25^\circ C$	-1.75	±1	1.75	%
Sensitivity Temperature Drift	E_{SENS_TC}	$T_A = 25^\circ C$ to $125^\circ C$, $E_{SENS} - E_{SENS@25^\circ C}$	-1.75	-0.4 ±1.1	1.75	%
		$T_A = 25^\circ C$ to $-40^\circ C$, $E_{SENS} - E_{SENS@25^\circ C}$	-1.75	±1	1.75	%
FACTORY PERFORMANCE ERROR INCLUDING LIFETIME DRIFT⁽¹⁾						
Factory QVO Error Including Lifetime Drift	$V_{OUT(Q)_ERR_LTD}$	$T_A = 25^\circ C$	-	6 ± 6	-	mV
QVO Temperature Drift Including Lifetime Drift	$V_{OUT(Q)_TC_LTD}$	$T_A = 25^\circ C$ to $125^\circ C$, $V_{OUT(Q)} - V_{OUT(Q)@25^\circ C}$	-	2 ± 6	-	mV
		$T_A = 25^\circ C$ to $-40^\circ C$, $V_{OUT(Q)} - V_{OUT(Q)@25^\circ C}$	-	- 1 ± 8	-	mV
Factory Reference Output Voltage Error Including Lifetime Drift	$V_{REF_ERR_LTD}$	$T_A = 25^\circ C$	-	- 1 ± 6	-	mV
Reference Voltage Temperature Drift Including Lifetime Drift	$V_{REF_TC_LTD}$	$T_A = 25^\circ C$ to $125^\circ C$, $V_{REF} - V_{REF@25^\circ C}$	-	1 ± 6	-	mV
		$T_A = 25^\circ C$ to $-40^\circ C$, $V_{REF} - V_{REF@25^\circ C}$	-	- 1 ± 6	-	mV
Factory Offset Output Voltage Error Including Lifetime Drift	$V_{OE_ERR_LTD}$	$T_A = 25^\circ C$, $V_{OUT(Q)} - V_{REF}$	-	- 5 ± 5	-	mV
Offset Error Temperature Drift Including Lifetime Drift	$V_{OE_TC_LTD}$	$T_A = 25^\circ C$ to $125^\circ C$, $V_{OE} - V_{OE@25^\circ C}$	-	3 ± 5	-	mV
		$T_A = 25^\circ C$ to $-40^\circ C$, $V_{OE} - V_{OE@25^\circ C}$	-	± 5	-	mV
Factory Sensitivity Error Including Lifetime Drift	$E_{SENS_ERR_LTD}$	$T_A = 25^\circ C$	-	± 1.7	-	
Sensitivity Temperature Drift Including Lifetime Drift	$E_{SENS_TC_LTD}$	$T_A = 25^\circ C$ to $125^\circ C$, $E_{SENS} - E_{SENS@25^\circ C}$	-	-1 ± 1.6	-	%
		$T_A = 25^\circ C$ to $-40^\circ C$, $E_{SENS} - E_{SENS@25^\circ C}$	-	-0.6 ± 1.7	-	%
Overcurrent Fault Factory Error	V_{OCF_EFAC}	Fault trip point error in mV of equivalent output swing	-100	-	100	mV

⁽¹⁾ Performance including lifetime drift is based on a convolution of initial performance distributions and drift seen during commercial qualification. Typical values are the worst-case observed mean ±3 sigma drift during the commercial qualification.

ACS37600KLU DEVICE PERFORMANCE CHARACTERISTICS: Valid through the full operating temperature range, T_A , $C_{BYP} = 0.1 \mu F$, $V_{CC} = 5 V$, $eco_mode = 0$, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
PERFORMANCE ERROR INCLUDING LIFETIME DRIFT AFTER END-OF-LINE CALIBRATION^[1]						
QVO Lifetime Drift	V_{QVO_LTD}	$T_A = 25^\circ C$	–	5 ± 5	–	mV
QVO Temperature Drift Including Lifetime Drift	$V_{OUT(Q)_TC_LTD}$	$T_A = 25^\circ C$ to $125^\circ C$, $V_{OUT(Q)} - V_{OUT(Q)@25^\circ C}$	–	2 ± 6	–	mV
		$T_A = 25^\circ C$ to $-40^\circ C$, $V_{OUT(Q)} - V_{OUT(Q)@25^\circ C}$	–	-1 ± 8	–	mV
Reference Voltage Lifetime Drift	V_{REF_LTD}	$T_A = 25^\circ C$	–	± 5	–	mV
Reference Voltage Temperature Drift Including Lifetime Drift	$V_{REF_TC_LTD}$	$T_A = 25^\circ C$ to $125^\circ C$, $V_{REF} - V_{REF@25^\circ C}$	–	1 ± 6	–	mV
		$T_A = 25^\circ C$ to $-40^\circ C$, $V_{REF} - V_{REF@25^\circ C}$	–	-1 ± 6	–	mV
Offset Error Voltage Lifetime Drift	V_{OFF_LTD}	$T_A = 25^\circ C$	–	-4 ± 4	–	mV
Offset Error Temperature Drift Including Lifetime Drift	$V_{OE_TC_LTD}$	$T_A = 25^\circ C$ to $125^\circ C$, $V_{OE} - V_{OE@25^\circ C}$	–	3 ± 5	–	mV
		$T_A = 25^\circ C$ to $-40^\circ C$, $V_{OE} - V_{OE@25^\circ C}$	–	± 5	–	mV
Sensitivity Lifetime Drift	E_{SENS_LTD}	$T_A = 25^\circ C$	–	± 1.4	–	%
Sensitivity Temperature Drift Including Lifetime Drift	$E_{SENS_TC_LTD}$	$T_A = 25^\circ C$ to $125^\circ C$, $E_{SENS} - E_{SENS@25^\circ C}$	–	-1 ± 1.6	–	%
		$T_A = 25^\circ C$ to $-40^\circ C$, $E_{SENS} - E_{SENS@25^\circ C}$	–	-0.6 ± 1.7	–	%
Overcurrent Fault Reprogramming Error	V_{OCF_ERR}	Fault trip point error in mV of equivalent output swing	–200	–	200	mV

^[1] Lifetime drift characteristics are based on the commercial qualification results from zero hours reads. Performance including lifetime drift is based on a convolution of initial performance distributions and drift seen during commercial qualification. Typical values are the worst-case observed mean ± 3 sigma drift during the commercial qualification.

FUNCTIONAL DESCRIPTION

Power-On Reset Operation

The POR thresholds of the ACS37600 is based on a combination of a check on the internal regulator supplied and V_{CC} . This allows the ACS37600 to accurately report a signal, including internal stress and temperature compensation, at startup. Refer to Figure 2 and Figure 7 for power factory on/off profile of ACS37600.

Power-On

As V_{CC} ramps up, the ACS37600 V_{OUT} and V_{REF} pins are high impedance until V_{CC} reaches and passes $V_{UVD(H)}$ [2] (or $V_{POR(H)}$ [1] if UVD is disabled). Once V_{CC} passes [2], the device takes a time, t_{POD} , without V_{CC} dropping below $V_{POR(L)}$ [8] before the outputs enters normal operation.

Power-Off

As V_{CC} drops below $V_{POR(L)}$ [8], the outputs will enter a high impedance state. If UVD is enabled, before the device powers off it will force V_{OUT} to GND if $V_{CC} < V_{UVD(L)}$ [6] until $V_{POR(L)}$ [8] is reached at which point V_{OUT} and V_{REF} will go high Z. If UVD is disabled, then V_{REF} and V_{OUT} will continue to report until V_{CC} is less than $V_{POR(L)}$ [8] at which point they will go high Z.

Note: Since the device is entering a high Z state, and not forcing the output, the time it takes the output to settle will depend on the external circuitry used.

Power-On Timing

The descriptions in this section assume: temperature = 25°C, with the labeled test conditions. The provided graphs in this section show V_{OUT} moving with V_{CC} . V_{OUT} during a high-impedance state will be most consistent with a known load (R_{LOAD} , C_{LOAD}).

Power-On Reset (POR)

If V_{CC} falls below $V_{POR(L)}$ [8] while in operation, the output will re-enter a high-impedance state. After V_{CC} recovers and exceeds $V_{UVD(H)}$ [2] the output will begin reporting again after the delay of t_{POD} . This t_{POD} depends on t_{PORR} , $t_{POR-OUT}$ and, $t_{POR-REF}$.

Power-On Reset Release Time (t_{PORR})

When V_{CC} rises above $V_{UVD(H)}$ [2], the Power-On Reset delay counter starts. If UVD is disabled, this threshold is $V_{POR(H)}$ [1]. The output will only release from high impedance to nominal operation after the Power-On Reset counter has reached the internal t_{PORR} and the temperature compensation has updated. This allows for robust and stable output reporting that is temperature compensated. If V_{CC} falls below $V_{POR(L)}$ [8] before the counter finishes the counter is reset and the part remains in the reset state.

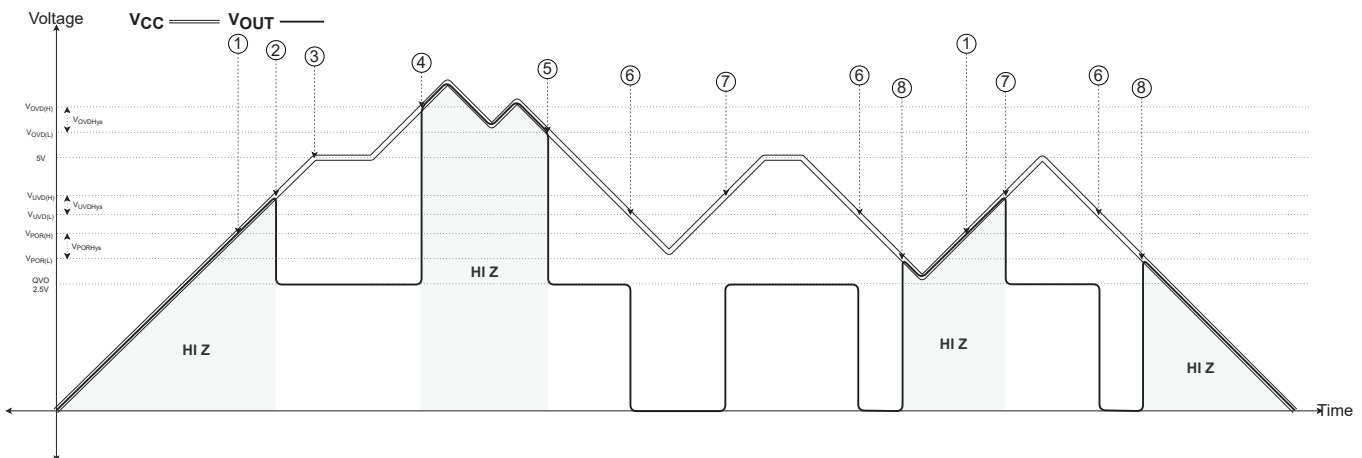


Figure 2: Power States Thresholds with V_{OUT} Behavior, R_L = Pull-Up, UVD Enabled

Power-On Reset Output Delay ($t_{POR-OUT}$)

The term $t_{POR-OUT}$ is defined as the time required for the output to reach 90% of its stable state around V_{REF} after t_{PORR} POR from its high Z state. This is best measured with V_{REF} either being overdriven or externally supplied as seen in Figure 5. This is the time between $V_{UVD(H)}$ [2] + t_{PORR} and point [A]. Since V_{OUT} takes direct input and is centered at V_{REF} , the output stable state is $V_{OUT(Field)} = Sens \times Field + V_{REF}$. Refer to the next section for discussion of the implications of V_{REF} driven internally.

Power-On Reset Reference Delay($t_{POR-REF}$)

The term $t_{POR-REF}$ is defined as the time required for the V_{REF} output to drive the pin to 90% V_{REF} stable state from the high Z state. This is the time between $V_{UVD(H)}$ [2] + t_{PORR} and point [a] seen in Figure 6. The voltage on the VREF pin is the common mode voltage for the V_{OUT} amplifier and will dictate the zero for V_{OUT} .

The VREF pin is meant to be overdriven, which is achieved by limiting the drive strength of the output amplifier. This drive limitation makes the $t_{POR-REF}$ extremely dependent on the application circuit elements R_{REF} and C_{REF} . This dependency should be considered when selecting the R_{REF} and C_{REF} values.

Overcurrent Fault Startup Time ($t_{POR-OCF}$)

The term $t_{POR-OCF}$ is defined as the amount of time the Overcurrent Fault (OCF) circuit takes to be active, stable, and accurate from $V_{UVD(H)}$ (or $V_{POR(H)}$ if UVD is disabled) to OCF actively being controlled. The OCF circuit will be able to report with an active low when a fault condition is present after this time.

Power-On Delay (t_{POD})

When the supply is ramped to $V_{UVD(H)}$ (seen in Figure 5 as [2]), the device will require a finite time to power its internal components before the outputs are released from high Z and can responding to an input magnetic field. Power-On Time, t_{POD} , is defined as the time it takes for the output voltage to settle within $\pm 10\%$ of its steady-state value under an applied magnetic field, which can be seen the time from [2] to [A] or [a], depending on the V_{REF} configuration. After this delay, the output will quickly approach $V_{OUT(Gauss)} = Sens \times Field + V_{REF}$. Below in Figure 5, a driven V_{REF} t_{POD} can be seen and in Figure 6, the internal V_{REF} t_{POD} can be seen.

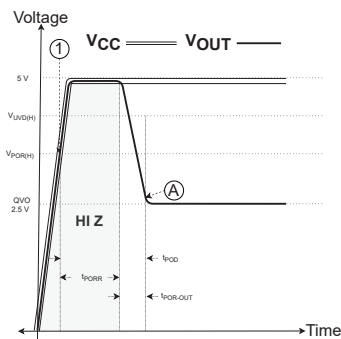


Figure 3: POR behavior, UVD disabled, $R_L =$ Pull-Up

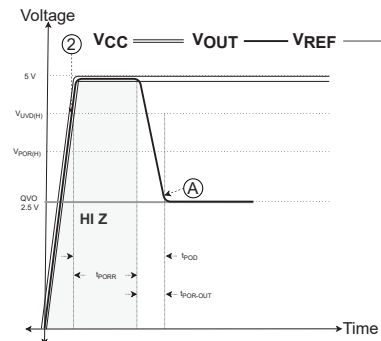


Figure 5: t_{POD} V_{OUT} Behavior with V_{REF} Externally Driven, $t_{POR-OUT}$, $R_L =$ Pull-Up

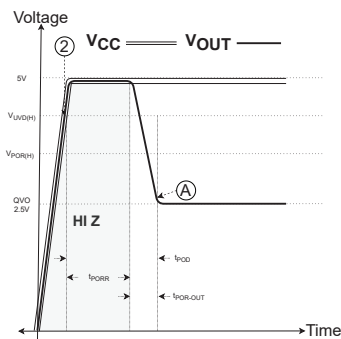


Figure 4: POR behavior, UVD enabled, $R_L =$ Pull-Up

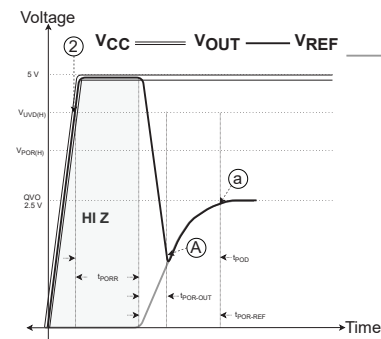


Figure 6: t_{POD} V_{OUT} Behavior with V_{REF} Internally Driven, $t_{POR-REF}$, $R_L =$ Pull-Up

Overvoltage and Undervoltage Detection

To ensure that the device’s output can be trusted, the device contains an overvoltage and undervoltage detection flag. This will Use V_{OUT} and V_{REF} to alert the system when the supply voltage is outside of the operational ranges. If one or both are not desired, the functionality can be individually toggled off.

Undervoltage Detection Voltage Thresholds ($V_{UVD(H/L)}$)

The ACS37600 comes factory programmed with UVD enabled. It is important to note that when powering up the device for the first time after a POR event, the V_{OUT} and V_{REF} will remain high Z until V_{CC} raises above $V_{UVD(H)}$ (seen in Figure 7 as [2]), at which point the V_{OUT} and V_{REF} pin will begin to operate. If UVD is disabled, V_{OUT} and V_{REF} will begin report after V_{CC} raises above $V_{POR(H)}$ (seen in Figure 7 as [1]) under the same conditions.

If V_{CC} drops below $V_{UVD(L)}$ [6] after normal operation, V_{OUT} will go to GND regardless of R_{LOAD} configuration. The V_{OUT} pin will stay at GND until V_{CC} raises above the $V_{UVD(H)}$ [7] or V_{CC} falls below $V_{POR(L)}$ [8]. If V_{CC} rises above $V_{UVD(H)}$ [7] after a UVD event, the outputs will resume operation. If V_{CC} drops below the $V_{POR(L)}$ [8], the device will enter a POR event and reset, V_{OUT} and V_{REF} will switch to high Z if this occurs. During UVD flagging, V_{REF} is high Z, but is always pulled down so will float to GND.

Overvoltage Detection Voltage Thresholds ($V_{OVD(H/L)}$)

When V_{CC} raises above $V_{OVD(H)}$ (seen in Figure 7 as [4]), the output of the V_{REF} and V_{OUT} pins will go high Z, V_{REF} be pulled

to GND, and V_{OUT} will be pulled to either V_{CC} or GND, depending if R_{LOAD} is in a pull-up or pull-down configuration.

Overvoltage/Undervoltage Detection Hysteresis (V_{OVDHys}/V_{UVDHys})

To prevent toggling, there is hysteresis between enable and disable thresholds to reducing nuisance flagging and clears. There is about 1 V and 0.4 V of hysteresis for Overvoltage and Undervoltage respectively. These can be seen represented in Figure 7 and Figure 8 between the relevant thresholds.

Overvoltage and Undervoltage Enable and Disable Time ($t_{OVD(E/D)}$, $t_{UVD(E/D)}$)

The enable time for OVD, $t_{OVD(E)}$, is the time from $V_{OVD(H)}$ [4] to OVD flag [B] in Figure 8. The UVD enable time, $t_{UVD(E)}$, is the time from $V_{UVD(L)}$ [6] to the UVD flag [D] also in Figure 8. The enable flag for both OVD and UVD have a counter to reduce transients faster than 64 μ s from nuisance flags.

If V_{CC} ramps from $>V_{UVD(L)}$ [6] to $<V_{POR(L)}$ [8] (both seen in Figure 7) faster than $t_{UVD(E)} \approx 64 \mu$ s, then the device will not have time to report a UVD event before power off occurs.

The disable time for OVD, $t_{OVD(D)}$, is the time from $V_{OVD(L)}$ [5] to the OVD clear to normal operation [E] in Figure 8. The UVD disable time, $t_{UVD(D)}$, is the time from $V_{UVD(H)}$ [7] to the UVD flag clear to nominal operation [E] also seen in Figure 8. The disable time does not have a counter for either UVD or UVD to release the output and resume reporting as soon as possible.

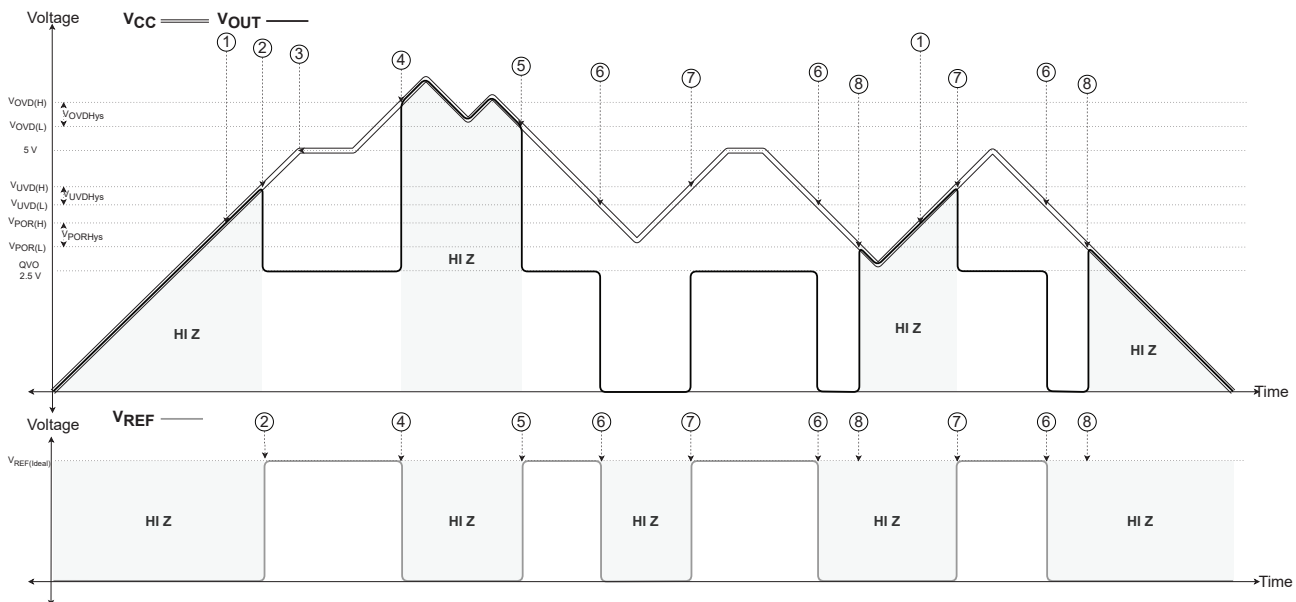


Figure 7: Power States Thresholds with VOUT and VREF Behavior, $R_L =$ Pull Up, UVD enabled

Supply Zener Clamp Voltages

If the voltage applied to the device continues to increase past the overvoltage detection, to extreme levels, there is a point at which Zener diodes will turn on (V_Z). These internal diodes are in place to protect the device from short high voltage or ESD events and should NOT be used as a feature to reduce the voltage on a line. Continued exposure to voltages higher than normal operating voltage $V_{CC(ypical)}$ can weaken or even damage the Zener diodes and potentially lead to damage of the part.

Operating Ranges

These are the environmental operation ranges that affect device performance.

Operational Ambient Temperature Range

This is the temperature range that the operating and electrical characteristics tables are valid unless otherwise stated.

Optimal Ambient Temperature Range

This is the temperature range that the performance characteristics

are valid unless otherwise stated. This is the region the accuracy performance characteristics are factory-programmed for over temperature performance.

Optimal Absolute Field Range

This is the input field range with the tightest linearity limits and is recommended for highest accuracy applications.

Nominal Absolute Field Range

This is the input field range beyond the optimal range that has wider linearity limits than the optimal range but still falls at or below 1% error. This range could be used if linearity is not a concern or is required by the physical application.

Extended Absolute Field Range

This is the input field range beyond the nominal field range to the absolute maximum rated field. The device can still respond in this range, but the linearity will degrade in the region. Linearity is not characterized and does not have limits associated with this field range.

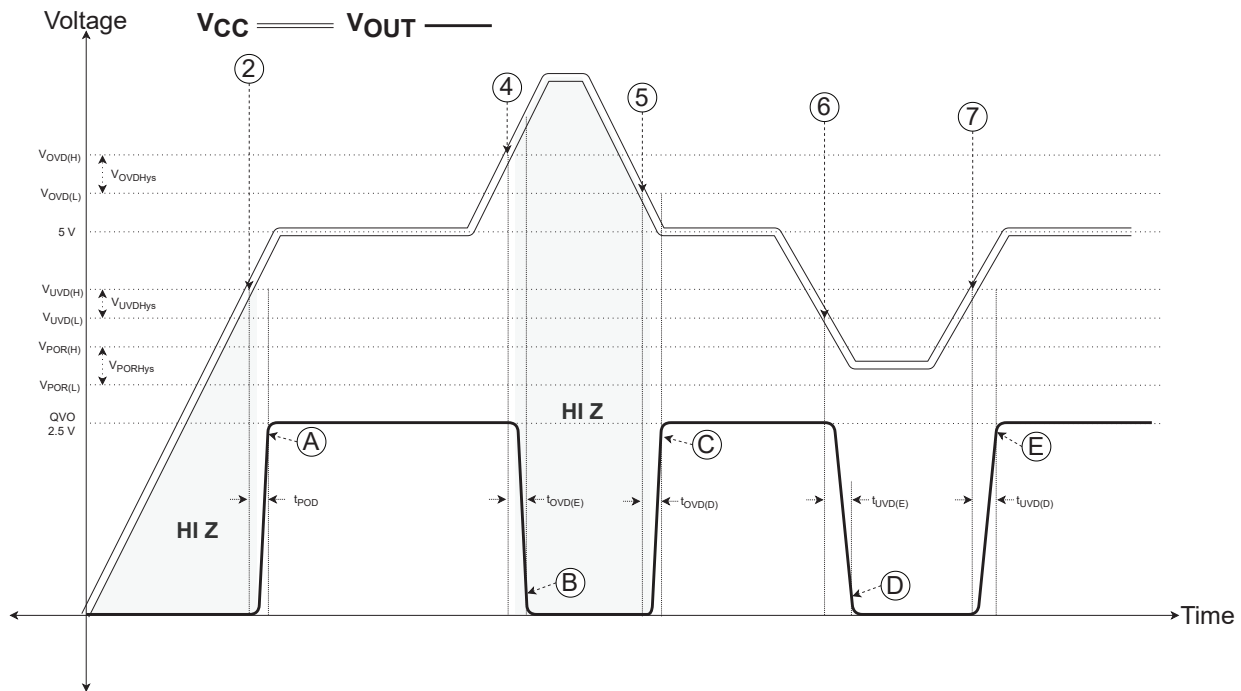


Figure 8: t_{POD} , $t_{OVD(E/D)}$, and $t_{UVD(E/D)}$ behavior with “fast” V_{CC} ramping

Absolute Maximum Ratings

These are the maximum application or environmental condition that the device can be subjected before damage may occur.

Forward and Reverse Supply Voltage

This is the greatest voltage that can be supplied to VCC from GND during programming or transient switching. This voltage should not be used as a DC voltage bias for an extended time.

Forward and Reverse Output Voltage

Forward Output Voltage or V_{FOUT} rating should be read as a voltage of no greater than $V_{CC} + 0.5$ V up to 15 V. This is the greatest voltage that the output can be biased with from GND during programming or transient switching. The Reverse Output Voltage or V_{ROUT} should not drop below -0.5 V during programming or transient switching. These voltages should not be used as a DC voltage bias for an extended time.

Forward and Reverse Reference/Fault Voltage

Forward Reference/Fault Voltage or V_{F-RF} rating should be read as a voltage of no greater than $V_{CC} + 0.5$ V up to 6.5 V. This is the greatest voltage that the output can be biased with from GND during programming or transient switching. The Reverse Output Voltage or V_{R-RF} should not drop below -0.5 V during programming or transient switching. These voltages should not be used as a DC voltage bias for an extended time.

Output Source and Sink Current

This is the maximum current that VOUT can passively sink or source before damage may occur.

Maximum Input Gauss

This is the maximum field that the transducer of the device may respond. This field greater in magnitude than this limit is beyond the known performance of the device.

Additional Functional Descriptions

Uni/Bidirectional Functionality

This device does not have an Allegro-typical unidirectional mode. V_{REF} can be overdriven or programmed to achieve a $V_{OUT(Q)}$ of 0.5 V which will function unidirectionally when the device is bidirectional. Devices in this unidirectional configuration do not extend the fault sensing range, and the effective $V_{OCF(OP)}$ is the same absolute swing from the V_{REF} . If unidirectional functionality is desired the overtemperature performance is only valid while the device is in the factory default `vref_coarse` configuration. This should only be changed for prototyping or applications that do not require overtemperature accuracy.

DEFINITIONS OF OPERATING AND PERFORMANCE CHARACTERISTICS

Quiescent Voltage Output ($V_{OUT(Q)}$)

The quiescent voltage output is defined as the voltage on the output VOUT when zero gauss is applied. $V_{OUT(Q)}$ is determined by two quantities, VREF pin voltage and voff_fine register that adjusts the output channel offset error from the VREF pin.

QVO Temperature Drift ($V_{OUT(Q)_TC}$)

QVO Temperature Drift or $V_{OUT(Q)_TC}$ is defined as the drift of $V_{OUT(Q)}$ from room to hot or room to cold (25°C to 125°C or 25°C to -40°C respectively). Temperature drift is compensated with Allegro's factory trim to remain within the limits across temperature; because of this, only room trimming/programming is needed. This parameter is controlled by the voff_fine register. Programming too close (<32 LSB) to the minimum and maximum values of the voff_fine will affect temperature performance. This compensation is done in increments of $STEP_{V_{OFF}}$ over temperature.

Reference Voltage (V_{REF})

The voltage reference output pin (VREF) is used as the common-mode voltage reference for the output channel V_{OUT} . VREF pin voltage determines the quiescent voltage ($V_{OUT(Q)}$) of the output amplifier, allowing the pin to be driven internally, externally, and overdriven to change the outputs quiescent voltage. This pin can be programmed to operate as an input only, output only, or input/output with the io_vref_mode register. The output voltage can also be adjusted with two internal VREF DACs: vref_coarse which determines the coarse range that vref_fine can adjust, and fine tune. For further information about these registers, refer to Programming Parameters section.

V_{REF} programmable range: 0.35 to 2.65 V

V_{REF} can be overdriven to 0.5 to 2.65 V

Reference Voltage Temperature Drift (V_{VREF_TC})

Reference Voltage Temperature Drift or V_{VREF_TC} is defined as the drift of VREF from room to hot or room to cold (25°C to 125°C or 25°C to -40°C respectively). Only room trimming/programming is needed because temperature drift is compensated with Allegro's factory trim to remain within the limits across temperature. This parameter is controlled by the vref_fine register. Programming too close (<32 LSB) to the minimum and maximum values of the vref_fine will affect temperature performance. This compensation is done in increments of $STEP_{V_{REF}}$ over temperature. V_{VREF_TC} is dependent on the vref_coarse register, V_{VREF_TC} may not meet

datasheet parameters if vref_coarse is changed from factory default.

Reference Voltage Programming Step Size ($STEP_{V_{REF}}$)

Reference Voltage Programming Step Size is defined as the average change in VREF voltage per an LSB change in vref_fine register.

Offset Voltage (V_{OFF})

Offset Voltage or V_{OFF} is defined as $V_{OUT(Q)} - V_{REF}$ and can be seen in Figure 9. The voltage offset between the output and V_{REF} can be adjusted with the voff_fine register. For best accuracy, verify the device's actual step size and result when trimming.

Offset Error Temperature Drift (V_{OFF_TC})

Offset Error Temperature Drift or V_{OFF_TC} is defined as the drift of $V_{OUT(Q)} - V_{REF}$ from room to hot or room to cold (25°C to 125°C or 25°C to -40°C respectively). Refer to QVO Temperature Drift for further information.

Offset Voltage Programming Step Size ($STEP_{V_{OFF}}$)

Offset Voltage Programming Step Size is defined as the average of change in $V_{OUT(Q)} - V_{REF}$ voltage per an LSB change in voff_fine register. For best accuracy, verify the devices actual step size and result when trimming.

Output Saturation Voltage ($V_{SAT(HIGH/LOW)}$)

Output Saturation Voltage or V_{SAT} is defined as the voltage that output no longer changes when the magnitude of the magnetic field is increased. $V_{SAT(HIGH)}$ is the highest voltage the output can drive to, while $V_{SAT(LOW)}$ is the lowest. This can be seen in Figure 21. Note that changing the sensitivity does not change the V_{SAT} points.

Sensitivity (Sens)

Sensitivity or Sens is the output swing in the presence of a magnetic field, perpendicular to and out of the top surface of the package face (refer to polarity section and Figure 12). This magnetic field moves the output voltage away from its $V_{OUT(Q)}$ and towards the supply voltage rails. The magnitude and direction of the output voltage swing is proportional by Sens to the magnitude and direction of the applied magnetic field. The Sens of the device is calculated slightly differently for “unidirectional” (positive or negative V_{OOR}) and “bidirectional” (positive and negative V_{OOR}) parts.

Bidirectional parts have sensitivity defined as follows:

$$Sens = \frac{V_{OUT(B1)} - V_{OUT(B2)}}{B_1 - B_2}$$

Unidirectional parts have sensitivity defined as follows:

$$Sens = \frac{V_{OUT(BPOS)} - V_{OUT(Q)}}{BPOS}$$

where BPOS and BNEG are two magnetic fields with opposite polarities, and $V_{OUT(BPOS)}$ and $V_{OUT(BNEG)}$ are the voltages recorded of the device with the applied fields. $V_{OUT(Q)}$ is the actual measured offset voltage, not calculated. The fine sensitivity of device can be programmed and controlled by the sns_fine register. The effect of changing sns_fine can be seen in Figure 10 in the right most breakout frame.

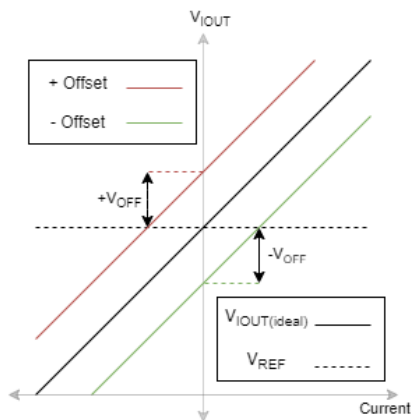


Figure 9: V_{OFF} , V_{REF} , $V_{OUT(Q)}$. Numbers are exaggerations and not representative of device performance

Sensitivity Programming Range (Sens_{PR})

Sensitivity Programming Range or Sens_{PR} is the sensitivity programming range of the device with sns_fine register. The sns_fine register scales with the sns_coarse register to determine the Sens range of a given device; refer to Device Performance Characteristics section for specific devices. Sens can be programmed from factory value within the sensitivity range limits: Sens_{PR(min)} and Sens_{PR(max)}. Exceeding the specified Sens_{PR} can cause the device to operate outside datasheet limits and changes. For further information about these registers, refer to Programming Parameters.

Sensitivity Temperature Drift (E_{SENS_TC})

Sensitivity Temperature Drift or E_{SENS_TC} is defined as the drift of Sens from room to hot or room to cold (25°C to 125°C or 25°C to -40°C respectively). Only room trimming/programming is needed because temperature drift is compensated with Allegro’s factory trim to remain within limits across temperature. This parameter is controlled by the sns_fine register. Programming too close (<32 LSB) to STEP_{SENS} min and max values will affect temperature performance. This compensation is done in increments of STEP_{SENS} over temperature and because STEP_{SENS} is dependent on sns_coarse , the E_{SENS_TC} limit is only valid for factory-programmed sns_coarse .

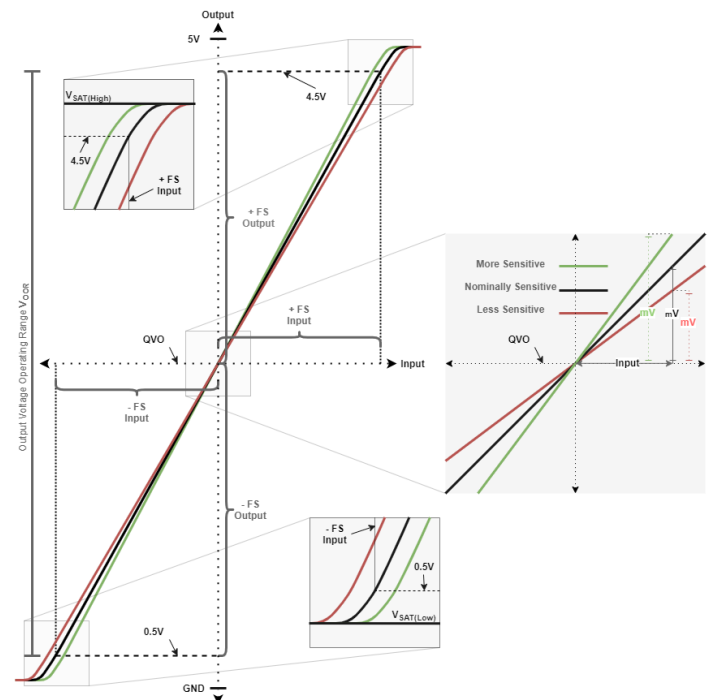


Figure 10: V_{SAT} , Sensitivity with $G_{OCF(fact)}$ and $V_{OCF(fact)}$

Average Sensitivity Step Size ($STEP_{SENS}$)

Average Sensitivity Step Size or $STEP_{SENS}$ is defined as the average change in the magnetic sensitivity of the device with an LSB change to the sns_fine register. $STEP_{SENS}$ is sns_coarse dependent; as such, device $STEP_{SENS}$ will not be equal for the different sns_coarse settings.

Polarity

Polarity can be changed using the gc_pol register, inverting the output response to a magnetic field. If this is changed from the factory default, then E_{SENS_TC} , V_{OFF_TC} , V_{REF_TC} may not meet datasheet limits. The default fault polarity is a positive output swing in the presence of a magnetic field, perpendicular and out of the top surface of the package face as seen in Figure 12.

Nonlinearity (E_{LIN})

As the amount of field applied to the part changes, the sensitivity of the device can also change slightly. This is referred to as linearity error or E_{LIN} , and an exaggerated example can be seen in Figure 13. Consider two magnetic fields, $B_1(1/2 FS)$ and $B_2(FS)$. Ideally, the sensitivity of the device is the same for both fields; everything else equal. Linearity Error is calculated as the percent change in sensitivity from one field to another. Error is calculated separately for positive ($E_{LIN(+)}$) and negative ($E_{LIN(-)}$) magnetic fields, and the percent errors are defined as:

$$E_{LIN(\pm)} = [1 - Sens_{B_{2\pm}} / (Sens_{B_{1\pm}})] \times 100\%$$

where:

$$Sens_{B_{x+}} = (V_{OUTB_{x+}} - QVO) / B_{x+}$$

and

$$Sens_{B_{x-}} = (V_{OUTB_{x-}} - QVO) / B_{x-}$$

B_x are positive and negative magnetic fields, such that $|B_{+2}| = 2 \times |B_{+1}|$ and $|B_{-2}| = 2 \times |B_{-1}| \times E_{LIN} = \max(E_{LIN(+)}, E_{LIN(-)})$.

Assumed fields are within the part's response range.

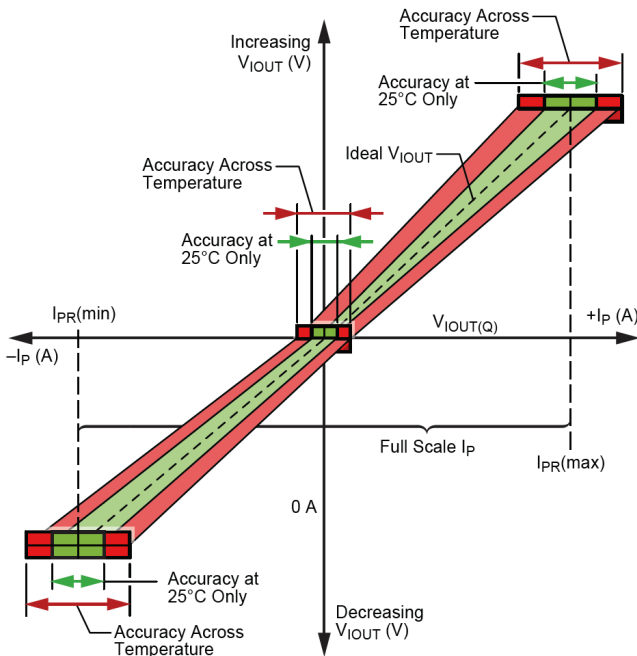


Figure 11: Output Accuracy Pocket for Room and Across Temperature

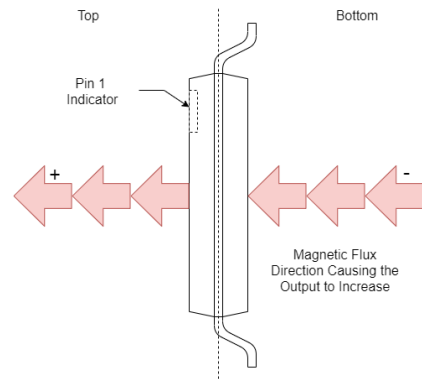


Figure 12: LU Package Flux and Output Directionality

Total Output Error

Total Output Error is the difference between the field measurement from the sensor IC and the actual field (B), relative to the actual field. This is equivalent to the difference between the ideal output voltage and the actual output voltage, divided by the ideal sensitivity, relative to the field applied to the device:

$$E_{TOT(\pm)} = (1 - V_{OUT_Actual(B\pm)} / V_{OUT_Ideal(B\pm)})$$

where $V_{OUT_Actual(B\pm)} = \pm B \times Sens_{Actual} + V_{OUT(Q)_Actual}$

and $V_{OUT_Ideal(B\pm)} = \pm B \times Sens_{Ideal} + V_{OUT(Q)_Ideal}$

Total Output Error incorporates all sources of error and is a function of magnetic field B. At relatively high fields, Total Output Error will be mostly due to sensitivity error, and at relatively low fields, Total Output Error will be mostly due to Offset Voltage (V_{OE}). In fact, at $B = 0$, Total Output Error approaches infinity due to the offset. An example of total error at FS can be seen in Figure 13.

Note: Total Output Error goes to infinity as the amount of applied field approaches zero gauss.

Symmetry Error (E_{SYM})

Symmetry Error is the difference between the sensitivity for two applied magnetic fields with equal magnitude and opposite polarity. Symmetry Error, E_{SYM} (%) is defined as:

$$E_{SYM} = (1 - Sens_{B+} / Sens_{B-}) \times 100\%$$

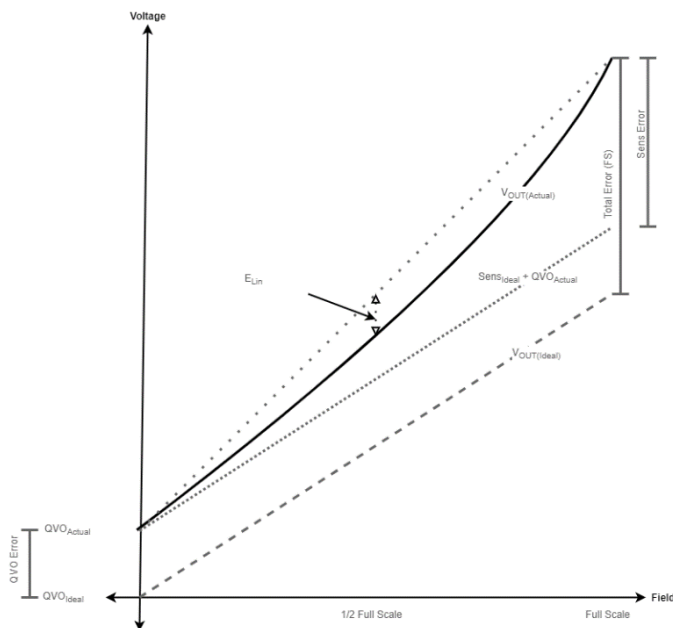


Figure 13: Accuracy Error

where $Sens_{B+}$ and $Sens_{B-}$ are measured with magnetic field B such that $B_+ = |-B_-|$. This can be seen in Figure 14.

Power Supply Offset Error (V_{PS})

Power Supply Offset Error or V_{PS} is defined at the offset error in mV between V_{CC} at 5 V to 4.5 V and 5 V to 5.5 V.

Offset Power Supply Rejection Ratio (PSRR_O)

Offset Power Supply Rejection Ratio or $PSRR_O$ is defined as $20 \times \log$ of the ratio of the change of QVO in volts over a ± 100 mV variable AC V_{CC} centered at 5 V reported as dB in a specified frequency range. This is an AC version of the V_{PS} parameter. The equation can be seen below:

$$PSRR_O = 20 \times \log(\Delta QVO / \Delta V_{CC})$$

Power Supply Sensitivity Error (E_{PS})

Power Supply Sensitivity Error or EPS is defined as the % sensitivity error measured between V_{CC} at 5 V to 4.5 V and 5 V to 5.5 V.

Sensitivity Power Supply Rejection Ratio (PSRR_S)

Sensitivity Power Supply Rejection Ratio or $PSRR_S$ is defined as $20 \log$ of the ratio of the % change the sensitivity over the % change in V_{CC} (± 100 mV variable AC V_{CC} centered at 5 V) reported as dB in a specified frequency range. This is the AC version of the EPS parameter. The equation is as follows:

$$PSRR_S = 20 \log(\Delta \% Sens / \Delta \% V_{CC})$$

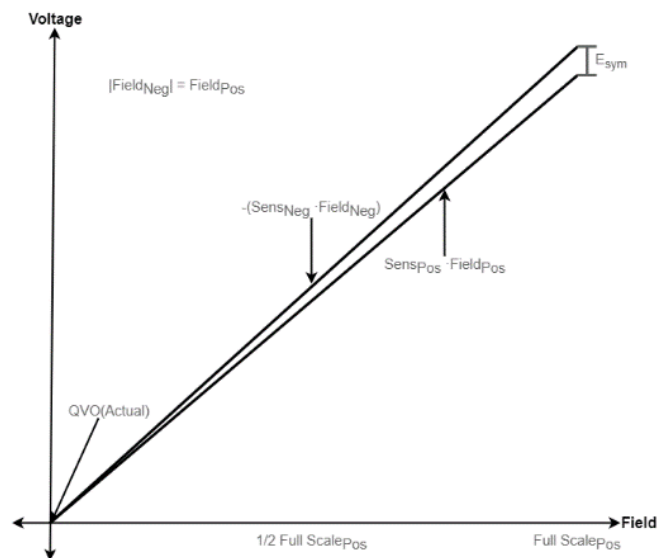


Figure 14: Symmetry Error with Absolute Outputs

Fault Behavior

OVERCURRENT FAULT (OCF)

As the output swings because of a sensed field, the Overcurrent Fault or OCF pin will trigger with an active low flag if the sensed field exceeds its programmed threshold. This is internally compared via voltages with the flag tripping symmetrically for the positive and negative OCF operating point. This trip point, like V_{OUT} , is centered around V_{REF} , so if V_{REF} changes, the trip point remains the same in terms of output swing from V_{REF} .

The implementation for the OCF circuitry is accurate over temperature and does not require further temperature compensation, as it is dependent on the Sens and V_{OFF} parameters that are already trimmed flat over temperature.

OVERCURRENT FAULT OPERATING POINT ($V_{OCF(OP)}$)

Overcurrent Fault Operating Point has two definitions, one for input and one for output-referred thresholds related by the device’s actual sensitivity. The Output Referred OCF Operating Point or $V_{OCF(OP)}$ is defined as the equivalent output in mV to which the OCF flag corresponds, while the Input Referred OCF Operating Point or $G_{OCF(OP)}$ (seen in Figure 15 as [9]) is the field equivalent to the $V_{OCF(OP)}$. Both $V_{OCF(OP)}$ and $G_{OCF(OP)}$ give the same functional trip point. The OCF threshold is programmed by the `ocf_thr` register. The factory $V_{OCF(OP)}$, or $V_{OCF(fact)}$, is 2000 mV swing on the output. The functional range is 0.5 V to 5 V swing from V_{REF} for the $V_{OCF(OP)}$.

$$V_{OCF(OP)} = (\text{Field} \times \text{Sens}_{ACTUAL}) \times 1000 \text{ (mV)}$$

$$G_{OCF(OP)} = V_{OCF(OP)} / \text{Sens}_{ACTUAL}$$

The minimum and maximum codes for `ocf_thr` registers do not correspond to the minimum and maximum OCF functional range.

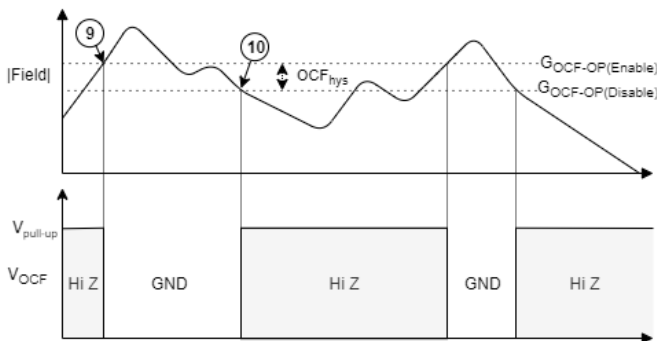


Figure 15: Fault Thresholds and Functional OCF Pin States

Refer to the programming section for further information on `ocf_thr` programming.

OVERCURRENT FAULT HYSTERESIS (V_{OCF_HYS})

Overcurrent Fault Hysteresis or V_{OCF_HYS} is defined as both output-referred or input-referred magnitudes from the OCF flag assertion threshold (seen in Figure 16 as [9]) to the OCF clear threshold (seen in Figure 16 as [10]). The ACS37600 comes standard with an V_{OCF_HYS} of 120 mV equivalent output swing. If a larger hysteresis is desired, this can be doubled to 240 mV by setting `ocf_hys = 1`.

OVERCURRENT FAULT STEP SIZE ($STEP_{OCF}$)

The Overcurrent Fault Step Size or $STEP_{OCF}$ is defined as the average change in $V_{OCF(OP)}$ or $G_{OCF(OP)}$ with an LSB change to the `ocf_thr` register.

OVERCURRENT FAULT FACTORY ERROR (V_{OCF_EFAC})

Overcurrent Fault Factory Error or V_{OCF_EFAC} is the error, in mV, of the actual OCF trip point and the factory target of 2 V swing on the output.

OVERCURRENT FAULT REPROGRAMMED ERROR (V_{OCF_ERR})

Overcurrent Fault Reprogrammed Error or V_{OCF_ERR} is the error in mV of the actual OCF trip point and the reprogrammed target.

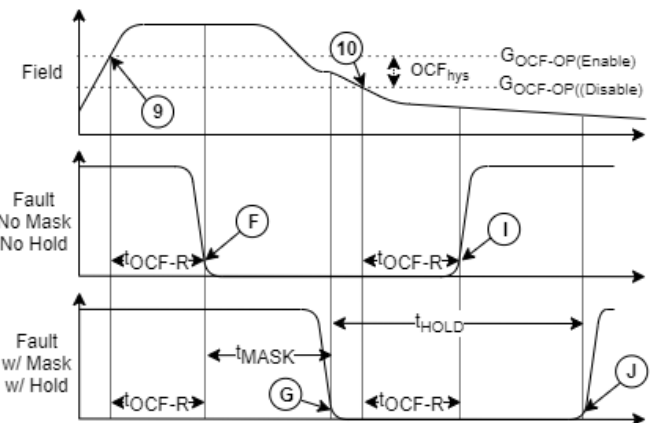


Figure 16: General Fault Timing

OVERCURRENT RESPONSE TIME (t_{OCF})

Overcurrent Response Time or t_{OCF} is defined as the time from when the input reaches the operating point [9] until the device’s OCF pin falls below V_{OCF_ON} [G]. If the OCF Mask is disabled, t_{OCF} is equal to t_{OCF-R} seen as the time from [9] until [F].

OVERCURRENT REACTION TIME (t_{OCF-R})

Overcurrent Reaction Time or t_{OCF-R} is defined as the time from the field input rising above $G_{OCF(OP)}$ at point [9] until the OCF pin reaches V_{OCF_ON} at point [F] with the OCF mask disable. This is also the time required for the device to recognize and clear the fault, seen as the time between [10] until [I]. This can be seen in Figure 16.

OVERCURRENT FAULT HOLD TIME ($t_{OCF-HOLD}$)

Overcurrent Fault Hold Time or $t_{OCF-HOLD}$ is defined as the minimum time the OCF flag will be asserted after a sufficient OCF event. After the hold time has been reached, OCF will release if the OCF condition has ended (seen in Figure 16, [G] until [J]) or persist if the OCF condition is still present (seen in Figure 17, [F] until [K]). Factory default is 0 ms and can be changed in the ocf_mask register.

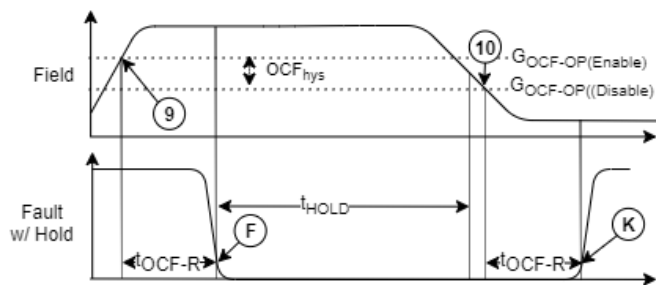


Figure 17: Fault Hold with Clear Fault After Hold Time

OVERCURRENT FAULT MASK TIME ($t_{OCF-MASK}$)

Overcurrent Fault Mask Time or $t_{OCF-MASK}$ is defined as the additional amount of time the OCF must be present beyond t_{OCF-R} (seen in Figure 16, [F] until [G]). To prevent nuisance tripping, a programmable ocf_mask time is used. If an OCF occurs but does not persist beyond $t_{OCF} + t_{OCF-MASK}$, it is not reported by the device (seen in Figure 18). This prevents short transient spikes from causing erroneous OCF flagging. In the event where transient error reporting is desired, the ocf_mask can be disabled by setting the register to 0. Factory default setting is 1 in the ocf_mask register corresponding to $t_{OCF-MASK} = 0.5 \mu s$.

OCF PERSIST

The ACS37600 has a fault persist option that will maintain the OCF flag if a flag occurred until a POR event. This is disabled as factory default but can be toggled on by setting the $ocf_persist$ register to 1.

OCF DISABLE

The ACS37600 also contains an OCF disable bit ocf_dis that will disable the OCF pin functionality. When this bit is set to 1, the OCF pin will remain in high Z. Factory default is 0, enabling the OCF functionality.

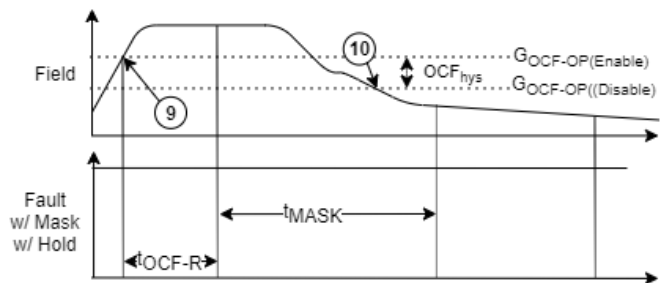


Figure 18: Fault Condition Clearing Before Mask Time Is Reached

Dynamic Response Parameters

The descriptions in this section assume: temperature = 25°C, and output loads are within specifications provided. The step applied is an input step that corresponds to 1 V excursion on the output, unless otherwise stated.

PROPAGATION DELAY ($t_{REACTION}$)

The time interval between a) when the sensed field reaches 10% of its stable value, and b) when the sensor output reaches 10% of its stable value for a step input. See Figure 19 for visual description of parameter.

RISE TIME (t_{RISE})

The time interval between a) when the sensor reaches 10% of its stable value, and b) when it reaches 90% of the stable value for a step input. See Figure 19 for visual description of parameter.

RESPONSE TIME ($t_{RESPONSE}$)

The time interval between a) when the sensed field reaches 90% of its stable value, and b) when the sensor output reaches 90% of its stable value. See Figure 19 for visual description of parameter.

OVERSHOOT (V_{OS})

The amount, in percent of step size, the output voltage (V_{OUT}) rises past the steady-state output voltage. The equation used to calculate this is shown in Figure 20; also see Figure 20 for description of parameters in the equation.

SETTLING TIME (t_{SETTLE})

The amount of time it takes for the output voltage (V_{OUT}) to settle to between $\pm 3\%$ of the steady-state output. See Figure 20 for description of parameter.

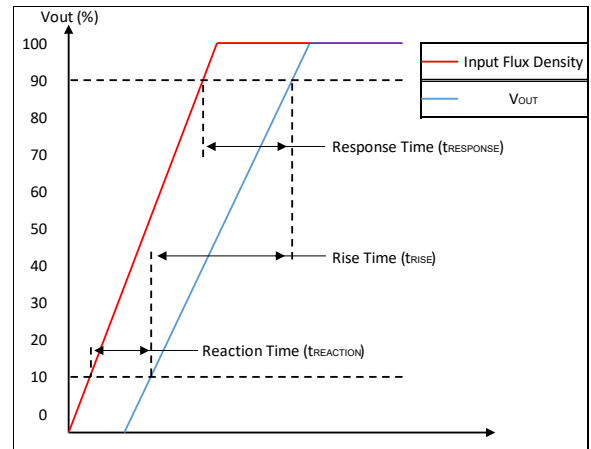


Figure 19: Dynamic Response Parameters

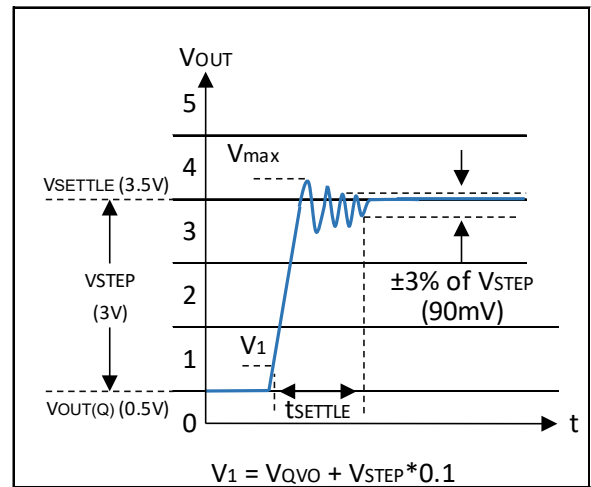


Figure 20: Overshoot and Settling Time (3 V step is shown)

Temperature Compensation

To remove the effects temperature has on the performance of the ACS37600, an internal temperature sensor is integrated. This sensor, along with compensation algorithms, help to standardize device performance over the full range of operating temperatures.

TEMPERATURE COMPENSATION UPDATE RATE (t_{UR})

After Power-On Delay (t_{POD}) elapses, t_{UR} is also required to maintain a valid temperature compensated output. Further information in temperature compensation section.

GAIN TEMPERATURE COEFFICIENT ($SENS_{SLOPE}$)

Sensitivity Temperature Coefficient or $SENS_{SLOPE}$ is a parameter that allows the user to increase or decrease the sensitivity linearly overtemperature. This allows for temp compensation of other elements in the application system i.e. magnetic cores.

GAIN TEMPERATURE COEFFICIENT STEP SIZE ($STEP_{SENS_SLOPE}$)

Sensitivity Temperature Coefficient Step Size or $STEP_{SENS_SLOPE}$ is defined as the average change in % Sens/°C per LSB change in the gain_{tc} register.

Package Stress Compensation

Sensitivity drift due to package hysteresis is internally compensated to reduce the effects of temperature and lifetime drift error. Package stress and relaxation can cause the device sensitivity at $T_A = 25^\circ\text{C}$ to change during and after temperature cycling and over life stress.

APPLICATION AND THEORY

Parameter Trim Algorithm

For best results, a trim flow of Sens, V_{REF} , and $V_{OFF}/V_{OUT(Q)}$ is recommended, because sensitivity and V_{REF} will affect $V_{OFF}/V_{OUT(Q)}$.

SENS:

1. Knowing the actual sensitivity and target sensitivity, take the difference:

$$Sens_{STEP} = Sens_{Target} - Sens_{Actual}$$
2. Using the calculated $Sens_{STEP}$, divide it by the $STEP_{Sens}$ to determine the number of codes to change the sns_fine register.
 - A. If more accuracy is required or desired, measuring the device’s actual $STEP_{Sens}$ is required. This should be done if an iterative process is used.

$$\# \text{ sens codes} = \text{round}(Sens_{STEP}/STEP_{Sens})$$
3. Read the sns_fine register and add the # sens codes to the register value. Write the result back into sns_fine.
4. Measure the new sensitivity. If it is not within $0.5 \times STEP_{Sens}$ or within desired error, repeat 1-4; be sure to measure $STEP_{Sens}$ for best accuracy.

VREF:

5. Knowing the actual V_{REF} and target V_{REF} , take the difference:

$$V_{REF-STEP} = V_{REF-Target} - V_{REF-Actual}$$
6. Using the calculated $V_{REF-STEP}$, divide it by $STEP_{VREF}$ to determine the number of codes to change for the vref_fine register.

A. If more accuracy is required or desired, measuring the devices actual $STEP_{VREF}$ is required. This should be done if an iterative process is being used.

$$\# VREF \text{ codes} = \text{round}(V_{REF-STEP} / STEP_{VREF})$$

7. Read the vref_fine register and add the # V_{REF} codes to the register value. Write the result back into vref_fine.
8. Measure the new V_{REF} . If it is not within $0.5 \times STEP_{VREF}$ or within desired error, repeat 5-8; be sure to measure $STEP_{VREF}$ for best accuracy.

$V_{OUT(Q)}$:

9. Knowing the actual V_{OFF} and target V_{OFF} , take the difference:

$$V_{OFF-STEP} = V_{OFF-Target} - V_{OFF-Actual}$$
10. Using the calculated $V_{OFF-STEP}$, divide it by the $STEP_{VOFF}$ to determine the number of codes to change the voff_fine register.
 - A. If more accuracy is required or desired, measuring the device’s actual $STEP_{VOFF}$ is required. This should be done if an iterative process is used.

$$\# V_{OFF} \text{ codes} = \text{round}(V_{OFF-STEP} / STEP_{VOFF})$$
11. Read the voff_fine register and add the # V_{OFF} codes to the register value. Write the result back into voff_fine.
12. Measure the new V_{OFF} . If it is not within $0.5 \times STEP_{VOFF}$ or within desired error, repeat 9-12; be sure to measure $STEP_{VREF}$ for best accuracy.

OCF Pulled Up to Different Power Domain

The OCF pin was designed to be compatible with power domains that are not the VCC and GND networks. Because the output is not a push or pull output but an active low, this allows it to be pulled up to a different voltage. The OCF must be pulled up to a voltage no greater than the absolute maximum rating of the OCF pin and supplied from the same GND as the device. A common example of this is attaching this pin to a 3.3 V network while the device is being supplied by 5 V.

Overdriving V_{REF} : Dynamic Output and Accelerated t_{POD}

The VREF pin can be overdriven while in the factory `vref_io_mode`. This can be used to dynamically change the effective range of field the output is mapped to, as well as overdriving the VREF pin during startup POR to reduce the t_{POD} time. To increase V_{REF} voltage, the pin must be supplied with a source that can maintain the desired higher voltage level while being capable of supplying a current greater than I_{SINK_REF} . To decrease the voltage, the pin must be supplied with a sink that can maintain the desired lower voltage while being able to sink I_{SOURCE_REF} .

DYNAMIC OUTPUT

Range changing can be done by adjusting the VREF pin by overdriving the pin voltage. For an example of this in use, consider the factory default fault at 2 V swing from V_{REF} and during normal operation. The expected operation is going to fall reasonably within ± 2 V swing, but there are expected excursions that are +3 V that are of interest. If there is an excursion of 3 V from V_{REF} , which is beyond $2 \text{ V } V_{OCF(\text{fact})}$, the OCF pin will trigger and the direction is known because $V_{OUT} > V_{REF}$. V_{REF} can be overdriven in the opposite direction down 2 V from 2.5 V to 0.5 V, allowing for the output report a signal that is otherwise outside its capabilities. In addition, when this input starts to fall and reduces below 1.88 V from V_{REF} , the OCF will release and the VREF pin can now be let go or driven back to 2.5 V. This effectively allows for a dynamic output operation range, allowing for better accuracy during low current needs while maintaining the ability to capture signals that would otherwise be out of range for the device with this accuracy requirements.

ACCELERATED t_{POD}

When the ACS37600 powers up, the power-on time can be limited by the low internal drive strength of the VREF pin. One way to reduce this is by overdriving the VREF pin during POR to remove the VREF limited drive strength from slowing t_{POD} . This allows t_{POD} to depend on t_{POR_OUT} instead of t_{POR_REF} which is twice as slow.

Manchester Communication and Device Features

USING THE ANALOG_LOCK BIT

The `analog_lock` configuration is located in register 0x0F bit 24 and controls whether an OVD event is required for read/write communications after the initial unlock. With this bit set to the factory default of 0, OVD is not required to send a read or write command. With this bit set to 1, OVD is required for every read/write. This bit does not change the unlock procedure, but only communication after unlock.

USING THE UNLOCK_CODE BIT

The `unlock_code` register is located in register 0x0F bit 25 and sets the requirement for an additional unlock code to unlock and communicate with the device. With this bit set to the factory default of 0, only one unlock code is required to unlock the part. With this bit set to 1, two codes must be used in succession in order to successfully unlock the part for communication. This bit does not affect communication after unlock.

HOW OVD CAN BE USED WITH PROGRAMMING

Using OVD during read/write removes the need for the MCU to overdrive the Vref pin for successful communication. Using the OVD flag to make Vref Hi-Z during communication can be used with `analog_lock = 1` or 0, but only when `ovd_dis = 0` which is the factory default.

PROGRAMMING PARAMETERS

Fine Tuning Sensitivity, Reference and Quiescent Voltage

Sensitivity and V_{OFF} can be adjusted by programming `sns_fine` and `voff_fine` bits, as illustrated below. Customers should not program sensitivity or $V_{OUT(Q)}$ beyond the maximum or minimum programming ranges specified in the Operating Characteristics table. Exceeding the specified limits will cause sensitivity and $V_{OUT(Q)}$ drift through temperature range, V_{REF_TC} , V_{OFF_TC} , and E_{SENS_TC} , to deteriorate beyond the specified values.

Programming sensitivity might cause a small change in $V_{OUT(Q)}$ / V_{OFF} ; as a result, Allegro recommends programming sensitivity first, then programming $V_{OUT(Q)}$ / V_{OFF} .

FINE SENSITIVITY (`sns_fine`)

Device sensitivity can be programmed by adjusting the `sns_fine` register. This register is a 2's complement number, meaning that the sensitivity can be programmed up or down from its nominal value at `sns_fine` = 0. As part of final testing, the `sns_fine` register is set by Allegro in the trimming process, so devices may already contain a non-zero `sns_fine` value. Programming too close (<32 LSB) to $STEP_{SENS}$ minimum and maximum values will affect temperature performance. It is recommended that the user keep the codes from 0-223 and 288-511.

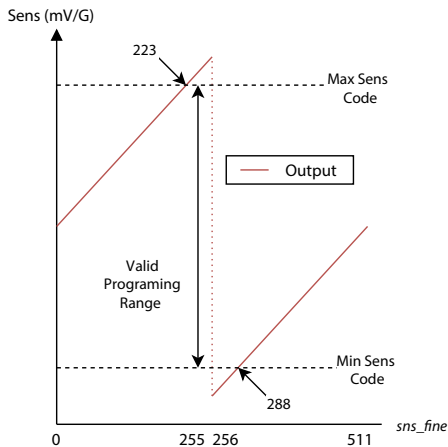


Figure 21: Sensitivity Register/DAC Transfer Curve

FINE REFERENCE VOLTAGE (`vref_fine`)

The reference voltage (V_{REF}) is determined by one of two stimuli. The value can be programmed internally, in which case the `vref_fine` and `vref_coarse` (see the Coarse Reference Voltage) settings determine which voltage the device outputs on the V_{REF} pin. The second method of setting the reference voltage is

by externally overdriving the V_{REF} pin to the desired voltage. In this case, the internal settings do not matter, as the reference is the physical voltage on the pin, not internal settings. Programming too close (<32 LSB) to the $STEP_{SENS}$ minimum and maximum values will affect temperature performance. It is recommended that the user keeps the codes from 0-223 and 288-511.

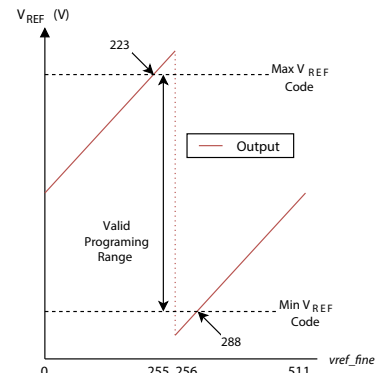


Figure 22: V_{REF} Register/DAC Transfer Curve

QUIESCENT OR OFFSET VOLTAGE ($V_{OUT(Q)}$, V_{OFF})

The quiescent voltage $V_{OUT(Q)}$ is defined as the output voltage when zero gauss is present on the device's sensing element. In application, this is determined by the reference voltage (V_{REF}) and any offset voltage from the reference (V_{OFF}). To eliminate this offset, `voff_fine` can be adjusted to remove any error. This 2's complement number allows $V_{OUT(Q)}$ to be moved up and down without affecting V_{REF} to remove V_{OFF} . At final test, this value is set to trim for the chosen V_{REF} and may need to be adjusted if V_{REF} is changed or overdriven. Programming too close (<32 LSB) to $STEP_{SENS}$ minimum and maximum values will affect temperature performance. It is recommended that the user keep the codes from 0-223 and 288-511.

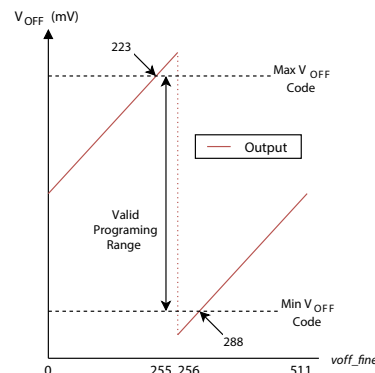


Figure 23: V_{OFF} Register/DAC Transfer Curve

Overcurrent Fault

OCF OPERATING POINT THRESHOLD (ocf_thr)

The OCF(OP) threshold is controlled by the ocf_thr register. This register is programmed by the factory to a value that corresponds to 2 V excursion from V_{REF} on the output. If programming OCF(OP) to a different threshold is desired, there are two ways to calculate the code for the desired OCF(OP). If programming the fault such that $0.5\text{ V} \leq |V_{OCF(OP)}| \leq 3.5\text{ V}$, the fault error should be within the V_{OCF_EFAC} limits. If programming $V_{OCF(OP)} \geq 3.5\text{ V}$ swing from V_{REF} , the INL error of the ocf_thr DAC will introduce error and the fault error should perform within the V_{OCF_ERR} limits. For best accuracy, OCF(OP) should be validated for each device after trimming.

For the first method, take the difference between the current trip point and the desired trip point. Figure 24 shows two equations that can be used to calculate the desired ocf_thr.

The second method attempts to mitigate average DAC INL error. The equation in Figure 25 will give the desired average INL compensated ocf_thr code. Note that this only compensates for

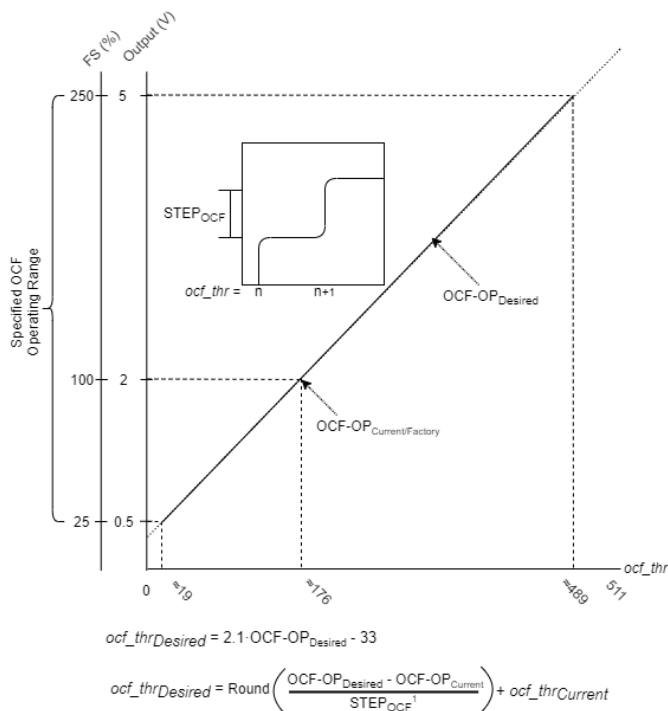


Figure 24: Overcurrent Fault Threshold DAC Transfer Function in Full Scale (FS) and Corresponding Output Swing from V_{REF}

the average INL error measured in production. Measuring after programming and reprogramming as needed is the most accurate way to mitigate the device specific INL error. A visual representation and equations of the INL compensation and impact on the OCF(OP) are shown in Figure 25.

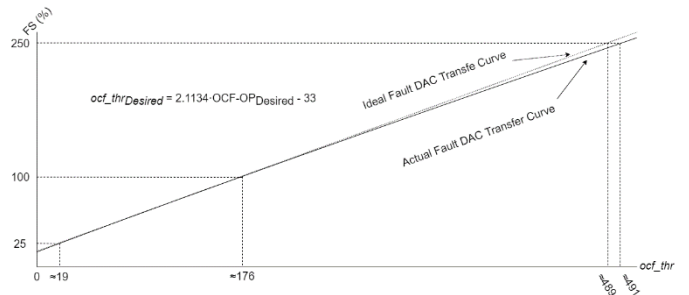


Figure 25: OCF DAC Nonidealities, INL Error

OCF MASK TIME (ocf_mask)

To avoid nuisance OCF tripping from transient signals, the OCF block contains a mask feature that requires the OCF condition to be at or beyond OCF(OP) for a programmable amount of time beyond the reaction time, t_{OCF-R} . This device comes with a factory default $ocf_mask = 1$ for $t_{OCF-MASK} = 0.5\ \mu s$. If a different value is desired, refer to the table below for the appropriate ocf_mask setting.

ocf_mask (code)	$t_{OCF-MASK}$ (μs)
0	0
1 (factory default)	0.5
2	1
3	2
4	2.5
5	3
6	3.5

OCF HOLD (ocf_hold)

In some applications, the fault pin is not constantly monitored, but it is still important to catch fault conditions. The OCF Hold sets the minimum time that the fault flag can be asserted, so slower systems can catch the fault. This OCF hold is controlled by the ocf_hold register. The factory default is ocf_hold = 0, with a corresponding t_{OCF-HOLD} of 0 ms. To change to a different setting, refer to the table below for available options.

ocf_hold (code)	t _{OCF-HOLD} (ms)
0 (factory default)	0
1	0.1
2	0.25
3	0.5
4	1
5	2
6	3.5
7	5

OCF HYSTERESIS DOUBLE (ocf_hys)

This device has some hysteresis between the OCF(OP)_{enable} and the OCF(OP)_{disable} thresholds to avoid nuisance toggling. If toggling is still occurring, this hysteresis can be doubled by setting ocf_hys = 1. The factory default is ocf_hys = 0 which is equivalent to 120 mV on the output.

ocf_hys ocf_hys	V _{OCF_Hyst}
	output referred (mV)
0 (factory default)	120
1	240

VREF INPUT/OUTPUT OPERATIONAL MODES (io_ref_mode)

The VREF pin has two different operational modes. The VREF pin factory default is input/output mode; this means that the

output is internally driving but is configured to be overdriven. If it is desired to change this to either a dedicated input or dedicated output, the value of io_ref_mode can be changed to the corresponding value below.

io_ref_mode(code)	Outcome
0	Input only
1	Input only
2	Output only
3 (factory default)	Input/Output

ECONOMY MODE (vout_eco_mode)

This device has an aggressive drive strength at the cost of current consumption during normal operation. If this is not desired, then the vout_eco_mode register can be set to 1. This will cut the drive strength and quiescent current down reducing the overall current consumption.

vout_eco_mode(code)	Name	Max. Output Drive
0 (factory default)	Turbo	15 mA
1	Economy	7.5 mA

Additional Core / Temperature Compensation

SENSITIVITY TEMPERATURE COMPENSATION SLOPE (gain_tc)

This device has a user-programmable temperature sensitivity slope DAC, gain_tc. This 6-bit 2's complementary DAC linearly alters the device's gain over temperature, allowing the user to compensate for other systemic temperature drifts like a magnetic core. The gain_tc register linearly changes the existing sensitivity slope over temperature centered at 25°C; this can be seen in Figure 26. To calculate the code needed to obtain the desired gain slope, determine the Gain_{TC(T)}, which is the % change from room sensitivity at temperature T and follow the equation below.

$$\text{gain_tc} = \text{SENS}_{\text{SLOPE}(T)} / [(T - 25) \times 2.5 \times 10^{-5}]$$

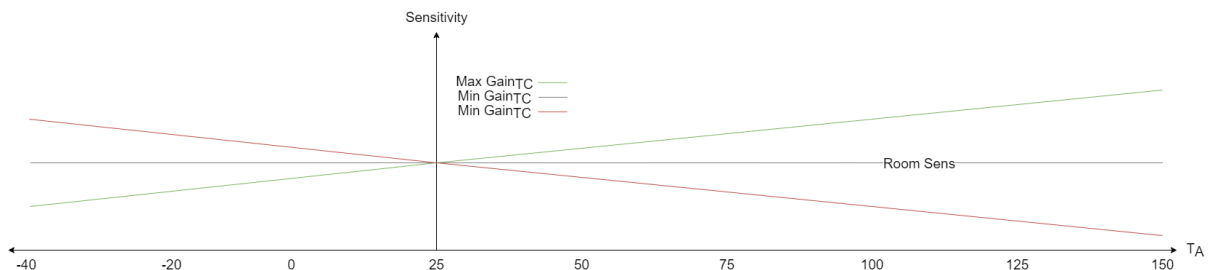


Figure 26: gain_tc and Sensitivity Over Temperature Performance

Note: When calculating E_{SENS_TC} , use the expected $Sens_{(T)}$ that can be calculated with the equations for $Sens_{(T)}$. The hot and cold ranges are not symmetric and the $Gain_{TC}$ for hot and cold will not match at the extreme temperatures.

$$Sens_{(T)} = Sens_{(25^{\circ}C)} \times [1 + SENS_{SLOPE(T)}]$$

$$SENS_{SLOPE(T)} = (T - 25) \times gain_tc \times 2.6 \times 10^{-5}$$

Registers Useful for Prototyping

The registers that are contained in this section are useful for prototyping and room applications. Changing the values of these registers from the factory default may affect the over temperature performance.

COARSE SENSITIVITY (sns_coarse)

Each ACS37600 is programmed to a different coarse sensitivity setting. Devices are tested and temperature-compensated for the specific coarse sensitivity setting. If the coarse sensitivity is changed, by programming the `sns_coarse` bits, Allegro cannot guarantee the specified sensitivity drift through temperature and lifetime limits.

COARSE REFERENCE VOLTAGE (vref_coarse)

This device has a coarse reference DAC that changes the centered voltage for the `vref_fine` DAC. To program `vref_coarse`, refer to the following table. If this register is not in the factory default setting, Allegro cannot guarantee the over temperature performance of the device.

vref_coarse (code)	Approx. Center Voltage (V)
0	0.5
1	1.5
2	1.65
3	2.5

OUTPUT POLARITY (gc_pol)

It is possible to change the direction of the output excursion for a given field by changing the `gc_pol` register. Refer to polarity for a more detailed explanation in the definitions section. The factory default setting is `gc_pol = 0`. If the `gc_pol` is changed from the factory default, Allegro cannot guarantee the over temperature performance of the device.

MEMORY LOCKING MECHANISMS

The ACS37600 is equipped with multiple memory-locking mechanisms. The purpose of these mechanisms is to allow the user to reduce the likelihood of unintended communication and programming in the future.

Note: Due to the nature of locking a part, some of these settings may limit the user's ability to debug issues in the future, and in some cases may even limit Allegro's ability to provide assistance in any issues. Make sure that when locking a part, the settings chosen are desired, and functionality of the part is fully understood.

CHOPPER STABILIZING TECHNIQUE

When using Hall-effect technology, a limiting factor for total accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionately small relative to the offset that can be produced at the output of the Hall sensor. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges. Chopper stabilization is a unique approach used to minimize Hall offset on the chip.

DEVICE PROGRAMMING

Serial Communication

The serial interface allows an external controller to read and write registers, including EEPROM, in the device using a point-to-point command/acknowledge protocol. The device does not initiate communication; it only responds to commands from the external controller. Each transaction consists of a command from the controller. If the command is a write, there is no acknowledging from the device. If the command is a read, the device responds by transmitting the requested data.

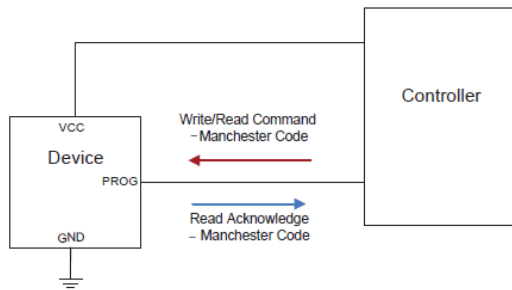


Figure 27: Programming Connections

The serial interface uses a Manchester-encoding-based protocol per G.E. Thomas (0 = rising edge, 1 = falling edge), with address and data transmitted MSB first. Four commands are recognized by the device: Write Access Code, Write to Volatile Memory, Write to Non-Volatile Memory (EEPROM) and Read. One frame type, Read Acknowledge, is sent by the device in response to a Read command.

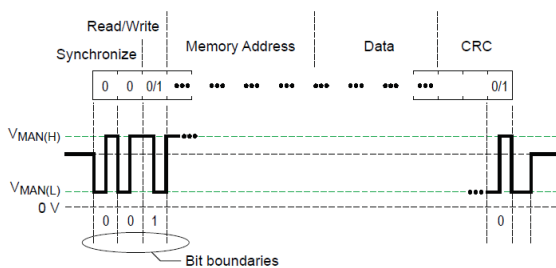


Figure 28: General Format for Serial Interface Communication

READ (CONTROLLER TO DEVICE)

The fields for the Read command are:

- Sync (2 zero bits)
- Read/Write (1 bit, must be 1 for read)
- CRC (3 bits)

Figure 29 shows the sequence for a Read command.

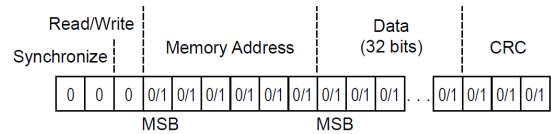


Figure 29: Read Sequence

READ ACKNOWLEDGE (DEVICE TO CONTROLLER)

The fields for the data return frame are:

- Sync (2 zero bits)
- Data (32 bits):
 - [31:28] Don't Care
 - [27:26] ECC Pass/Fail
 - [25:0] Data

Figure 30 shows the sequence for a Read Acknowledge. Refer to the Detecting ECC Error section for instructions on how to detect Read/Write Synchronize Memory Address Data (32 bits) and ECC failure.

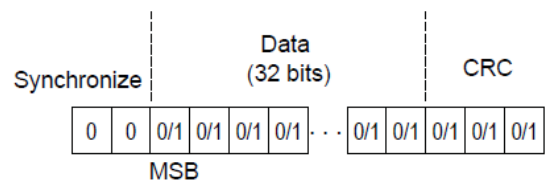


Figure 30: Read Acknowledge Sequence

WRITE (CONTROLLER TO DEVICE)

The fields for the Write command are:

- Sync (2 zero bits)
- Read/Write (1 bit, must be 0 for write)
- Address (6 bits)
- Data (32 bits):
 - [31:26] Don't Care
 - [25:0] Data
- CRC (3 bits)

Figure 31 shows the sequence for a Write command. Bits [31:26] are Don't Care because the device automatically generates 6 ECC bits based on the content of bits [25:0]. These ECC bits will be stored in EEPROM at locations [31:26].

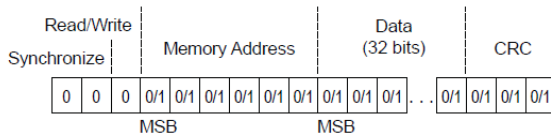


Figure 31: Write Sequence

WRITE ACCESS CODE (CONTROLLER TO DEVICE)

The fields for the Access Code command are:

- Sync (2 zero bits)
- Read/Write (1 bit, must be 0 for write)
- Address (6 bits)
- Data (32 bits)
- CRC (3 bits)

Figure 32 shows the sequence for an Access Code command.

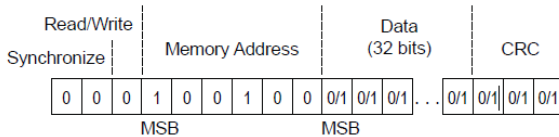


Figure 32: Write Access Code

The controller must open the serial communication with the device by sending an Access Code. It must be sent within Access Code Timeout, t_{ACC} , from power-up, or the device will be disabled for read and write access.

Name	Serial Interface Format	
Register Address	Data (Hex)	(Hex)
User Access	0x26	0x2C413736
Unlock Code	0x26	0xAF6C27

EEPROM ERROR CHECKING AND CORRECTION (ECC)

Hamming code methodology is implemented for EEPROM checking and correction. The device has ECC enabled after power-up.

The device always returns 32 bits.

The message received from controller is analyzed by the device EEPROM driver and ECC bits are added. The first six received bits from device to controller are dedicated to ECC.

DETECTING ECC ERROR

If an uncorrectable error has occurred, bits 27:26 are set to 10, the VOUT pin will go to a high-impedance state, and the device will not respond to the applied magnetic field.

Bits	Name	Description
31:28	–	No meaning
27:26	ECC	00 = No Error 01 = Error detected and message corrected 10 = Uncorrectable error 11 = No meaning
25:0	D[25:0]	EEPROM data

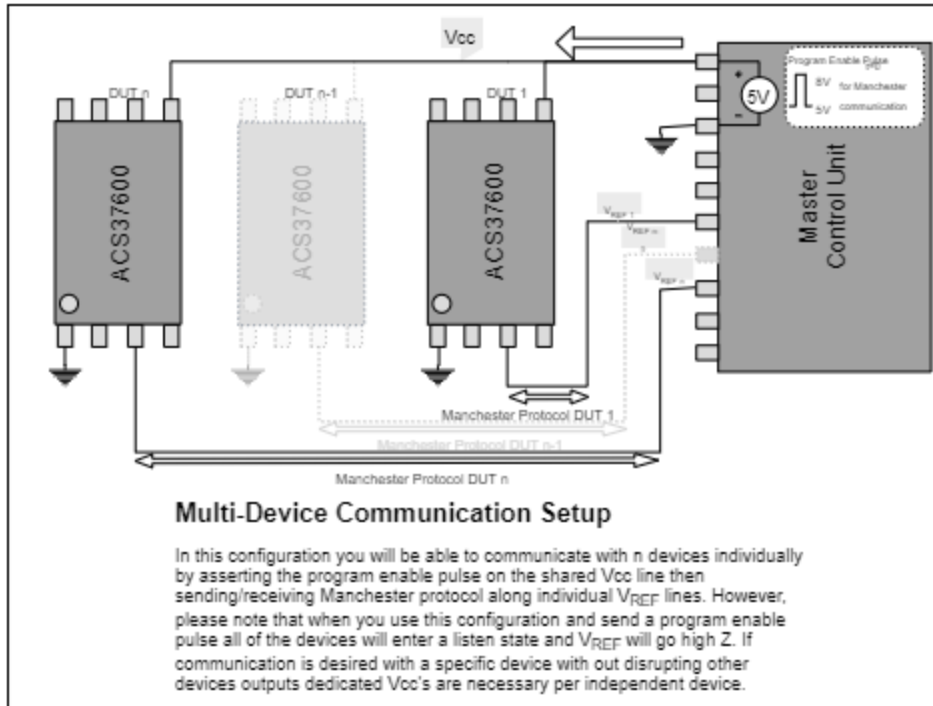
Characteristics	Symbol	Note	Min.	Typ.	Max.	Unit
V_{CC} Programming Enable Voltage	V_{PROG}	V_{CC} pulse required when initializing first communication	8	–	–	V
Program Time Delay	t_d		–	74	–	μ s
Program Write Delay	t_w		–	20	–	ms
Manchester High Voltage	$V_{MAN(H)}$	Data pulses on VREF	4	5	V_{CC}	V
Manchester Low Voltage	$V_{MAN(L)}$	Data pulses on VREF	0	–	1	V
Bit Rate	t_{BITR}	Communication rate	1	30	100	kbps
Bit Time	t_{BIT}	Data bit pulse width at 30 kbps	–	(33)	–	μ s
Access Code Timeout	t_{ACC}		–	10	–	ms

Customer Memory Map

Address	Register Name	Parameter Name	Location	Description	R/W	Bits	Factory Default		
							Decimal	Binary	Effect
0x05	eeprom_5	vref_coarse	0:1	Coarse setting for V_{REF}	R/W [1]	2	3	11	$V_{REF(OUT)} = 2.35$ to 2.65 V
		sens_coarse	2:3	Coarse for sensitivity.	R/W [1]	2	DS	DS	Sets sens range
		bw_sel	4:5	Internal bandwidth selection	R/W	2	2	10	400 kHz
		io_ref_mode	6:7	VREF input/output mode selection	R/W	2	0	00	Input/Output
		vout_eco_mode	8	Reduces operational I_{CC} and I_{OD}	R/W	1	0	0	Turbo
		ovd_dis	9	Disables OVD flag	R/W	1	0	0	OVD enabled
		uvd_dis	10	Disables UVD flag	R/W		0	0	UVD enabled
		spare_user	11:14	No internal function. Customer scratch.	R/W	4	0	0000	N/A
		voff_fine	15:23	Adjusts V_{OUT} offset from V_{REF}	R/W	9	N/A	N/A	Sets offset
ECC	26:31		R	6	N/A	N/A			
0x06	eeprom_6	ocf_hys	0	Doubles OCF hysteresis	R/W	1	0	0	Standard hysteresis
		ocf_persist	1	OCF flag can only be cleared with POR event	R/W	1	0	0	OCF clears normally
		ocf_mask	2:4	Sets additional time fault condition needs to be present before OCF flag is asserted	R/W	3	1	001	0.5 μ s OCF mask
		ocf_hold	5:7	Sets minimum time OCF can be asserted	R/W	3	0	000	OCF clears when condition is removed
		ocf_dis	8	Disables OCF functionality	R/W	1	0	0	OCF is enabled
		ocf_thr	9:17	Sets OCF trip threshold	R/W	9	DS	DS	OCF will trip at 100% FS
		gc_pol	18	Changes direction output will respond with field	R/W [1]	1	0	0	Positive field perpendicular to top face of package will cause positive increase in output
		ECC	26:31		R	6	N/A	N/A	
0x0F	eeprom_f	vref_fine	0:8	Adjusts the V_{REF} output voltage within vref_coarse dependent range	R/W	9	DS	DS	2.5 V
		sens_fine	9:17	Adjusts sensitivity of the device within sens_coarse dependent range	R/W	9	DS	DS	Selection specific sensitivity
		gain_tc	18:23	Adjusts change in sensitivity over temperature up or down	R/W	6	0	000000	Flat over temperature
		analog_lock	24		R/W	1	0	0	
		unlock_code	25		R/W	1	0	0	
		ECC	26:31		R	6	N/A	N/A	

[1] Temperature performance is guaranteed while the gc_pol, sens_coarse, vref_coarse are in the factory default state.

Multi-Device Communication Setup



Error Checking

CYCLICAL REDUNDANCY CHECK (CRC)

The serial interface uses a 3-bit CRC with polynomial $g(x) = x^3 + x + 1$. The CRC is initialized at '111'. Synchronization bits are ignored during calculation of CRC. If the serial interface receives a command with a CRC error, the error is ignored, and it is up to the host controller to resend the command.

EEPROM ERROR CHECKING AND CORRECTION (ECC)

The EEPROM space includes check bits for the purpose of Error Checking and Correction (ECC); these bits are called Hamming codes. ECC can be enabled or disabled via the ECC_DISABLE register. This register has the following effects.

ECC_DISABLE = '0' (ECC ENABLED)

Read – 26 bits are returned [25:0]

A single bit read error will be corrected and the ECC_SINGLE register will be set to '1'

A double bit read error will cause the data in EEPROM to remain unchanged, and the Dual Bit Error be set to '1' and force the output to its diagnostic state (High Impedance).

Write – 26 bits are accepted.

Hamming check bits will be handled internally and written with each write to the EEPROM.

ECC_DISABLE = '1' (ECC DISABLED)

Read – 32 bits are returned [31:0]

Data is passed through unchecked. Check bits are passed to Serial Interface, so checks can be made by host controller.

Write – 32 bits are accepted.

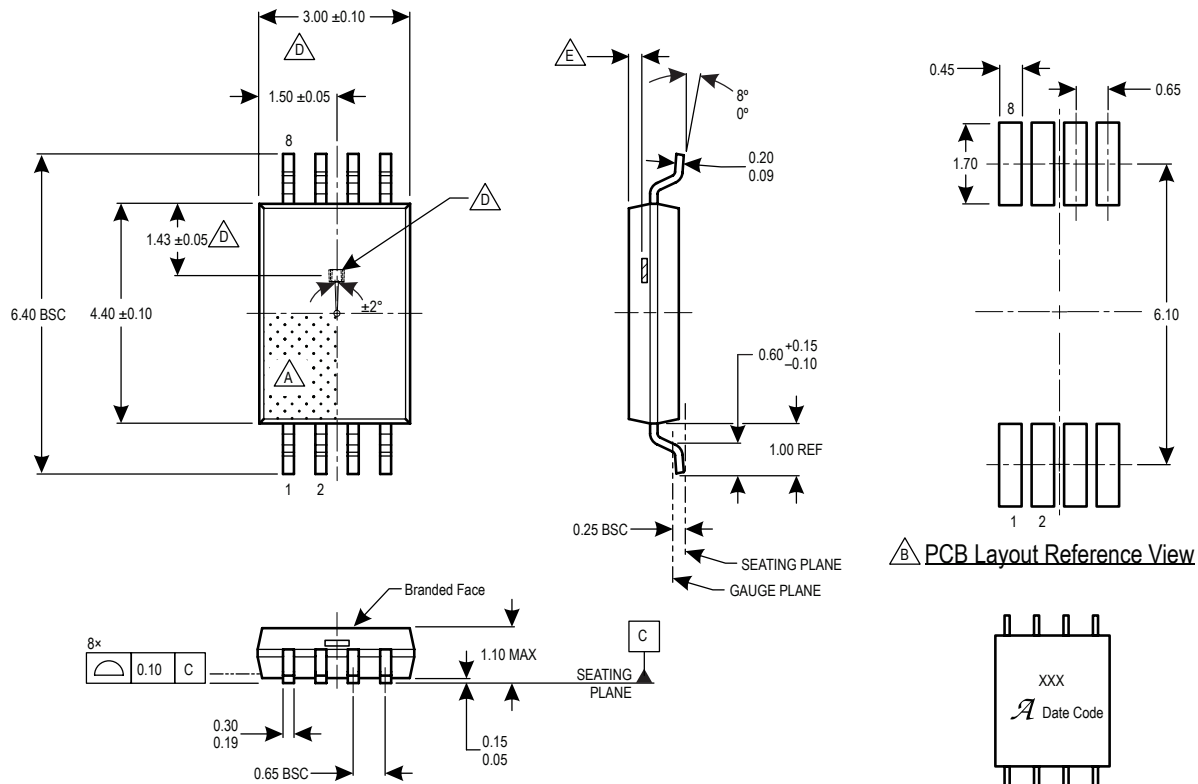
Check bits can be written by the Serial Interface.

In the event of a single or dual bit error, the respective flag is set in register. These flags are read only and will reset after a read command to the register.

PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000381, Rev. 1 and JEDEC MO-153AA)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



- A** Terminal #1 mark area
- B** Reference land pattern layout (reference IPC7351 SOP65P640X110-8M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)
- C** Branding scale and appearance at supplier discretion
- D** Hall element, not to scale
- E** Active Area Depth 0.36 mm REF

- C** **Standard Branding Reference View**
Line 1: Maximum 3 characters
Line 2: Maximum 5 characters

Line 1: Part Number
Line 2: Logo A, 4-digit Date Code

Figure 33: Package LU, 8-Pin TSSOP

Revision History

Number	Date	Description
–	October 13, 2020	Initial release
1	December 9, 2020	Updated Selection Guide and Part Numbering Specification (page 2), Functional Block Diagram (page 5), Characteristics table headings, Temperature Compensation Update Rate (page 6), Output Saturation Voltage, Response Time, Overshoot, Input Referred Noise Density, Output Noise, and Power Supply Sensitivity Error (page 7), Reference Output Noise, OCF Operating Characteristics (page 8), Programmable Characteristics (pages 9-10), Performance Characteristics (pages 11-12), Uni/Bidirectional Functionality (page 17), Definitions of Operating and Performance Characteristics (pages 18-25), Dynamic Output (page 27), Programming Parameters (pages 28-31), and Package Outline Drawing (page 36).
2	January 7, 2022	Updated package drawing (page 36)
3	March 28, 2023	Updated Nominal Absolute Field Range minimum value (page 4)
4	January 14, 2026	Updated features and benefits section (page 1)

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