ACS37610OK

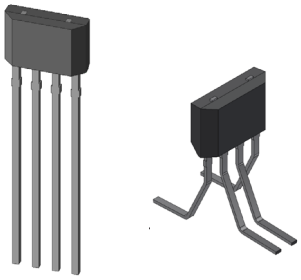
Coreless, High Precision, Current Sensor IC in SIP
with Common-Mode Field Rejection

FEATURES AND BENEFITS

- Contactless, lossless, noninvasive current sensing
- Single in-line package (SIP) easily integrates with sensor placement perpendicular to busbar, greatly reducing misplacement error without the need for a concentrator core or shield
- High operating bandwidth for fast control loops or where high-speed switching currents are monitored
  - DC to 210 kHz
  - 2 µs typical response time
- Customer-programmable, high-resolution offset and sensitivity trim
- High accuracy and low noise
  - ±1% typical sensitivity error over temperature
  - ±3 mV typical offset voltage over temperature
  - Ultra-sensitive Hall elements for improved noise
  - 3.3 V and 5 V ratiometric supply operation
  - Ideal for sensing currents from 100 A to >4000 A
  - Multiple gain options available (4 to 60 mV/G)
  - Differential Hall sensing rejects common-mode magnetic fields
- Wide ambient temperature range: –40°C to 150°C
- Grade 0, AEC-Q100 automotive qualified

PACKAGE

4-pin SIP (suffix OK)
Not to scale



TN Leadform TX Leadform

DESCRIPTION

The ACS37610 enables low-cost solutions for AC and DC current sensing without the need for an external field concentrator core or a U-shaped magnetic shield. It is designed for applications where hundreds or thousands of amps flow through a busbar. Current flowing through a busbar generates a magnetic field that is sensed by the monolithic, low-offset, linear Hall integrated circuit (IC). The differential sensing topology virtually eliminates all types of errors due to common-mode stray magnetic fields. The wide spacing between the differential Hall elements (2.43 mm) coupled with the increased sensitivity of each Hall element enables the ACS37610 to achieve a superior signal-to-noise ration (SNR) and improved resolution. High isolation is achieved via the no-contact nature of this simple assembly.

Built-in diagnostics, including broken ground and V_{CC} detection, make this sensor ideal for safety-critical applications. The accuracy and flexibility of this device is enhanced by user programmability, performed via the output pin or through the dedicated programming pin. This allows the device to be optimized in application and cancels errors due to mechanical assembly tolerances. Device specifications apply across an

Continued on next page ...

TYPICAL APPLICATIONS

- High voltage traction motor inverter
- 48 V/12 V auxiliary inverter
- Heterogeneous redundant battery monitoring
- DC/DC converter
- Smart fuse
- Power distribution unit (PDU)
- Power supplies

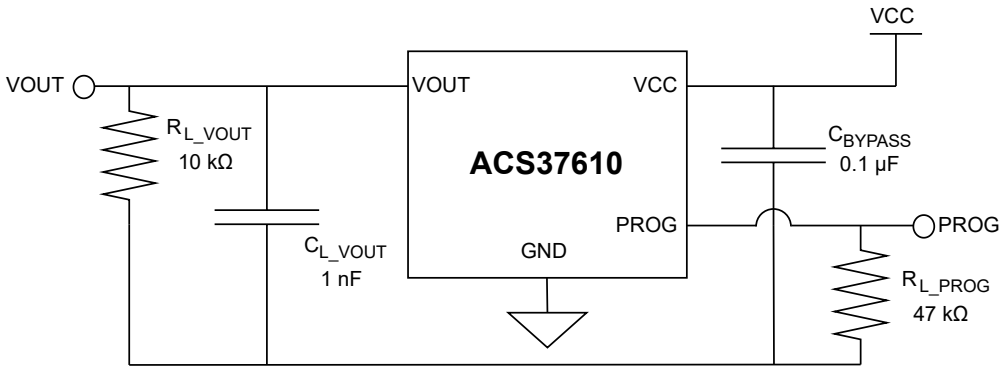


Figure 1: Typical Application Circuit (Programming Pin Used)

The device outputs an analog signal, V_{OUT}, that varies linearly with the bidirectional AC or DC primary current, I_P, within the ranges specified. C_{L_VOUT} is used for optimal noise management, with values that depend on the application. R_{L_VOUT} is an optional pull-down to GND or pull-up to V_{CC} for broken-wire detection. For a broken GND function, tie the PROG pin to VCC when not in use (recommended).

DESCRIPTION (continued)

extended ambient temperature range: –40°C to 150°C. The ACS37610 is offered with regular and low-power mode, enabling customers to achieve the optimal SNR and power consumption.

The ACS37610 is offered in a 4-pin single in-line package (SIP) (Allegro suffix OK) that is lead (Pb) free, with 100% matte tin leadframe plating. A TX leadform option is available, offering higher stability against misplacement (lead bending) with mechanical vibration. The sensor can be easily mounted perpendicular to the busbar and printed circuit board (PCB) in a configuration that gives extremely low misplacement errors, providing superior simplicity in mechanical design and assembly.

TABLE OF CONTENTS

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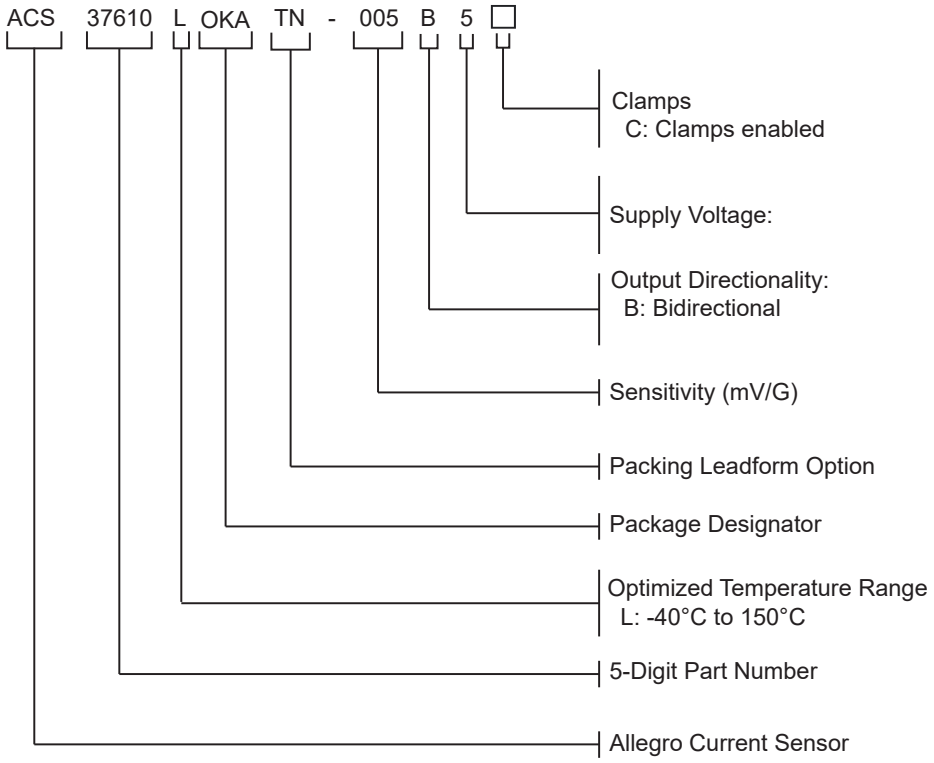
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SELECTION GUIDE

Part Number	Nominal Supply Voltage (V_{CC})	Differential Magnetic Input Range (G)	Sensitivity [1] (mV/G)	Sensitivity Range (mV/G)	Optimized Temp. Range T_A (°C)	Packing [2]
ACS37610LOKATN-005B5 [3]	5	±400	5	4 to 6	–40 to 150	4000 pieces per 13-inch reel
ACS37610LOKATN-010B5	5	±200	10	8 to 12		
ACS37610LOKATN-020B5 [3]	5	±100	20	16 to 24		
ACS37610LOKATN-050B5 [3][4]	5	±40	50	40 to 60		

[1] For additional sensitivity options, contact Allegro MicroSystems.
[2] For additional packing options, contact Allegro MicroSystems.
[3] Pending validation.
[4] This device is configured in low-power mode, where the current drawn by the IC is reduced through factory programing.

PART NAMING SPECIFICATION



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ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Min.	Max.	Unit
Supply Voltage	V_{CC}	For a maximum duration of 1 minute	–0.5	7.5	V
Output Voltage	V_O	Applies to V_{OUT}	–0.5	6.5	V
Output Source Current	$I_{OUT(SOURCE)}$		–	25	mA
Output Sink Current	$I_{OUT(SINK)}$		–	10	mA
Operating Ambient Temperature	T_A	L temperature range	–40	150	°C
Storage Temperature	T_{STG}		–65	165	°C
Maximum Junction Temperature	$T_{J(MAX)}$		–	165	°C

[1] A stress that exceeds a listed Absolute Maximum Ratings might cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions that exceed those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum ratings for an extended duration might affect device reliability.

PINOUT DIAGRAM AND PINOUT LIST

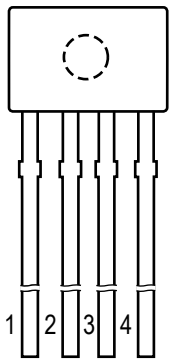

Figure 2: Pinout Diagram

PINOUT LIST

Number	Name	Description
1	VCC	Input power supply; also used for programming
2	PROG	Bidirectional programming pin
3	VOUT	Analog output signal; also used for programming
4	GND	Ground pin

PACKAGE CHARACTERISTICS

Characteristic	Symbol	Notes	Min.	Typ.	Max.	Unit
Moisture Sensitivity Level	MSL	Per IPC/JEDEC J-STD-020	–	2	–	–

ESD RATINGS

Characteristic	Symbol	Test Conditions	Value	Unit
Human Body Model	V_{HBM}	Per JEDEC JS-001	8	kV
Charged Device Model	V_{CDM}	Per JEDEC JS-002	1	kV

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FUNCTIONAL BLOCK DIAGRAM

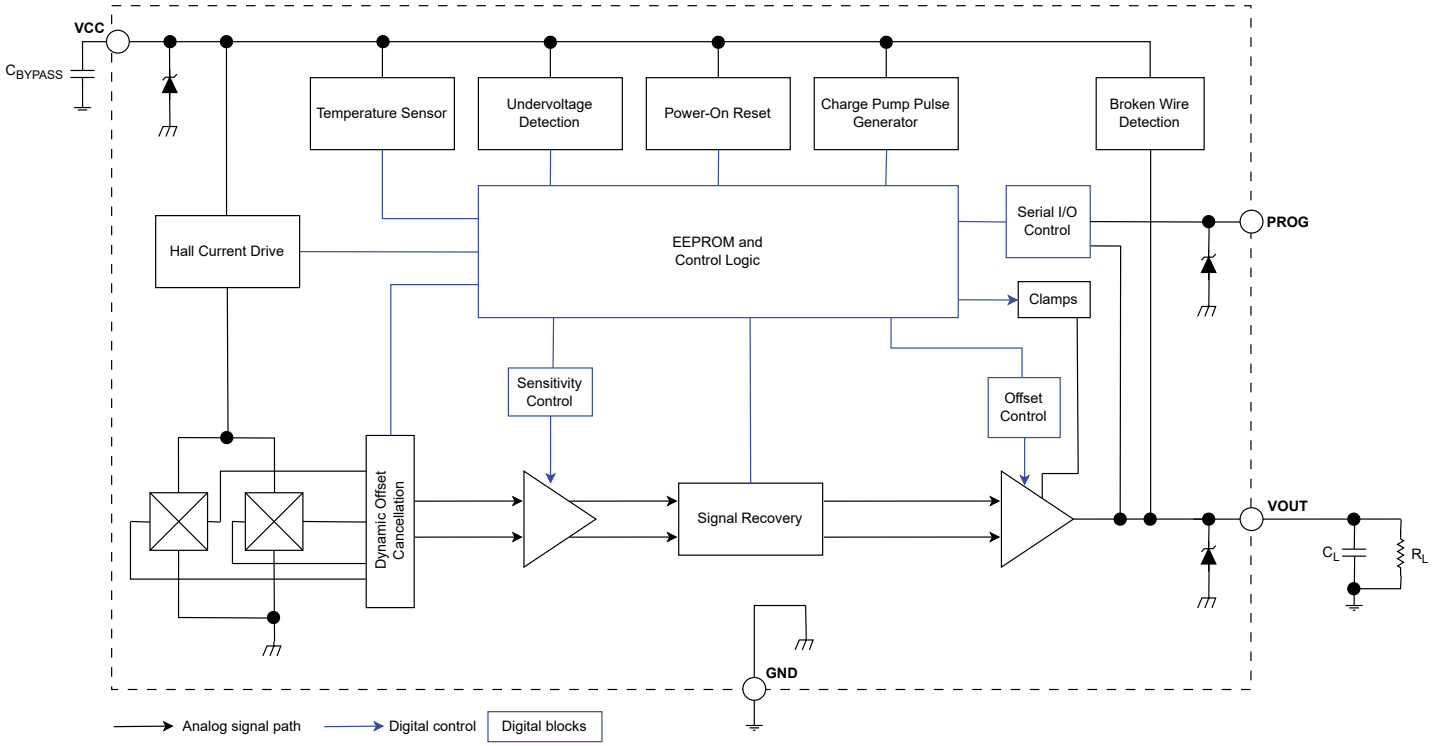

Figure 3: Functional Block Diagram

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COMMON ELECTRICAL CHARACTERISTICS: Valid through the full operating temperature range, T_A = –40°C to 150°C, C_{BYPASS} = 0.1 µF, and V_{CC} = $V_{CC(TYP)}$, unless specified otherwise. Minimum and maximum values are tested in production or validated by design and characterization.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{DD}	3.3 V variant	3	3.3	3.6	V
		5 V variant	4.5	5	5.5	V
Supply Current	I_{DD}	3.3 V variant; load on VOUT not present	–	14.5	19	mA
		Default power mode; 5 V variant; load on VOUT not present	–	16.5	21	mA
		Low-power mode variant; load on VOUT not present	–	13.5	18	mA
Supply Bypass Capacitor [1]	C_{BYPASS}		0.1	–	–	µF
Power-On Reset Voltage	V_{POR}	T_A = 25°C, V_{DD} rising 1 V/ms	2.7	2.9	3	V
Power-On Reset Hysteresis	V_{POR_HYS}		50	150	–	mV
Power-On Time	t_{PO}	T_A = 25°C, C_{L_PROBE} = 10 pF, C_{BYPASS} = open	–	116	–	µs
Power-On Release Time [2]	t_{POR}	T_A = 25°C, V_{CC} rising	–	120	–	µs
Temperature Compensation Power-On Time [3]	t_{TC}	C_{BYPASS} = open, C_{L_VOUT} = 1 nF	–	75	–	µs
OUTPUT SIGNAL CHARACTERISTICS (VOUT)						
VOUT Capacitive Load	C_{L_VOUT}	VOUT to GND	–	1	10	nF
VOUT Resistive Load	R_{L_VOUT}	VOUT to GND	4.7	10	–	kΩ
Output Saturation Voltage [4]	V_{SAT_H}	R_{L_VOUT} = 10 kΩ to GND	V_{CC} – 0.2	–	–	V
	V_{SAT_L}	R_{L_VOUT} = 10 kΩ to VDD	–	–	0.2	V
Bandwidth [5]	BW	Small signal –3 dB, T_A = 25°C, C_{L_VOUT} = 1 nF	–	205	–	kHz
Rise Time [5]	t_R	T_A = 25°C, C_{L_VOUT} = 1 nF	–	1.5	–	µs
Response Time [5]	t_{RESP}	T_A = 25°C, C_{L_VOUT} = 1 nF	–	1.9	–	µs
Propagation Delay [5]	t_{PD}	T_A = 25°C, C_{L_VOUT} = 1 nF	–	1.1	–	µs
Noise Density	N_D	Default power mode; T_A = 25°C, C_{L_VOUT} = 1 nF	–	0.9	–	mG/√(Hz)
		Low-power mode; T_A = 25°C, C_{L_VOUT} = 1 nF	–	1.2	–	mG/√(Hz)
Common-Mode Field Rejection Ratio	CMFRR	Measured at 100 G uniform magnetic field	–	40	–	dB

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Undervoltage (UVD) Detection	V_{UVD_E}	5 V variant only; T_A = 25°C, V_{CC} rising and device function disabled	–	4.1	4.3	V
	V_{UVD_D}	5 V variant only; T_A = 25°C, V_{CC} falling and device function enabled	3.45	3.75	–	V
	V_{UVD_HYS}	5 V variant only; T_A = 25°C	–	600	–	mV
Undervoltage Delay Time [6]	t_{UVD_E}	5 V variant only; T_A = 25°C, C_{L_VOUT} = 1 nF, C_{BYPASS} = open	–	96	–	µs
	t_{UVD_D}		–	14	–	µs
Overvoltage (OVD) Detection	V_{OVD_E}	T_A = 25°C, V_{CC} rising and device function disabled	6.35	6.9	7.2	V
	V_{OVD_D}	T_A = 25°C, V_{CC} falling and device function enabled	5.75	6	6.25	V
	V_{OVD_HYS}	T_A = 25°C	–	450	–	mV
Overvoltage Delay Time	t_{OVD_E}	T_A = 25°C, C_{L_VOUT} = 1 nF, C_{BYPASS} = open	–	87	–	µs
	t_{OVD_D}		–	7	–	µs
Delay to Clamp	t_{CLP}	T_A = 25°C; C_L = 1 nF	–	5	–	µs
Output Voltage Clamp	V_{CLP_H}	V_{CC} = 5 V, R_{L_VOUT} = 10 kΩ to GND	4.48	–	4.8	V
		V_{CC} = 3.3 V, R_{L_VOUT} = 10 kΩ to GND	2.94	–	3.18	V
	V_{CLP_L}	V_{CC} = 5 V, R_{L_VOUT} = 10 kΩ to VCC	0.25	–	0.5	V
		V_{CC} = 3.3 V, R_{L_VOUT} = 10 kΩ to VCC	0.15	–	0.33	V
Broken-Wire Voltage	V_{BRK_H}	R_{L_VOUT} = 10 kΩ to VCC	V_{CC} – 0.1	V_{CC}	V_{CC}	V
	V_{BRK_L}	R_{L_VOUT} = 10 kΩ to GND	0	0	100	mV
Clamp Ratiometry Error	E_{CLP}	V_{CC} = ±3% variation of nominal supply voltage	–	< ±0.5	–	%
DC Output Impedance	R_{OUT}		–	1	–	Ω

[1] Validated by design and characterization.
[2] Following V_{CC} > V_{UVLOD}, the duration for which V_{CC} must be held at greater than V_{POR} to allow the transition from high impedance to typical operation before counting begins for t_{UVLOD}.
[3] Time after t_{PO} required to obtain a valid temperature-compensated output.
[4] The sensor might continue to respond to current beyond the specified current sensing range, I_{PR}, until the output saturates at the high or low saturation voltage; however, the linearity and performance beyond the specified current sensing range are not validated.
[5] Timing specified does not include the potential effects of the skin effect on the conductor; timing value depends on the design of the application.
[6] Time measured from rising V_{CC} > V_{UVD_D} to UVD disabled.

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
NOMINAL PERFORMANCE						
Differential Magnetic Range	B	Corresponding full-scale magnetic range based on typical sensitivity	–400	–	400	G
Initial Factory-Programmed Sensitivity	SENS	T_A = 25°C	4.925	5	5.075	mV/G
Initial Factory-Programmed Quiescent Voltage Output	V_{QVO}	T_A = 25°C	2.495	2.5	2.505	V
Noise [1]	N	T_A = 25°C, C_L = 1 nF, BW = 250 kHz, initial sensitivity	–	2.8	–	mV_{RMS}
Nonlinearity	E_{LIN}	Tested up to full-scale output	–0.55	±0.15	0.55	%
ERROR COMPONENTS						
Sensitivity Drift Over Temperature [2]	E_{SENS}	Factory-programmed sensitivity	–1.5	±1	1.5	%
		Up to ±20% sensitivity change	–1.6	±1	1.6	%
Quiescent Voltage Output Temperature Error [2]	V_{QVO}	Factory-programmed sensitivity	–5	±3	5	mV
		Up to ±20% sensitivity change	–5	±3	5	mV
Sens Ratiometry Error [3]	E_{SENS_RAT}	V_{CC} = ±3% variation of nominal supply voltage	–0.75	±0.25	0.75	%
QVO Ratiometry Error [3]	V_{QVO_RAT}	V_{CC} = ±3% variation of nominal supply voltage	–5	±2	5	mV
LIFETIME DRIFT CHARACTERISTICS [4]						
Sens Lifetime Drift	E_{SENS_LT}	Factory-programmed sensitivity	–	±0.6	–	%
QVO Lifetime Drift	V_{QVO_LT}	Factory-programmed sensitivity	–	±0.8	–	mV

[1] Noise scales with sensitivity.
[2] Minimum and maximum limits for these specifications cover ±4.5σ, or 99.87%, of all devices.
[3] Ratiometry error linearly scales with V_{CC}; e.g., ±1.5% variation on V_{CC} instead of ±3% leads to E_{SENS_RAT} and V_{QVO_RAT} to be divided by 2.
[4] Pending validation. Typical lifetime-drift values are the mean drift observed on a population of parts from 0 hours until the end of stress, including MSL 2 preconditioning. These values are taken from the worst-case AEC-Q100 Grade 0 stress (HAST, TC, HTOL, UHST, or HTSL) at the worst-case temperature.

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ACS37610LOKATN-010B5 PERFORMANCE CHARACTERISTICS: Valid through the full operating temperature range, T_A = –40°C to 150°C, C_{BYPASS} = 0.1 µF, and V_{CC} = 5 V, unless specified otherwise. Minimum and maximum values are tested in production or validated by design and characterization.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
NOMINAL PERFORMANCE						
Differential Magnetic Range	B	Corresponding full-scale magnetic range based on typical sensitivity	–200	–	200	G
Initial Factory-Programmed Sensitivity	SENS	T_A = 25°C	9.85	10	10.15	mV/G
Initial Factory-Programmed Quiescent Voltage Output	V_{QVO}	T_A = 25°C	2.495	2.5	2.505	V
Noise [1]	N	T_A = 25°C, C_L = 1 nF, BW = 250 kHz, initial sensitivity	–	5	–	mV_{RMS}
Nonlinearity	E_{LIN}	Tested up to full-scale output	–0.55	±0.15	0.55	%
ERROR COMPONENTS						
Sensitivity Drift Over Temperature [2]	E_{SENS}	Factory-programmed sensitivity	–1.5	±1	1.5	%
		Up to ±20% sensitivity change	–1.6	±1	1.6	%
Quiescent Voltage Output Temperature Error [2]	V_{QVO}	Factory-programmed sensitivity	–5	±3	5	mV
		Up to ±20% sensitivity change	–5	±3	5	mV
Sens Ratiometry Error [3]	E_{SENS_RAT}	V_{CC} = ±3% variation of nominal supply voltage	–0.75	±0.25	0.75	%
QVO Ratiometry Error [3]	V_{QVO_RAT}	V_{CC} = ±3% variation of nominal supply voltage	–5	±2	5	mV
LIFETIME DRIFT CHARACTERISTICS [4]						
Sens Lifetime Drift	E_{SENS_LT}	Factory-programmed sensitivity	–	±0.3	–	%
QVO Lifetime Drift	V_{QVO_LT}	Factory-programmed sensitivity	–	±0.6	–	mV

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[2] Minimum and maximum limits for these specifications cover ±4.5σ, or 99.87%, of all devices.
[3] Ratiometry error linearly scales with V_{CC}; e.g., ±1.5% variation on V_{CC} instead of ±3% leads to E_{SENS_RAT} and V_{QVO_RAT} to be divided by 2.
[4] Typical lifetime-drift values are the mean drift observed on a population of parts from 0 hours until the end of stress, including MSL 2 preconditioning. These values are taken from the worst-case AEC-Q100 Grade 0 stress (HAST, TC, HTOL, UHST, or HTSL) at the worst-case temperature.

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
NOMINAL PERFORMANCE						
Differential Magnetic Range	B	Corresponding full-scale magnetic range based on typical sensitivity	–100	–	100	G
Initial Factory-Programmed Sensitivity	SENS	T_A = 25°C	19.7	20	20.3	mV/G
Initial Factory-Programmed Quiescent Voltage Output	V_{QVO}	T_A = 25°C	2.4925	2.5	2.5075	V
Noise [1]	N	T_A = 25°C, C_L = 1 nF, BW = 250 kHz, initial sensitivity	–	10	–	mV_{RMS}
Nonlinearity	E_{LIN}	Tested up to full-scale output	–0.55	±0.25	0.55	%
ERROR COMPONENTS						
Sensitivity Drift Over Temperature [2]	E_{SENS}	Factory-programmed sensitivity	–1.5	±1	1.5	%
		Up to ±20% sensitivity change	–1.8	±1.2	1.8	%
Quiescent Voltage Output Temperature Error [2]	V_{QVO}	Factory-programmed sensitivity	–7	±5	7	mV
		Up to ±20% sensitivity change	–10	±7	10	mV
Sens Ratiometry Error [3]	E_{SENS_RAT}	V_{CC} = ±3% variation of nominal supply voltage	–1	±0.4	1	%
QVO Ratiometry Error [3]	V_{QVO_RAT}	V_{CC} = ±3% variation of nominal supply voltage	–7.5	±3	7.5	mV
LIFETIME DRIFT CHARACTERISTICS [4]						
Sens Lifetime Drift	E_{SENS_LT}	Factory-programmed sensitivity	–	±0.3	–	%
QVO Lifetime Drift	V_{QVO_LT}	Factory-programmed sensitivity	–	±0.6	–	mV

[1] Noise scales with sensitivity.
[2] Minimum and maximum limits for these specifications cover ±4.5σ, or 99.87%, of all devices.
[3] Ratiometry error linearly scales with V_{CC}; e.g., ±1.5% variation on V_{CC} instead of ±3% leads to E_{SENS_RAT} and V_{QVO_RAT} to be divided by 2.
[4] Pending validation. Typical lifetime-drift values are the mean drift observed on a population of parts from 0 hours until the end of stress, including MSL 2 preconditioning. These values are taken from the worst-case AEC-Q100 Grade 0 stress (HAST, TC, HTOL, UHST, or HTSL) at the worst-case temperature.

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ACS37610LOKATN-050B5 PERFORMANCE CHARACTERISTICS: Valid through the full operating temperature range, T_A = –40°C to 150°C, C_{BYPASS} = 0.1 µF, and V_{CC} = 5 V, unless specified otherwise. Minimum and maximum values are tested in production or validated by design and characterization.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
NOMINAL PERFORMANCE						
Differential Magnetic Range	B	Corresponding full-scale magnetic range based on typical sensitivity	–40	–	40	G
Initial Factory-Programmed Sensitivity	SENS	T_A = 25°C	49	50	51	mV/G
Initial Factory-Programmed Quiescent Voltage Output	V_{QVO}	T_A = 25°C	2.485	2.5	2.515	V
Noise [1]	N	T_A = 25°C, C_L = 1 nF, BW = 250 kHz, initial sensitivity	–	25	–	mV_{RMS}
Nonlinearity	E_{LIN}	Tested up to full-scale output	-1	±0.25	1	%
ERROR COMPONENTS						
Sensitivity Drift Over Temperature [2]	E_{SENS}	Factory-programmed sensitivity	–2	±1.3	2	%
		Up to ±20% sensitivity change	–2.5	±1.7	2.5	%
Quiescent Voltage Output Temperature Error [2]	V_{QVO}	Factory-programmed sensitivity	–17	±11	17	mV
		Up to ±20% sensitivity change	–27	±18	27	mV
Sens Ratiometry Error [3]	E_{SENS_RAT}	V_{CC} = ±3% variation of nominal supply voltage	–1.75	±0.4	1.75	%
QVO Ratiometry Error [3]	V_{QVO_RAT}	V_{CC} = ±3% variation of nominal supply voltage	–12.5	±3	12.5	mV
LIFETIME DRIFT CHARACTERISTICS [4]						
Sens Lifetime Drift	E_{SENS_LT}	Factory-programmed sensitivity	–	1.9	–	%
QVO Lifetime Drift	V_{QVO_LT}	Factory-programmed sensitivity	–	±31.5	–	mV

[1] Noise scales with sensitivity.
[2] Minimum and maximum limits for these specifications cover ±4.5σ, or 99.87%, of all devices.
[3] Ratiometry error linearly scales with V_{CC}; e.g., ±1.5% variation on V_{CC} instead of ±3% leads to E_{SENS_RAT} and V_{QVO_RAT} to be divided by 2.
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FUNCTIONAL DESCRIPTION

Principle of Operation

When AC or DC current flows through a busbar, as shown in Figure 4, the ACS37610 device senses the magnetic field difference induced between its two Hall elements, Hall 1 and Hall 2. In the cross-section view in Figure 4, the Hall plates are sensitive to the component of the magnetic field in the left-to-right direction. With a dual-bridge busbar structure, the field components from each bridge sum together as:

$$B_{Hall1} = B1 + B1', B_{Hall2} = B2 + B2'$$

The device output is proportional to the differential field, B_{diff}, which in turn is proportional to the applied current:

$$B_{diff} = B_{Hall1} - B_{Hall2} = (B1 + B1') - (B2 + B2')$$

The relationship between applied current and generated field is:

$$B_{diff} = CF \times I,$$

where CF is the differential coupling factor (G/A), which depends on the shape of the busbar, and I is the current through the busbar. As shown in this equation, the differential coupling factor (CF) is the linear relationship between the differential field sensed and the current flowing in the conductor.

Device Diagnostics

The ACS37610 device offers multiple built-in diagnostics with effects and programmability as described in Table 1.

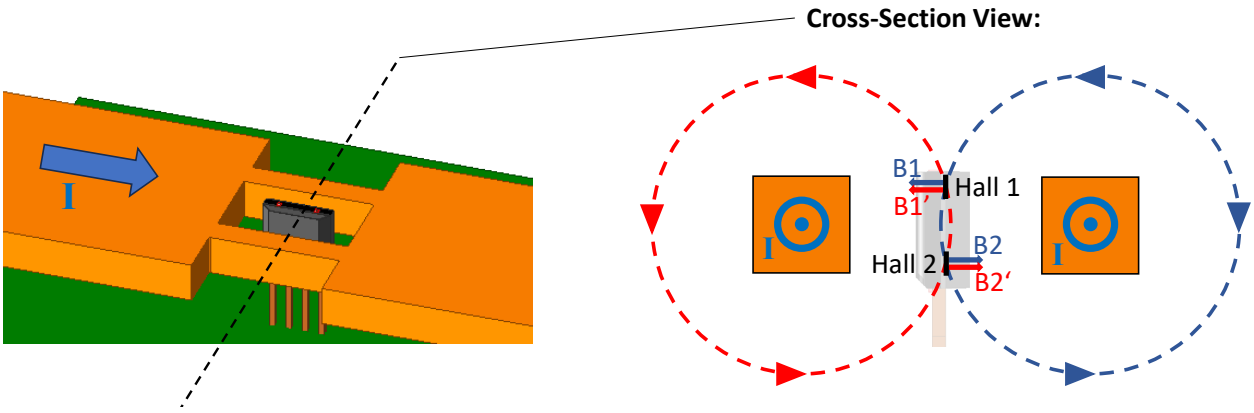

Figure 4: Current-Sensing Principle

Table 1: Device Diagnostics Table

Diagnostic	Effect on V_{OUT}	Note
Overvoltage Detection	If V_{CC} exceeds V_{OVDE} for longer than t_{OVDE} (64 µs typ.), V_{OUT} transitions to the high-impedance state.	NOTE 1: When V_{OUT} transitions to the high-impedance state, the voltage on V_{OUT} is pulled down to GND or pulled up to V_{CC}, depending on application wiring. If the COM_LOCK bit is set, the OVD feature is disabled.
Undervoltage Detection	If V_{CC} reduces to less than V_{UVLOE} for longer than t_{UVLOE} (64 µs typ.), V_{OUT} is pulled to GND; if V_{CC} reduces further below V_{PORL}, V_{OUT} transitions to the high-impedance state.	
Broken Wire	V_{OUT} transitions to the high-impedance state.	
Clamps	V_{OUT} can range from $V_{CLP(Low)}$ to $V_{CLP(High)}$.	Clamps can be enabled/disabled in EEPROM.
EEPROM Error Checking and Correction	If an uncorrectable error occurs in EEPROM, V_{OUT} transitions to the high-impedance state.	See NOTE 1.

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Broken-Wire Detection

If the GND pin is disconnected, node A becoming open (Figure 58), the VOUT pin transitions to a high-impedance state. If a load resistor ($R_{L(PULLUP)}$) is connected to VCC, the output voltage transitions to $V_{BRK(HIGH)}$. If a load resistor ($R_{L(PULLDOWN)}$) is connected to GND, the output voltage transitions to $V_{BRK(LOW)}$.

If the VCC pin is disconnected, node B becoming open (Figure 5), the VOUT pin transitions to a high-impedance state. If a load resistor $R_{L(PULLDWN)}$ is connected to GND, the output voltage transitions to $V_{BRK(LOW)}$.

Detection for broken VCC can only be guaranteed when a pull-down resistor is used.

Following a broken-wire event, the device does not respond to any applied magnetic field. If the disconnected wire is reconnected, the device resumes typical operation.

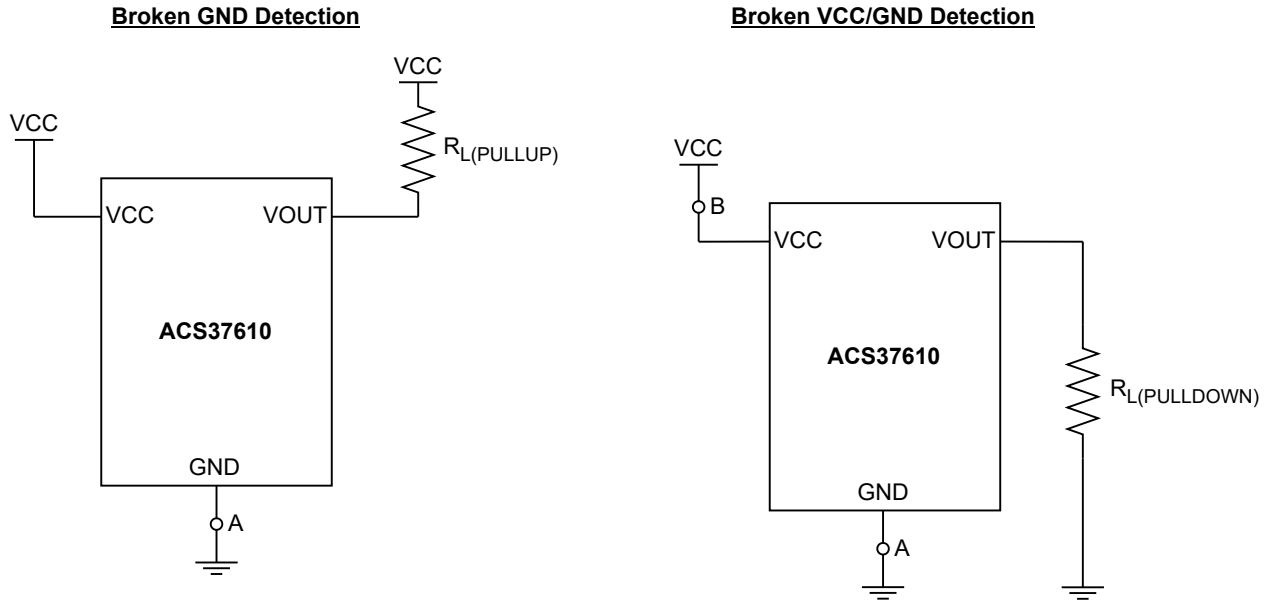

Figure 5: Connection for Detecting Broken Ground Wire

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DEVICE PROGRAMMING

- The serial interface uses Manchester protocol to communicate.
- Device programming can be achieved with bidirectional communication on VOUT or on the dedicated PROG pin.
- The device has an internal charge pump to generate the EEPROM pulses.
- The PROG pin can be left unconnected or tied to GND or VCC when not used.

Serial Communication

The serial interface allows an external controller to read and write registers, including EEPROM, in the device using a point-to- point command/acknowledge protocol. The device does not initiate communication; it only responds to commands from the external controller. Each transaction consists of a command from the controller. If the command is a write command, the device does not acknowledge it. If the command is a read command, the transmits the requested data. Two modes are available for device communication, discussed next.

Mode 1, Programming on VOUT Pin (see Figure 6): Voltage is raised on V_{CC} (V_{OVDE}) for at least t_{OVDE}, followed by the access code on VOUT to enable bidirectional programming on VOUT. If the COM_LOCK bit is set (COM_LOCK = 1), bidirectional programming on VOUT is disabled. If the COM_LOCK bit is not set (COM_LOCK = 0), there is not a timeout limit to send the access code as long as V_{CC} remains at greater than V_{OVDE} for at least t_{OVDE}. The start of any Manchester command should begin with holding the output low for t_{BIT} to ensure reset of the Manchester state machine. If an incorrect access code is sent, VOUT remains in the typical analog mode (responds to magnetic stimulus) and the device remains locked for communication on VOUT until a power reset occurs.

When writing into nonvolatile memory (EEPROM), V_{CC} must not exceed 5 V to ensure safe EEPROM writing. To achieve this, two methods can be used:

Method 1 (to write EEPROM in Mode 1):

Locking VOUT into communication mode such that VCC can returned to the typical supply voltage (5 V or 3.3 V):

1. Set V_{CC} to V_{OVDE} (OVD).
2. Send the access code plus COMM_EN.
3. Set V_{CC} back to the typical level (5 V/3.3 V).
4. Send EEPROM write commands.
5. Power-cycle the device to re-enable the analog output on VOUT.

Method 2 (to write EEPROM in Mode 1):

Reducing VCC back to typical supply voltage (5 V/3.3 V) after sending the EEPROM write sequence:

1. Set V_{CC} to V_{OVDE} (OVD).
2. Send the access code.
3. Send EEPROM write commands.
4. Set V_{CC} to the typical level (5 V/3.3 V).
5. Wait 20 ms for EEPROM write.

With method 2, the PROG pin must not be connected to GND (can be left floating or connect to VCC).

For more details, refer to the Manchester Protocol section. When not used, it is recommended for the PROG pin to be tied to VCC (for the broken GND feature).

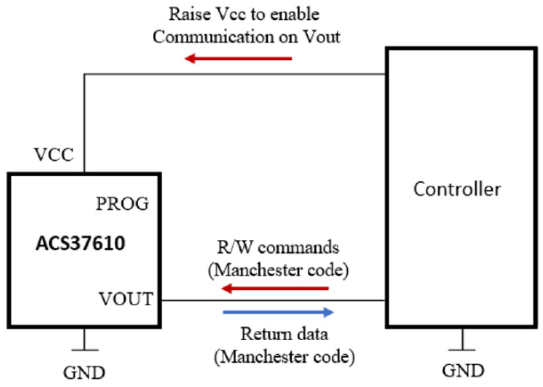

Figure 6: Programming Connection—Mode 1

Mode 2, Programming on PROG Pin (see Figure 7): V_{CC} remains at 5 V (less than V_{OVDE}), and bidirectional programming is achieved on the PROG pin by sending an access code (independently of the COM_LOCK value). A pull-up on the PROG pin is not required.

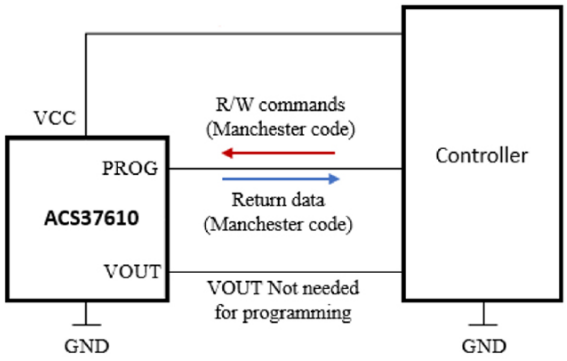

Figure 7: Programming Connections—Mode 2

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Manchester Protocol

The serial interface uses a Manchester-encoding-based protocol per G.E. Thomas (0 = rising edge, 1 = falling edge), with address and data transmitted most significant bit (MSB) first. Four commands are recognized by the device: write access code, write to volatile memory, write to nonvolatile memory (EEPROM), and read. One frame type, read acknowledge, is sent by the device in response to a read command.

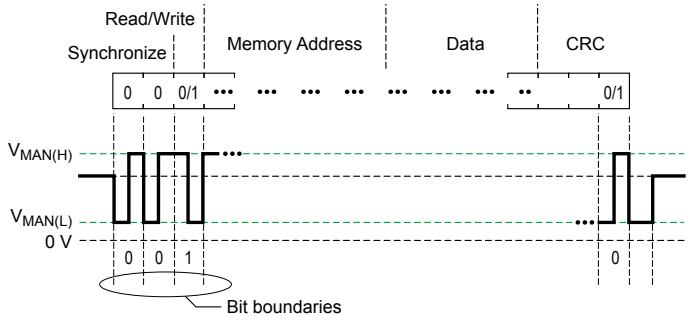

Figure 8: General Format For Serial Interface Commands

Read (Controller to Device)

The fields for the read command are:

- Sync (2 zero bits)
- Read/Write (1 bit, must be 1 for read)
- CRC (3 bits)

The sequence for a read command is shown in Figure 9.

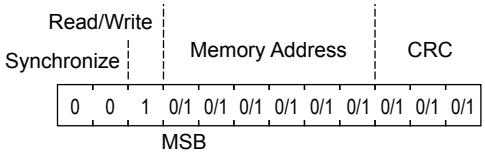

Figure 9: Read Sequence

Read Acknowledge (Device to Controller)

The fields for the data return frame are:

- Sync (2 zero bits)
- Data (32 bits):
  - □ [31:28] Not relevant
  - □ [29:28] ECC Pass/Fail
  - □ [25:0] Data
- CRC (3 bits)

The sequence for a read acknowledge command is shown in Figure 10. For instructions about how to detect read/write synchronize memory address data (32 bits) and ECC failure, refer to Refer to the Detecting ECC Error section.

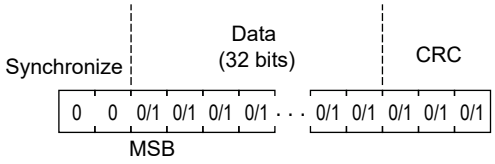

Figure 10: Read Acknowledge Sequence

Write (Controller to Device)

The fields for the write command are:

- Sync (2 zero bits)
- Read/Write (1 bit, must be 0 for write)
- Address (6 bits)
- Data (32 bits):
  - □ [31:26] Not relevant
  - □ [25:0] Data
- CRC (3 bits)

The sequence for a write command is shown in Figure 11. Bits [31:26] are not relevant because the device automatically generates 6 error correction and calibration (ECC) bits based on the content of bits [25:0]. These ECC bits are stored in EEPROM at locations [31:26].

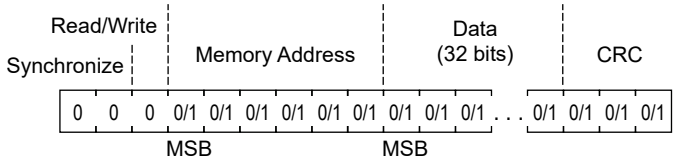

Figure 11: Write Sequence

Write Access Code (Controller to Device)

The fields for the access code command are:

- Sync (2 zero bits)
- Read/Write (1 bit, must be 0 for write)
- Address (6 bits)
- Data (32 bits)
- CRC (3 bits)

The sequence for an access code command is shown in Figure 12.

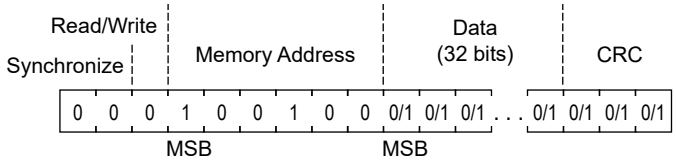

Figure 12: Write Access Code

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The controller must open the serial communication with the device by sending an access code. The access code can be sent on the PROG pin at any time to enable communication on the PROG pin. For VOUT communication, the OVD event must be sent followed by the access code on VOUT. The OVD event must be maintained during the first full transaction.

Register Address	Address(Hex)	Data(Hex)
Customer Access	0x31	0x2C413736
Customer Access + COM_ENABLE	0x31	0x2C413737

The least significant bit (LSB) of the 32-bit customer access code is used to disable the output and leave the device in communication mode until a reset occurs. When the output is disabled, V_{CC} can be restored to a level inferior to V_{OVDE} without altering the Manchester communication and thus until a reset occurs.

Using the COM_LOCK Bit

This bit prevents VOUT from changing state following an unwanted OVD event in the application. If the COM_LOCK bit is set, OVD is disabled and the device can only be programmed using the PROG pin (communication mode 2).

WRITE_LOCK Bit

Locks a bit after EEPROM has been programmed by the user. To permanently disable the ability to write any EEPROM register, set the WRITE_LOCK bit 1 and power-cycle VCC. Writing to the volatile register can still be performed.

EEPROM Error Checking and Correction (ECC)

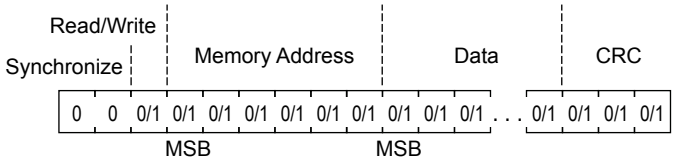
Hamming-code methodology is implemented for EEPROM checking and correction. The device has ECC enabled after power-up. The device always returns 32 bits. The message received from the controller is analyzed by the device EEPROM driver and the ECC bits are added. The first 6 bits sent from the device to the controller are dedicated to ECC.

The Manchester serial interface uses a 3-bit cyclic redundancy check (CRC) for data-bit error checking (synchronized bits are ignored during the check). The CRC algorithm is based on the polynomial $g(x) = x^3 + x + 1$ and is initialized to 111 when power-up first occurs. Write commands written to the peripheral device are compared to the embedded CRC field.

Detecting ECC Error

If an uncorrectable error has occurred, bits [29:28] are set to 10, the VOUT pin transitions to a high-impedance state, and the device does not respond to the applied magnetic field.

Bits	Name	Description
31:28	–	No meaning
29:28	ECC	00 = Error not present 01 = Error detected and message corrected 10 = Uncorrectable error 11 = No meaning
25:0	Data[25:0]	EEPROM data



Quantity of Bits	Name	Values	Description
2	Synchronization	00	Used to identify the beginning of a serial interface command
1	Read/Write	0	[As required] Write operation
		1	[As required] Read operation
6	Address	0/1	[Read/Write] Register address (volatile memory or EEPROM)
32	Data	0/1	26 data bits and 6 ECC bits. For a read command frame, the data consists of 32 bits: [31:28] not relevant, [29:28] ECC pass/fail, and [25:0] data, where bit 0 is the LSB For a write command frame, the data consists of 32 bits: [31:26] not relevant and [25:0] data, where bit 0 is the LSB
3	CRC	0/1	Bits to check the validity of frame

Figure 13: Command Frame General Format

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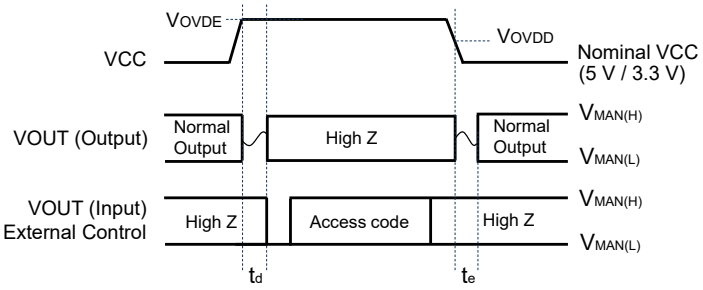

Figure 14: VOUT Programming (Mode 1) Write Access Code

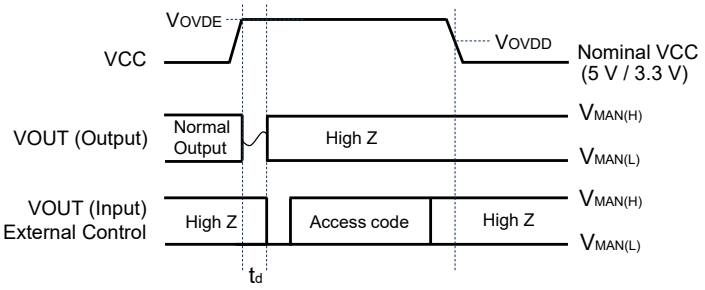

Figure 15: VOUT Programming (Mode 1) Write Access Code + COMM_EN

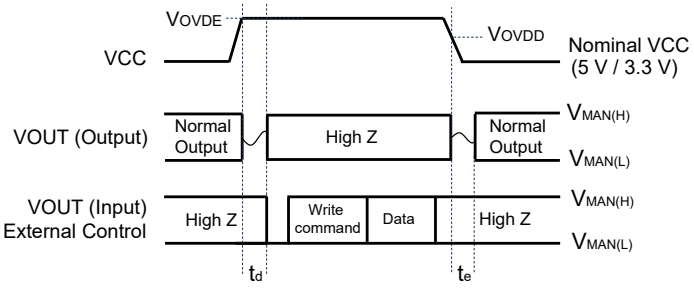

Figure 16: VOUT Programming (Mode 1) Write Volatile Memory

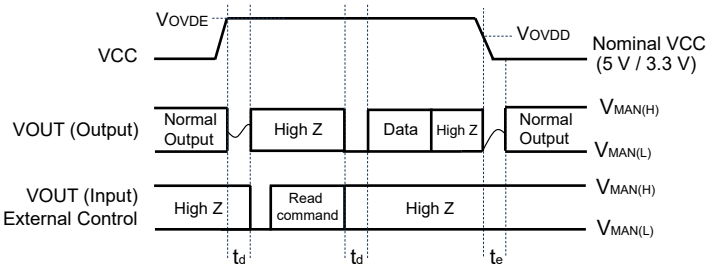

Figure 17: VOUT Programming (Mode 1) Read Memory

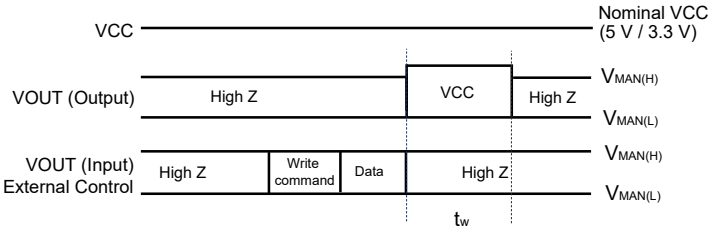

Figure 18: VOUT Programming (Mode 1) Write to EEPROM (Method 1, COMM_EN = 1)

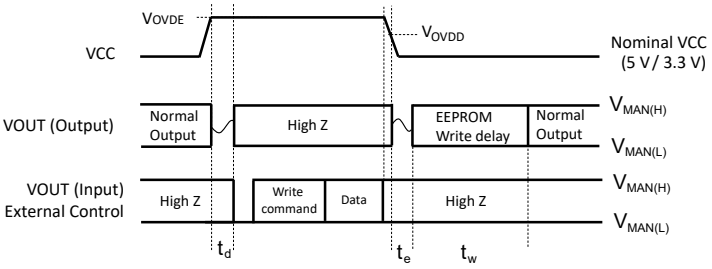

Figure 19: VOUT Programming (Mode 1) Write to EEPROM (Method 2)

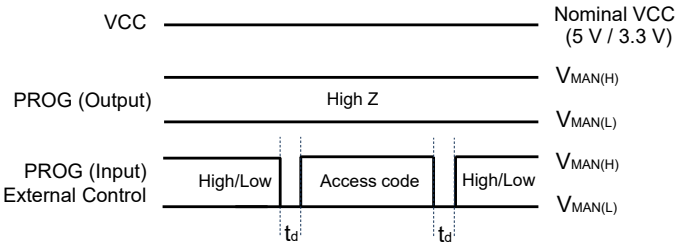

Figure 20: PROG Programming (Mode 2) Write Access Code

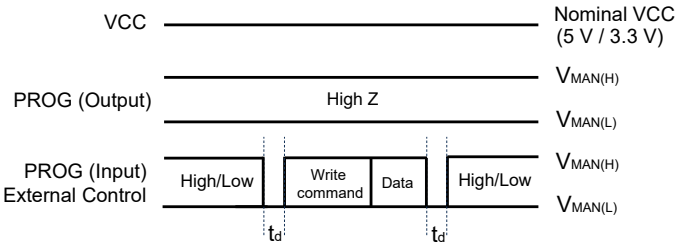

Figure 21: PROG Programming (Mode 2) Write Volatile Memory

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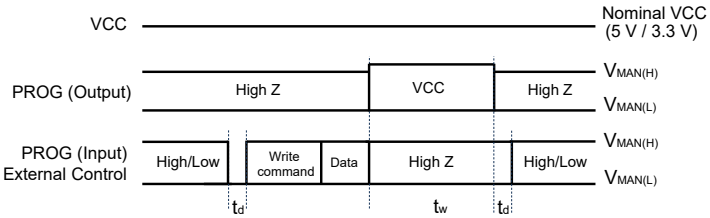

Figure 22: PROG Programming (Mode 2) Write to EEPROM

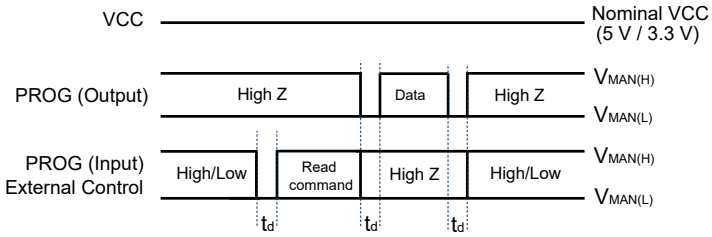

Figure 23: PROG Programming (Mode 2) Read Memory

Table 2: Programming Parameters, C_{BYPASS} = 0.1 µF, V_{CC} = 5 V

Characteristics	Symbol	Note	Min.	Typ.	Max. [1]	Unit
Program Time Delay	t_d	Delay between consecutive read/writes during same Manchester event	–	74	–	µs
Program Write Delay	t_w	Delay between EEPROM writes	–	25	35	ms
Manchester High Voltage	$V_{MAN(H)}$	Data pulses on VOUT/PROG pin, V_{CC} = 5 V	4	5	V_{CC}	V
		Data pulses on VOUT/PROG pin, V_{CC} = 3.3 V	2.4	3.3	V_{CC}	V
Manchester Low Voltage	$V_{MAN(L)}$	Data pulses on VOUT/PROG pin, V_{CC} = 5 V	0	–	1	V
		Data pulses on VOUT/PROG pin, V_{CC} = 3.3 V	0	–	0.75	V
Bit Rate	t_{BITR}	Communication rate	1	30	133	kbps
Bit Time	t_{BIT}	Data-bit pulse width	1000	33	7.5	µs
Output Enable Delay	t_e	External capacitance (CLX) on VOUT may increase the output enable delay	–	125	–	µs

[1] Limit guaranteed by design and characterization.

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EEPROM and Programming Parameters

EEPROM PROGRAMMABLE PARAMETERS: Valid through full range of T_A and V_{CC}, unless otherwise specified

Parameter	Symbol	Description	Min.	Default Value	Max.	Unit	Bit	Typ. Step Size
Sensitivity Fine [1]	SENS_FINE	Sensitivity fine adjustment; signed 2's complement	2.5	5	7.5	mV/G	9	15 µV/G
			5	10	15	mV/G	9	30 µV/G
			10	20	30	mV/G	9	60 µV/G
QVO [1]	QVO	Quiescent Output Voltage adjustment ($V_{OUT(Q)}$); signed 2's complement V_{CC} = 5 V, bidirectional	2.4	2.5	2.6	V	9	1 mV
		Quiescent Output Voltage adjustment ($V_{OUT(Q)}$); signed 2's complement V_{CC} = 5 V, Unidirectional	0.4	0.5	0.6	V	9	1 mV
		Quiescent Output Voltage adjustment ($V_{OUT(Q)}$); signed 2's complement V_{CC} = 3.3 V, bidirectional	1.6	1.65	1.7	V	9	0.6 mV
Polarity	POL	Output polarity	0	0	1	–	1	–
Communication Lock	COM_LOCK	Used to disable Manchester communication	0	0	1	–	1	–
Clamp Enable	CLAMP_EN	Enable clamps on the output	0	0	1	–	1	–
Customer Scratch	SCRATCH_C	Customer scratch pad	–	0	–	–	26	–

[1] Although the device programming range might be larger, programming sensitivity beyond ±20% of change from the initial value causes $V_{OUT(Q)TC}$ and ΔSensTC drift to deteriorate beyond the specified values.

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Lock Bits Mechanism

The device has two lock bits to disable communication and EEPROM programming. The achieved behavior is summarized Table 3.

Table 3: Lock Bit Mechanism

WRITE_ LOCK	COM_ LOCK	EEPROM Write	EEPROM Read
0	0	Enabled—PROG pin or VOUT with OVD	Enabled—PROG pin or VOUT with OVD
0	1	Enabled—PROG pin only	Enabled—PROG pin only
1	0	Disabled	Enabled—PROG pin or VOUT with OVD
1	1	Disabled	Enabled—PROG pin only

Programming Sensitivity and Quiescent Voltage Output

Sensitivity and $V_{OUT(Q)}$ can be adjusted by programming the SENS_FINE and QVO bits, as illustrated in Figure 24 and Figure 25. The SENS_FINE and QVO codes use a 2's complement encoding to either reduce or increase sensitivity and $V_{OUT(Q)}$. Customers should not program sensitivity or $V_{OUT(Q)}$ beyond the maximum or minimum programming ranges specified in the Performance Characteristics table. Exceeding the specified limit causes the sensitivity and $V_{OUT(Q)}$ drift over the temperature range (E_{Drift} and V_{OED}) to deteriorate beyond the specified values. Programming sensitivity might cause a small drift in $V_{OUT(Q)}$. As a result, it is recommended to program sensitivity first, then $V_{OUT(Q)}$.

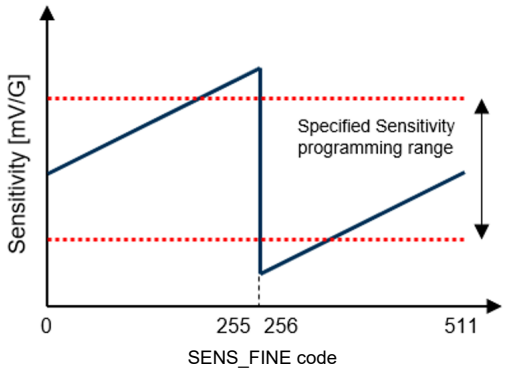

Figure 24: Sensitivity Trim Range

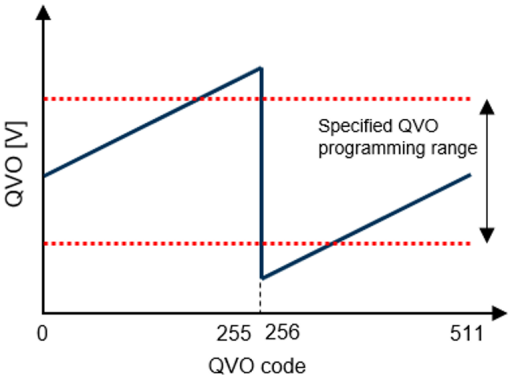

Figure 25: QVO Trim Range

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Polarity (POL)

Device output polarity is programmable to 1 (default) or 0; this allows the output polarity to be reversed. Default polarity (POL bit set to 1) corresponds to an increasing output from 2.5 to 4.5 V typical (0.5 to 4.5 V on unidirectional versions) when positive current flows from pin 1 to pin 4, as shown in Figure 26. Changing the device polarity from its initially programmed value can cause the offset error, $V_{OUT(Q)TC}$, to exceed the specification limits.

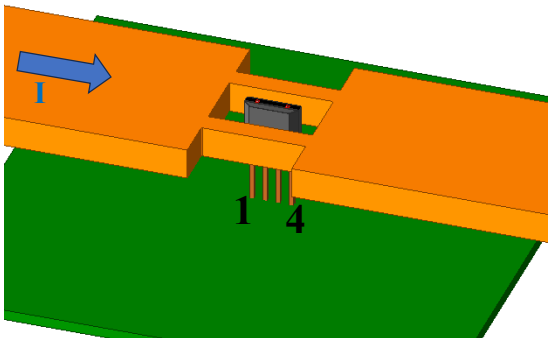

Figure 26: Polarity Definition, Positive Current Direction Shown in Blue

Temperature Output (TEMP_OUT)

This feature allows read of the device temperature stored into a 12-bit digital value.

The digital temperature converts to ambient temperature in degrees Celsius as:

$$\text{TempAmbient [°C]} = (\text{TEMP\_OUT} - 2200)/13.5 + 25$$

Due to device self-heating, the temperature reaches 90% of its steady state approximately 10 seconds after power-on.

Temperature accuracy is typically ±3°C and is guaranteed by characterization only.

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MEMORY MAP

Register Name	Address	Parameter Name	Description	Access	Size	MSB	LSB
EEPROM: (EE_CUST0) Shadow Register [1]: (SH_CUST0)	EEPROM: (0x09) Shadow Register [1]: (0x19)	WRITE_LOCK	Lock the device	R/W	1	25	25
		COM_LOCK	Disable communication on VOUT/disables OVD	R/W	1	24	24
		SPARE	–	R/W	2	23	22
		POL	Change output polarity	R/W	1	21	21
		CLAMP_EN	Enable output clamps	R/W	1	20	20
		SPARE	–	R/W	2	19	18
		QVO	Offset adjustment	R/W	9	17	9
		SENS_FINE	Sensitivity fine adjustment	R/W	9	8	0
EEPROM: (EE_CUST1) Shadow Register [1]: (SH_CUST1)	EEPROM: (0x0A) Shadow Register [1]: (0x1a)	SPARE	–	R/W	26	25	0
EEPROM: (EE_CUST2)	EEPROM: (0x0B)	C_SPARE	Customer scratch pad Does not effect device functionality	R/W	26	25	0
Volatile Register: (FAULT_STATUS)	Volatile Register: (0x20)	TEMP_OUT	Temperature output	R	12	27	16
		UV_STAT	Undervoltage status	R	1	12	12
		OV_STAT	Overvoltage status	R	1	11	11
		SPARE	–	R	2	10	8
		UV_EV	Undervoltage event	R	1	4	4
		OV_EV	Overvoltage event	R	1	3	3
		SPARE	–	R	3	2	0

[1] Shadow registers are volatile memory. Upon startup, the device loads EEPROM memory into shadow registers. Shadow registers can be used to test different programming options without erasing EEPROM (e.g., finding sensitivity and QVO codes before writing into EEPROM).

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DEFINITIONS OF ACCURACY CHARACTERISTICS

SENSITIVITY (Sens)

The amount of the output voltage increase is proportional to the magnitude of the magnetic field applied. This proportionality is specified as the magnetic sensitivity, Sens (mv/G), of the device, and it is defined as:

$$Sens = \frac{V_{OUT(B1)} - V_{OUT(B2)}}{B1 - B2}$$

where B1 and B2 are two different magnetic field levels.

SENSITIVITY ERROR

The sensitivity error is the percent difference between the measured sensitivity and the ideal sensitivity. For example, in the case of V_{CC} = 5 V:

$$E_{Sens} = \frac{Sens_{Meas(5V)} - Sens_{Ideal(5V)}}{Sens_{Ideal(5V)}} \times 100\ (\%)$$

SENSITIVITY ERROR RELATIVE TO SENSITIVITY AT 25°C ($\Delta SENS_{TC}$)

The sensitivity error relative to sensitivity at 25°C is the percent difference between the measured sensitivity at a given temperature and the sensitivity measured at 25°C. For example, in the case of V_{CC} = 5 V:

$$\Delta SENS_{TC} = \frac{Sens_{Meas(5V)} - Sens_{Meas25C(5V)}}{Sens_{Meas25C(5V)}} \times 100\ (\%)$$

NONLINEARITY (E_{LIN})

Nonlinearity is a measure of how linear the output of the sensor IC is over the full current measurement range. The nonlinearity is calculated as:

$$E_{LIN} = \left\{1 - \left[\frac{Sens_{BPRMax}}{Sens_{BPRHalf}}\right]\right\} \times 100\ (\%)$$

where $Sens_{BPRMax}$ is the sensitivity measured at the full range output level and $Sens_{BPRHalf}$ is the sensitivity measured at half of the full range output level.

RATIOMETRY

The device features a ratiometric output. This means that the quiescent voltage output, $V_{OUT(Q)}$, and the magnetic sensitivity, Sens, are proportional to the supply voltage, V_{CC}.

The ratiometric change in the quiescent voltage output is defined as:

$$V_{RatERRQVO} = \left[\left(V_{OUTQ(5V)} \times \frac{V_{CC}}{5\ V}\right) - V_{OUTQ(VCC)}\right] \times 1000\ (mV)$$

The ratiometric change (%) in sensitivity is defined as:

$$Rat_{ERRSens} = \left[1 - \frac{\left(\frac{Sens_{(VCC)}}{Sens_{(5V)}}\right)}{\left(\frac{V_{CC}}{5\ V}\right)}\right] \times 100\ (\%)$$

The ratiometric change (%) in clamp voltage is defined as:

$$Rat_{ERRCLP} = \left[1 - \frac{\left(\frac{V_{CLP(VCC)}}{V_{CLP(5V)}}\right)}{\left(\frac{V_{CC}}{5\ V}\right)}\right] \times 100\ (\%)$$

QUIESCENT OUTPUT VOLTAGE—QVO (ZERO FIELD OUTPUT VOLTAGE)

The output of the sensor when the sensed differential field is zero (in typical applications, when no current is flowing in the busbar/PCB). It nominally remains at 0.5 × V_{CC} for a bidirectional device and 0.1 × V_{CC} for a unidirectional device. For example, in the case of a bidirectional output device, V_{CC} = 5 V translates to $V_{OUT(Q)}$ = 2.5 V. Variation in $V_{OUT(Q)}$ can be attributed to the resolution of the Allegro linear IC quiescent voltage trim and thermal drift.

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POWER-ON RESET VOLTAGE (V_{POR})

On power-up, to initialize to a known state and avoid current spikes, the device is held in the reset state. The reset signal is disabled when V_{CC} reaches V_{PORH} and time t_{PORR} has elapsed, allowing the output voltage to transition from a high-impedance state to typical operation. After t_{PORR}, the output remains high impedance until V_{CC} exceeds V_{UVLOD} for longer than t_{UVLOD}. During power-down, the reset signal is enabled when V_{CC} reaches V_{PORL}, causing the output voltage to transition to a high-impedance state.

POWER-ON RESET RELEASE TIME (t_{PORR})

When V_{CC} rises to V_{PORH}, the power-on reset counter starts. The device output voltage transitions from a high-impedance state to typical operation only when the power-on reset counter has reached t_{PORR} and V_{CC} has been maintained above V_{PORH}.

OVERVOLTAGE DETECTION (V_{OVD})

When V_{CC} increases to greater than the overvoltage detection enable voltage (V_{OVDE}), the ACS37610 output stage enters high impedance. When (V_{OVDE}) is reached, V_{OUT} floats to V_{CC} with a pull-up R_L or to GND with a pull-down R_L. For communication, overvoltage detection must be active. The device output resumes typical operation after V_{CC} reduces to less than the overvoltage detection disable voltage (V_{OVDD}).

If the COM_LOCK bit is set, Overvoltage detection becomes disabled and the device output does not respond to the overvoltage condition.

Supply voltage limits still apply for operating characteristic. Following an overvoltage condition, the supply voltage should not exceeds 7.5 V for more than 1 minute. For more details, see the Overvoltage Detection (VOVD) section.

OUTPUT SATURATION VOLTAGE (V_{SAT})

When output voltage clamps are disabled, the output voltage can swing to a maximum of $V_{SAT(HIGH)}$ and to a minimum of $V_{SAT(LOW)}$.

BROKEN-WIRE VOLTAGE (V_{BRK})

If the GND pin is disconnected (broken-wire event), the output voltage transitions to $V_{BRK(HIGH)}$ (if a load resistor is connected to VCC) or to $V_{BRK(LOW)}$ (if a load resistor is connected to GND).

UNDERVOLTAGE DETECTION (V_{UVLO})

When V_{CC} reduces to less than the undervoltage detection enable voltage (V_{UVLOE}), the ACS37610 output stage drops close to GND beyond the clamp or saturation voltage. The device output resumes typical operation after V_{CC} is greater than the undervoltage detection disable voltage (V_{UVLOD}).

Undervoltage detection is only active on the 5 V variant.

For more details, see the Undervoltage Detection (VUVLO) section.

LOW-POWER MODE

The device is available in a low-power mode variant where the current drawn by the IC is reduced through factory programing. In this variant, the output noise is increased by ~30% compared to the typical power mode variant.

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DEFINITIONS OF DYNAMIC RESPONSE CHARACTERISTICS

Power-On Time (t_{PO}). When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field. Power-on time, t_{PO}, is defined as the time it takes for the output voltage to settle within ±10% of its steady-state value under an applied magnetic field, after the power supply has reached its minimum specified operating voltage, V_{CC}(min), as shown in Figure 27.

Temperature Compensation Power-On Time (t_{TC}). After the power-on time (t_{PO}) elapses, t_{TC} is also required before a valid temperature-compensated output.

Response Time ($t_{RESPONSE}$). The time interval between a) when the sensed current reaches 90% of its final value, and b) when the sensor output reaches 90% of its full-scale value, as shown in Figure 28.

Rise Time (t_r). The time interval between a) when the sensor reaches 10% of its full-scale value, and b) when the sensor reaches 90% of its full-scale value, as shown in Figure 29.

Propagation Delay (t_{pd}). The time interval between a) when the sensed current reaches 20% of its full-scale value, and b) when the sensor output reaches 20% of its full-scale value, as shown in Figure 29.

Delay to Clamp (t_{CLP}). A large magnetic input step may cause the clamp to overshoot its steady-state value. The delay to clamp, t_{CLP}, is defined as: the time it takes for the output voltage to settle within ±1% of clamp voltage dynamic range, after initially passing through its steady-state voltage, as shown in Figure 30.

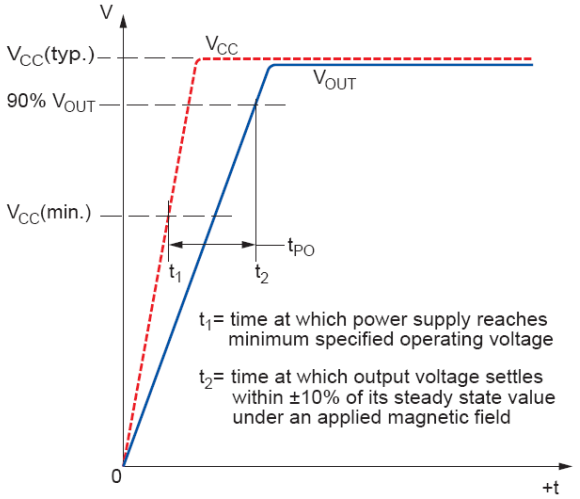

Figure 27: Power-On Time (t_{PO})

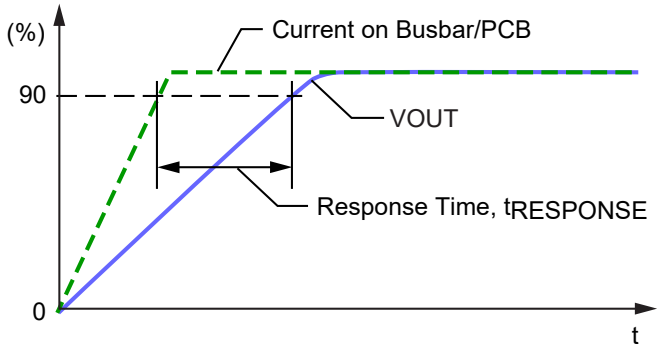

Figure 28: Response Time ($t_{RESPONSE}$)

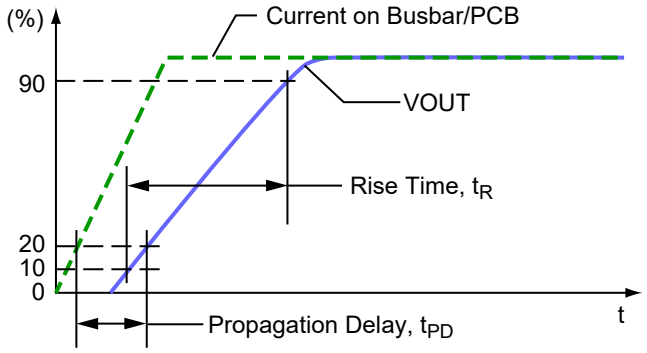

Figure 29: Propagation Delay (t_{PD}) and Rise Time (t_r)

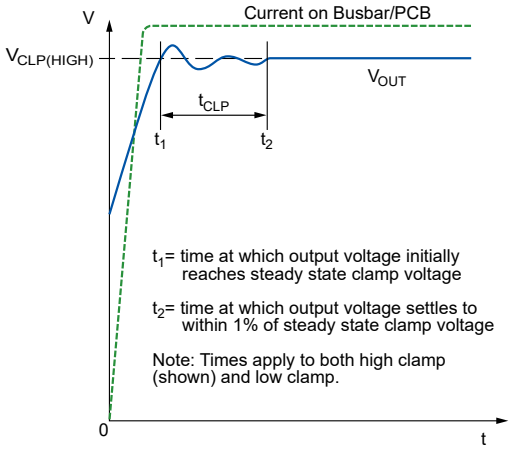

Figure 30: Delay to Clamp

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POWER-ON RESET, UNDERVOLTAGE AND OVERVOLTAGE DETECTION OPERATION

The descriptions in this section assume: temperature = 25°C, output load (R_L, C_L) is not present, and significant magnetic field is not present.

Power-Up. At power-up, as V_{CC} ramps up, the output is in a high-impedance state. When V_{CC} crosses V_{PORH} (locations [1] in Figure 31 and [1'] in Figure 32), the POR release counter starts counting for t_{PORR}. At this point, if V_{CC} exceeds V_{UVLOD} [2'], the output transitions to $V_{CC}/2$ after t_{UVLOD} [3'].

If V_{CC} does not exceed V_{UVLOD} [2], the output remains in the high-impedance state until V_{CC} reaches V_{UVLOD} [3], then transitions to $V_{CC}/2$ after t_{UVLOD} [4].

V_{CC} Drops Below V_{CC}(min) = 4.5 V. If V_{CC} reduces to less than V_{UVLOE} [4', 5], the UVLO enable counter begins to count. If V_{CC} remains at less than V_{UVLOE} when the counter reaches t_{UVLOE}, the UVLO function becomes enabled, and the output is pulled near GND [6]. If V_{CC} exceeds V_{UVLOE} before the UVLO enable counter reaches t_{UVLOE} [5'], the output continues to be $V_{CC}/2$.

Coming Out of UVLO. While UVLO is enabled [6], if V_{CC} exceeds V_{UVLOD} [7], UVLO becomes disabled after t_{UVLOD}, and the output becomes $V_{CC}/2$ [8].

Power-Down. As V_{CC} ramps down to less than V_{UVLOE} [6', 9], the UVLO enable counter begins to count. If V_{CC} is greater than V_{PORL} when the counter reaches t_{UVLOE}, the UVLO function becomes enabled and the output is pulled near GND [10]. As V_{CC} reduces to less than V_{PORL} [11], the output enters a high-impedance state. If V_{CC} reduces to less than V_{PORL} before the UVLO enable counter reaches t_{UVLOE}, the output transitions directly to a high-impedance state [7'].

Overvoltage. If V_{CC} increases to greater than V_{OVDE}, the OVD enable counter begins to count. If the internal pull-up mode is used, the fault pull-up voltage follows V_{CC}; otherwise, it remains at the V_F level. If V_{CC} continues to remain at greater than V_{OVDE} when the counter reaches t_{OVDE}, the OVD function becomes enabled and the output transitions to the high-impedance state. During the transition to the high-impedance state, the fault pin becomes disabled.

Coming Out of OVD. While OVD is enabled, if V_{CC} reduces to less than V_{OVDD}, OVD becomes disabled after t_{OVDD}, and the output returns to typical operation in analog mode with output of $V_{CC}/2$. The fault pin becomes active and recovers typical operation.

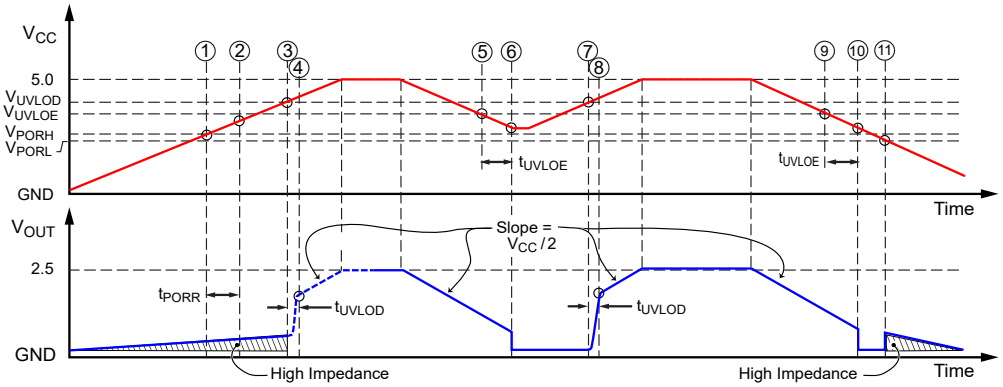

Figure 31: POR and UVLO Operation, Slow Rise Time Case, 5 V Variant

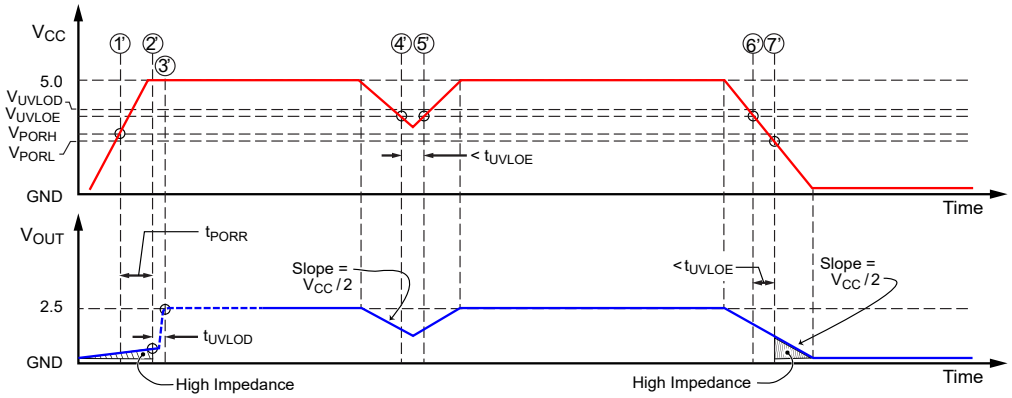

Figure 32: POR and UVLO Operation, Fast Rise Time Case, 5 V Variant

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Power-On Reset (POR); Undervoltage Lockout (UVLO) Disabled— Nominal Supply Voltage = 3.3 V

Power-Up

At power-up, as V_{CC} ramps up, the output is in a high-impedance state. When V_{CC} crosses V_{PORH} (locations [1] in Figure 33 and [1'] in Figure 34), the POR release counter begins to count for t_{PORR} [2], [2'] and the output transitions to $V_{CC}/2$ after t_{PORD} [3], [3']. The temperature-compensation engine then adjusts device sensitivity and QVO after t_{TC} [4], [4'].

V_{CC} Reduces to Less Than V_{CC}(min) = 3 V

If V_{CC} reduces to less than V_{PORH} [5'] but remains greater than V_{PORL} [6'], the output continues to be $V_{CC}/2$.

Power-Down

As V_{CC} ramps down to less than V_{PORL} [5],[7'], the output enters a high-impedance state.

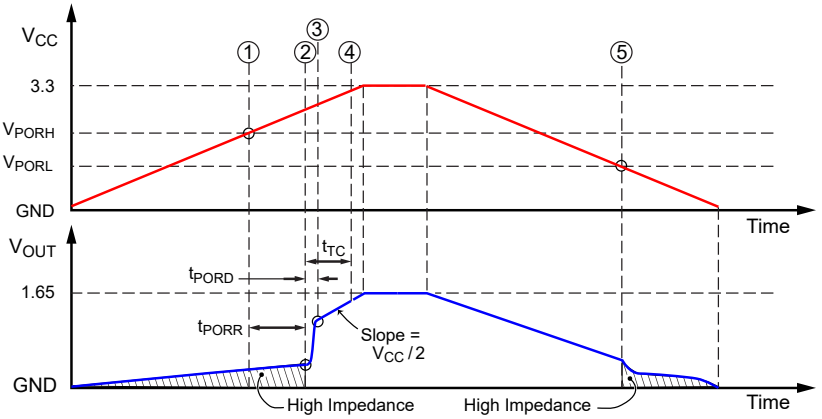

Figure 33: POR and UVLO Operation, Slow Rise Time Case, 3.3 V Mode

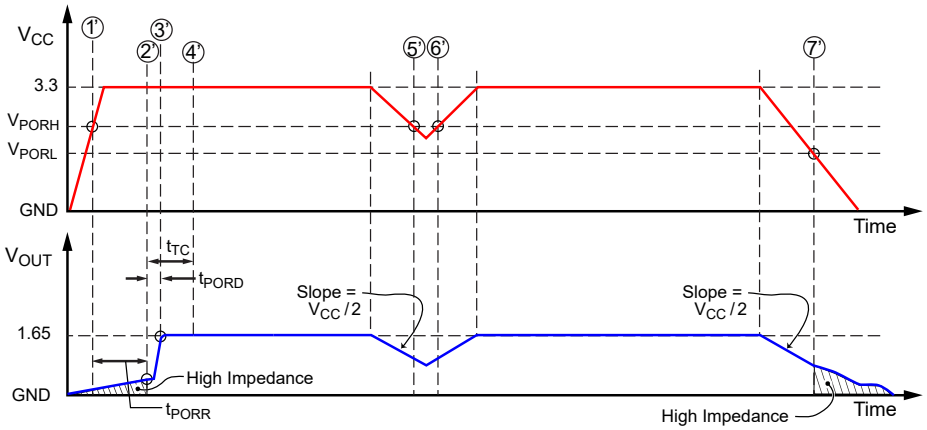

Figure 34: POR and UVLO Operation, Fast Rise Time Case, 3.3 V Mode

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APPLICATION INFORMATION

Typical Application—Busbar Current Sensing

The ACS37610OK is ideal for busbar current sensing applications. The magnitude of the differential magnetic field sensed by the IC depends on the distance between the Hall plates and the current density in the busbar. The addition of cutouts to the busbar serves to concentrate current density close to the sensor, improving sensitivity, signal-to-noise ratio, and bandwidth. Minimized cutout sizes results in minimal increase in the resistance of the busbar or degradation of thermal performance.

Different busbar shapes and dimensions can be used to optimize system performance and respond to application constraints. Figure 35 and Table 4 highlight the dimensions of an Allegro evaluation board designed to measure ±700 A.

NOTE: Compare to a bare busbar (without cutouts), the busbar with the double slit described in Figure 35 increases the overall impedance by less than 12 μΩ, increasing busbar temperature by only few degrees.

Bandwidth and the Skin Effect

Due to the skin effect, the distribution of current density in the busbar varies with frequency, resulting in a change in sensitivity over frequency that depends strongly on the busbar shape and orientation. For example, the busbar design shown in Figure 35 has been optimized to provide <1% sensitivity error at 1 kHz.

Depending on customer requirements, tradeoffs can be made between noise, misplacement error, bandwidth, crosstalk, voltage isolation, power loss, and mechanical stability. For busbar design support, contact an Allegro representative.

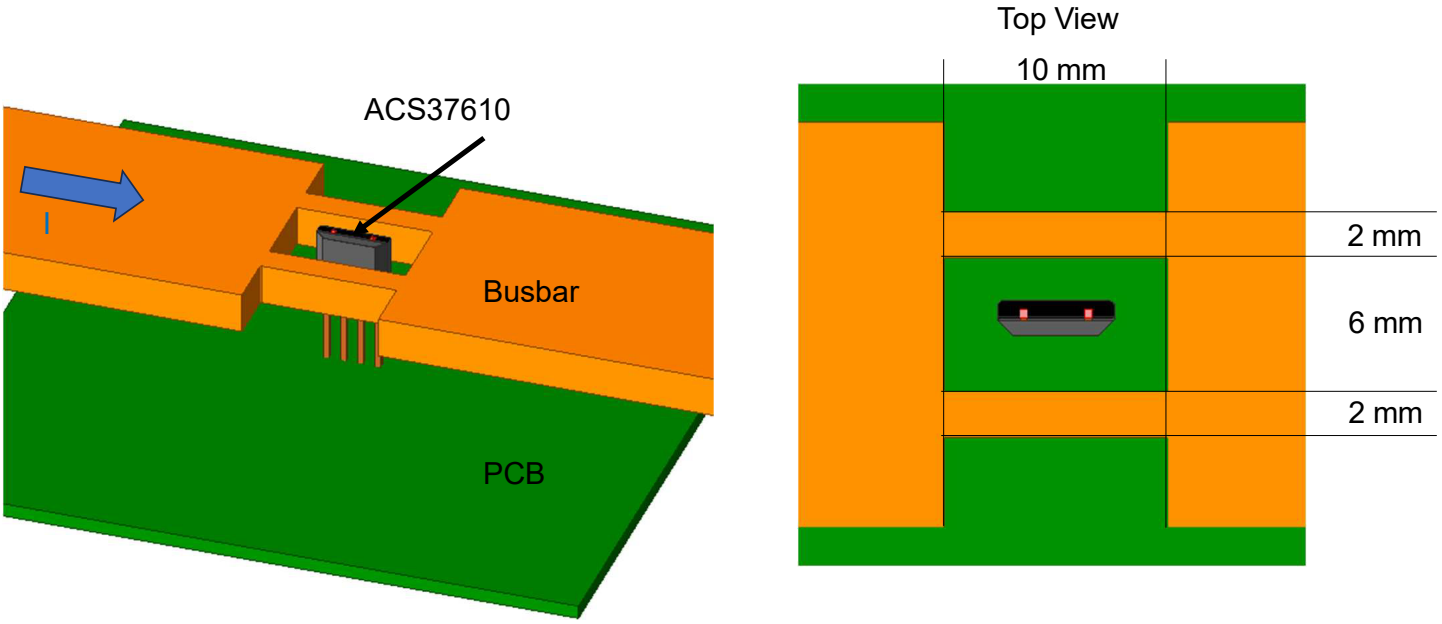

Figure 35: Busbar Current-Sensing Application—Reference Busbar Design with Dual Bridge

Table 4: Current Range Based on Reference Busbar Design

Busbar Application	Cross Section [mm²]	Cross Section at Sensor Location [mm²]	Max. Current [1] [A]	Coupling Factor [2] [G/A]	IC Sensitivity [2] [mV/G]	Added Impedance [3] [μΩ]
20 × 3 mm Busbar with Dual Bridge	60	12	±700	0.26	11	11.5

[1] Full-scale current is required to cover the full-scale output range (bidirectional = ±2 V).
[2] Sensor placed with Hall elements centered in the busbar slit.
[3] Calculated at DC.

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Busbar Design Options

The ACS37610 offers different mounting possibilities, addressing different needs (low noise, misplacement error, bandwidth, crosstalk, voltage isolation, power loss, and mechanical stability). The two most common mounting options are shown in Figure 36 and Figure 37.

The standard Allegro recommendation for most ACS37610 applications is the dual bridge design, shown in Figure 37. This design provides all-around good performance, very low sensor misplacement error, and good frequency response up to approximately 2 kHz. The dual-bridge reference design shown in Figure 38 is also the busbar design used on the Allegro evaluation board for this product. This design forces the current through two relatively small “bridges” that pass on either side of the sensor. The coupling factor can be tuned by adjusting the distance between the bridges in order to match the desired full-scale current sensing range to one of the factory-programmed sensitivities. While reducing the cross section of the bridges increases sensitivity and reduces error at high frequencies, this also increases the resistance of the busbar, which results in higher power losses. For application-specific support navigating these tradeoffs, contact an Allegro representative

A similar busbar structure without cutouts on the sides is shown in Figure 36. This design is a good choice when the busbar is relatively narrow, such that the cutouts on the sides are not necessary to achieve good frequency response. This type of design can also be a good choice for low-frequency high-current applications where the frequency response in the kHz range is not important and the busbar resistance needs to be minimized.

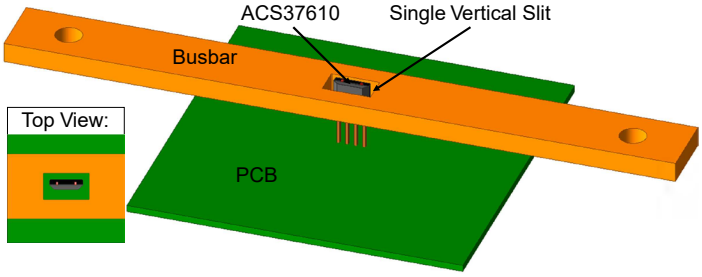

Figure 36: Single Vertical Slit Busbar Design
Lowest misplacement error and crosstalk, high coupling factor, high bandwidth when busbar width is short. For DC to low-frequency AC applications.

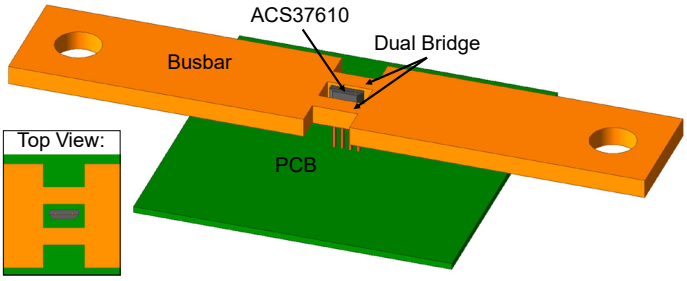

Figure 37: Dual-Bridge Busbar Design
Lowest misplacement error and crosstalk, high coupling factor, high bandwidth. For DC to low-frequency AC applications.

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PACKAGE OUTLINE DRAWING

For Reference Only - Not for Tooling Use

(Reference DWG-0000395)
Dimensions in millimeters - NOT TO SCALE
Dimensions exclusive of mold flash, gate burs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

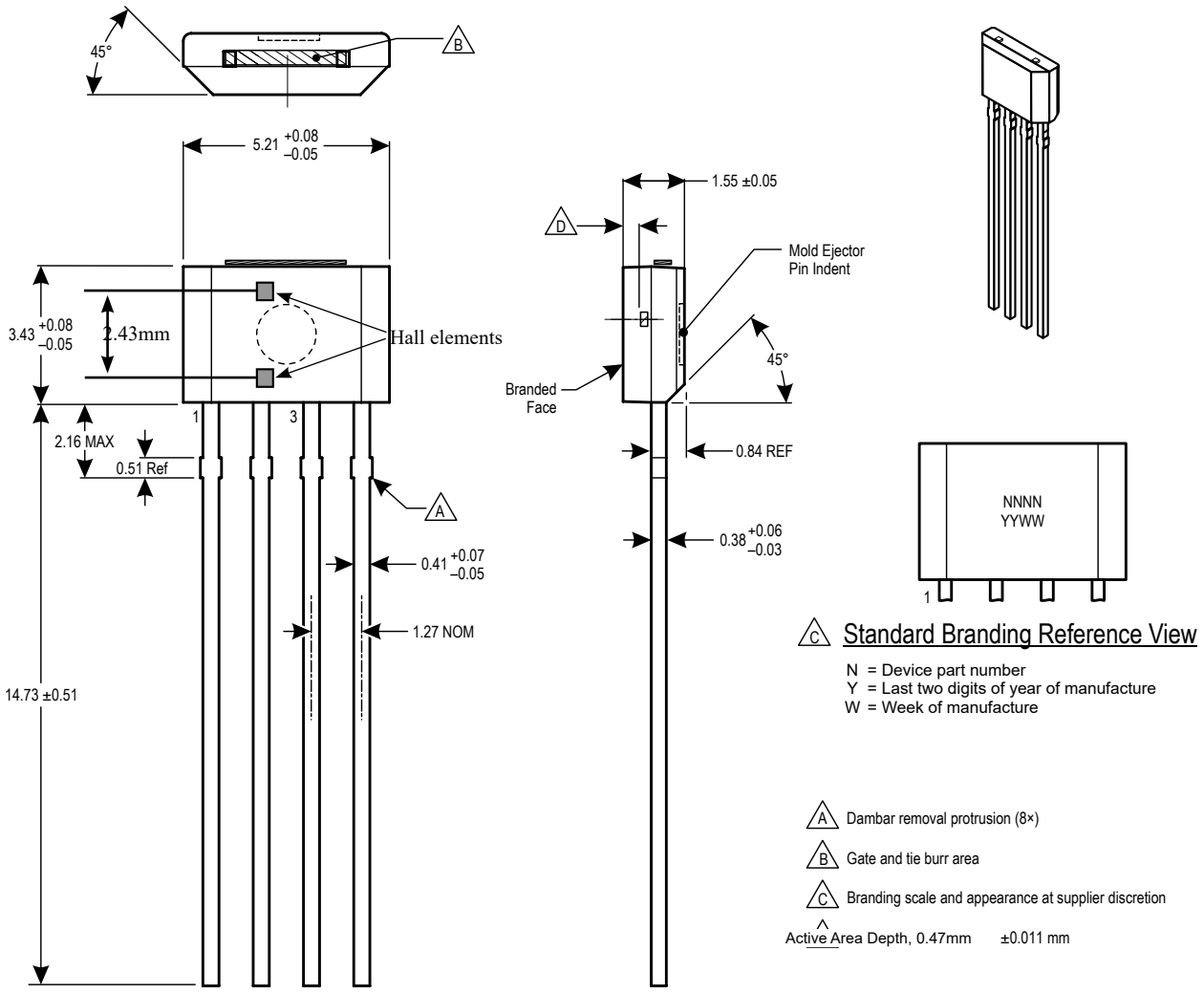

Figure 38: Package OK, 4-Pin SIP

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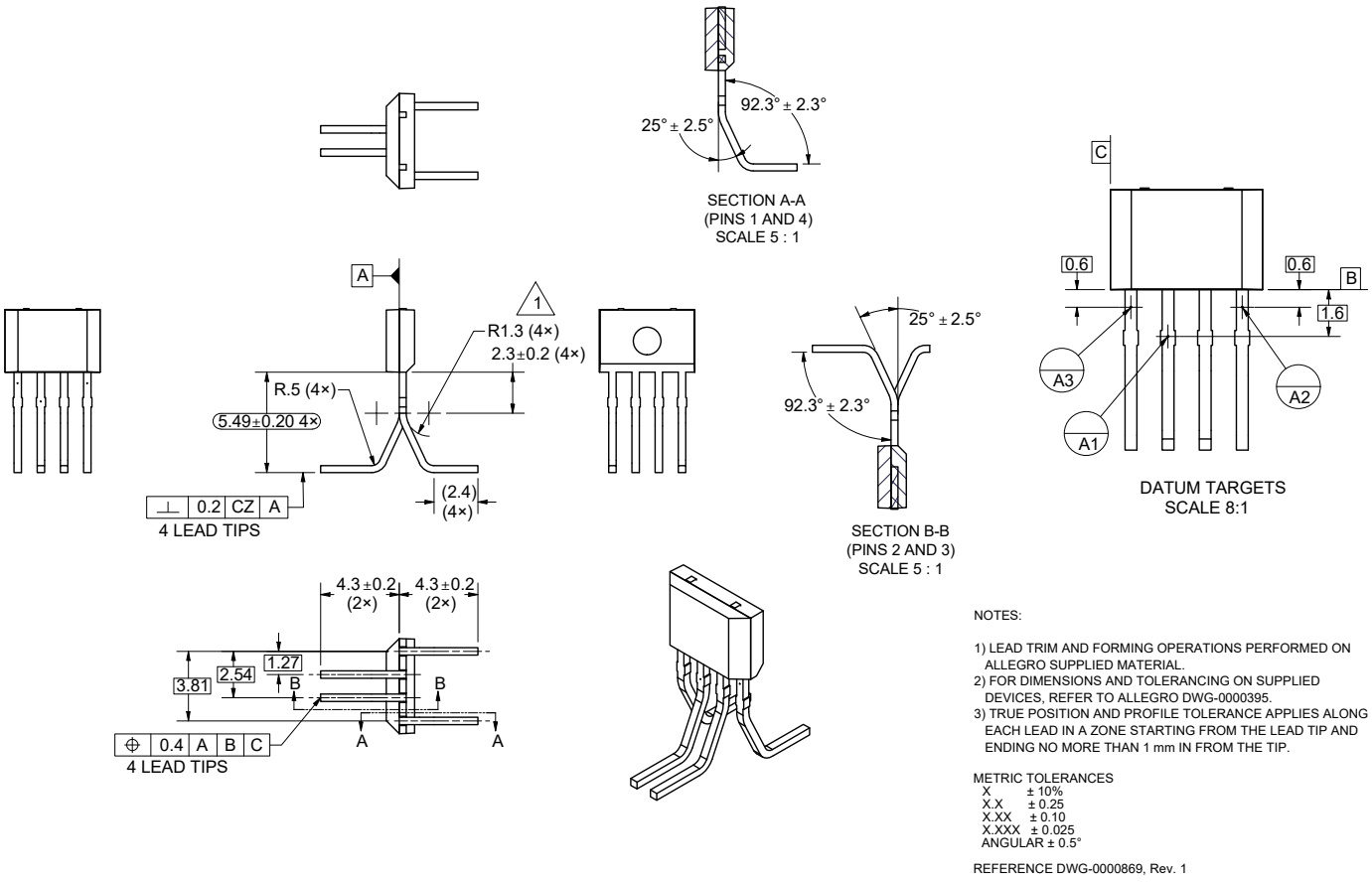

NOTES:

1) LEAD TRIM AND FORMING OPERATIONS PERFORMED ON ALLEGRO SUPPLIED MATERIAL.
2) FOR DIMENSIONS AND TOLERANCING ON SUPPLIED DEVICES, REFER TO ALLEGRO DWG-0000395.
3) TRUE POSITION AND PROFILE TOLERANCE APPLIES ALONG EACH LEAD IN A ZONE STARTING FROM THE LEAD TIP AND ENDING NO MORE THAN 1 mm IN FROM THE TIP.

METRIC TOLERANCES
X ± 10%
X.X ± 0.25
X.XX ± 0.10
X.XXX ± 0.025
ANGULAR ± 0.5°

REFERENCE DWG-0000869, Rev. 1

Figure 39: Package OK, 4-Pin SIP, TX Leadform

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REVISION HISTORY

Number	Date	Description
–	September 22, 2025	Initial release

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