ACS37800

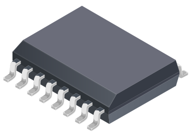
Isolated, Digital Output, Power Monitoring IC with Zero-Crossing Detection, Overcurrent and Overvoltage Flagging

FEATURES AND BENEFITS

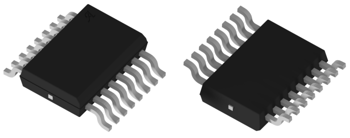
- Accurate power monitoring for AC and DC applications
- UL 62368-1 (edition 2) certified for reinforced isolation
- Accurate measurements of active, reactive, and apparent power, as well as power factor
- Separate RMS and instantaneous measurements for both voltage and current channels
- Two programmable averaging blocks
- Low primary conductor resistance for low power loss and high inrush current withstand capability
- Compatible with floating and non-floating GND
- Dedicated voltage or current zero crossing pin
- Fast, user-programmable overcurrent fault pin (5 µs typ.)
- User-programmable undervoltage and overvoltage RMS thresholds
- 1 kHz bandwidth
- Current sensing range up to 90 A
- Options for I^{2}C or SPI digital interface protocols

PACKAGE

16-pin SOICW (suffix MA)



16-pin SOICW (suffix MC)



Not to scale

DESCRIPTION

The Allegro ACS37800 power monitoring IC greatly simplifies the addition of power monitoring to many AC or DC powered systems. The sensor may be powered from the same supply as the system MCU, eliminating the need for multiple power supplies. The device construction includes a copper conduction path that generates a magnetic field proportional to applied current. The magnetic field is sensed differentially to reject errors introduced by common mode fields.

Allegro Hall-effect-based, galvanically isolated current sensing technology achieves reinforced isolation ratings in a small PCB footprint. These features enable isolated current sensing without expensive Rogowski coils, oversized current transformers, isolated operational amplifiers, or the power loss of shunt resistors.

The ACS37800 power monitoring IC offers key power measurement parameters that can easily be accessed through its SPI or I^{2}C digital protocol interfaces. Dedicated and configurable I/O pins for voltage/current zero crossing, undervoltage and overvoltage reporting, and fast overcurrent fault detection are available in I^{2}C mode. User configuration of the IC is available through on-chip EEPROM.

The ACS37800 is provided in the SOIC16 wide-body package, is lead (Pb) free, and is fully calibrated prior to shipment from the Allegro factory. Customer calibration can further increase accuracy in application.

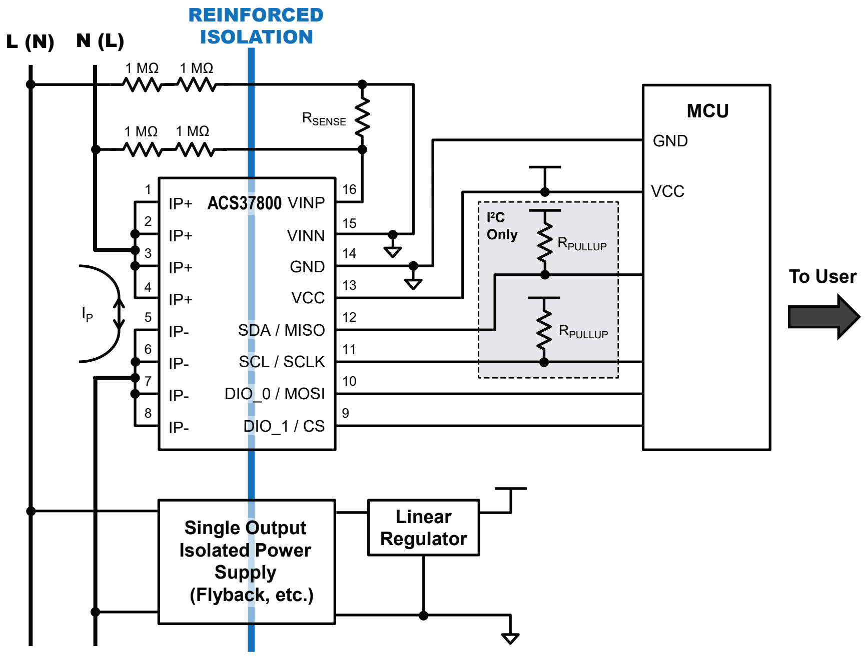
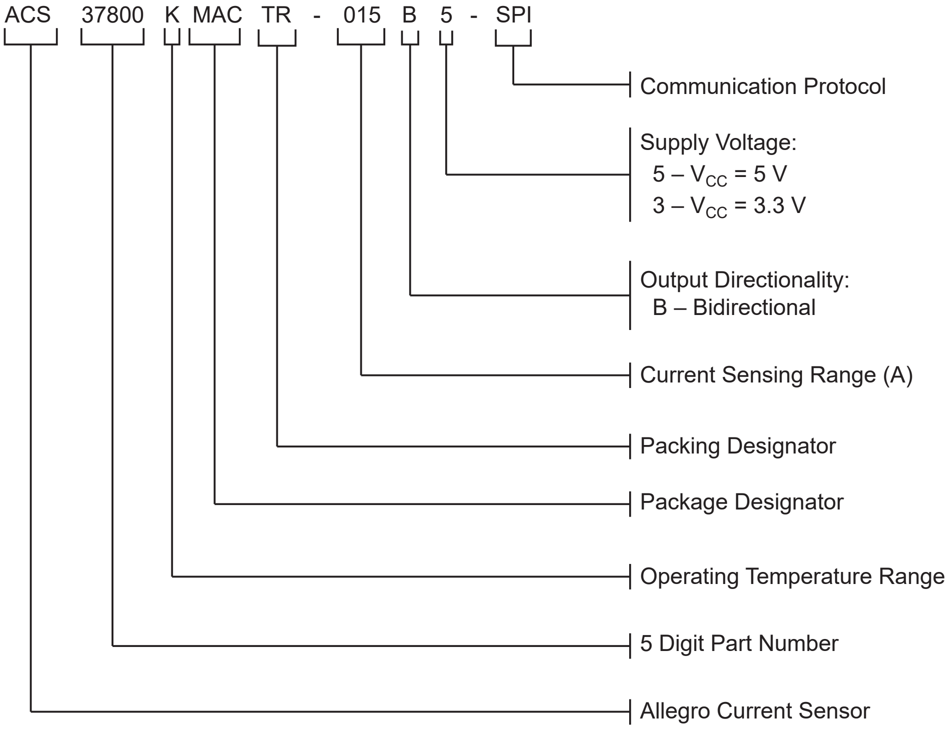


Figure 1: Typical Application

SELECTION GUIDE

Part Number	$V_{CC(typ)}$ (V)	I_{PR} Current Sensing Range (A)	Communication Protocol	Package	T_A (°C)	Packing
ACS37800KMACTR-015B5-SPI	5	±15	SPI	MA	–40 to 125	Tape and reel, 1000 pieces per reel, 3000 pieces per box
ACS37800KMACTR-030B3-SPI	3.3	±30				
ACS37800KMACTR-030B3-I2C	3.3	±30	I^2C			
ACS37800KMACTR-090B3-I2C	3.3	±90				
ACS37800KMCTR-030B5-SPI-A	5	±30	SPI	MC	–40 to 125	Tape and reel, 1000 pieces per reel, 3000 pieces per box
ACS37800KMCTR-030B3-SPI-A	3.3	±30				
ACS37800KMCTR-030B5-I2C-A	5	±30	I^2C			
ACS37800KMCTR-030B3-I2C-A	3.3	±30				



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{CC}		6.5	V
Reverse Supply Voltage	V_{RCC}		–0.5	V
Input Voltage	V_{INP}, V_{INN}		V_{CC} + 0.5	V
Reverse Input Voltage	V_{RNP}, V_{RNN}		–0.5	V
Digital I/O Voltage	V_{DIO}	SPI, I^2C, and general purpose I/O	6	V
Reverse Digital I/O Voltage	V_{RDIO}		–0.5	V
Operating Ambient Temperature	T_A	Range K	–40 to 125	°C
Junction Temperature	$T_{J(max)}$		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

MA PACKAGE ISOLATION CHARACTERISTICS

Characteristic	Symbol	Notes	Rating	Unit
Withstand Voltage [1][2]	V_{ISO}	Agency type-tested for 60 seconds per UL 62368-1 (edition 3)	5000	V_{RMS}
Working Voltage for Basic Isolation [2]	V_{WVBI}	Maximum approved working voltage for basic (single) isolation according to UL 62368-1 (edition 3)	1550	V_{PK} or VDC
			1097	V_{RMS}
Working Voltage for Reinforced Isolation [2]	V_{WVRI}	Maximum approved working voltage for reinforced isolation according to UL 62368-1 (edition 3)	800	V_{PK} or VDC
			565	V_{RMS}
Impulse Withstand Voltage [2]	$V_{IMPULSE}$	Tested ±5 pulses at 2/minute in compliance to IEC 61000-4-5, 1.2 µs (rise) / 50 µs (width)	6000	V_{PK}
Clearance	D_{CL}	Minimum distance through air from IP leads to signal leads	8	mm
Creepage	D_{CR}	Minimum distance along package body from IP leads to signal leads	8	mm
Distance Through Insulation	DTI	Minimum internal distance through insulation	105	µm
Comparative Tracking Index	CTI	Material Group II	400 to 599	V

[1] 100% Production-tested for 1 second in accordance with UL 62368-1 (edition 3).
[2] Certification pending.

MA PACKAGE CHARACTERISTICS

Characteristic	Symbol	Notes	Min.	Typ.	Max.	Unit
Internal Conductor Resistance	R_{IC}	T_A = 25°C	–	0.85	–	mΩ
Internal Conductor Inductance	L_{IC}	T_A = 25°C	–	4.2	–	nH
Moisture Sensitivity Level	MSL	Per IPC/JEDEC J-STD-020	–	3	–	–

MC PACKAGE ISOLATION CHARACTERISTICS

Characteristic	Symbol	Notes	Rating	Unit
Withstand Voltage [1][2]	V_{ISO}	Agency type-tested for 60 seconds per UL 62368-1 (edition 3)	5000	V_{RMS}
Working Voltage for Basic Isolation [2]	V_{WVBI}	Maximum approved working voltage for basic (single) isolation according to UL 62368-1 (edition 3)	1618	V_{PK} or VDC
			1160	V_{RMS}
Working Voltage for Reinforced Isolation [2]	V_{WVRI}	Maximum approved working voltage for reinforced isolation according to UL 62368-1 (edition 3)	809	V_{PK} or VDC
			580	V_{RMS}
Impulse Withstand Voltage [2]	$V_{IMPULSE}$	Tested ±5 pulses at 2/minute in compliance to IEC 61000-4-5, 1.2 µs (rise) / 50 µs (width)	6000	V_{PK}
Clearance	D_{cl}	Minimum distance through air from IP leads to signal leads	8.7	mm
Creepage	D_{cr}	Minimum distance along package body from IP leads to signal leads	8.7	mm
Distance Through Insulation	DTI	Minimum internal distance through insulation	110	µm
Comparative Tracking Index	CTI	Material Group II	400 to 599	V

[1] 100% Production-tested for 1 second in accordance with UL 62368-1 (edition 3).

[2] Certification pending.

MC PACKAGE CHARACTERISTICS

Characteristic	Symbol	Notes	Min.	Typ.	Max.	Unit
Internal Conductor Resistance	R_{IC}	T_A = 25°C	–	0.265	–	mΩ
Internal Conductor Inductance	L_{IC}	T_A = 25°C	–	4.5	–	nH
Moisture Sensitivity Level	MSL	Per IPC/JEDEC J-STD-020	–	3	–	–

THERMAL CHARACTERISTICS

Characteristic	Symbol	Notes	Value	Unit
MA Package, 16-Pin SOICW				
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	Mounted on the standard MA/LA Current Sensor Evaluation Board (ACSEVB-MA16-LA16)	20	°C/W
Package Thermal Metric (Junction to Top)	Ψ_{JT}		2.4	°C/W
Package Thermal Resistance (Junction to Case)	$R_{\theta JC}$	Simulated per the methods in JESD51-1	14	°C/W
Package Thermal Resistance (Junction to Board)	$R_{\theta JB}$	Simulated per the methods in JESD51-8	14	°C/W
MC Package, 16-Pin SOICW				
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	Mounted on the standard MC Current Sensor Evaluation Board (ACSEVB-MC16)	19	°C/W
Package Thermal Characterization (Junction to Top)	Ψ_{JT}		2.4	°C/W
Package Thermal Resistance (Junction to Case)	$R_{\theta JC}$	Simulated per the methods in JESD51-1	15	°C/W
Package Thermal Resistance (Junction to Board)	$R_{\theta JB}$	Simulated per the methods in JESD51-8	7.3	°C/W

FUNCTIONAL BLOCK DIAGRAM

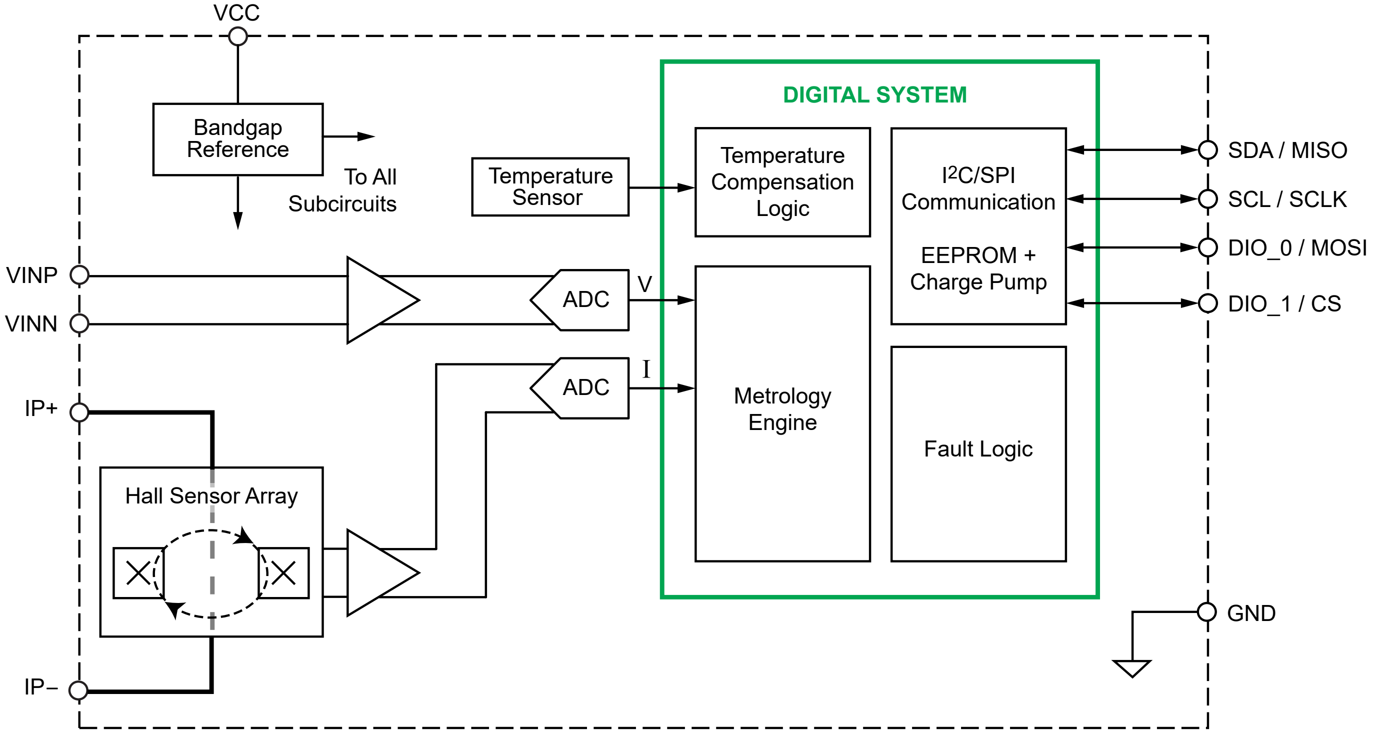
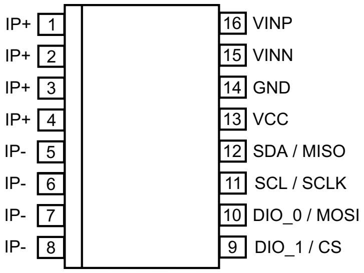


Figure 2: Functional Block Diagram

PINOUT DIAGRAM AND TERMINAL LIST



Pinout Diagram

Terminal List Table

Number	Name	Description	
		I²C	**SPI**
1, 2, 3, 4	IP+	Terminals for current being sensed; connected internally	
5, 6, 7, 8	IP-	Terminals for current being sensed; connected internally	
9	DIO_1 / CS	Digital I/O 1	Chip Select (CS)
10	DIO_0 / MOSI	Digital I/O 0	MOSI
11	SCL / SCLK	SCL	SCLK
12	SDA / MISO	SDA	MISO
13	VCC	Device power supply terminal	
14	GND	Device ground terminal	
15	VINN	Negative input voltage (always connect to GND)	
16	VINP	Positive input voltage	

Table of Contents

COMMON ELECTRICAL CHARACTERISTICS [1]: Valid through the full range of T_A and $V_{CC} = V_{CC(typ)}$, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}	5 V variant	4.5	5	5.5	V
		3.3 V variant	2.97	3.3	3.63	V
Supply Current	I_{CC}	$V_{CC(min)} \le V_{CC} \le V_{CC(max)}$, no load on output pins	–	12	15	mA
Supply Bypass Capacitor	C_{BYPASS}	V_{CC} to GND recommended	0.1	–	–	µF
Power-On Time	t_{PO}		–	90	–	µs
VOLTAGE INPUT BUFFER						
Differential Input Range	ΔV_{INR}	$\Delta V_{IN} = V_{INP} – V_{INN(GND)}$	–250	–	250	mV
Dynamic Input Frequency	f_{dyn_in}	BYPASS_N_EN = 0	35	–	300	Hz
VOLTAGE CHANNEL ADC						
Sample Frequency	f_{S_V}		–	32	–	kHz
Number of Bits	ADC_{V_B}		–	16	–	bits
ADC Full-Scale	ADC_{V_FS}	$\Delta V_{IN} = \pm 250$ mV, V_{INN}= GND	–27500	–	27500	codes
Sensitivity	$Sens_{(V)}$	$\Delta V_{INR(min)} < \Delta V_{IN} < \Delta V_{INR(max)}$	–	110	–	LSB / mV
Voltage Channel Power Supply Error	PSE_{V_O}	Ratio of change on V_{CC} to change in offset at DC, 100% ±10% $V_{CC(typ)}$	–7	–	7	codes / %V_{CC}
	PSE_{V_S}	Ratio of change on V_{CC} to change in sensitivity at DC, 100% ±10% $V_{CC(typ)}$	–0.1	–	0.1	% / %V_{CC}
Voltage Channel Power Supply Rejection Ratio	$PSRR_{V\_O}$	Ratio of change on V_{CC} to change in offset, 10 Hz to 10 kHz, 10% $V_{CC(pk-pk)}$	60	70	–	dB
	$PSRR_{V\_S}$	Ratio of change on V_{CC} to change in sensitivity, 10 Hz to 10 kHz, 10% $V_{CC(pk-pk)}$	60	75	–	dB
VOLTAGE CHANNEL						
Internal Bandwidth	BW		–	1	–	kHz
RMS Noise	N_V	Input referred	–	±0.3	–	mV
Linearity Error	E_{LIN_V}		–	±0.2	–	%
CURRENT CHANNEL						
Sample Frequency	f_{S_C}		–	32	–	kHz
Number of Bits	ADC_{I_B}		–	16	–	bits
ADC Full-Scale	ADC_{I_FS}	$I_P = I_{PR(min)}$ or $I_{PR(max)}$	–27500	–	27500	codes
Current Channel Power Supply Error	PSE_{I_O}	Ratio of change on V_{CC} to change in offset at DC, 100% ±10% $V_{CC(typ)}$	–60	–	60	codes / %V_{CC}
	PSE_{I_S}	Ratio of change on V_{CC} to change in sensitivity at DC, 100% ±10% $V_{CC(typ)}$	–0.3	–	0.3	% / %V_{CC}
Current Channel Power Supply Rejection Ratio	$PSRR_{I\_O}$	Ratio of change on V_{CC} to change in offset, 10 Hz to 10 kHz, 10% $V_{CC(pk-pk)}$	60	65	–	dB
	$PSRR_{I\_S}$	Ratio of change on V_{CC} to change in sensitivity, 10 Hz to 10 kHz, 10% $V_{CC(pk-pk)}$	20	40	–	dB
Internal Bandwidth	BW		–	1	–	kHz

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COMMON ELECTRICAL CHARACTERISTICS [1] (continued): Valid through the full range of T_A and $V_{CC} = V_{CC(typ)}$, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
CURRENT CHANNEL (continued)						
RMS Noise	N_I	MA only, input referred	–	±0.1	–	A
		MC only, input referred	–	±0.23	–	A
Linearity Error	E_{LIN_I}		–	±1.5	–	%
OVERCURRENT FAULT CHARACTERISTICS						
Fault Response Time	t_{RF}	Time from I_P rising above I_{FAULT} until $V_{FAULT} < V_{FAULT(max)}$ for a current step from 0 to 1.2 × I_{FAULT}; 10 kΩ and 100 pF from DIO_1 to ground; FLTDLY = 0	–	5	–	µs
Internal Bandwidth	BW		–	200	–	kHz
Fault Hysteresis [2]	I_{HYST}		–	0.06 × FS	–	A
Fault Range	I_{FAULT}	Set using FAULT field in EEPROM	0.65 × FS	–	2.00 × FS	A
VOLTAGE ZERO CROSSING						
Voltage Zero-Crossing Delay	t_d		–	250	–	µs
DIO PINS						
DIO Output High Level	$V_{OH(DIO)}$	V_{CC} = 3.3 V	3	–	–	V
DIO Output Low Level	$V_{OL(DIO)}$	V_{CC} = 3.3 V	–	–	0.3	V
DIO Input Voltage for Address Selection 0	V_{ADD0}	V_{CC} = 3.3 V	–	0	–	V
DIO Input Voltage for Address Selection 1	V_{ADD1}	V_{CC} = 3.3 V	–	1.1	–	V
DIO Input Voltage for Address Selection 2	V_{ADD2}	V_{CC} = 3.3 V	–	2.2	–	V
DIO Input Voltage for Address Selection 3	V_{ADD3}	V_{CC} = 3.3 V	–	3.3	–	V

[1] Device may be operated at higher primary current levels (I_P), ambient temperatures (T_A), and internal leadframe temperatures, provided that the maximum junction temperature ($T_{J(max)}$) is not exceeded.

[2] After I_P goes above I_{FAULT}, tripping the internal fault comparator, I_P must go below $I_{FAULT} - I_{HYST}$ before the internal fault comparator will reset.

ACS37800KMC-XXXB5-A PERFORMANCE CHARACTERISTICS: Valid through the full operating temperature range, T_A = –40°C to 125°C, C_{BYPASS} = 0.1 µF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min. [1]	Typ.	Max. [1]	Unit
GENERAL CHARACTERISTICS						
Nominal Supply Voltage	$V_{CC(typ)}$		–	5	–	V
NOMINAL PERFORMANCE – FACTORY CURRENT CHANNEL						
Current Sensing Range	I_{PR}	DIG_CRS_SNS_I = 2	–30	–	30	A
Sensitivity	$Sens_{(I)}$	$I_{PR(min)} < I_P < I_{PR(max)}$, DIG_CRS_SNS_I = 2	–	916.7	–	LSB/A
NOMINAL PERFORMANCE – INPUT REFERRED FACTORY POWER (POWER SEEN BY THE DEVICE) [2]						
Active Power Sensitivity	$Sens_{Pd\_act}$		–3.08	–	3.08	LSB/mW
Imaginary Power Sensitivity	$Sens_{Pd\_img}$		–6.15	–	6.15	LSB/mVAR
Apparent Power Sensitivity	$Sens_{Pd\_app}$		–6.15	–	6.15	LSB/mVA
TOTAL OUTPUT ERROR COMPONENTS [3] **– CURRENT CHANNEL**						
Sensitivity Error	$E_{SENS(I)}$	Measured at $I_P = I_{PR(max)}$, T_A = 25°C to 125°C	–1.9	–	1.9	%
		Measured at $I_P = I_{PR(max)}$, T_A = –40°C to 25°C	–2.4	–	2.4	%
Offset Error	$E_{O(I)}$	I_P = 0 A, T_A = 25°C to 125°C, DIG_CRS_SNS_I = 0	–312	–	312	LSB
		I_P = 0 A, T_A = –40°C to 25°C, DIG_CRS_SNS_I = 0	–390	–	390	LSB
Input Referred Offset Error	$E_{O(I)}$	I_P = 0 A, T_A = 25°C to 125°C	–340	–	340	mA
		I_P = 0 A, T_A = –40°C to 25°C	–426	–	426	mA
Total Output Error	$E_{TOT(I)}$	Measured at $I_P = I_{PR(max)}$, T_A = 25°C to 125°C	–2.6	–	2.6	%
		Measured at $I_P = I_{PR(max)}$, T_A = –40°C to 25°C	–3.3	–	3.3	%
TOTAL OUTPUT ERROR COMPONENTS [3] **– VOLTAGE CHANNEL**						
Sensitivity Error	$E_{SENS(V)}$	Measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = 25°C to 125°C	–1.3	–	1.3	%
		Measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = –40°C to 25°C	–1.5	–	1.5	%
Offset Error	$E_{O(V)}$	ΔV_{IN} = 0 mV, T_A = 25°C to 125°C	–40	–	40	LSB
		ΔV_{IN} = 0 mV, T_A = –40°C to 25°C	–30	–	30	LSB
Total Output Error	$E_{TOT(V)}$	Measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = 25°C to 125°C	–1.3	–	1.3	%
		Measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = –40°C to 25°C	–1.6	–	1.6	%
ACCURACY PERFORMANCE – ACTIVE POWER						
Total Output Error	$E_{TOT(P)}$	$I_P = I_{PR(max)}$, measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = 25°C to 125°C	–2.5	–	2.5	%
		$I_P = I_{PR(max)}$, measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = –40°C to 25°C	–4	–	4	%

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ACS37800KMC-XXXB5-A PERFORMANCE CHARACTERISTICS: Valid through the full operating temperature range, T_A = –40°C to 125°C, C_{BYPASS} = 0.1 µF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min. [1]	Typ.	Max. [1]	Unit
TOTAL OUTPUT ERROR COMPONENTS INCLUDING LIFETIME [3] – CURRENT CHANNEL						
Sensitivity Error	$E_{SENS(I)}$	Measured at $I_P = I_{PR(max)}$, T_A = 25°C to 125°C	–3.4	–	3.4	%
		Measured at $I_P = I_{PR(max)}$, T_A = –40°C to 25°C	–3.5	–	3.5	%
Offset Error	$E_{O(I)}$	I_P = 0 A, T_A = 25°C to 125°C, DIG_CRS_SNS_I = 0	–304	–	304	LSB
		I_P = 0 A, T_A = –40°C to 25°C, DIG_CRS_SNS_I = 0	–400	–	400	LSB
Input Referred Offset Error	$E_{O(I)}$	I_P = 0 A, T_A = 25°C to 125°C	–332	–	332	mA
		I_P = 0 A, T_A = –40°C to 25°C	–436	–	436	mA
Total Output Error	$E_{TOT(I)}$	Measured at $I_P = I_{PR(max)}$, T_A = 25°C to 125°C	–3.4	–	3.4	%
		Measured at $I_P = I_{PR(max)}$, T_A = –40°C to 25°C	–4.4	–	4.4	%
TOTAL OUTPUT ERROR COMPONENTS INCLUDING LIFETIME [3] – VOLTAGE CHANNEL						
Sensitivity Error	$E_{SENS(V)}$	Measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = 25°C to 125°C	–1.5	–	1.5	%
		Measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = –40°C to 25°C	–1.8	–	1.8	%
Offset Error	$E_{O(V)}$	ΔV_{IN} = 0 mV, T_A = 25°C to 125°C	–39	–	39	LSB
		ΔV_{IN} = 0 mV, T_A = –40°C to 25°C	–31	–	31	LSB
Total Output Error	$E_{TOT(V)}$	Measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = 25°C to 125°C	–1.6	–	1.6	%
		Measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = –40°C to 25°C	–1.9	–	1.9	%
ACCURACY PERFORMANCE INCLUDING LIFETIME – ACTIVE POWER						
Total Output Error	$E_{TOT(P)}$	$I_P = I_{PR(max)}$, measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = 25°C to 125°C	–4	–	4	%
		$I_P = I_{PR(max)}$, measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = –40°C to 25°C	–5	–	5	%

[1] "Min." and "Max." interval for performance characteristics is determined such that 99.73% of devices lie within the interval during initial characterization. The worst case of mean ±3 σ was calculated and applied symmetrically. These values can drift after solder reflow and over lifetime operation.

[2] These sensitivity characteristics are referred to the inputs seen by the device, i.e. the voltage channel resistor divider must be accounted to determine the system sensitivies.

[3] E_{TOT} = E_{SENS} + 100 x V_{OE}/(Sens x I_P)

ACS37800KMC-XXXB3-A PERFORMANCE CHARACTERISTICS: Valid through the full operating temperature range, T_A = –40°C to 125°C, C_{BYPASS} = 0.1 µF, and V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min. [1]	Typ.	Max. [1]	Unit
GENERAL CHARACTERISTICS						
Nominal Supply Voltage	$V_{CC(typ)}$		–	3.3	–	V
NOMINAL PERFORMANCE – CURRENT CHANNEL						
Current Sensing Range	I_{PR}	DIG_CRS_SNS_I = 2	–30	–	30	A
Sensitivity	$Sens_{(I)}$	$I_{PR(min)} < I_P < I_{PR(max)}$, DIG_CRS_SNS_I = 2	–	916.7	–	LSB/A
NOMINAL PERFORMANCE – INPUT REFERRED FACTORY POWER (POWER SEEN BY THE DEVICE) [2]						
Active Power Sensitivity	$Sens_{Pd\_act}$		–3.08	–	3.08	LSB/mW
Imaginary Power Sensitivity	$Sens_{Pd\_img}$		–6.15	–	6.15	LSB/mVAR
Apparent Power Sensitivity	$Sens_{Pd\_app}$		–6.15	–	6.15	LSB/mVA
TOTAL OUTPUT ERROR COMPONENTS [3] **– CURRENT CHANNEL**						
Sensitivity Error	$E_{SENS(I)}$	Measured at $I_P = I_{PR(max)}$, T_A = 25°C to 125°C	–1.3	–	1.3	%
		Measured at $I_P = I_{PR(max)}$, T_A = –40°C to 25°C	–1.9	–	1.9	%
Offset Error	$E_{O(I)}$	I_P = 0 A, T_A = 25°C to 125°C, DIG_CRS_SNS_I = 0	–421	–	421	LSB
		I_P = 0 A, T_A = –40°C to 25°C, DIG_CRS_SNS_I = 0	–620	–	620	LSB
Input Referred Offset Error	$E_{O(I)}$	I_P = 0 A, T_A = 25°C to 125°C	–460	–	460	mA
		I_P = 0 A, T_A = –40°C to 25°C	–677	–	677	mA
Total Output Error	$E_{TOT(I)}$	Measured at $I_P = I_{PR(max)}$, T_A = 25°C to 125°C	–2.5	–	2.5	%
		Measured at $I_P = I_{PR(max)}$, T_A = –40°C to 25°C	–3.7	–	3.7	%
TOTAL OUTPUT ERROR COMPONENTS [3] **– VOLTAGE CHANNEL**						
Sensitivity Error	$E_{SENS(V)}$	Measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = 25°C to 125°C	–1.0	–	1.0	%
		Measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = –40°C to 25°C	–1.1	–	1.1	%
Offset Error	$E_{O(V)}$	ΔV_{IN} = 0 mV, T_A = 25°C to 125°C	–25	–	25	LSB
		ΔV_{IN} = 0 mV, T_A = –40°C to 25°C	–25	–	25	LSB
Total Output Error	$E_{TOT(V)}$	Measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = 25°C to 125°C	–1.0	–	1.0	%
		Measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = –40°C to 25°C	–1.1	–	1.1	%
ACCURACY PERFORMANCE – ACTIVE POWER						
Total Output Error	$E_{TOT(P)}$	$I_P = I_{PR(max)}$, measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = 25°C to 125°C	–2.8	–	2.8	%
		$I_P = I_{PR(max)}$, measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = –40°C to 25°C	–4.0	–	4.0	%

Continued on next page...

ACS37800KMC-XXXB3-A PERFORMANCE CHARACTERISTICS: Valid through the full operating temperature range, T_A = –40°C to 125°C, C_{BYPASS} = 0.1 µF, and V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min. [1]	Typ.	Max. [1]	Unit
TOTAL OUTPUT ERROR COMPONENTS INCLUDING LIFETIME [3] – CURRENT CHANNEL						
Sensitivity Error	$E_{SENS(I)}$	Measured at $I_P = I_{PR(max)}$, T_A = 25°C to 125°C	–1.7	–	1.7	%
		Measured at $I_P = I_{PR(max)}$, T_A = –40°C to 25°C	–2.9	–	2.9	%
Offset Error	$E_{O(I)}$	I_P = 0 A, T_A = 25°C to 125°C, DIG_CRS_SNS_I = 0	–449	–	449	LSB
		I_P = 0 A, T_A = –40°C to 25°C, DIG_CRS_SNS_I = 0	–651	–	651	LSB
Input Referred Offset Error	$E_{O(I)}$	I_P = 0 A, T_A = 25°C to 125°C	–490	–	490	A
		I_P = 0 A, T_A = –40°C to 25°C	–710	–	710	A
Total Output Error	$E_{TOT(I)}$	Measured at $I_P = I_{PR(max)}$, T_A = 25°C to 125°C	–3	–	3	%
		Measured at $I_P = I_{PR(max)}$, T_A = –40°C to 25°C	–4.5	–	4.5	%
TOTAL OUTPUT ERROR COMPONENTS INCLUDING LIFETIME [3] – VOLTAGE CHANNEL						
Sensitivity Error	$E_{SENS(V)}$	Measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = 25°C to 125°C	–1	–	1	%
		Measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = –40°C to 25°C	–1.3	–	1.3	%
Offset Error	$E_{O(V)}$	ΔV_{IN} = 0 mV, T_A = 25°C to 125°C	–40	–	40	LSB
		ΔV_{IN} = 0 mV, T_A = –40°C to 25°C	–31	–	31	LSB
Total Output Error	$E_{TOT(V)}$	Measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = 25°C to 125°C	–1.1	–	1.1	%
		Measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = –40°C to 25°C	–1.4	–	1.4	%
ACCURACY PERFORMANCE INCLUDING LIFETIME – ACTIVE POWER						
Total Output Error	$E_{TOT(P)}$	$I_P = I_{PR(max)}$, measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = 25°C to 125°C	–3	–	3	%
		$I_P = I_{PR(max)}$, measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = –40°C to 25°C	–4.5	–	4.5	%

[1] "Min." and "Max." interval for performance characteristics is determined such that 99.73% of devices lie within the interval during initial characterization. The worst case of mean ±3 σ was calculated and applied symmetrically. These values can drift after solder reflow and over lifetime operation.

[2] These sensitivity characteristics are referred to the inputs seen by the device, i.e. the voltage channel resistor divider must be accounted to determine the system sensitivies.

[3] $E_{TOT} = E_{SENS} + 100 \times V_{OE}/(Sens \times I_P)$

ACS37800KMAC-015B5 PERFORMANCE CHARACTERISTICS: Valid through the full operating temperature range, T_A = –40°C to 125°C, C_{BYPASS} = 0.1 µF, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min. [1]	Typ.	Max. [1]	Unit
GENERAL CHARACTERISTICS						
Nominal Supply Voltage	$V_{CC(typ)}$		–	5	–	V
NOMINAL PERFORMANCE – FACTORY CURRENT CHANNEL						
Current Sensing Range	I_{PR}		–15	–	15	A
Sensitivity	$Sens_{(I)}$	$I_{PR(min)} < I_P < I_{PR(max)}$	–	1833.3	–	LSB/A
NOMINAL PERFORMANCE – INPUT REFERRED FACTORY POWER (POWER SEEN BY THE DEVICE) [2]						
Active Power Sensitivity	$Sens_{Pd\_act}$		–6.15	–	6.15	LSB/mW
Imaginary Power Sensitivity	$Sens_{Pd\_img}$		–12.31	–	12.31	LSB/mVAR
Apparent Power Sensitivity	$Sens_{Pd\_app}$		–12.31	–	12.31	LSB/mVA
TOTAL OUTPUT ERROR COMPONENTS [3] – CURRENT CHANNEL						
Sensitivity Error	$E_{SENS(I)}$	Measured at $I_P = I_{PR(max)}$, T_A = 25°C to 125°C	–1.1	–	1.1	%
		Measured at $I_P = I_{PR(max)}$, T_A = –40°C to 25°C	–1.5	–	1.5	%
Offset Error	$E_{O(I)}$	I_P = 0 A, T_A = 25°C to 125°C	–720	–	720	LSB
		I_P = 0 A, T_A = –40°C to 25°C	–780	–	780	LSB
Total Output Error	$E_{TOT(I)}$	Measured at $I_P = I_{PR(max)}$, T_A = 25°C to 125°C	–2.1	–	2.1	%
		Measured at $I_P = I_{PR(max)}$, T_A = –40°C to 25°C	–2.7	–	2.7	%
TOTAL OUTPUT ERROR COMPONENTS [3] – VOLTAGE CHANNEL						
Sensitivity Error	$E_{SENS(V)}$	Measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = 25°C to 125°C	–1.2	–	1.2	%
		Measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = –40°C to 25°C	–1.2	–	1.2	%
Offset Error	$E_{O(V)}$	ΔV_{IN} = 0 mV, T_A = 25°C to 125°C	–55	–	55	LSB
		ΔV_{IN} = 0 mV, T_A = –40°C to 25°C	–55	–	55	LSB
Total Output Error	$E_{TOT(V)}$	Measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = 25°C to 125°C	–1.4	–	1.4	%
		Measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = –40°C to 25°C	–1.4	–	1.4	%
ACCURACY PERFORMANCE – ACTIVE POWER						
Total Output Error	$E_{TOT(P)}$	$I_P = I_{PR(max)}$, measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = 25°C to 125°C	–2.1	–	2.1	%
		$I_P = I_{PR(max)}$, measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = –40°C to 25°C	–3	–	3	%

[1] "Min." and "Max." interval for performance characteristics is determined such that 99.73% of devices lie within the interval during initial characterization. The worst case of mean ±3 σ was calculated and applied symmetrically. These values can drift after solder reflow and over lifetime operation.

[2] These sensitivity characteristics are referred to the inputs seen by the device, i.e. the voltage channel resistor divider must be accounted to determine the system sensitivities.

[3] $E_{TOT} = E_{SENS} + 100 \times V_{OE}/(Sens \times I_P)$

ACS37800KMAC-030B3 PERFORMANCE CHARACTERISTICS: Valid through the full operating temperature range, T_A = –40°C to 125°C, C_{BYPASS} = 0.1 µF, and V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min. [1]	Typ.	Max. [1]	Unit
GENERAL CHARACTERISTICS						
Nominal Supply Voltage	$V_{CC(typ)}$		–	3.3	–	V
NOMINAL PERFORMANCE – CURRENT CHANNEL						
Current Sensing Range	I_{PR}		–30	–	30	A
Sensitivity	$Sens_{(I)}$	$I_{PR(min)} < I_P < I_{PR(max)}$	–	916.7	–	LSB/A
NOMINAL PERFORMANCE – INPUT REFERRED FACTORY POWER (POWER SEEN BY THE DEVICE) [2]						
Active Power Sensitivity	$Sens_{Pd\_act}$		–3.0	–	3.08	LSB/mW
Imaginary Power Sensitivity	$Sens_{Pd\_img}$		–	–	6.15	LSB/mVAR
Apparent Power Sensitivity	$Sens_{Pd\_app}$		–	–	6.15	LSB/mVA
TOTAL OUTPUT ERROR COMPONENTS [3] – CURRENT CHANNEL						
Sensitivity Error	$E_{SENS(I)}$	Measured at $I_P = I_{PR(max)}$, T_A = 25°C to 125°C	–1	–	1	%
		Measured at $I_P = I_{PR(max)}$, T_A = –40°C to 25°C	–1.5	–	1.5	%
Offset Error	$E_{O(I)}$	I_P = 0 A, T_A = 25°C to 125°C	–510	–	510	LSB
		I_P = 0 A, T_A = –40°C to 25°C	–570	–	570	LSB
Total Output Error	$E_{TOT(I)}$	Measured at $I_P = I_{PR(max)}$, T_A = 25°C to 125°C	–2	–	2	%
		Measured at $I_P = I_{PR(max)}$, T_A = –40°C to 25°C	–2.7	–	2.7	%
TOTAL OUTPUT ERROR COMPONENTS [3] – VOLTAGE CHANNEL						
Sensitivity Error	$E_{SENS(V)}$	Measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = 25°C to 125°C	–0.75	–	0.75	%
		Measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = –40°C to 25°C	–0.75	–	0.75	%
Offset Error	$E_{O(V)}$	ΔV_{IN} = 0 mV, T_A = 25°C to 125°C	–55	–	55	LSB
		ΔV_{IN} = 0 mV, T_A = –40°C to 25°C	–55	–	55	LSB
Total Output Error	$E_{TOT(V)}$	Measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = 25°C to 125°C	–1	–	1	%
		Measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = –40°C to 25°C	–1	–	1	%
ACCURACY PERFORMANCE – ACTIVE POWER						
Total Output Error	$E_{TOT(P)}$	$I_P = I_{PR(max)}$, measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = 25°C to 125°C	–2.1	–	2.1	%
		$I_P = I_{PR(max)}$, measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = –40°C to 25°C	–3	–	3	%

[1] "Min." and "Max." interval for performance characteristics is determined such that 99.73% of devices lie within the interval during initial characterization. The worst case of mean ±3 σ was calculated and applied symmetrically. These values can drift after solder reflow and over lifetime operation.

[2] These sensitivity characteristics are referred to the inputs seen by the device, i.e. the voltage channel resistor divider must be accounted to determine the system sensitivies.

[3] $E_{TOT} = E_{SENS} + 100 \times V_{OE}/(Sens \times I_P)$

ACS37800KMAC-090B3 PERFORMANCE CHARACTERISTICS: Valid through the full operating temperature range, T_A = –40°C to 125°C, C_{BYPASS} = 0.1 µF, and V_{CC} = 3.3 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min. [1]	Typ.	Max. [1]	Unit
GENERAL CHARACTERISTICS						
Nominal Supply Voltage	$V_{CC(typ)}$		–	3.3	–	V
NOMINAL PERFORMANCE – CURRENT CHANNEL						
Current Sensing Range	I_{PR}		–90	–	90	A
Sensitivity	$Sens_{(I)}$	$I_{PR(min)} < I_P < I_{PR(max)}$	–	305.6	–	LSB/A
NOMINAL PERFORMANCE – INPUT REFERRED FACTORY POWER (POWER SEEN BY THE DEVICE) [2]						
Active Power Sensitivity	$Sens_{Pd\_act}$		–1.03	–	1.03	LSB/mW
Imaginary Power Sensitivity	$Sens_{Pd\_img}$		–2.05	–	2.05	LSB/mVAR
Apparent Power Sensitivity	$Sens_{Pd\_app}$		–2.05	–	2.05	LSB/mVA
TOTAL OUTPUT ERROR COMPONENTS [3] – CURRENT CHANNEL						
Sensitivity Error	$E_{SENS(I)}$	Measured at $I_P = I_{PR(max)}$, T_A = 25°C to 125°C	–1	–	1	%
		Measured at $I_P = I_{PR(max)}$, T_A = –40°C to 25°C	–1.5	–	1.5	%
Offset Error	$E_{O(I)}$	I_P = 0 A, T_A = 25°C to 125°C	–180	–	180	LSB
		I_P = 0 A, T_A = –40°C to 25°C	–210	–	210	LSB
Total Output Error	$E_{TOT(I)}$	Measured at I_P = 45 A, T_A = 25°C to 125°C	–2	–	2	%
		Measured at I_P = 45 A, T_A = –40°C to 25°C	–2.6	–	2.6	%
TOTAL OUTPUT ERROR COMPONENTS [3] – VOLTAGE CHANNEL						
Sensitivity Error	$E_{SENS(V)}$	Measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = 25°C to 125°C	–0.75	–	0.75	%
		Measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = –40°C to 25°C	–0.75	–	0.75	%
Offset Error	$E_{O(V)}$	ΔV_{IN} = 0 mV, T_A = 25°C to 125°C	–55	–	55	LSB
		ΔV_{IN} = 0 mV, T_A = –40°C to 25°C	–55	–	55	LSB
Total Output Error	$E_{TOT(V)}$	Measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = 25°C to 125°C	–1	–	1	%
		Measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = –40°C to 25°C	–1	–	1	%
ACCURACY PERFORMANCE – ACTIVE POWER						
Total Output Error	$E_{TOT(P)}$	I_P = 45 A, measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = 25°C to 125°C	–1.3	–	1.3	%
		I_P = 45 A, measured at $\Delta V_{IN} = \Delta V_{INR(max)}$, T_A = –40°C to 25°C	–2.1	–	2.1	%

[1] "Min." and "Max." interval for performance characteristics is determined such that 99.73% of devices lie within the interval during initial characterization. The worst case of mean ±3 σ was calculated and applied symmetrically. These values can drift after solder reflow and over lifetime operation

[2] These sensitivity characteristics are referred to the inputs seen by the device, i.e. the voltage channel resistor divider must be accounted to determine the system sensitivies.

[3] $E_{TOT} = E_{SENS} + 100 \times V_{OE}/(Sens \times I_P)$

xKMACTR-I2C OPERATING CHARACTERISTICS [1]: Valid through the full range of T_A, $V_{CC} = V_{CC(typ)}$, R_{EXT} = 10 kΩ, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
I²C INTERFACE CHARACTERISTICS [2]						
Bus Free Time Between Stop and Start	t_{BUF}		1.3	–	–	μs
Hold Time Start Condition	t_{hdSTA}		0.6	–	–	μs
Setup Time for Repeated Start Condition	t_{suSTA}		0.6	–	–	μs
SCL Low Time	t_{LOW}		1.3	–	–	μs
SCL High Time	t_{HIGH}		0.6	–	–	μs
Data Setup Time	t_{suDAT}		100	–	–	μs
Data Hold Time	t_{hdDAT}		0	–	900	μs
Setup Time for Stop Condition	t_{suSTO}		0.6	–	–	μs
Logic Input Low Level (SDA, SCL pins)	V_{IL}		–	–	30	$\%V_{CC}$
Logic Input High Level (SDA, SCL pins)	V_{IH}		70	–	–	$\%V_{CC}$
Logic Input Current	I_{IN}	Input voltage on SDA or SCL = 0 V to V_{CC}	–1	–	1	μA
Output Low Voltage (SDA)	V_{OL}	SDA sinking = 1.5 mA	–	–	0.36	V
Clock Frequency (SCL pin)	f_{CLK}		–	–	400	kHz
Output Fall Time (SDA pin)	t_f	R_{EXT} = 2.4 kΩ, C_B = 100 pF	–	–	250	ns
I²C Pull-Up Resistance	R_{EXT}		2.4	10	–	kΩ
Total Capacitive Load for Each of SDA and SCL Buses	C_B		–	–	20	pF

[1] Validated by characterization and design.
[2] These values are ratiometric to the supply voltage. I²C Interface Characteristics are ensured by design and not factory tested.

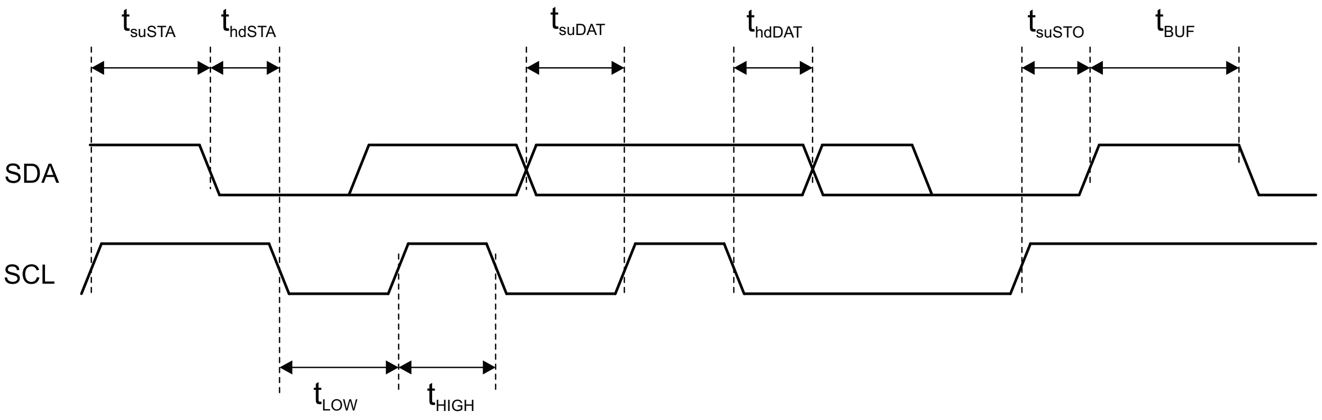


Figure 3: I²C Interface Timing

xKMATR-SPI OPERATING CHARACTERISTICS [1]: Valid through the full range of T_A, $V_{CC} = V_{CC(typ)}$, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SPI INTERFACE CHARACTERISTICS						
Digital Input High Voltage	V_{IH}	MOSI, SCLK, CS pins, V_{CC} = 3.3 V	2.8	–	3.63	V
		MOSI, SCLK, CS pins, V_{CC} = 5 V	4	–	5.5	V
Digital Input Low Voltage	V_{IL}	MOSI, SCLK, CS pins	–	–	0.5	V
SPI Output High Voltage	V_{OH}	MISO pin, C_L = 20 pF, T_A = 25°C, $V_{CC(typ)}$ = 3.3 V	2.8	3.3	3.8	V
		MISO pin, C_L = 20 pF, T_A = 25°C, $V_{CC(typ)}$ = 5 V	4	5	5.5	V
SPI Output Low Voltage	V_{OL}	MISO pin, C_L = 20 pF, T_A = 25°C	–	0.3	0.5	V
SPI Clock Frequency	f_{SCLK}	MISO pin, C_L = 20 pF	0.1	–	10	MHz
SPI Frame Rate	t_{SPI}		5.8	–	588	kHz
Chip Select to First SCLK Edge	t_{CS}	Time from CS going low to SCLK falling edge	50	–	–	ns
Data Output Valid Time	t_{DAV}	Data output valid after SCLK falling edge	–	40	–	ns
MOSI Setup Time	t_{SU}	Input setup time before SCLK rising edge	25	–	–	ns
MOSI Hold Time	t_{HD}	Input hold time after SCLK rising edge	50	–	–	ns
SCLK to CS Hold Time	t_{CHD}	Hold SCLK high time before CS rising edge	5	–	–	ns
Load Capacitance	C_L	Loading on digital output (MISO) pin	–	–	20	pF

[1] Validated by characterization and design.

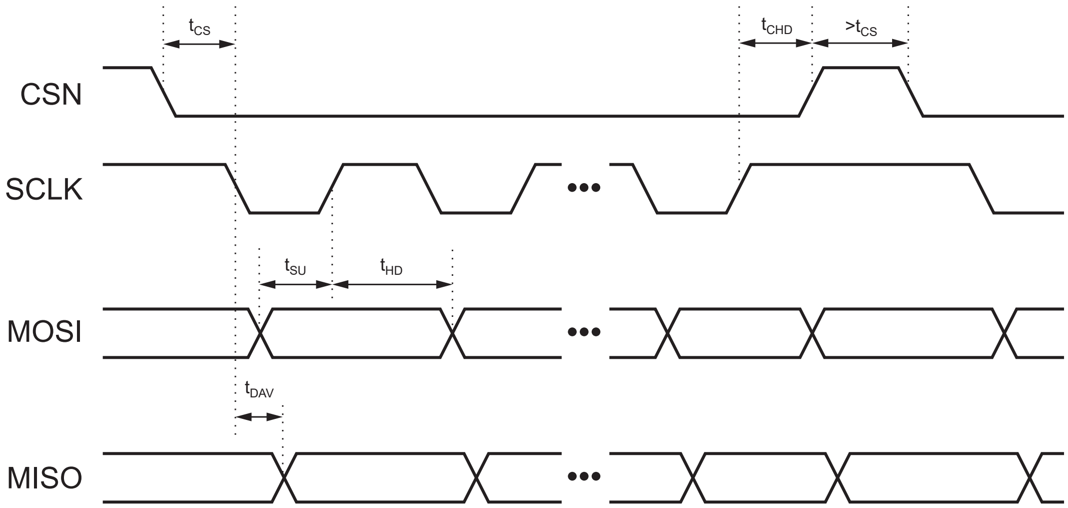


Figure 4: SPI Timing

THEORY OF OPERATION

Introduction

The ACS37800 provides a simple solution for voltage, current, and power monitoring in 60 Hz AC and DC applications and is particularly well suited for high isolation. The voltage is measured by resistor dividing it down to fit the input range of the on-board voltage sense amplifier, as well as to add isolation. The current is measured using the integrated current loop and galvanically isolated Hall sensor. Both analog signals are then sampled using high accuracy ADCs before entering the digital system. Here, the metrology engine is used to determine frequency, calculate RMS values of current, voltage, and power, as well as provide a range of averaging and configuration options. One can choose to read out all the different information provided using SPI or I^2C. When using I^2C, there are also options for using some of the digital I/O pins for overcurrent or zero crossing detection. Overall, with a high degree of configurability and integrated features, the ACS37800 can fit most power monitoring applications. The following sections will help explain in more detail these features and configuration options, as well as how to best use the ACS37800 for particular applications.

Voltage and Current Measurements

The main signal paths for the current and voltage measurement, through the ADCs and internal filtering, have a bandwidth of 1 kHz and an update rate of 32 kHz. These “instantaneous” current and voltage measurements are stored in the ICODES and VCODES fields. The instantaneous apparent power, which is the product of ICODES and VCODES, is stored in the field PINSTANT.

Overcurrent Measurement Path

A separate filter on the current ADC is used to create a lower resolution but higher bandwidth sample rate measurement of the current to be used for overcurrent detection. This filter outputs a 12-bit word at a 1 MHz update rate and 200 kHz bandwidth. The overcurrent fault logic compares this auxiliary current value to the user-defined overcurrent fault threshold, defined by the field FAULT.

It is important to note that the trim for the main 16-bit current path is also applied to the overcurrent path, such that the overcurrent fault has the same level of accuracy as the main signal path.

Trim Methods

The trim logic for the voltage and current channels is depicted in Figure 5 and Figure 6. Refer to the Register Details section for more information regarding trim fields. In general, each channel, voltage and current, is trimmed for gain and offset both at room and over temperature. This trim is done before the ICODES and VCODES registers. The user has the ability to trim the nominal room temperature value.

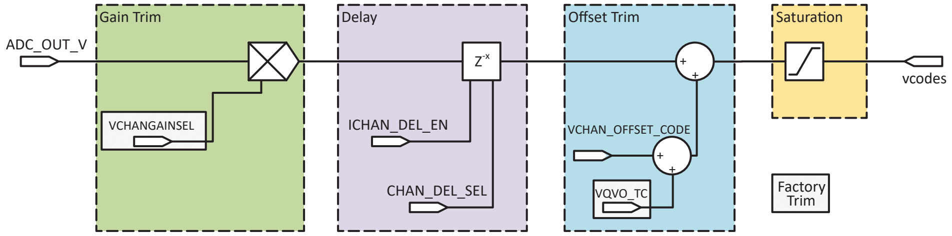


Figure 5: Voltage Channel Trim Flow

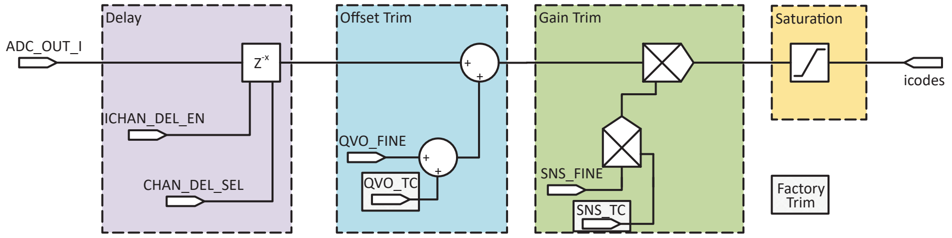


Figure 6: Current Channel Trim Flow

Power Calculations

VOLTAGE ZERO CROSSING

The RMS and power calculations of the ACS37800 are calculated over a window of N samples. By default, this window is calculated dynamically based on the zero crossings of the voltage signal. A rising voltage zero crossing triggers the start of a new window. N then increases with each 32 kHz sample until the next rising voltage zero crossing, recording the current and voltage readings at each sample. This ends the calculation window, and all RMS and power calculations are performed on the saved data. During this time, the next calculation window is started.

Voltage zero crossings are detected with time-based hysteresis that removes the possibility of noise causing multiple zero crossings to be reported at each true zero crossing.

I_{RMS} AND V_{RMS}

The cycle-by-cycle calculation of the root mean square of both the current and voltage channels is:

$$I_{RMS} = \sqrt{\frac{\sum_{n=0}^{n=N-1} I_n^2}{N}} \qquad V_{RMS} = \sqrt{\frac{\sum_{n=0}^{n=N-1} V_n^2}{N}}$$

where I_n (ICODES) and V_n (VCODES) are the instantaneous measurements of current and voltage, respectively.

APPARENT POWER

The magnitude of the complex power being measured; calculated at the end of each cycle is:

$$|S| = I_{RMS} \times V_{RMS}$$

ACTIVE POWER

The real component of power being measured, calculated cycle by cycle is:

$$P_{ACTIVE} = \frac{\sum_{n=0}^{n=N-1} P_n}{N} \qquad P_n = I_n \times V_n$$

REACTIVE POWER

The imaginary component of power being measured, calculated at the end of each cycle is:

$$Q = \sqrt{S^2 - P_{ACTIVE}^{\ \ 2}}$$

POWER FACTOR

The magnitude of the ratio of the real power to apparent power, calculated at the end of each cycle is:

$$|PF| = \frac{P_{ACTIVE}}{|S|}$$

LEADING OR LAGGING POWER FACTOR

The current leading or lagging voltage is communicated as a single bit, POSANGLE. This bit represents the sign of the reactive power. The sign of the reactive power is determined by comparing the timing of the zero crossings of the current and voltage. As such, it is only meaningful in the case of a linear load.

The sign of the reactive power, POSANGLE, along with the sign of the power factor, POSPF, can be used to determine whether the load is inductive or capacitive, as well as whether power is being generated or consumed. This is shown in the four-quadrant figure below (refer to Figure 7).

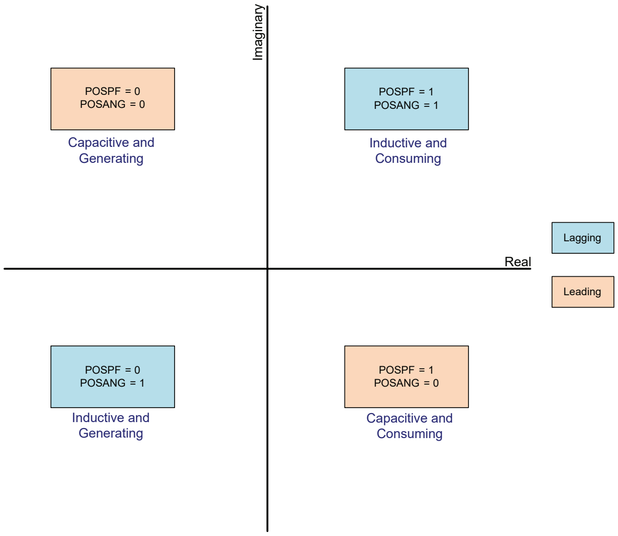


Figure 7: Four Quadrant, Power Factor

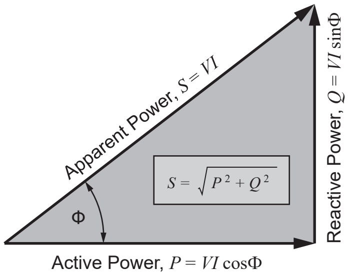


Figure 8: Power Triangle

OPERATIONAL BLOCK DIAGRAM

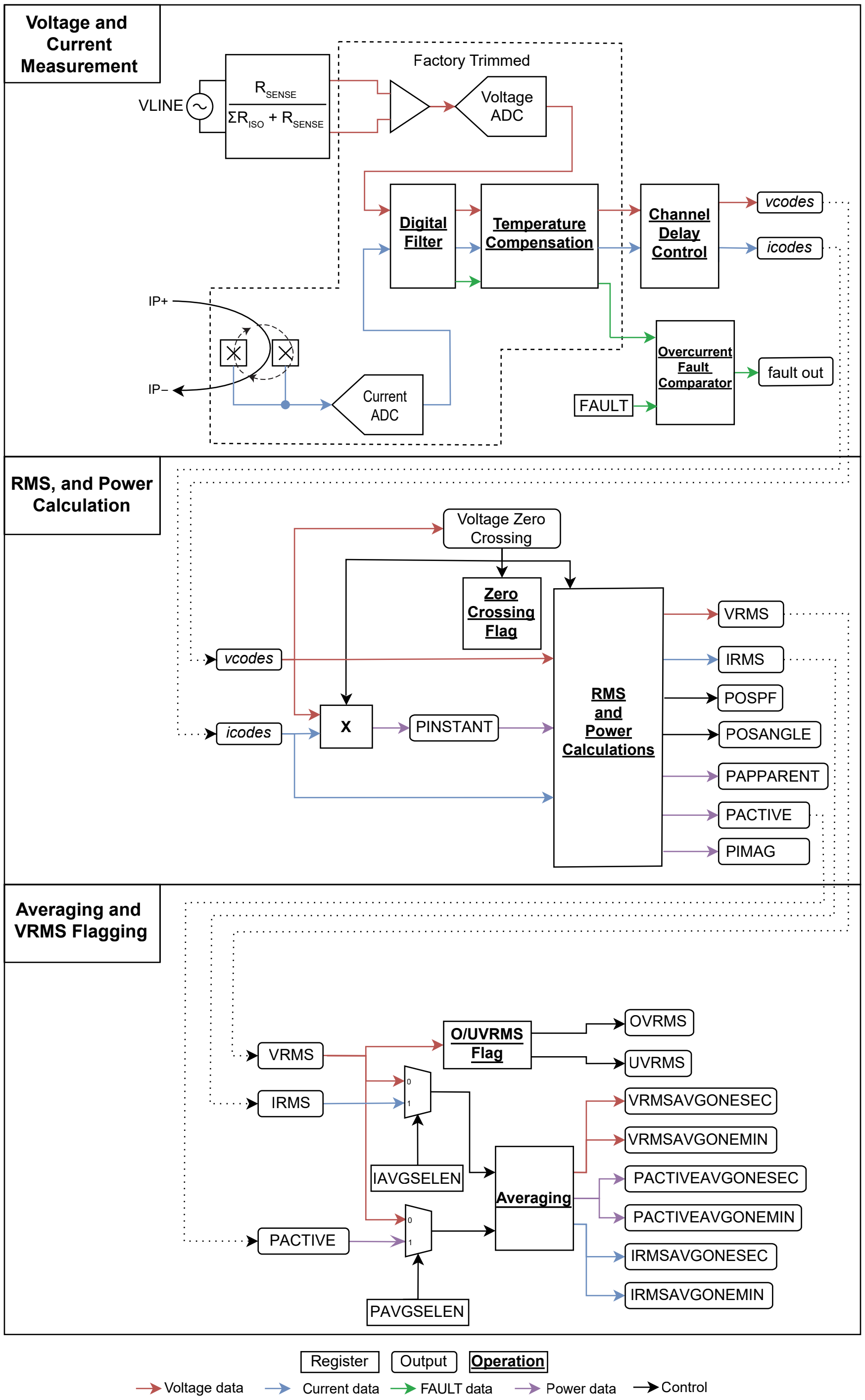


Figure 9: Operational Block Diagram

Configurable Settings

PHASE DELAY

Phase delay may be introduced on either the voltage or current channel to account for known phase delay at other points in the system using the ICHAN_DEL_EN and CHAN_DEL_SEL fields. ICHAN_DEL_EN determines if the voltage channel or current channel will be delayed. The chosen channel will be delayed by the configured amount in CHAN_DEL_SEL, up to 5° of delay.

AVERAGING CHANNEL

The ACS37800 contains two averaging paths. V_{RMS}, I_{RMS}, and P_{ACTIVE} can be routed to these average blocks as shown in Figure 9 using IAVGSELEN and PAVGSELEN.

AVERAGING TIME

Each averaging path on the ACS37800 consists of two averaging blocks that each allow for a configurable number of averages based on the EEPROM fields RMS_AVG_1 and RMS_AVG_2.

The output of the first averaging block feeds into the input of the second averaging block. The output of each block is accessible for each channel.

OVERVOLTAGE AND UNDERVOLTAGE DETECTION FOR VRMS

This device has programmable overvoltage and undervoltage RMS flags that will signal when the VRMS is above or below the respective thresholds. The VRMS is compared to the overvoltage and undervoltage RMS thresholds set by the fields OVERVREG and UNDERVREG to determine a flag condition. The number of successive sample sets required to trigger either the overvoltage or undervoltage RMS flag can be set by the VEVENT_CYCS field.

The OVRMS and UVRMS flags can be routed to the DIO pins when the device is used in I^{2}C mode. See Configuring the DIO Pins.

OVERCURRRENT DETECTION FOR INSTANTANEOUS CURRENT

The overcurrent fault threshold may be set from 0.65 × I_{PR} to 2.0 × I_{PR}. The user sets the trip point with the field FAULT. The user can add a digital delay to the overcurrent fault with the field FLT_DLY. Up to 32 µs delay can be added to the overcurrent fault.

BYPASSING THE DYNAMIC FRAMING OF THE RMS CALCULATION WINDOW

By default, the ACS37800 dynamically calculates the value of N to be used in the RMS and power calculations based on the zero crossings on the voltage channel. This functionality can be disabled using the BYPASS_N_EN field.

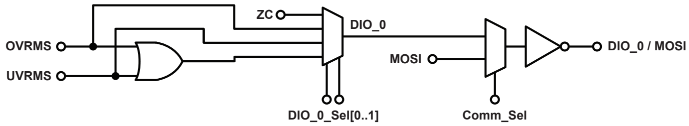
When BYPASS_N_EN = 1, it is important to define the number of samples used to calculate RMS. This can be done in the field N. The field N is the number of 32 kHz samples that are used to calculate the RMS. The minimum effective N that is used when calculating RMS is 4. If a value of less than 4 is chosen for N, then 4 is internally used. The first useable RMS calculation on start up with BYPASS_N_EN = 1 is after 2 × N samples.

Configuring the DIO Pins (I^{2}C Devices)

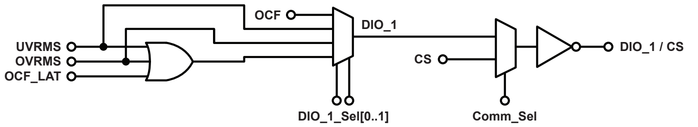
FLAGS TO BE ROUTED TO THE DIO PINS

When the device is configured to be in I^{2}C mode (COMM_SEL in EEPROM = 1), pins 9 and 10 become digital I/O pins, DIO_1 and DIO_0, respectively. The digital I/O pins are low true, meaning that a voltage below the DIO Output Low Level maximum ($V_{OL(DIO)max}$) is to be interpreted as logic 1 and a voltage above DIO Output High Level minimum ($V_{OH(DIO)min}$) is to be interpreted as a logic 0. The Digital I/O pins can be configured in EEPROM to represent the following functions:

DIO_0	
DIO_0_SEL value (EEPROM)	Function
0	ZC: zero crossing
1	OVRMS: the VRMS overvoltage flag
2	UVRMS: The VRMS undervoltage flag
3	The OR of OVRMS and UVRMS (if either flag is triggered, the DIO_0 pin will be asserted)



DIO_1	
DIO_1_SEL value (EEPROM)	Function
0	OCF: Overcurrent fault
1	UVRMS: The VRMS undervoltage flag
2	OVRMS: The VRMS overvoltage flag
3	The OR of OVRMS and UVRMS, and OCF_LAT [Latched Overcurrent Fault] (if any of the three flags are triggered, the DIO_1 pin will be asserted)



ZERO CROSSING OUTPUT CONFIGURATIONS

The dynamic calculation of N for the RMS and power calculations uses exclusively the voltage zero crossing, but both current and voltage zero crossing can be flagged and reported on the DIO pins.

Voltage Zero Crossing (VZC)

The voltage zero crossing has two basic modes of operation, pulse mode and square wave mode.

Pulse Mode – VZC

In pulse mode, a voltage zero crossing is reported as a short pulse. There are three available configurations to customize the voltage zero crossing pulse mode operation: rising or falling edge selection, every edge selection, and pulse width.

Rising Edge or Falling Edge Aligned Pulse

The EEPROM field ZEROCROSSEDGESEL is used to select whether the zero crossing output pulses are aligned to the rising zero crossing of the voltage channel or the falling zero crossing of the voltage channel.

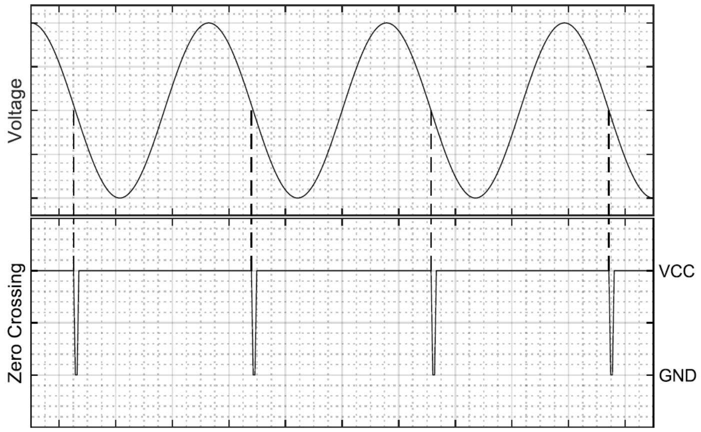


Figure 10: ZEROCROSSEDGESEL = 0, Falling Zero Crossing

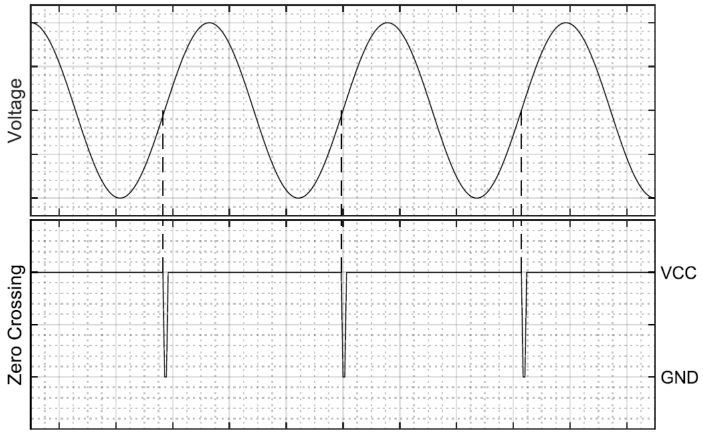


Figure 11: ZEROCROSSEDGESEL = 1, Rising Zero Crossing

Pulse Every Edge

The EEPROM field HALFCYCLE_EN is used to output a pulse at every zero crossing.

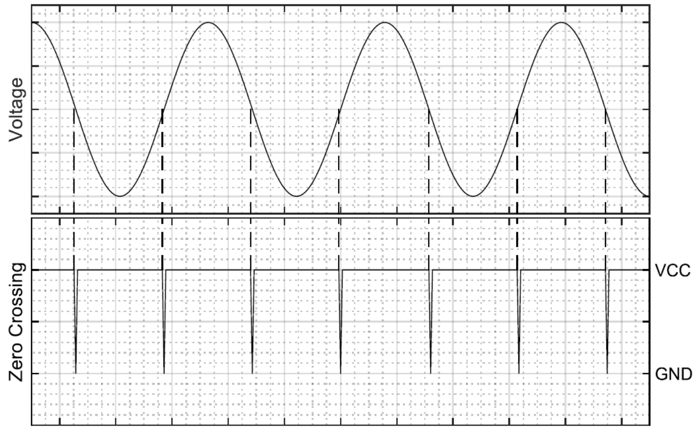


Figure 12: HALFCYCLE_EN = 1, Both Rising and Falling Zero Crossings Signaled

Pulse Width Selection

The EEPROM field DELAYCNT_SEL is used to select the width of the voltage zero crossing pulse.

Table 1: DELAYCNT_SEL

Range	Value	Units
0	32	µs
1	256	µs

Square Wave Mode

Square wave mode can be configured using the EEPROM field SQUAREWAVE_EN. In square wave mode, a voltage zero crossing is reported as a square wave that changes state on each reported zero crossing. The ZEROCROSSEDGESEL EEPROM field can be used to align the low to high transition of the flag with either the rising voltage zero crossing or the falling voltage zero crossing.

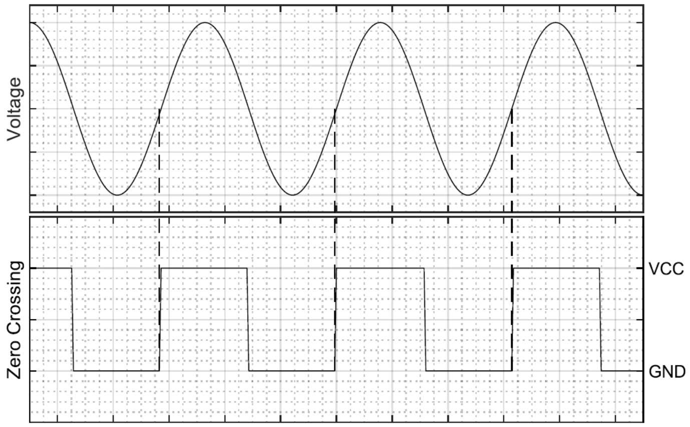


Figure 13: ZEROCROSSEDGESEL = 0, Square Wave Mode

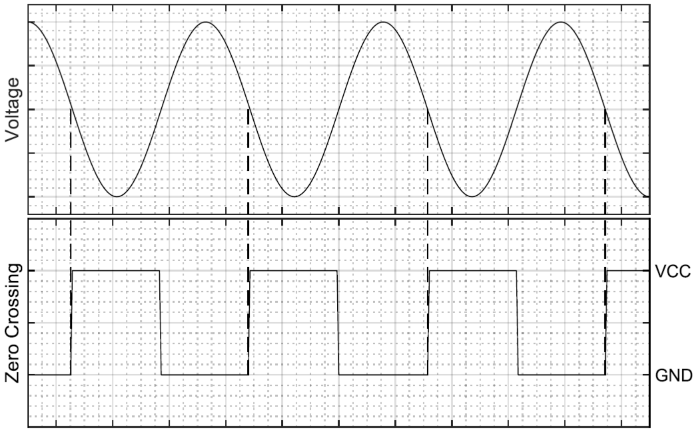


Figure 14: ZEROCROSSEDGESEL = 1, Square Wave Mode

Current Zero Crossing (CZC)

The current zero crossing function can be enabled using the EEPROM field ZEROCROSSCHANSEL. When the zero crossing flag is configured to flag zero crossings of the current path, this has no effect on the RMS and power calculations; the voltage zero crossing is still used for these calculations.

The current zero crossing has just one basic mode of operation: pulse mode.

Pulse Mode – CZC

In pulse mode, a current zero crossing is reported as a short pulse. There are three available configurations to customize the current zero crossing pulse mode operation: rising or falling edge selection, every edge selection, and pulse width.

Rising Edge or Falling Edge Aligned Pulse

The EEPROM field ZEROCROSSEDGESEL is used to select whether the zero crossing output pulses are aligned to the rising zero crossing of the current channel or the falling zero crossing of the current channel.

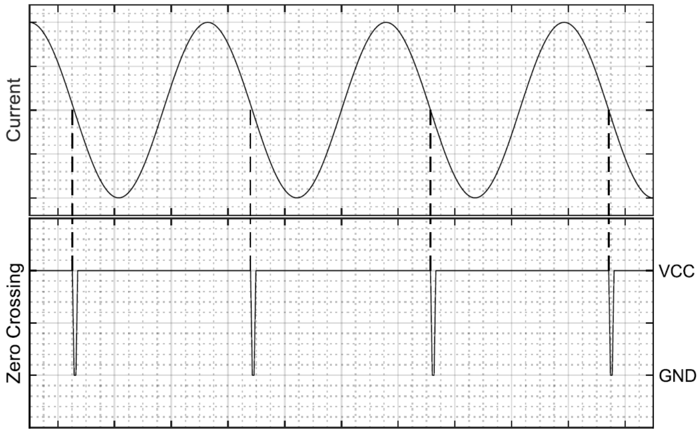


Figure 15: ZEROCROSSEDGESEL = 0, Falling Zero Crossing

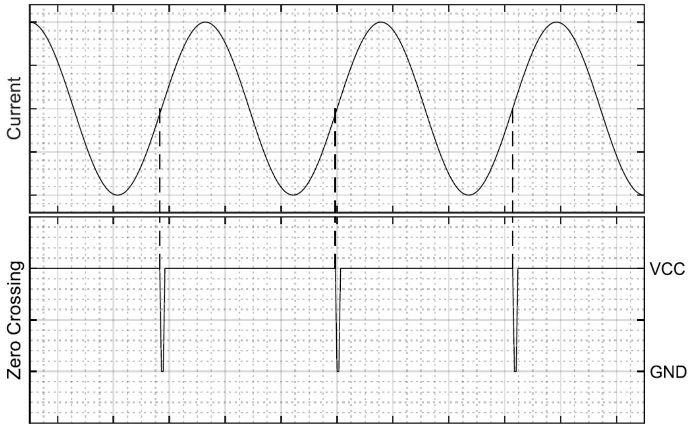


Figure 16: ZEROCROSSEDGESEL = 1, Rising Zero crossing

Pulse Every Edge

The EEPROM field HALFCYCLE_EN is used to output a pulse at every zero crossing.

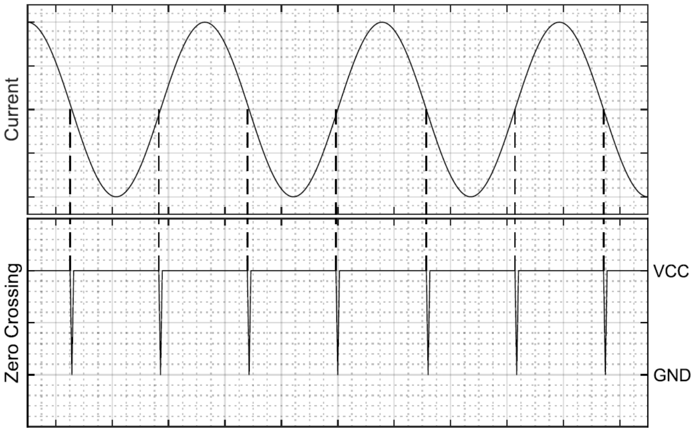


Figure 17: HALFCYCLE_EN = 1, Both Rising and Falling Zero Crossings Signaled

CONFIGURING THE DEVICE FOR AC APPLICATIONS

Device EEPROM Settings

For AC power monitoring applications using the ACS37800, the following device settings are recommended:

DYNAMIC CALCULATION OF N

Set BYPASS_N_EN = 0 (default). This setting enables the device to dynamically calculate N based off the voltage zero crossings. See the Register Details – EEPROM section for additional details.

Voltage Measurement

RECOMMENDED APPLICATION CIRCUITS

An important aspect to consider when designing in the ACS37800 into AC applications is the design of the voltage measurement path. Typically, a resistor divider network is employed to provide both isolation and transform the high voltage signal into the ±250 mV signal that the ACS37800 can measure.

There are two basic application circuits recommended based on the isolation requirements of the system. The first, see Figure 18, is to be used when the ACS37800 GND and the neutral terminal of the voltage input are connected. R_{ISO1}, R_{ISO2}, and R_{SENSE} form a resistor divider network where,

$$V_{IN} = V_{LINE} \times \frac{R_{SENSE}}{R_{ISO1} + R_{ISO2} + R_{SENSE}}$$

R_{ISO1} and R_{ISO2} should be equal. A value of 1 MΩ is appropriate for many applications, but ultimately, the resistance value used needs to comply with the required isolation of the system.

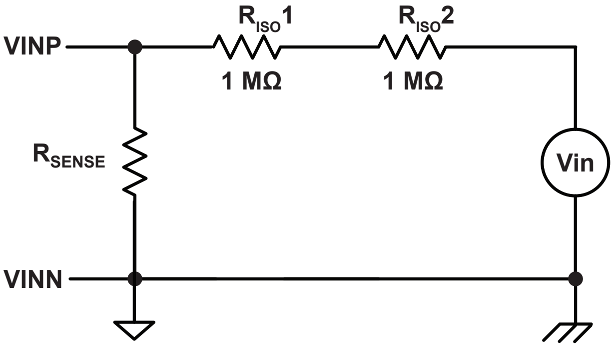


Figure 18: Voltage Channel Application Circuit; Device GND is Connected to Neutral

Another application circuit recommendation for the voltage channel is shown in Figure 19. This is to be used in systems where the ACS37800 GND and the neutral terminal of the voltage input are to be isolated. Here, R_{ISO3} and R_{ISO4} are added to the resistor divider network.

$$V_{IN} = V_{LINE} \times \frac{R_{SENSE}}{R_{ISO1} + R_{ISO2} + R_{ISO3} + R_{ISO4} + R_{SENSE}}$$

R_{ISO1}, R_{ISO2}, R_{ISO3}, and R_{ISO4} should be equal and their value is determined by the isolation requirements of the system. A value of 1 MΩ is appropriate for many applications, but ultimately, the resistance value used needs to comply with the required isolation of the system.

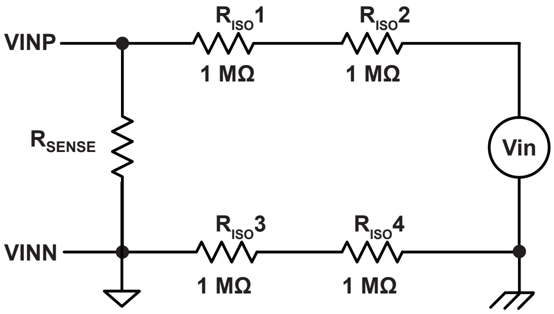


Figure 19: Voltage Channel Application; Device GND is Isolated from Neutral

To determine the value of R_{SENSE} required for a particular application using either of the recommended circuits, the following equation can be used:

$$R_{SENSE} = \frac{\Delta V_{INR(MAX)}}{V_{LINE(MAX)} - \Delta V_{INR(MAX)}} \times R_{ISO}$$

Where $\Delta V_{INR(MAX)} = 250$ mV, $V_{LINE(MAX)}$ is the maximum V_{LINE} voltage to be measured, and R_{ISO} is the sum of all of the isolation resistors.

If using the overvoltage detection functionality of the ACS37800, this should be considering when determining the maximum V_{LINE} voltage to be measured. For example, in an application when the nominal V_{LINE} is equal to 120 V_{RMS} and a 50% over-voltage detection is required, $V_{LINE(MAX)}$ is:

$$120\ V_{RMS} \times \sqrt{2} \times 1.5 = 255\ \text{V},$$

where the √2 is used to approximate the peak voltage assuming a sinusoidal input.

Additionally, the tolerance of the all resistors should be considered when determining R_{SENSE}. The minimum tolerance of the isolation resistors should be used along with the maximum tolerance of R_{SENSE}.

If the R_{SENSE} is not sized appropriately, this can lead to the voltage input to the ACS37800 exceeding the maximum input range, which can cause the instantaneous voltage measurement to saturate. This can lead to errors in the RMS calculations as shown in Figure 20.

After the resistor network is known, the VCODES and VRMS output fields can be interpreted to line voltages with the following method. Starting with known values for V_{LINE} to the V_{IN} resistor network, the user should calculate the actual R_{SENSE} scale factor, $SF_{Line2Device}$, using the following equation:

$$SF_{Line2Device} = \frac{R_{SENSE}}{(R_{SENSE} + \Sigma R_{ISO})} \times 1000\ {}^{mV}\!/_{V}$$

After the application scale factor is known, VCODES can be interpreted into line voltage using $SF_{Line2Device}$ and $Sens_{(V)}$ with the following equation:

$$V_{Line} = \frac{{}^{vcodes}\!/_{Sens_{(V)}}}{SF_{Line2Device}}$$

The full-scale line voltage occurs at VCODE = ± 27500 and VRMS = 55000, which is 0.84 of both the VCODES and VRMS whole registers. The VCODES and VRMS registers are the same size but, rms is unsigned so the same equivalent voltage between the two registers is VRMS = 2×|VCODES| which makes the V_{Line_RMS} calculation:

$$V_{Line\_RMS} = \frac{{}^{vrms}\!/_{(2 \times Sens_{(V)})}}{SF_{Line2Device}}$$

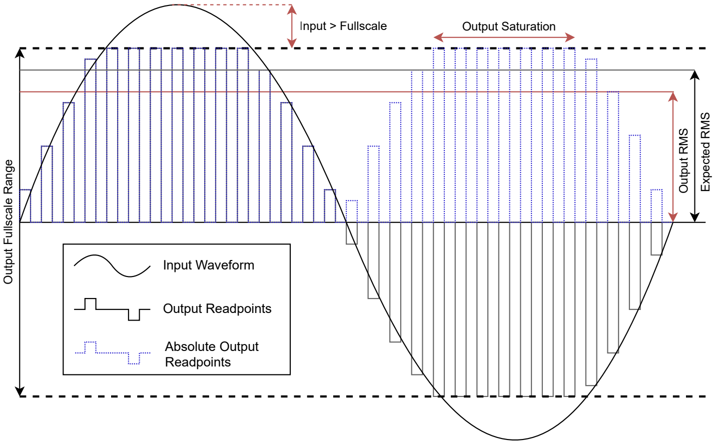


Figure 20: Output Saturation

Current Measurement

For the current path, there are two current ranges to consider: the range of RMS current to be measured and the range required for overcurrent fault detection.

When considering the range of RMS current to be measured, the Current Sensing Range (I_{PR}) is not to be exceeded. This can lead to saturation, as shown in Figure 20, and lead to error in the RMS calculations.

The overcurrent fault detection can exceed I_{PR} and is defined as Fault Range Max, $I_{FAULT(MAX)}$. Once the current exceeds I_{PR}, the RMS calculations will no longer be accurate.

CONFIGURING THE DEVICE FOR DC APPLICATIONS OR FOR APPLICATIONS WITH NO VOLTAGE ZERO CROSSING

The follow recommendations are provided for DC applications, as well as any other applications where there is no voltage zero crossing. Possible applications include current sensing only, sensing of a rectified voltage signal, or applications where the nominal frequency on the voltage channel is greater than 300 Hz.

Device EEPROM Settings

For DC power monitoring applications using the ACS37800 or applications only using the current measurement capability of the ACS37800, the following device settings are recommended.

FIXED SETTING OF N

Set BYPASS_N_EN = 1. This setting disables the dynamic calculation of *n* based off voltage zero crossings and sets N to a fixed value, which is set using EERPOM field N. See the Register Details – EEPROM section for additional details.

Voltage Measurement

RECOMMENDED APPLICATION CIRCUITS

The recommended application circuit for the voltage channel in DC operation is the same as the AC application circuit where Device GND is connected to Neutral (refer to Figure 18).

Current Measurement

The same considerations for AC applications can be used for the current path for DC applications.

Current Channel Trimming

To interpret the ICODES register into line current, the user can use $Sens_{(I)\_measured}$ to calculate the current most accurately or the user can assume $Sens_{(I)\_ideal}$ to calculate current. Regardless of the chosen $Sens_{(I)}$, the equation for line current, I_P, will be the same:

$$I_P = \frac{icodes}{Sens_{(I)}}$$

The user can also trim the current channels offset and gain. This is further described with the following recommended trim flow.

The current channels offset (QVO_FINE, bits 8:0) and gain (SENS_FINE, bits 18:9) can be trimmed with fields in EEPROM (0x0B) and shadow (0x1B). It is important to note that full-scale measurement current should not exceed code ±27500 in ICODES when trimming for the best accuracy performance. The recommended current channel trim flow starts with sensitivity trim:

1. Read and average ICODES over a second with two fully settled and measured applied currents.
    A. The device cannot be trimmed to be more accurate than the current forced and external measurement tolerances.
2. Calculate the devices initial $Sens_{(I)\_intial}$ with the following equation:

$$Sens_{(I)\_initial} = \frac{icodes_{2\_avg} - icodes_{1\_avg}}{I_{P\_2} - I_{P\_1}}$$

3. Read the initial SNS_FINE register (0x0B/0x1B, bits 18:9) value signed.
4. Change the SNS_FINE register by a fixed amount in the desired direction.
5. Repeat steps 1 and 2 to calculated $Sens_{(I)\_step}$.
6. The SNS_FINE step size can now be calculated by the following equation:

$$LSB_{sns\_fine} = \frac{Sens_{(I)\_step} - Sens_{(I)\_initial}}{sns\_fine_{step} - sens\_fine_{initial}}$$

7. Calculate the SENS_FINE change needed to reach the desired trim using the following equation:

$$sns\_fine_{new} = sns\_fine_{step} + \frac{Sens_{(I)\_step} - Sens_{(I)\_desired}}{LSB_{sns\_fine}}$$

8. Change SNS_FINE to the new calculated value in step 7.
9. Repeat step 1 and 2 to calculate $Sens_{(I)\_new}$.
10. Repeat steps 6-9 until the device is within ½ LSB_{sns_fine} or within error tolerance.

After the current channel sensitivity has been trim the offset can now be trimmed using the following steps:

1. Measure the initial quiescent code offset by reading and averaging ICODES over a second with no current running through the IP pins.
   A. Even small leakage currents can affect results.
2. Record the initial QVO_FINE register value (0x0B/0x1B, bits 8:0).
3. Change the QVO_FINE by a fixed amount towards signed 0.
4. Repeat step one to record the quiescent code offset with the applied change to QVO_FINE.
5. Calculate the step size of the QVO_FINE register using the following equation:

$$LSB_{qvo\_fine} = \frac{QVO_{step} - QVO_{intial}}{qvo\_fine_{step} - qvo\_fine_{initial}}$$

6. Calculate the new QVO_FINE value based on the QVO_{step} using the following equation:

$$qvo\_fine_{new} = qvo\_fine_{step} \frac{QVO_{step}}{LSB_{qvo\_fine}}$$

7. Repeat step 1 and record the new quiescent code offset.
8. Repeat steps 5-7 until the device is within ½ LSB_{qvo_fine} or within the error tolerance.

RMS AND POWER ACCURACY VS. OPERATION POINT

RMS and Power Output Error vs. Applied Input

When using the ACS37800 to measure for RMS calculations and power monitoring, it is important to consider the error specifications of the device.

For DC applications, the impact of offset and gain error on the final output is straightforward, but for RMS and power calculations, the impact of any errors, specifically offset errors, becomes dependent on the magnitude of the applied signal.

Figure 21 shows an example system where the maximum measurable power is ~1.3 kW, based on the system design. The over-temperature offset performance of the ACS37800 causes an error in the measured power that is larger when the applied power is close to 0 W.

The offset performance of the voltage channel is such that its contribution to this error is negligible. The current RMS measurement and the power calculations are where this error is observed.

The following figures (Figure 22 through Figure 27) display the measurement error for the RMS current and active power for each available device variant.

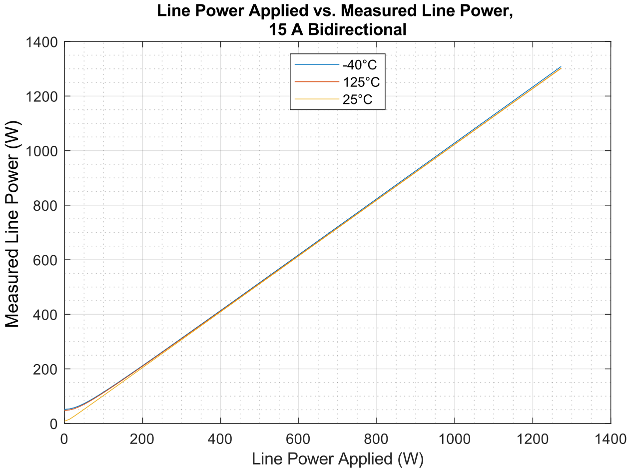


Figure 21: Line Power Applied (W) vs. Measured Line Power (W), 15B5 Device

15B5 I_{RMS} and Power Error

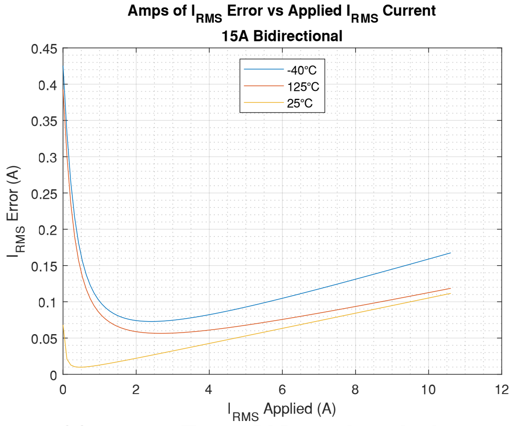


Figure 22: I_{RMS} Error [A] vs. Applied I_{RMS} [A]

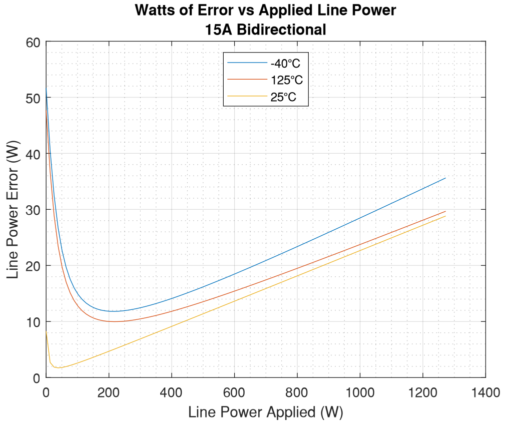


Figure 23: Line Power Error [W] vs. Applied Line Power [W]

30B3 I_{RMS} and Power Error

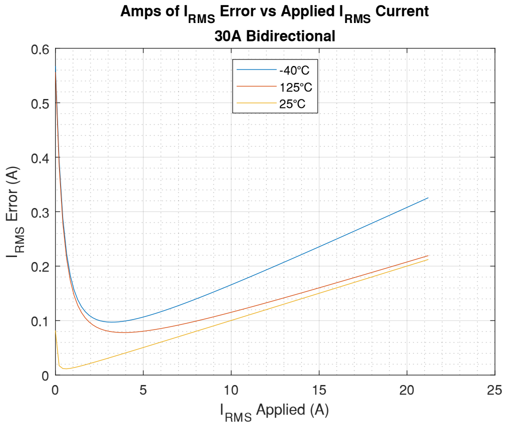


Figure 24: I_{RMS} Error [A] vs. Applied I_{RMS} [A]

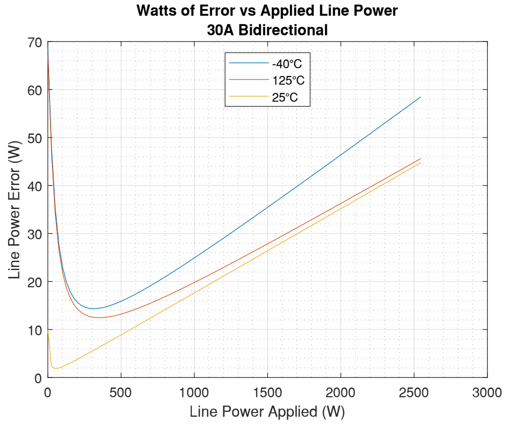


Figure 25: Line Power Error [W] vs. Applied Line Power [W]

90B3 I_{RMS} and Power Error

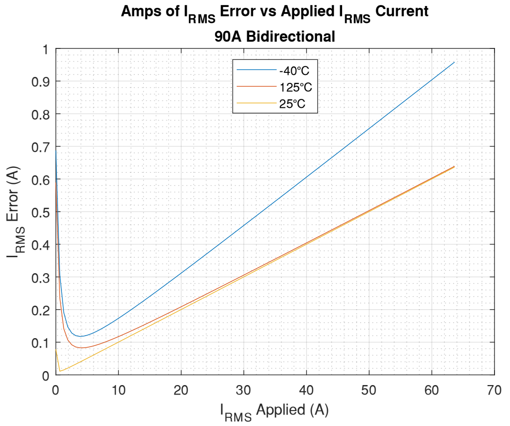


Figure 26: I_{RMS} Error [A] vs. Applied I_{RMS} [A]

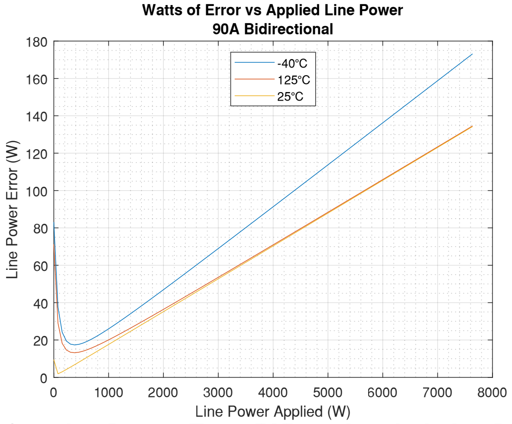


Figure 27: Line Power Error [W] vs. Applied Line Power [W]

DIGITAL COMMUNICATION

Communication Interfaces

The ACS37800 supports communication over 1 MHz I^{2}C and 10 MHz SPI. However, the communication protocol is fixed during factory programming. The ACS37800 MISO pin continues to drive the MISO line when CS goes high. This may prevent other devices from communicating properly. It is recommended that the ACS37800 be the only device on the SPI bus if using SPI communication.

SPI

The SPI frame consists of:

- The Controller writes on the MOSI line the 7-bit address of the register to be read from or written to.
- The next bit on the MOSI line is the read/write (RW) indicator. A high state indicates a Read and a low state indicates a Write.
- The device sends a 32-bit response on the MISO line. The contents correspond to the previous command.
- On the MOSI line, if the current command is a write, the 32 bits correspond to the Write data, and in the case of a read, the data is ignored.

Registers and EEPROM

WRITE ACCESS

The ACS37800 supports factory and customer EEPROM space as well as volatile registers. The customer access code must be sent prior to writing these customer EEPROM spaces. In addition, the device includes a set of free space EEPROM registers that are accessible with or without writing the access code.

READ ACCESS

All EEPROM and volatile registers may be read at any time regardless of the access code.

EEPROM

At power up, all shadow registers are loaded from EEPROM, including all configuration parameters. The shadow registers can be written to in order to change the device behavior without having to perform an EEPROM write. Any changes made in shadow memory are volatile and do not persist through a reset event.

WRITING

The Timing Diagram for an EEPROM write is shown in Figure 28 and Figure 29.

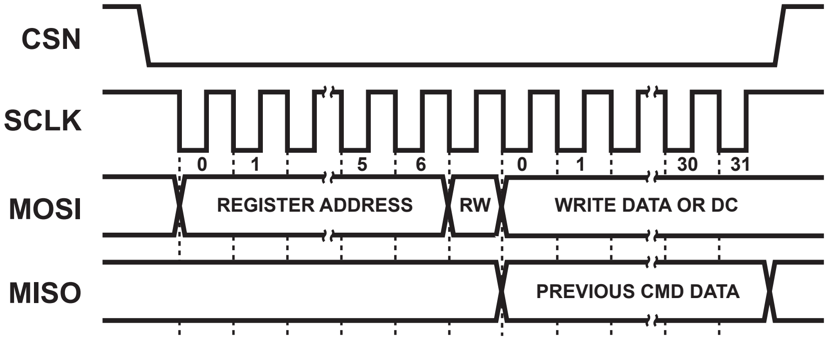


Figure 28: EEPROM Write – SPI Mode

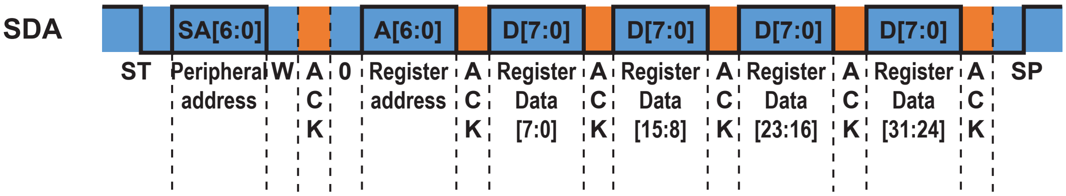


Figure 29: EEPROM Write – I^{2}C Mode
Blue represents data sent by the controller and orange is the data sent by the peripheral.

READING

The timing diagram for an EEPROM read is shown in Figure 30 and Figure 31.

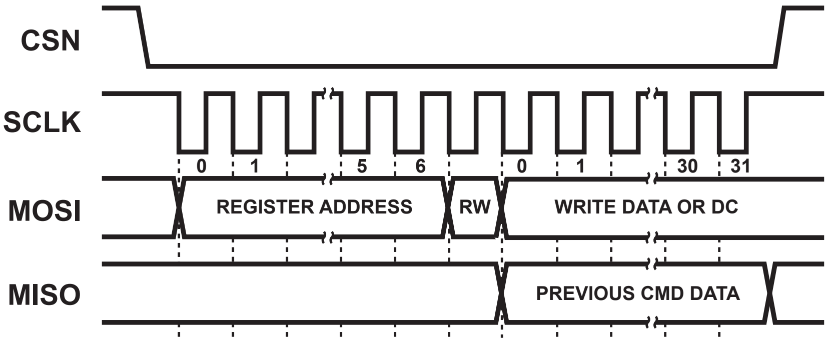


Figure 30: EEPROM Read – SPI Mode
For SPI, the read data will be sent out during the above command.

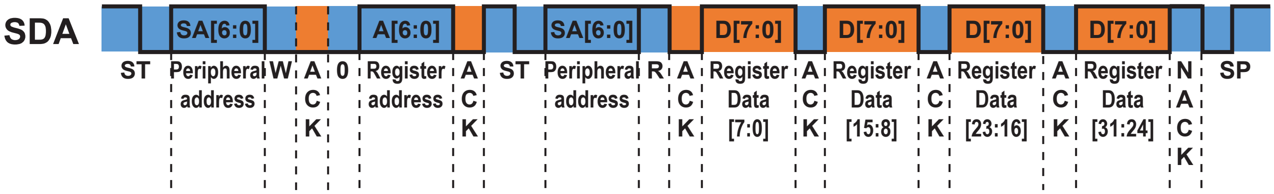


Figure 31: EEPROM Read – I²C Mode
Blue represents data sent by the controller and orange is the data sent by the peripheral.

EEPROM Error Checking and Correction (ECC)

Hamming code methodology is implemented for EEPROM checking and correction (ECC). ECC is enabled after power-up.

The ACS37800 analyzes message data sent by the controller and the ECC bits are added. The first 6 bits sent from the device to the controller are dedicated to ECC. The device always returns 32 bits.

EEPROM ECC Errors

Bits	Name	Description
31:28	–	No meaning
27:26	ECC	00 = No Error 01 = Error detected and message corrected 10 = Uncorrectable error 11 = No meaning
25:0	D[25:0]	EEPROM data

I^{2}C Peripheral Addressing

The ACS37800 supports I^{2}C communication over the SCL and SDA lines at speeds of up to 400 kHz. When the device first powers on, it measures the voltage level on the two DIO pins. It converts both voltage levels into a 4-bit code for a total of sixteen peripheral addresses. Table 2 shows the sixteen possible I^{2}C configurations that can be set with externally applied voltage. If both pins are pulled to V_{CC}, then the internal peripheral address stored in EEPROM is used. By default, the value of I2C_SLV_ADDR is programmed at the Allegro factory to 127, but this can be changed with programming by the customer.

If for any reason the external peripheral address setting feature is not desired, the DIO polling can be disabled by setting the I2C_DIS_SLV_ADDR. When this bit is set, the ACS37800 will automatically use the number stored in I2C_SLV_ADDR as the I^{2}C peripheral address regardless of the voltage on the DIO pins. Note that the device must be repowered for these changes to take effect.

Table 2: DIO Startup Voltage Addressing

DIO_1		DIO_2		A6	A5	A4	A3	A2	A1	A0	Peripheral Address (decimal)
0	0	0	0	1	1	0	0	0	0	0	96
0	0	0	1	1	1	0	0	0	0	1	97
0	0	1	0	1	1	0	0	0	1	0	98
0	0	1	1	1	1	0	0	0	1	1	99
0	1	0	0	1	1	0	0	1	0	0	100
0	1	0	1	1	1	0	0	1	0	1	101
0	1	1	0	1	1	0	0	1	1	0	102
0	1	1	1	1	1	0	0	1	1	1	103
1	0	0	0	1	1	0	1	0	0	0	104
1	0	0	1	1	1	0	1	0	0	1	105
1	0	1	0	1	1	0	1	0	1	0	106
1	0	1	1	1	1	0	1	0	1	1	107
1	1	0	0	1	1	0	1	1	0	0	108
1	1	0	1	1	1	0	1	1	0	1	109
1	1	1	0	1	1	0	1	1	1	0	110
1	1	1	1	EE	EE	EE	EE	EE	EE	EE	EEPROM value

MEMORY MAP

EEPROM/Shadow Memory

<table>
<tr><th rowspan="2"></th><th rowspan="2">Address</th><th colspan="32">Bits</th></tr>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td rowspan="5">EEPROM</td><td>0x0B</td><td colspan="6">ECC</td><td>▨</td><td>▨</td><td>PAVGSELEN</td><td>IAVGSELEN</td><td colspan="3">CRS_SNS</td><td colspan="10">SNS_FINE</td><td colspan="9">QVO_FINE</td></tr>
<tr><td>0x0C</td><td colspan="6">ECC</td><td>▨</td><td colspan="8">VCHAN_OFFSET_CODE</td><td colspan="10">RMS_AVG_2</td><td colspan="7">RMS_AVG_1</td></tr>
<tr><td>0x0D</td><td colspan="6">ECC</td><td>▨</td><td>▨</td><td colspan="3">FLTDLY</td><td colspan="8">FAULT</td><td>▨</td><td colspan="3">CHAN_DEL_SEL</td><td>▨</td><td>ICHAN_DEL_EN</td><td>▨</td><td>▨</td><td>▨</td><td>▨</td><td>▨</td><td>▨</td><td>▨</td></tr>
<tr><td>0x0E</td><td colspan="6">ECC</td><td>▨</td><td>ZEROCROSSEDGESEL</td><td>ZEROCROSSCHANSEL</td><td>SQUAREWAVE_EN</td><td>HALFCYCLE_EN</td><td>DELAYCNT_SEL</td><td colspan="6">UNDERVREG</td><td colspan="6">OVERVREG</td><td>▨</td><td>▨</td><td colspan="6">VEVENT_CYCS</td></tr>
<tr><td>0x0F</td><td colspan="6">ECC</td><td>▨</td><td>BYPASS_N_EN</td><td colspan="10">N</td><td colspan="2">DIO_1_SEL</td><td colspan="2">DIO_0_SEL</td><td>I2C_DIS_SLV_ADDR</td><td colspan="7">I2C_SLV_ADDR</td><td>▨</td><td>▨</td></tr>
<tr><td rowspan="5">Shadow</td><td>0x1B</td><td>▨</td><td>▨</td><td>▨</td><td>▨</td><td>▨</td><td>▨</td><td>▨</td><td>▨</td><td>PAVGSELEN</td><td>IAVGSELEN</td><td colspan="3">CRS_SNS</td><td colspan="10">SNS_FINE</td><td colspan="9">QVO_FINE</td></tr>
<tr><td>0x1C</td><td>▨</td><td>▨</td><td>▨</td><td>▨</td><td>▨</td><td>▨</td><td>▨</td><td colspan="8">VCHAN_OFFSET_CODE</td><td colspan="10">RMS_AVG_2</td><td colspan="7">RMS_AVG_1</td></tr>
<tr><td>0x1D</td><td>▨</td><td>▨</td><td>▨</td><td>▨</td><td>▨</td><td>▨</td><td>▨</td><td>▨</td><td colspan="3">FLTDLY</td><td colspan="8">FAULT</td><td>▨</td><td colspan="3">CHAN_DEL_SEL</td><td>▨</td><td>ICHAN_DEL_EN</td><td>▨</td><td>▨</td><td>▨</td><td>▨</td><td>▨</td><td>▨</td><td>▨</td></tr>
<tr><td>0x1E</td><td>▨</td><td>▨</td><td>▨</td><td>▨</td><td>▨</td><td>▨</td><td>▨</td><td>ZEROCROSSEDGESEL</td><td>ZEROCROSSCHANSEL</td><td>SQUAREWAVE_EN</td><td>HALFCYCLE_EN</td><td>DELAYCNT_SEL</td><td colspan="6">UNDERVREG</td><td colspan="6">OVERVREG</td><td>▨</td><td>▨</td><td colspan="6">VEVENT_CYCS</td></tr>
<tr><td>0x1F</td><td>▨</td><td>▨</td><td>▨</td><td>▨</td><td>▨</td><td>▨</td><td>▨</td><td>BYPASS_N_EN</td><td colspan="10">N</td><td colspan="2">DIO_1_SEL</td><td colspan="2">DIO_0_SEL</td><td>I2C_DIS_SLV_ADDR</td><td colspan="7">I2C_SLV_ADDR</td><td colspan="2">▨</td></tr>
</table>

Register Details – EEPROM

Register 0x0B/0x1B

Bits	Name	Default Value	Description
8:0	QVO_FINE	Device Specific	Offset fine trimming on current channel
18:9	SNS_FINE	Device Specific	Fine gain trimming on the current channel
21:19	CRS_SNS	Selection Specific	Coarse gain setting
22	IAVGSELEN	0	Current Averaging selection
23	PAVGSELEN	0	Power Averaging selection
31:26	ECC	–	Error Code Correction

QVO_FINE

Offset adjustment for the current channel. This is a signed 9-bit number with an input range of –256 to 255. With a step size of 64 LSB, this equates to an offset trim range of –16384 to 16320 LSB, which is added to the ICODES value. Refer to Current Channel Trimming section for further information. QVO_FINE is further described in Table 3.

Table 3: QVO_FINE

Range	Value	Units
–256 to 255	–16,384 to 16,320	LSB

SNS_FINE

Gain adjustment for the current channel. This is a signed 10-bit number with an input range of –256 to 255. This gain adjustment is implemented as a percentage multiplier centered around 1 (i.e. writing a 0 to this field multiplies the gain by 1, leaving the gain unaffected). The fine sensitivity parameter ranges from 60% to 140% of code 0. Refer to Current Channel Trimming section for further information SNS_FINE is further described in Table 4.

Table 4: SNS_FINE

Range	Value	Units
–256 to 255	60 to 140	% of code 0

CRS_SNS

Coarse gain adjustment for the current channel. This gain is implemented in the analog domain before the ADC. This is a 3-bit number that allows for 8 gain selections. Adjustments to CRS_SNS may impact the device's performance over temperature. Datasheet limits apply only to the factory settings for CRS_SNS. The gain settings map to 1×, 2×, 3×, 3.5×, 4×, 4.5×, 5.5×, and 8×. CRS_SNS is further described in Table 5.

Table 5: CRS_SNS

Range	Value	Units
0	1×	–
1	2×	–
2	3×	–
3	3.5×	–
4	4×	–
5	4.5×	–
6	5.5×	–
7	8×	–

IAVGSELEN

Current Averaging selection enable. 0 will select VRMS for averaging. 1 will select IRMS for averaging.

PAVGSELEN

Power Averaging selection enable. 0 will select VRMS for averaging. 1 will select PACTIVE for averaging.

Register 0x0C/0x1C

Bits	Name	Default Value	Description
6:0	RMS_AVG_1	0	Average of the RMS voltage or current – stage 1
16:7	RMS_AVG_2	0	Average of the RMS voltage or current – stage 2
24:17	VCHAN_OFFSET_CODE	Device Specific	Controls the room offset for the voltage channel
31:26	ECC	–	Error Code Correction

RMS_AVG_1

Number of averages for the first averaging stage (VRMSAVGONESEC or IRMSAVGONESEC). The value written into this field directly maps to the number of averages ranging from 0 to 127. For optimal performance, an even number of averages should be used. The channel to be averaged is selected by the current average select enable bit (IAVGSELEN). RMS_AVG_1 is further described in Table 6.

Table 6: RMS_AVG_1

Range	Value	Units
0 to 127	0 to 127	number of averages

RMS_AVG_2

Number of averages for the second averaging stage (VRMSAVGONEMIN or IRMSAVGONEMIN). This stage averages the outputs of the first averaging stage. The value written into this field directly maps to the number of averages ranging from 0 to 1023. For optimal performance, an even number of averages should be used. The channel to be averaged is selected by the current average select enable bit (IAVGSELEN). RMS_AVG_2 is further described in Table 7.

Table 7: RMS_AVG_2

Range	Value	Units
0 to 1023	0 to 1023	number of averages

VCHAN_OFFSET_CODE

This controls the offset of the voltage channel at room.

Table 8: VCHAN_OFFSET_CODE

Range	Value	Units
–128 to 127	–2048 to 2032	codes

Register 0x0D/0x1D

Bits	Name	Default Value	Description
7	ICHAN_DEL_EN	0	Enable phase delay on voltage or current channel
11:9	CHAN_DEL_SEL	0	Sets phase delay on voltage or current channel
20:13	FAULT	70	Sets the overcurrent fault threshold
23:21	FLTDLY	0	Sets the overcurrent fault delay
31:26	ECC	–	Error Code Correction

ICHAN_DEL_EN

Enables delay for either the voltage or current channel. Setting to 1 enables delay for the current channel. ICHAN_DEL_EN is further described in Table 9.

Table 9: ICHAN_DEL_EN

Range	Value	Units
0	0 – voltage channel	LSB
1	1 – current channel	LSB

CHAN_DEL_SEL

Sets the amount of delay applied to the voltage or current channel (set by ICHAN_DEL_EN). CHAN_DEL_SEL is further described in Table 10.

Table 10: CHAN_DEL_SEL

Range	Value	Units
0 to 7	0 to 219	µs

FAULT

Overcurrent fault threshold. This is an unsigned 8-bit number with an input range of 0 to 255, which equates to a fault range of 65% to 200% of IP. The factory setting of this field is 70. FAULT is further described in Table 11.

Table 11: FAULT

Range	Value	Units
0 to 255	56 to 225	% of IP

FLTDLY

Fault delay setting of the amount of delay applied before flagging a fault condition. FLTDLY is further described in Table 12.

Table 12: FLTDLY

Range	Value	Units
0	0	µs
1	0	µs
2	4.75	µs
3	9.25	µs
4	13.75	µs
5	18.5	µs
6	23.25	µs
7	27.75	µs

Register 0x0E/0x1E

Bits	Name	Default Value	Description
5:0	VEVENT_CYCS	0	Sets the number of qualifying cycles needed to flag overvoltage or undervoltage
13:8	OVERVREG	0	Sets the overvoltage fault threshold
19:14	UNDERVREG	0	Sets the undervoltage fault threshold
20	DELAYCNT_SEL	0	Sets the width of the voltage zero-crossing output pulse
21	HALFCYCLC_EN	0	Sets the zero crossing flag triggering on half or full cycle (default: full cycle)
22	SQUAREWAVE_EN	0	Sets the zero crossing pulse characteristics (default: pulse)
23	ZEROCROSSCHANSEL	0	Sets the channel that triggers the zero crossing flag (default: voltage)
24	ZEROCROSSEDGESEL	0	Sets the edge that triggers zero crossing flag
31:26	ECC	–	Error Code Correction

VEVENT_CYCS

Sets the number of cycles required to assert the OVRMS flag or the UVRMS. This is an unsigned 6-bit number with an input range of 0 to 63. The value in this field directly maps to the number of cycles. VEVENT_CYCS is further described in Table 13.

Table 13: VEVENT_CYCS

Range	Value	Units
0 to 63	1 to 64	cycles

OVERVREG

Sets the threshold of the overvoltage RMS flag (OVRMS). This is a 6-bit number ranging from 0 to 63. This trip level spans the entire range of the VRMS register. The flag is set if the RMS value is above this threshold for the number of cycles selected in VEVENT_CYCS. OVERVREG is further described in Table 14.

Table 14: OVERVREG

Range	Value	Units
0 to 63	0 to 65536	LSB

UNDERVREG

Sets the threshold of the undervoltage RMS flag (UVRMS). This is a 6-bit number ranging from 0 to 63. This trip level spans one entire range of the VRMS register. The flag is set if the RMS value is below this threshold for the number of cycles selected in VEVENT_CYCS. UNDERVREG is further described in Table 15.

Table 15: UNDERVREG

Range	Value	Units
0 to 63	0 to 65536	LSB

DELAYCNT_SEL

Selection bit for the width of pulse for a voltage zero-crossing event. When set to 0, the pulse is 32 µs. When set to 1, the pulse is 256 µs. When the SQUAREWAVE_EN bit is set, this field is ignored. DELAYCNT_SEL is further described in Table 16.

Table 16: DELAYCNT_SEL

Range	Value	Units
0	32	µs
1	256	µs

HALFCYCLE_EN

Setting for the zero-crossing flag. When set to 0, the voltage zero-crossing will be indicated on every edge determined by ZEROCROSSINGEDGESEL. When set to 1, the voltage zero-crossing will be indicated on both rising and falling edges.

SQUAREWAVE_EN

Setting for the zero-crossing flag. When set to 0, the zero-crossing event will be indicated by a pulse on the DIO pin. When set to 1, the zero-crossing event will be indicated by a level change on the DIO pin.

ZERCROSSINGCHANSEL

Determines which channel will trigger the zero-crossing flag. 0 is the voltage channel. 1 is the current channel with zero-crossing flag for rising and falling with only one customizable register DELAYCNT_SEL.

ZEROCROSSINGEDGESEL

This determines whether the zero-crossing flag triggers on rising or falling. Note: if HALFCYCLE_EN = 1, this setting does not matter.

Register 0x0F/0x1F

Bits	Name	Default Value	Description
8:2	I2C_SLV_ADDR	127	I^2C peripheral address selection
9	I2C_DIS_SLV_ADDR	0	Disable I^2C peripheral address selection circuit
11:10	DIO_0_SEL	0	Digital output 0 multiplexor selection bits
13:12	DIO_1_SEL	0	Digital output 1 multiplexor selection bits
23:14	N	0	Sets the number of samples used in RMS calculations when BYPASS_N_EN = 1
24	BYPASS_N_EN	0	Set whether RMS is calculated based on voltage zero crossing or N samples from the above registers
31:26	ECC	–	Error Code Correction

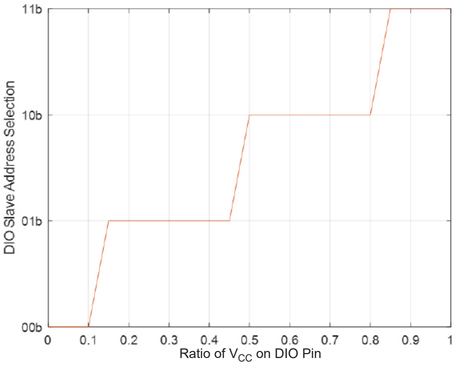
I2C_SLV_ADDR

Settings for the I^2C peripheral address externally. When I2C_DIS_SLV_ADDR is set to 0, the voltage on the DIO pins are measured at power on and are used to set the device's peripheral address.

Each DIO pin has 4 voltage "bins" which may be used to set the I^2C peripheral address. These voltages may be set using resistor divider circuits from V_{CC} to GND. I2C_SLV_ADDR is further described in Table 17.

Table 17: I2C_SLV_ADDR

DIO_1 (decimal)	DIO_0 (decimal)	Peripheral Address (decimal)
0	0	96
0	1	97
0	2	98
0	3	99
1	0	100
1	1	101
1	2	102
1	3	103
2	0	104
2	1	105
2	2	106
2	3	107
3	0	108
3	1	109
3	2	110
3	3	EEPROM value



I2C_DIS_SLV_ADDR

When I2C_DIS_SLV_ADDR is set to 1, the address is set through EEPROM field I2C_SLV_ADDR[6:0]. This enables or disables the analog I^2C peripheral address feature at power on. When this bit is set, the I^2C peripheral address will map directly to I2C_SLV_ADDR.

DIO_0_SEL

Determines which flags are output on the DIO0 pin. Only used when the device is in I^2C programming mode.

DIO_1_SEL

Determines which flags are output on the DIO1 pin. Only used when the device is in I^2C programming mode.

Volatile Memory

<table>
<tr><th rowspan="2"></th><th rowspan="2">Address</th><th colspan="32">Bits</th></tr>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td rowspan="18">VOLATILE</td><td>0x20</td><td colspan="16">IRMS</td><td colspan="16">VRMS</td></tr>
<tr><td>0x21</td><td colspan="16">PIMAG</td><td colspan="16">PACTIVE</td></tr>
<tr><td>0x22</td><td></td><td></td><td></td><td>POSPF</td><td>POSANGLE</td><td colspan="11">PFACTOR</td><td colspan="16">PAPPARENT</td></tr>
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<tr><td>0x26</td><td colspan="16">IRMSAVGONESEC</td><td colspan="16">VRMSAVGONESEC</td></tr>
<tr><td>0x27</td><td colspan="16">IRMSAVGONEMIN</td><td colspan="16">VRMSAVGONEMIN</td></tr>
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<tr><td>0x2A</td><td colspan="16">ICODES</td><td colspan="16">VCODES</td></tr>
<tr><td>0x2B</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
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<tr><td>0x2D</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>UNDERVOLTAGE</td><td>OVERVOLTAGE</td><td>FAULTLATCHED</td><td>FAULTOUT</td><td>VZEROCROSSOUT</td></tr>
<tr><td>0x2E</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>0x2F</td><td colspan="32">ACCESS_CODE</td></tr>
<tr><td>0x30</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>CUSTOMER_ACCESS</td></tr>
<tr><td>0x31</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
</table>

Register Details – Volatile

Register 0x20

Bits	Name	Description
15:0	VRMS	Voltage RMS value
31:16	IRMS	Current RMS value

VRMS

RMS voltage output. This field is an unsigned 16-bit fixed point number with 16 fractional bits, where $\Delta V_{IN(MAX)} = 0.84$, and $\Delta V_{IN(min)} = -0.84$. To convert the value (input voltage) to line voltage, divide the input voltage by the R_{SENSE} and R_{ISO} voltage divider ratio using actual resistor values.

Table 18: VRMS

Register Range	Valid Range	Value	Units
0 to ~1	0 to ~0.84	[0 to ~1] × $\Delta V_{IN(MAX)}$ ×1.19	mV

IRMS

RMS current output. This field is a signed 16-bit fixed point number with 16 fractional bits, where $I_{IP(MAX)} = 0.84$, and $I_{IP(MIN)} = -0.84$. To convert the value (input voltage) to line voltage, divide the input voltage by the R_{SENSE} and R_{ISO} voltage divider ratio using actual resistor values.

Table 19: IRMS

Register Range	Valid Range	Value	Units
0 to ~1	0 to ~0.84	[0 to ~1] × $I_{PR(MAX)}$ ×1.19	A

Register 0x21

Bits	Name	Description
15:0	PACTIVE	Active power
31:16	PIMAG	Reactive power

PACTIVE

Active power output. This field is a signed 16-bit fixed point number with 15 fractional bits, where positive MaxPow = 0.704, and negative MaxPow = –0.704. To convert the value (input power) to line power, divide the input power by the R_{SENSE} and R_{ISO} voltage divider ratio using actual resistor values.

Table 20: PACTIVE

Register Range	Valid Range	Value	Units
–1 to ~1	–0.704 to ~0.704	[1 to ~1] × MaxPow × 1.42	mW

PIMAG

Reactive power output. This field is an unsigned 16-bit fixed point number with 16 fractional bits, where MaxPow = 0.704. To convert the value (input power) to line power, divide the input power by the R_{SENSE} and R_{ISO} voltage divider ratio using actual resistor values.

Table 21: PIMAG

Register Range	Valid Range	Value	Units
0 to ~1	0 to ~0.704	[0 to ~1] × MaxPow × 1.42	mVA

Register 0x22

Bits	Name	Description
15:0	PAPPARENT	Apparent power magnitude
26:16	PFACTOR	Power factor
27	POSANGLE	Sign of the power angle
28	POSPF	Sign of the power factor

PAPPARENT

Apparent power output magnitude. This field is an unsigned 16-bit fixed point number with 16 fractional bits, where MaxPow = 0.704. To convert the value (input power) to line power, divide the input power by the R_{SENSE} and R_{ISO} voltage divider ratio using actual resistor values.

Table 22: PAPPARENT

Register Range	Valid Range	Value	Units
0 to ~1	0 to ~0.704	[0 to ~1] × MaxPow × 1.42	mVAR

PFACTOR

Power factor output. This field is a signed 11-bit fixed point number with 10 fractional bits. It ranges from –1 to ~1 with a step size of 2^{-10}. PFACTOR is further described in Table 23.

Table 23: PFACTOR

Range	Value	Units
–1 to ~1	–1 to ~1	–

POSANGLE

Bit to represent leading or lagging. A 0 represents the current leading and a 1 represents the current lagging.

POSPF

Sign bit to represent if the power is being generated (0) or consumed (1).

Register 0x25

Bits	Name	Description
9:0	NUMPTSOUT	Number of samples of current and voltage used for calculations

NUMPTSOUT

Number of points used in the RMS calculation. This will be the dynamic value that is evaluated internally to the device based on full cycle zero crossings of the voltage channel. NUMPTSOUT is further described in Table 24.

Table 24: NUMPTSOUT

Range	Value	Units
0 to 1023	0 to 1023	samples

Register 0x26

Bits	Name	Description
15:0	VRMSAVGONESEC	Averaged voltage RMS value; duration set by RMS_AVG_1. This register will be zero if IAVGSELEN = 1
31:16	IRMSAVGONESEC	Averaged current RMS value; duration set by RMS_AVG_1. This register will be zero if IAVGSELEN = 0

VRMSAVGONESEC

Voltage RMS value averaged according to RMS_AVG_1. This register will be zero if IAVGSELEN = 1.

IRMSAVGONESEC

Current RMS value averaged according to RMS_AVG_1. This register will be zero if IAVGSELEN = 0.

Register 0x27

Bits	Name	Description
15:0	VRMSAVGONEMIN	Averaged voltage RMS value; duration set by RMS_AVG_2. This register will be zero if IAVGSELEN = 1
31:16	IRMSAVGONEMIN	Averaged current RMS value; duration set by RMS_AVG_2. This register will be zero if IAVGSELEN = 0

VRMSAVGONEMIN

Voltage RMS value averaged according to RMS_AVG_2. This register will be zero if IAVGSELEN = 1.

IRMSAVGONEMIN

Current RMS value averaged according to RMS_AVG_2. This register will be zero if IAVGSELEN = 0.

Register 0x28

Bits	Name	Description
15:0	PACTAVGONESEC	Active Power value averaged over up to one second; duration set by RMS_AVG_1.

PACTAVGONESEC

Active power value averaged according to RMS_AVG_1.

Register 0x29

Bits	Name	Description
15:0	PACTAVGONEMIN	Active Power value averaged over up to one minute; duration set by RMS_AVG_2.

PACTAVGONEMIN

Active power value averaged according to RMS_AVG_2.

Register 0x2A

Bits	Name	Description
15:0	VCODES	Instantaneous voltage measurement
31:16	ICODES	Instantaneous current measurement

VCODES

This field contains the instantaneous voltage measurement before any RMS calculations are done. It is a 16-bit signed fixed point number with 15 fractional bits, where $\Delta V_{IN(MAX)} = 0.84$ and $\Delta V_{IN(min)} = -0.84$. To convert the value (input voltage) to line voltage, divide the input voltage by the R_{SENSE} and R_{ISO} voltage divider ratio using the resistor values.

Table 25: VCODES

Register Range	Valid Range	Value	Units
–1 to ~1	–0.84 to ~0.84	[–1 to ~1] × $\Delta V_{IN(MAX)}$ ×1.19	mV

ICODES

This field contains the instantaneous current measurement before any RMS calculations are done. This field is a signed 16-bit fixed point number with 15 fractional bits, where $I_{IP(MAX)} = 0.84$, and $I_{IP(MIN)} = -0.84$.

Table 26: ICODES

Register Range	Valid Range	Value	Units
–1 to ~1	–0.84 to ~0.84	[–1 to ~1] × $I_{PR(MAX)}$ ×1.19	A

Register 0x2C

Bits	Name	Description
15:0	PINSTANT	Instantaneous power – Multiplication of VCODES and ICODES

PINSTANT

This field contains the instantaneous power measurement before any RMS calculations are done. This field is a signed 16-bit fixed point number with 15 fractional bits, where positive MaxPow = 0.704, and negative MaxPow = –0.704. To convert the value (input power) to line power, divide the input power by the R_{SENSE} and R_{ISO} voltage divider ratio using the resistor values.

Table 27: PINSTANT

Register Range	Valid Range	Value	Units
–1 to ~1	–0.704 to ~0.704	[–1 to ~1] × MaxPow × 1.42	mVAR

Register 0x2D

Bits	Name	Description
0	ZEROCROSSOUT	Zero-crossing output
1	FAULTOUT	Current fault output
2	FAULTLATCHED	Current fault output latched
3	OVERVOLTAGE	Overvoltage flag
4	UNDERVOLTAGE	Undervoltage flag

ZEROCROSSOUT

Flag for the zero-crossing events. This will be present and active regardless of DIO_0_SEL and DIO_1_SEL. This flag will still follow the HALFCYCLE_EN and SQUAREWAVE_EN settings.

FAULTOUT

Flag for the overcurrent events. This will be present and active regardless of DIO_0_SEL and DIO_1_SEL and will only be set when FAULT is present.

FAULTLATCHED

Flag for the overcurrent events. This bit will latch and will remain 1 as soon as an overcurrent event is detected. This can be reset by writing a 1 to this field. This will be present and active regardless of DIO settings.

OVERVOLTAGE

Flag for the overvoltage events. This will be present and active regardless of DIO_0_SEL and DIO_1_SEL and will only be set when FAULT is present.

UNDERVOLTAGE

Flag for the undervoltage events. This will be present and active regardless of DIO_0_SEL and DIO_1_SEL and will only be set when FAULT is present.

Register 0x2F

Bits	Name	Description
31:0	ACCESS_CODE	Access code register: Customer code: 0x4F70656E

Register 0x30

Bits	Name	Description
0	CUSTOMER_ACCESS	Customer write access enabled. 0 = Non-Customer mode. 1 = Customer mode.

THERMAL PERFORMANCE

Thermal Rise vs. Primary Current

Self-heating due to the flow of current in the package IP conductor should be considered during the design of any current sensing system. The sensor, printed circuit board (PCB), and contacts to the PCB will generate heat and act as a heat sink as current moves through the system.

The thermal response is highly dependent on PCB layout, copper thickness, cooling techniques, and the profile of the injected current. The current profile includes peak current value, current “on-time”, and duty cycle.

Placing vias under the copper pads of the Allegro current sensor evaluation board minimizes the current path resistance and improves heatsinking to the PCB, while vias outside of the pads limit the current path to the top of the PCB trace and have worse heatsinking under the part (see Figure 32 and Figure 33 below). The ACSEVB-MA16-LA16 and the ACSEVB-MC16 bare evaluation boards used for data collection do include vias in pad and is recommended to improve thermal performance. The evaluation boards used for the ACS37800, the ACSEVB-MC16-POWER-IC or ACSEVB-MA16-POWER-IC, include additional application specific circuitry but follow identical board layout techniques and have similar thermal performance.

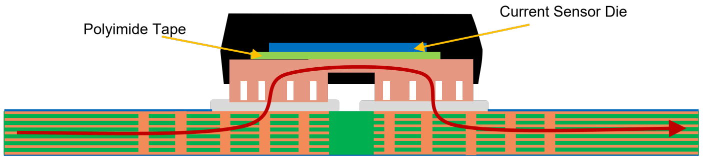


Figure 32: Vias Under Copper Pads (not to scale)

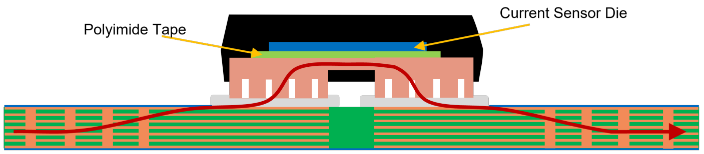


Figure 33: No Vias Under Copper Pads (not to scale)

The plot in Figure 34 shows the measured rise in steady-state die temperature of the MA package versus DC continuous current at an ambient temperature, T_A, of 25 °C for two board designs: filled vias under copper pads and no vias under copper pads.

The plot in Figure 35 shows the measured rise in steady-state die temperature of the MC package versus DC continuous current at an ambient temperature, T_A, of 25 °C for two board designs: filled vias under copper pads and no vias under copper pads.

Note: Using in-pad vias has better thermal performance that no in-pad vias, and this is the design the ACSEVB-MC16-POWER-IC or ACSEVB-MA16-POWER-IC use.

Top and bottom layers of each PCB are shown below in Figure 36 and Figure 37.

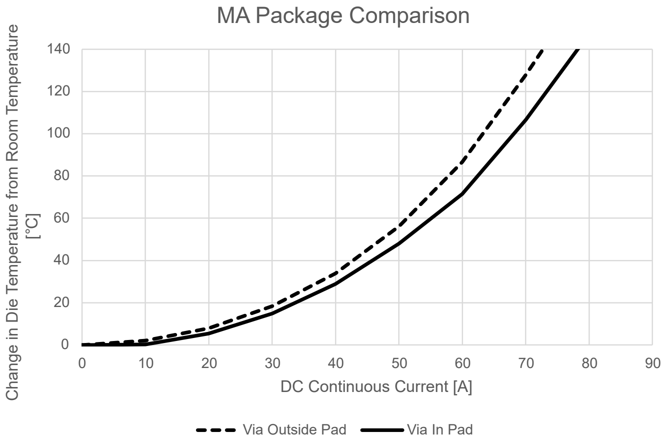


Figure 34: MA Package Comparison with and without In-Pad Vias

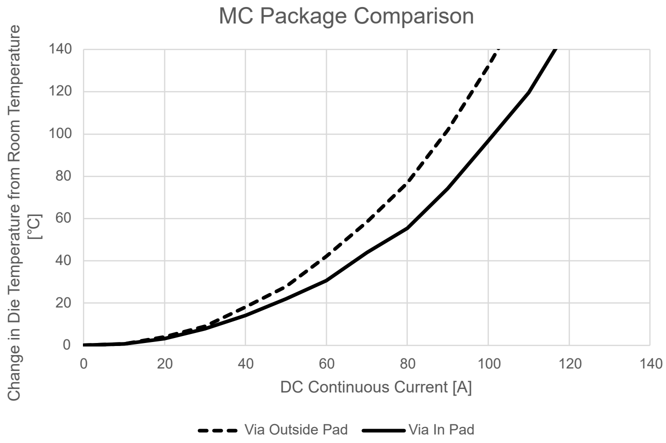


Figure 35: MC Package Comparison with and without In-Pad Vias

The thermal capacity of the MA and MC package should be verified by the end user in the application’s specific conditions. The maximum junction temperature, $T_{J(max)}$ (165°C), should not be exceeded. Measuring the temperature of the top of the package is a close approximation of the die temperature.

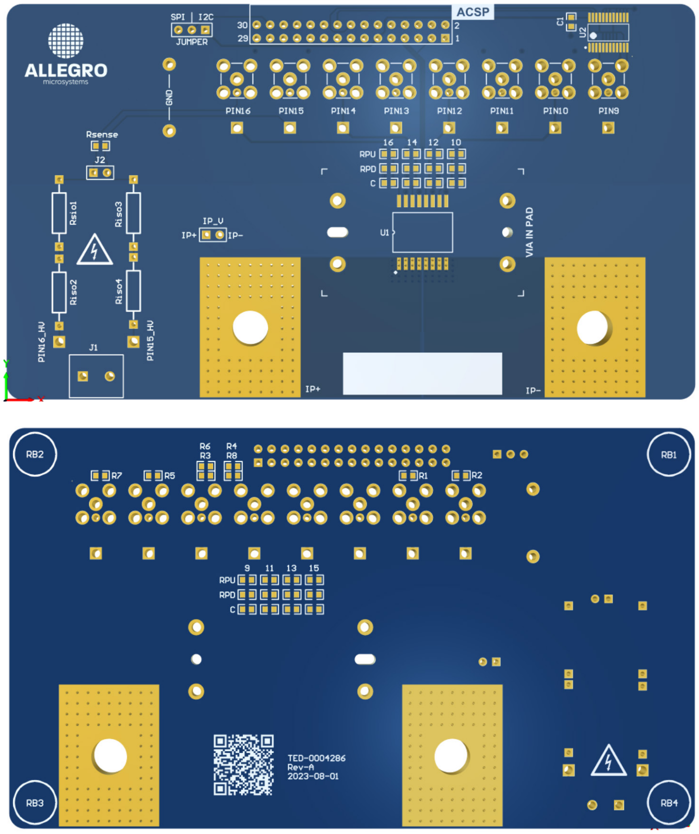
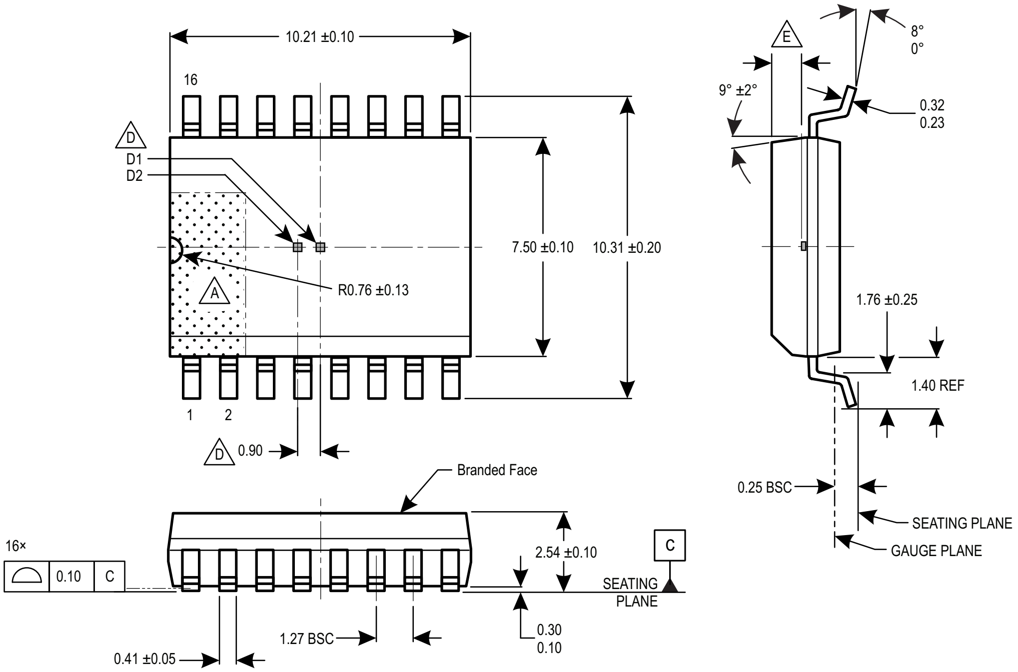


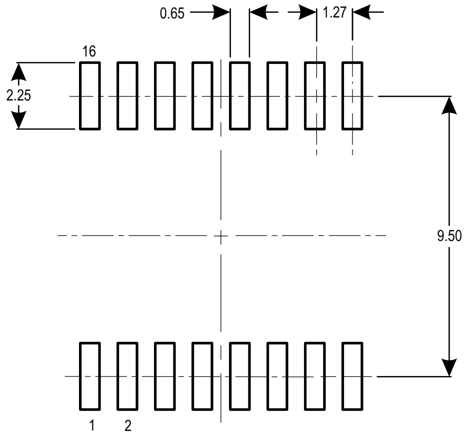
Figure 36: ACSEVB-MC16-POWER-IC /
ACSEVB-MC16-POWER-IC

MA PACKAGE OUTLINE DRAWING

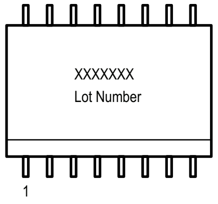
For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000388, Rev. 1 and JEDEC MS-013AA)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown





C PCB Layout Reference View



B Standard Branding Reference View

Lines 1, 2 = 12 characters

Line 1: Part Number
Line 2: First 8 characters of Assembly Lot Number

A Terminal #1 mark area

B Branding scale and appearance at supplier discretion

C Reference land pattern layout (reference IPC7351 SOIC127P600X175-8M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

D Hall elements (D1, D2), not to scale

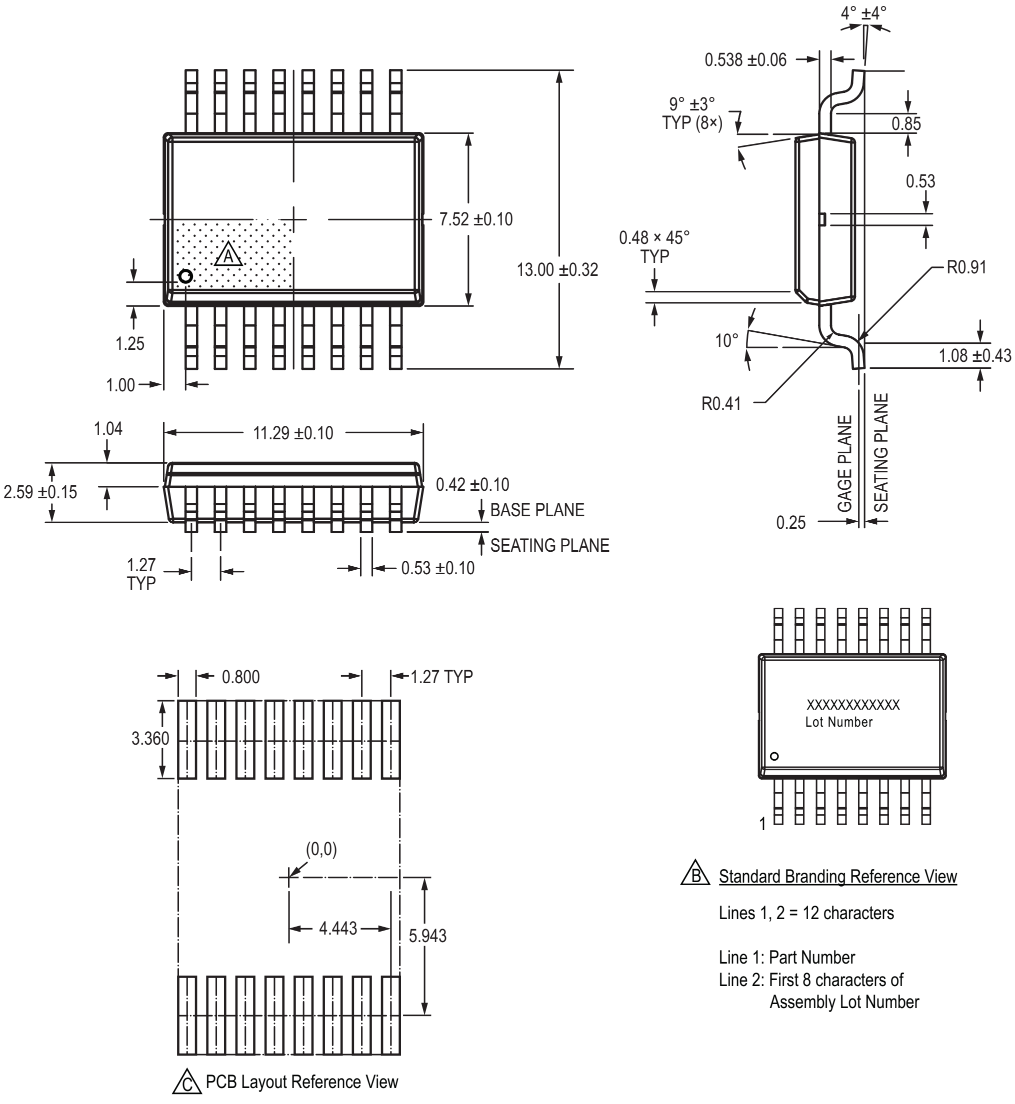
E Active Area Depth 0.293 mm

Figure 37: Package MA, 16-Pin SOICW

MC PACKAGE OUTLINE DRAWING

For Reference Only; Not for Tooling Use

(reference DWG-0000714, Rev. 2)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



C PCB Layout Reference View

B Standard Branding Reference View

Lines 1, 2 = 12 characters

Line 1: Part Number
Line 2: First 8 characters of
Assembly Lot Number

A Terminal #1 mark area

B Branding scale and appearance at supplier discretion

C Reference land pattern layout; all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Figure 38: Package MC, 16-Pin SOICW

Revision History

Number	Date	Description
–	November 30, 2020	Initial release
1	January 27, 2021	Updated Part Numbering schematic (page 2), Supply Bypass Capacitor unit, Current Channel Power Supply Error test conditions (page 6), Figure 4 (page 12), Figure 9 (page 15), and Figure 21 (page 21).
2	February 24, 2021	Removed TUV certificate mark (page 1)
3	March 17, 2022	Updated package drawing (page 40)
4	June 25, 2024	Updated Features and Benefits (page 1); added MC package drawing (page 1); updated selection guide (page 2); updated MA Package Isolation Characteristics (page 3); added MA Package Characteristics (page 3); added MC Package Isolation Characteristics (page 4); updated Thermal Characteristics (page 4); updated Table of Contents (page 6); updated RMS Noise characteristic (page 8); added and updated performance characteristics (pages 9-12, 13-15); updated all registers to conform to current standard (all caps, all pages); updated “master” to “controller” and “slave” to “peripheral” to conform to current standard (all pages); updated Configuring the Device for AC Applications section (page 25); updated Configuring the Device for DC Applications or For Applications with No Voltage Zero Crossing section (pages 26-27); updated Thermal Performance section (pages 44-45); added MC package outline drawing (page 47).

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