ACS39402

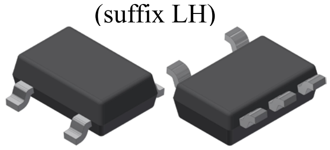
AEC-Q100-Qualified TMR Current Sensor in 5-Pin SOT23-W

FEATURES AND BENEFITS

- Self-contained single package current sensing solution with no external sense resistor required
- High operating bandwidth for fast control loops or where high-speed currents are monitored
  - □ 500 kHz bandwidth
  - □ 1 µs typical response time
- High performance for optimized energy applications
  - □ ±2.8% sensitivity error over temperature
  - □ ±30 mV maximum offset voltage (25°C)
  - □ Ratiometric operation from 3.0 to 5.5 V supply
  - □ No magnetic hysteresis
- Low ohmic loss with 1.6 mΩ primary conductor resistance
- Differential sensing robust against external magnetic fields
- Small footprint, wide body SOT-23 LH package
- 500 kHz bandwidth for fast response time
- UL 62368-1 (edition 3) certification (pending)
  - □ 1767 V_{RMS} withstand voltage
  - □ 285 V_{RMS} basic working voltage
- Ratiometric operation unidirectional current sensing
- Wide operating temperature, –40°C to 125°C
- AEC-Q100 Grade 1, automotive qualified

PACKAGE

5-pin SOT23-W
(suffix LH)



Not to scale

DESCRIPTION

The ACS39402 is a small, TMR-based current sensor for cost-optimized applications. The current applied to the pins of the primary conductor generates an internal differential magnetic field. The TMR sensor provides a proportional voltage to the differential magnetic field while rejecting common-mode stray fields. The pins of the primary conductive path and the sensor leads are galvanically isolated.

The ACS39402 is offered in the LH package, featuring a small and low-profile footprint well suited for space-constrained applications. The package features a 285 V_{RMS} basic working voltage, enabling high-side current sensing without the need for additional isolation techniques.

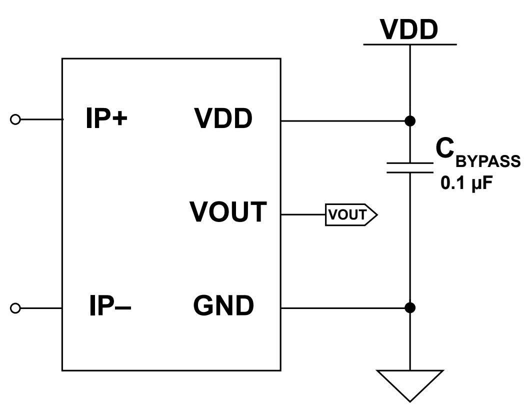
The current conductor has a low 1.6 mΩ resistance, ideal for low power dissipation constraints. The low primary conductor resistance enables the sensor to withstand high in-rush currents and minimizes power loss.

The ACS39402 has ratiometric operating range from 3.0 to 5.5 V, ideal for both 5 V and 3.3 V systems. The ACS39402 has a sensitivity error that is less than ±2.8% over temperature with the same footprint as a five-pin SOT23-W current-sense amplifier without the need for a shunt resistor.

The ACS39402 is a lead (Pb) free device plated with 100% matte tin, compatible with standard lead-free printed circuit board assembly processes.

APPLICATIONS

- Industrial motor control
- Micro solar inverters
- Robotics
- DC-DC converters



The ACS39402 outputs an analog signal at VOUT that varies linearly with the primary current, I_P, within the specified ranges.

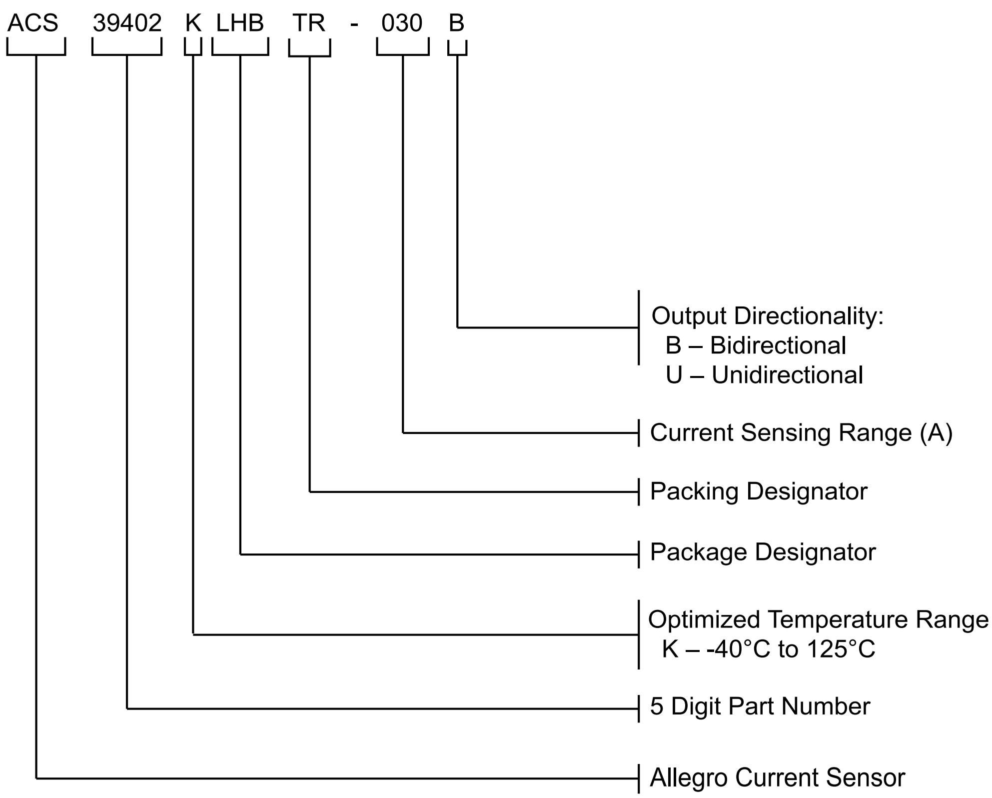
Figure 1: Typical Application Circuit

SELECTION GUIDE

Part Number	Current Sensing Range, I_{PR} (A)	Sensitivity [1] (mV/A)	V_{DD} (V)	V_{QVO} [1] (V)	Optimized Temperature Range T_A (°C)	Packing
ACS39402KLHBTR-010U	10	400	3.0 to 5.5	0.5	–40 to 125	Tape and reel, 3000 pieces per reel

[1] V_{DD} = 5 V.

PART NAMING SPECIFICATION



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ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Min	Max	Unit
Supply Voltage	V_{DD}	Applies to VDD	–0.3	6	V
Output Voltage	V_O	Applies to VOUT	–0.3	V_{DD} + 0.3 [2]	V
Operating Ambient Temperature	T_A	K temperature range	–40	125	°C
Storage Temperature	T_{STG}		–65	155	°C
Maximum Junction Temperature	T_J		–	150	°C
Lead Soldering Temperature	T_L	<10 seconds	–	260	°C

[1] Stresses in excess of those listed in the absolute maximum ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these limits or at any other condition that exceeds those indicated in the operational sections of this specification is not implied. Exposure to an absolute maximum rating for an extended period may affect device reliability.
[2] The lower of V_{DD} + 0.3 V or 6.0 V.

ISOLATION CHARACTERISTICS

Characteristic	Symbol	Notes	Rating	Unit
Withstand Voltage [1][2]	V_{ISO}	Agency rated for 60 seconds per UL 62368-1 (edition 3)	1767	V_{RMS}
Working Voltage for Basic Isolation [2]	V_{WVBI}	Maximum approved working voltage for basic insulation according to UL 62368-1 (edition 3)	403	V_{PK} or V_{DC}
			285	V_{RMS}
Impulse Withstand Voltage	$V_{IMPULSE}$	Tested ±5 pulses at 2/minute in compliance with IEC 61000-4-5, 1.2 µs (rise) and 50 µs (width)	2500	V_{PK}
Clearance	D_{CL}	Minimum distance through air from IP leads to signal leads	1.9	mm
Creepage	D_{CR}	Minimum distance along package body from IP leads to signal leads	2	mm
Distance Through Insulation	DTI	Minimum internal distance through insulation	25	µm
Comparative Tracking Index	CTI	Material Group II	400 to 599	V

[1] 100% production-tested in accordance with UL 62368-1 (edition 3).
[2] Certification pending.

PACKAGE CHARACTERISTICS

Characteristic	Symbol	Notes	Min.	Typ.	Max.	Unit
Internal Conductor Resistance	R_{IC}	T_A = 25°C	–	1.6	–	mΩ
Internal Conductor Inductance	L_{IC}	T_A = 25°C	–	2	–	nH
Moisture Sensitivity Level	MSL	Per IPC/JEDEC J-STD-020	–	1	–	–

THERMAL CHARACTERISTICS

Characteristic	Symbol	Notes	Value	Unit
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	Mounted on the Allegro LH Current Sensor Evaluation Board (ACSEVB-LH5)	32	°C/W
Package Thermal Metric (Junction to Top)	Ψ_{JT}		3	°C/W

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FUNCTIONAL BLOCK DIAGRAM

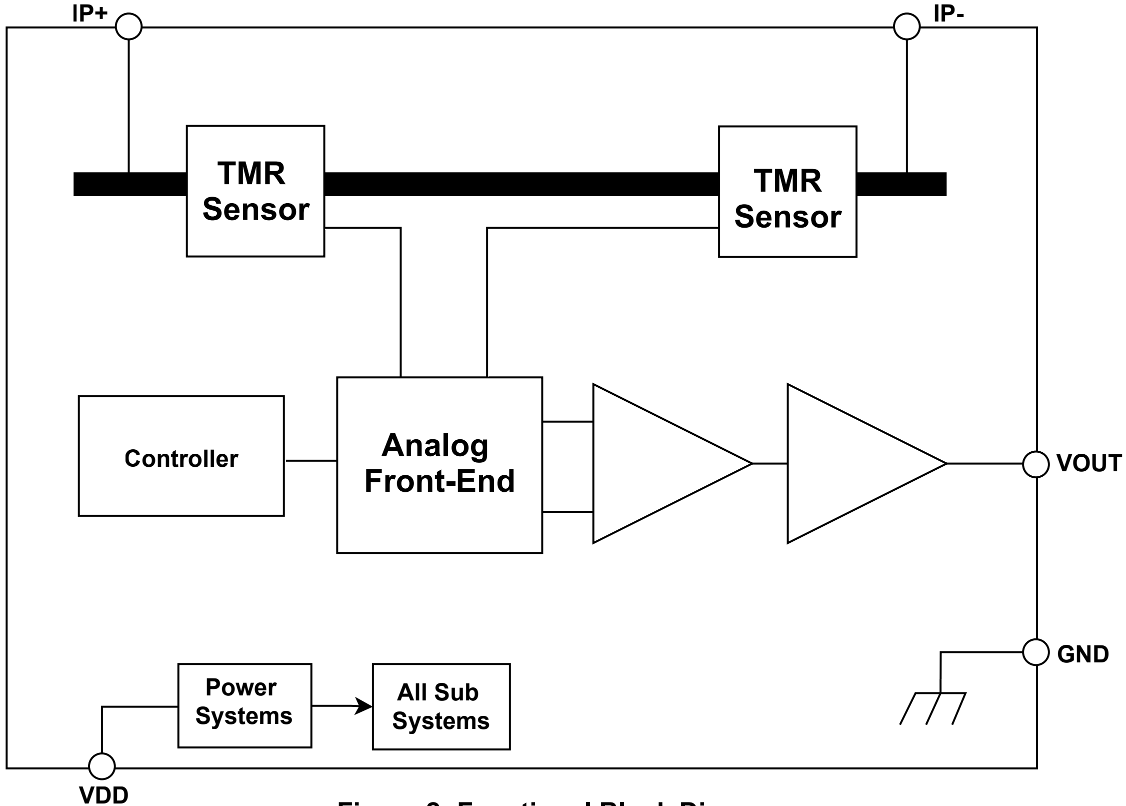

Figure 2: Functional Block Diagram

PINOUT DIAGRAM AND TERMINAL LIST TABLE

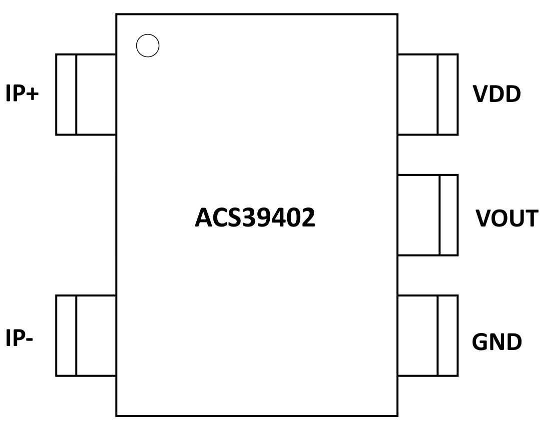

Figure 3: LH Package Pinout Diagram

Terminal List Table

Number	Name	Function
1, 2	IP	Integrated current sensing path
3	GND	Device ground
4	VOUT	Voltage output
5	VDD	Device supply voltage

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COMMON ELECTRICAL CHARACTERISTICS: Valid through full operating temperature range, T_A = –40°C to 125°C, C_{BYPASS} = 1 µF, and V_{DD} = 5.0 V unless otherwise specified. Minimum and maximum values are tested in production or validated by design and characterization.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{DD}		3.0	5	5.5	V
Supply Current	I_{DD}	No load present on VOUT	–	–	9	mA
Supply Bypass Capacitance	C_{BYPASS}	VDD to GND	–	1	–	µF
VOUT Resistive Load	R_{L_VOUT}	VOUT to GND, VOUT to VDD	4.7	–	–	kΩ
VOUT Capacitive Load	C_{L_VOUT}	VOUT to GND	–	–	10	nF
Power-On Reset Voltage	V_{POR}	V_{DD} rising 1 V/20 ms	–	–	2.9	V
Power-On Reset Hysteresis	V_{POR_HYS}	V_{DD} rising/falling 1 V/20 ms	70		–	mV
Power-On Time	t_{PO}	T_A = 25°C, V_{DD} rising 1 V/20 ms	–	2	–	µs
Rise Time	t_R	T_A = 25°C, C_L = 1 nF	–	0.75	–	µs
Response Time	t_{RESP}	T_A = 25°C, C_L = 1 nF	–	1	–	µs
Propagation Delay	t_{PD}	T_A = 25°C, C_L = 1 nF	–	0.4	–	µs
Bandwidth	BW	Small signal –3 dB, C_L = 1 nF	–	500	–	kHz
Output Saturation Voltage [1]	V_{SAT_H}	R_L = 4.7 kΩ to GND	V_{DD} – 0.3	–	–	V
	V_{SAT_L}	R_L = 4.7 kΩ to VCC	–	–	0.3	V

[1] The sensor may continue to respond to current beyond the specified current sensing range, I_{PR}, until the output saturates at the high or low saturation voltage; however, the linearity and performance beyond the specified current sensing range are not validated.

ACS39042KLHBTR-010U PERFORMANCE CHARACTERISTICS: Valid through full operating temperature range, T_A = –40°C to 125°C, C_{BYPASS} = 1 µF, and V_{DD} = 5.0 V unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
NOMINAL PERFORMANCE						
Current Sensing Range	I_{PR}		0	–	10	A
Sensitivity	Sens	$I_{PR(min)} < I_P < I_{PR(max)}$	–	400	–	mV/A
Quiescent Voltage Output	V_{QVO}	I_P = 0 A	–	0.5	–	V
ERROR COMPONENTS						
Sensitivity Error [1]	E_{SENS}	I_P = 3 A, T_A = 25°C to 125°C	–2.5	–	2.5	%
		I_P = 3 A, T_A = –40°C to 25°C	–2.8	–	2.8	%
Quiescent Voltage Output Error [1]	V_{QVO}	I_P = 0 A, T_A = 25°C	–30	–	30	mV
		I_P = 0 A, T_A = 125°C	–110	–	110	mV
		I_P = 0 A, T_A = –40°C	–65	–	65	mV
Noise	N	T_A = 25°C, C_L = 1 nF, BW = 125 kHz	–	4	–	mV_{RMS}
Ratiometry Sensitivity Error	$E_{SENS\_RAT\_E}$	$V_{DD(MIN)}$ to $V_{DD(MAX)}$, T_A = –40°C to 125°C	–1	–	1	%
Ratiometry Quiescent Voltage Output Error	$V_{QVO\_RAT\_E}$	$V_{DD(MIN)}$ to $V_{DD(MAX)}$ compared to 5 V, T_A = –40°C to 125°C	–30	–	30	mV
ERROR COMPONENTS INCLUDING LIFETIME DRIFT [2]						
Sensitivity Error Including Lifetime Drift	E_{SENS}	T_A = –40°C to 125°C	–	±1	–	%
Quiescent Voltage Output Error Including Lifetime Drift	V_{QVO_E}	I_P = 0 A, T_A = –40°C to 125°C	–	±4.5	–	mV

[1] Minimum (Min. or min) and maximum (Max. or max) of sensitivity and QVO error are calculated as $\mu \pm 3\sigma$ and applied symmetrically.
[2] Lifetime drift is the mean drift of worst-case distribution observed after AEC-Q100 qualification stresses.

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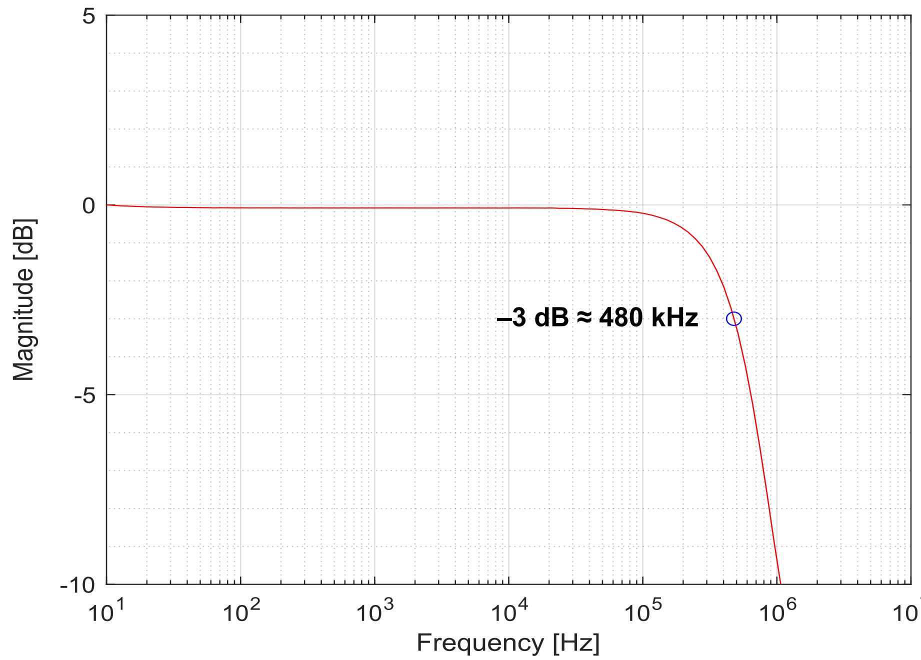
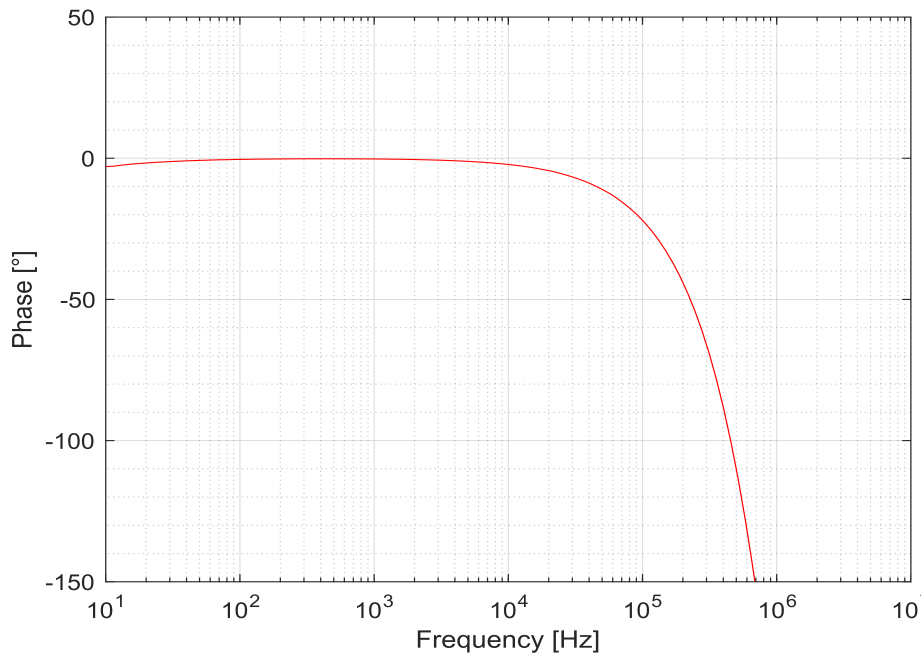
TYPICAL FREQUENCY RESPONSE PERFORMANCE DATA





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RESPONSE CHARACTERISTICS DEFINITIONS AND PERFORMANCE DATA

Response Time (t_{RESP})

The time interval between a) when the sensed input current reaches 90% of its full-scale value, and b) when the sensor output, V_{OUT}, reaches 90% of its full-scale output value.

Propagation Delay (t_{PD})

The time interval between a) when the sensed input current reaches 20% of its full-scale value, and b) when the sensor output, V_{OUT}, reaches 20% of its full-scale output value.

Rise Time (t_R)

The time interval between a) when the sensor output, V_{OUT}, reaches 10% of its full-scale value, and b) when the sensor output, V_{OUT}, reaches 90% of its full-scale value.

Response Time, Propagation Delay, Rise Time, and Output Slew Rate

Applied current step with 10%-90% rise time = 250 ns

Test Conditions: T_A = 25°C, C_{BYPASS} = 0.1 µF

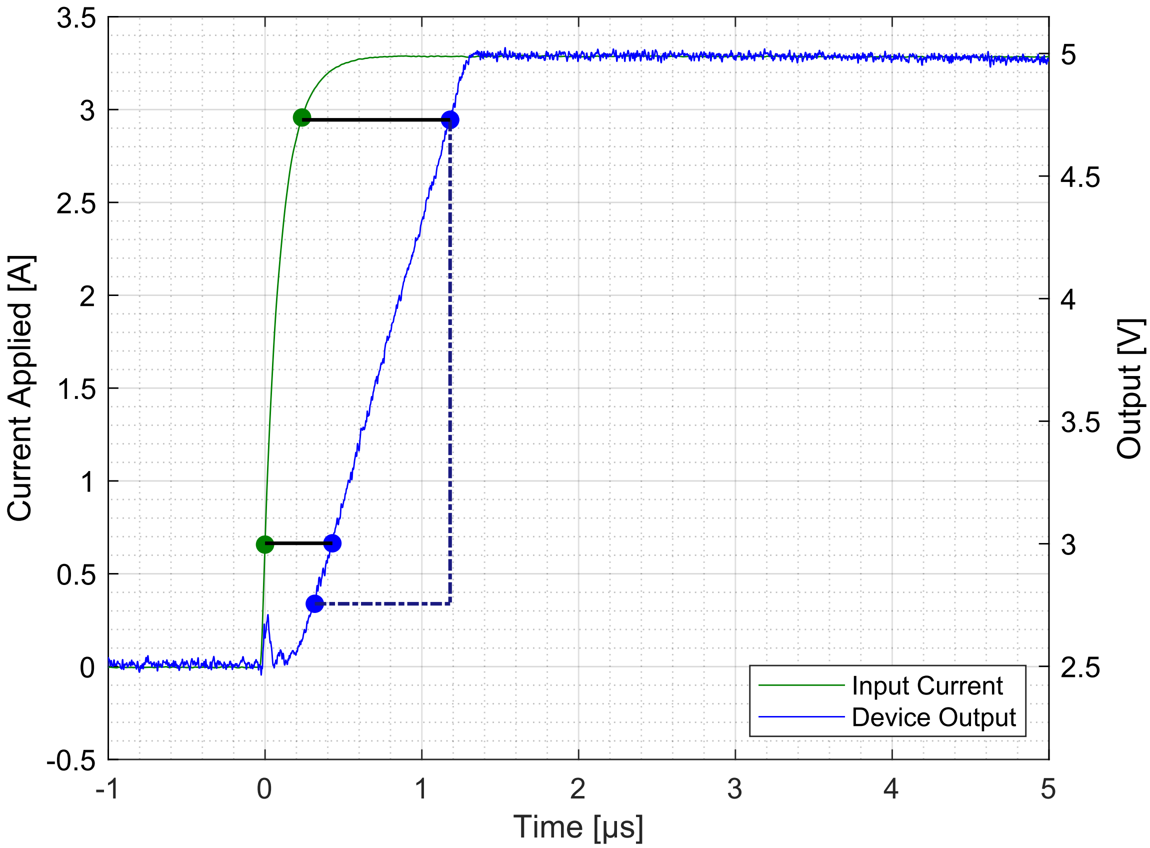

Figure 4: Step Response Characteristics

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FUNCTIONAL DESCRIPTION OF POWER-ON AND POWER-OFF OPERATION

Introduction

The graphs in this section show the behavior of V_{OUT} as V_{DD} reaches or reduces to less than the required power-on voltage. The same labeling convention for different voltage thresholds is used in Figure 5 and Figure 6. References in brackets "[ ]" are valid for each of these graphs.

POWER-ON OPERATION

As V_{DD} ramps up, the VOUT pin is in a high-impedance (high-Z) state until V_{DD} increases to greater than V_{POR} [1]. Once V_{DD} is greater than V_{POR} [1], V_{OUT} enters typical operation and starts to respond to applied current, I_P.

POWER-OFF OPERATION

As V_{DD} reduces to less than $V_{POR} – V_{POR\_HYS}$, the outputs enter a high-Z state. The hysteresis on the power-on voltage prevents noise on the supply line from causing V_{OUT} to repeatedly enter and exit the high-Z state at approximately the V_{POR} level.

NOTE: Because the device is entering a high-Z state and is not driving the output, the time it takes the output to reach a steady state depends on the external circuitry.

Voltage Thresholds

POWER-ON RESET RELEASE VOLTAGE (V_{POR})

If V_{DD} reduces to less than $V_{POR} – V_{POR\_HYS}$ [2] while the sensor is in operation, the digital circuitry turns off and the output re-enters a high-Z state. After V_{DD} recovers and exceeds V_{POR} [1], the output enters typical operation after a delay of t_{PO}.

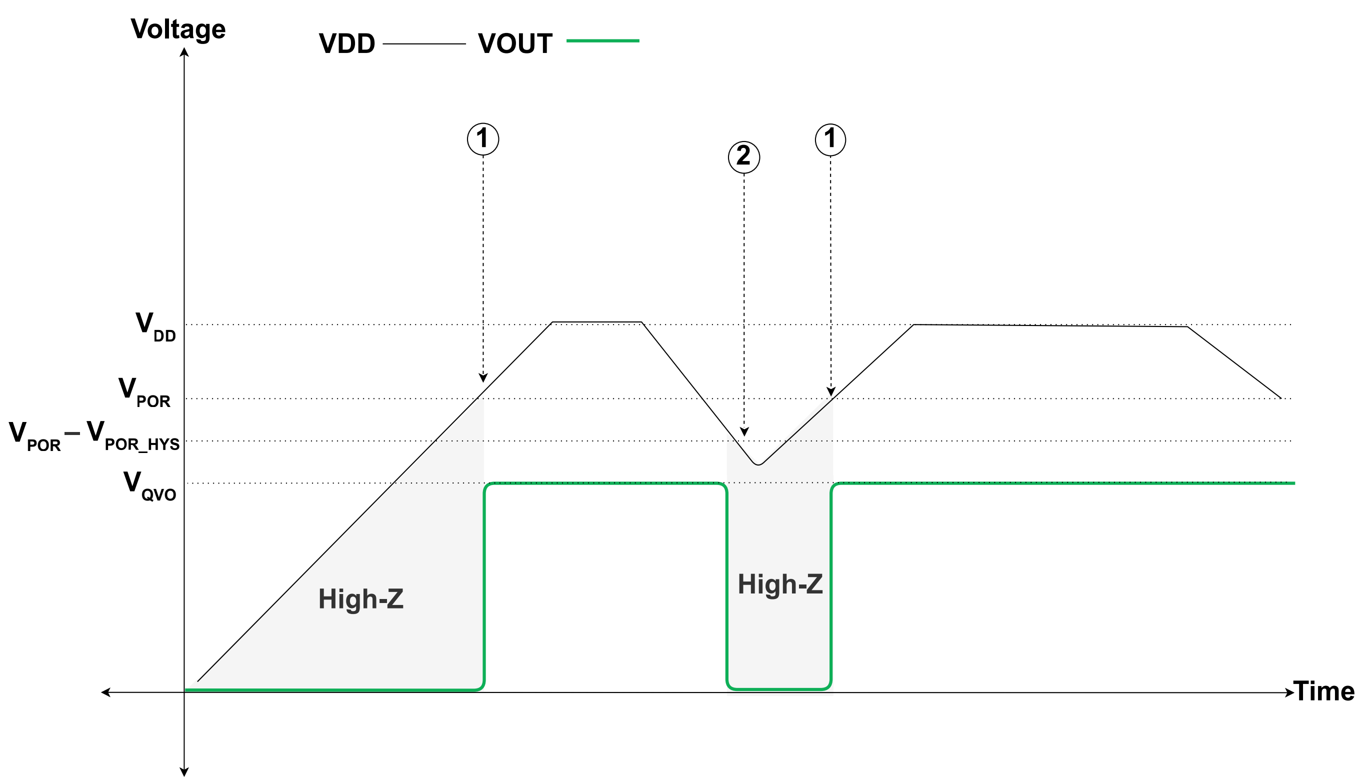

Figure 5: Power-On and Power-Off Behavior

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Timing Thresholds

POWER-ON DELAY (t_{PO})

When the supply voltage reaches V_{POR} [1], the device requires a finite time to power its internal components before the outputs are released from the high-impedance state and start to respond to the measured current, I_P. Power-on time, t_{PO}, is defined as the time it takes for the output voltage to settle within ±10% of its steady-state value under an applied current, I_P, which can be observed in Figure 6 as the time from [1] to [A].

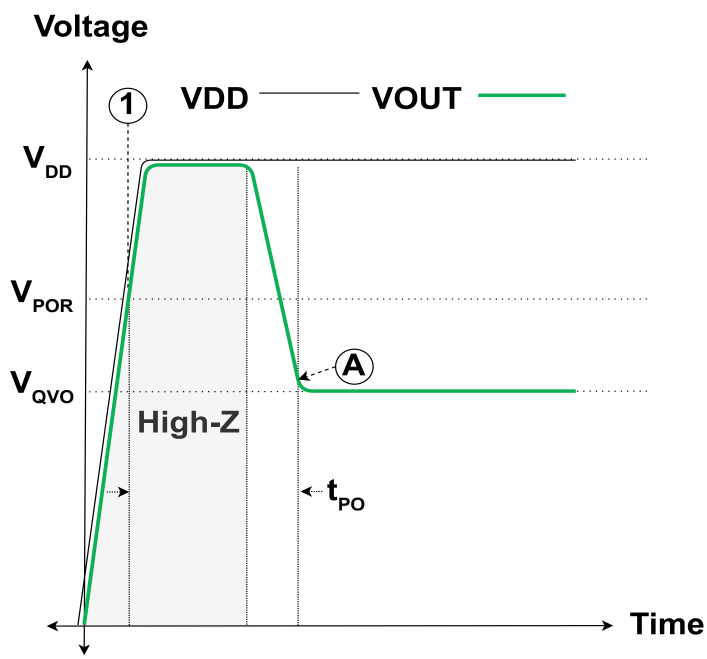

Figure 6: Power-On Delay, t_{PO}

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DEFINITIONS OF OPERATING AND PERFORMANCE CHARACTERISTICS

Quiescent Voltage Output (V_{QVO})

Quiescent voltage output, V_{QVO}, is defined as the voltage on the output, V_{OUT}, when current is not applied, $I_P = 0$.

Quiescent Voltage Output Error (V_{QVO_E})

Quiescent voltage output error, V_{QVO_E}, is defined as the deviation of V_{QVO} from the nominal target value in production testing.

Quiescent Voltage Output Temperature Drift (V_{QVO_T})

Quiescent voltage output temperature drift, V_{QVO_T}, is defined as the expected deviation of V_{QVO} from its value at T_A= 25°C throughout the temperature ranges T_A= –40°C to 25°C, and T_A= 25°C to 125°C, based on the observed three-sigma temperature drifts.

Output Saturation Voltage (V_{SAT_H} and V_{SAT_L})

Output saturation voltage, V_{SAT}, is defined as the low or high voltage that V_{OUT} does not exceed. V_{SAT_H} is the highest voltage the output can reach; V_{SAT_L} is the lowest.

NOTE: A change in sensitivity does not change the V_{SAT} points.

Sensitivity (Sens)

Sensitivity (Sens) is defined as the ratio of the V_{OUT} swing and the current through the primary conductor, I_P. The current causes a voltage change on V_{OUT} away from V_{QVO} until the V_{SAT} point is reached. The magnitude and direction of the output voltage is proportional to the magnitude and direction of the current, I_P. The proportional relationship between output voltage and current is sensitivity, defined as:

$$Sens = \frac{V_{OUT(IP_1)} - V_{OUT(IP_2)}}{IP_1 - IP_2}$$

where I_{P1} and I_{P2} are two different currents, and $V_{OUT}(I_{P1})$ and $V_{OUT}(I_{P2})$ are the respective output voltages, at VOUT, at those currents.

Sensitivity Error (E_{SENS})

Sensitivity error, E_{SENS}, is the deviation of Sensitivity from the nominal sensitivity target value in production testing.

Ratiometry Sensitivity Error ($E_{SENS\_RAT\_E}$)

The ACS39402 is a ratiometric sensor. When the power supply voltage is changed the output scales proportionally. Ratiometry Sensitivity error is the difference between the actual and the expected change in sensitivity relative to 5 V. For example, the ideal sensitivity of the ACS39042KLHBTR-010U at 3.3 V is:

400 mV/A × 3.3 / 5 = 264 mV/A

This scaling keeps the full-scale output current measurement the same, so that 10 A into the device gives a maximum output swing at both 5 V and 3.3 V supply without saturating.

Using the 5 V sensitivity error as a reference, an additional amount of sensitivity error up to $E_{SENS\_RAT\_E}$ can incurred within the operational range of V_{DD}. If the sensitivity error of a particular device at 5.0 V was 1%, and sensitivity error may increase by an amount equal to $E_{SENS\_RAT\_E}$.

Ratiometry Offset Error ($V_{QVO\_RAT\_E}$)

In the same manner as $E_{SENS\_RAT\_E}$, when changing V_{DD}, the offset of the sensor can shift from the scaled offset target by an additional amount equal to $V_{QVO\_RAT\_E}$.

For example, the target offset at 5 V of the ACS39042KLHBTR-010U is 0.5 V. Scaling that down for 3.3 V V_{DD} operation, the output target is 0.33 V. If the offset error at 5 V was 20 mV, at 3.3 V supply operation the offset could increase by an amount equal to $V_{QVO\_RAT\_E}$

Noise (N)

Noise, N, is the output-referred noise of the ACS39402. This is the total RMS noise at the output of the sensor, and it includes noise sources within the sensor itself.

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THERMAL PERFORMANCE

Thermal Rise vs. Primary Current

Resistive heating due to the flow of electrical current in the package should be considered during the thermal design of the application. The sensor, printed circuit board (PCB), and contacts to the PCB generate heat and act as a heat sink.

The thermal response is highly dependent on PCB layout, copper thickness, cooling methods, and the profile of the injected current, including peak current, current on-time, and duty cycle.

In-pad vias help improve thermal performance. Placing vias under the copper pads of the current sensor reduces electrical resistance and improves heat conduction to the PCB, while vias outside of the pads limit the current path to the top of the PCB trace and have worse heat-sink capability under the part (see Figure 7 and Figure 8).

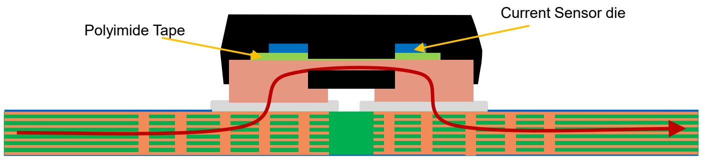

Figure 7: With In-Pad Vias

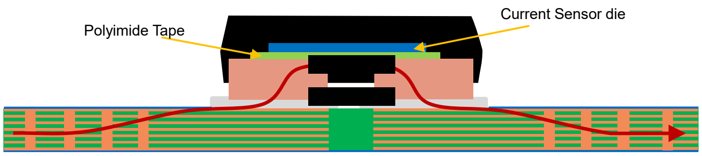

Figure 8: Without In-Pad Vias

The measured increase in steady-state die temperature of the ACS39402 versus DC continuous current at an ambient temperature, T_A, of 25°C, is shown in Figure 9 for two board designs: one with filled vias under copper pads and the other without vias under copper pads.

The measured increase in steady-state die temperature of the ACS39402 versus DC continuous current at an ambient temperature of 25°C and 125°C is shown in Figure 10.

The thermal capacity of the ACS39402 should be verified by the end user in the application-specific conditions. The maximum junction temperature, $T_{J(max)}$ (165°C), should not be exceeded. A measurement of the temperature at the top of the package is a close approximation of the die temperature.

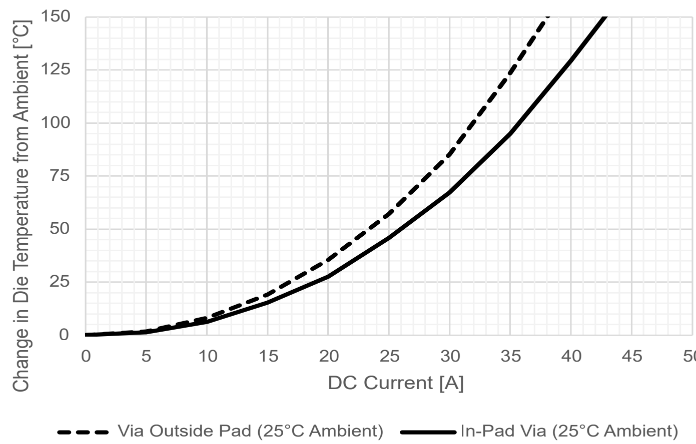

Figure 9: Comparison of Die-Temperature Increase With and Without In-Pad Vias at T_A = 25°C

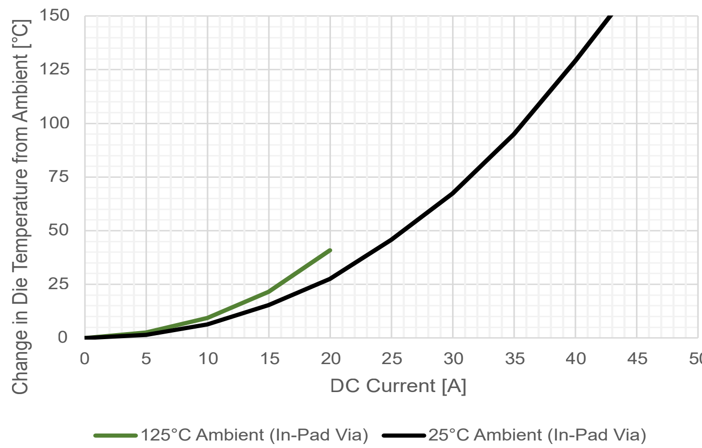

Figure 10: Comparison of Die-Temperature Increase at T_A = 25°C and T_A = 125°C With In-Pad Vias

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Evaluation Board Layout

Thermal data was collected using the LH current sensor evaluation board (ACSEVB-LH5, TED-0004112) in Figure 11.

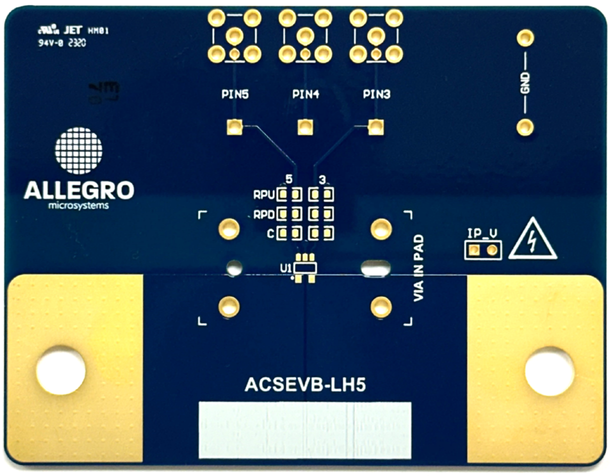

Figure 11: LH Package Allegro Evaluation Board

Design support files for the ACSEVB-LH5 evaluation board are available for download from the Allegro website. For more information, see the technical documents section of the ACS39402 product page on the Allegro website.

CURRENT RANGE VS. TEMPERATURE

From –40°C to 25°C, there is a rating of up to 60 A for up to 200 ms, and from 25°C to 125°C, there is a rating of up to 60 A to 40 A for up to 200 ms with a derating slope of –0.2 A/°C. This range is a statement of allowable current excursions and on-times during transient events, such as overcurrent events.

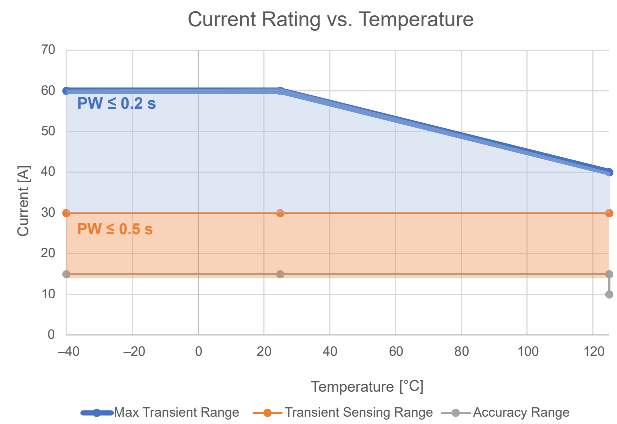

Figure 12: Current Ratings vs. Temperature

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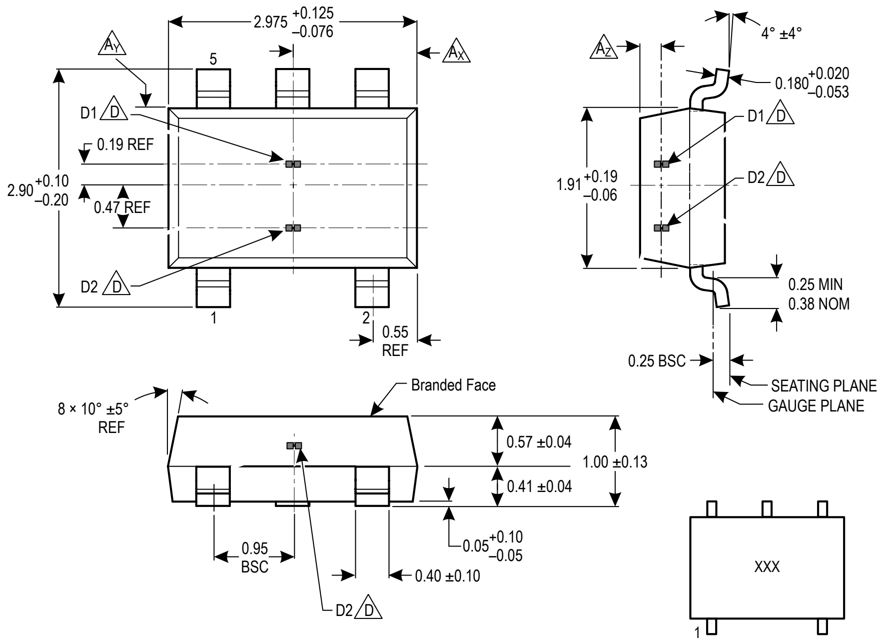
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use
(PRELIMINARY – Reference Drawing DWG-0000628, Rev. 01)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

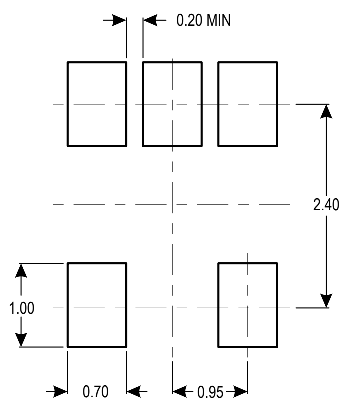


C Standard Branding Reference View

Line 1 = 3 characters

Line 1: Last 3 digits of Part Number

Branding scale and appearance at supplier discretion



B PCB Reference Layout View

- A_Y Active Area Distance, Y Axis, 0.765 mm +0.245/–0.18 and 1.425 mm +0.245/–0.18. A_Y includes package width and die placement tolerances.
- A_X Active Area Distance, X Axis, 1.49 mm +0.26/–0.24. A_X includes package length and die placement tolerances.
- A_Z Active Area Depth, Z Axis, 0.34 mm ±0.04
- B Reference land pattern layout; all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances (reference EIA/JEDEC Standard JESD51-5).
- C Branding Scale and appearance at supplier discretion
- D Hall Elements (D1 and D2), are 90 µm × 203.5 µm, not shown to scale

Figure 13: LH 5-Pin SOT23W Package Drawing

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Revision History

Number	Date	Description
–	December 19, 2025	Initial release

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