

Very High Precision, Programmable Linear Hall-Effect Sensor IC with Reverse Battery Protection and High-Bandwidth (240 kHz) Analog Output for Core-Based Current Sensing

FEATURES AND BENEFITS

- Factory-programmed segmented linear temperature compensation (TC) provides ultralow thermal drift
 - Sensitivity Error $\pm 1\%$
 - Offset Error ± 5 mV
- On-board supply regulator with reverse-battery protection provides high immunity to Electrical Overstress (EOS)
- Very fast response time (2 μ s)
- High operating bandwidth: DC to 240 kHz
- AEC-Q100 Grade 0, automotive qualified
- Customer-programmable, high-resolution offset, and sensitivity trim
- Extremely low noise and high resolution achieved via proprietary Hall element and low-noise amplifier circuits

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DESCRIPTION

The ACS70311 offers additional features than the ACS70310 and is recommended for new designs.

The Allegro ACS70310/1 IC incorporates a Hall element with BiCMOS integrated circuitry to provide a fully monolithic linear current sensor IC. The IC is sensitive to magnetic flux density orthogonal to the IC package surface and the output is an analog voltage proportional to the applied flux density. The ACS70310/1 is designed to be used in conjunction with a ferromagnetic core to provide highly accurate current sensing. The gain and offset drift over temperature is factory-programmed at Allegro and delivers a solution with $\pm 1\%$ sensitivity error and ± 5 mV offset error from 25°C to 150°C.

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PACKAGE: 4-pin SIP (suffix KT and OK)

TN Leadform



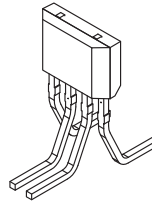
KT Package

TH Leadform (KT Only)



Contact Allegro about legacy leadform options

TX Leadform (OK Only)



OK Package
(ACS70311 Only)

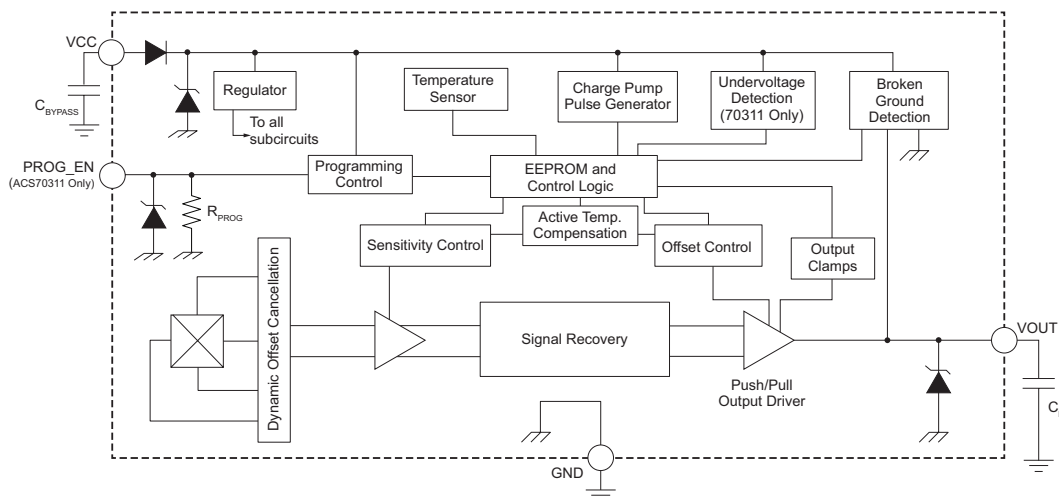


Figure 1: Functional Block Diagram

FEATURES AND BENEFITS (continued)

- Patented circuits suppress IC output spiking during fast current step inputs
- Wide selectable sensitivity range between 0.5 and 11.5 mV/G
- User-selectable ratiometric behavior of sensitivity, quiescent voltage, and clamps (ratiometry can be disabled), for simple interface with application A-to-D converter (ADC)
- Open circuit detection on the GND pin (broken wire)
- Customer-programmable Output Voltage Clamps provide short-circuit diagnostic capabilities
- Undervoltage detection (UVD), ACS70311 only
- Low-voltage programming, ACS70311 only
- Wide ambient temperature range: -40°C to 150°C
- Immune to mechanical stress
- Extremely thin package: 1 mm case thickness

DESCRIPTION (continued)

The ACS70310/1 is customer programmable. The absolute value of gain and offset can be programmed after manufacturing to provide customers with industry-leading current sensing accuracy. The sensor has a high operating bandwidth from DC to 240 kHz and a fast 2 μs response time. The ACS70310/1 is ideal for use in high-frequency automotive inverters and DC/DC converters where fast switching is required.

The ACS70311 offers all the features of the ACS70310 with the addition of undervoltage detection (UVD) as well as low-voltage programming that eliminates the need for voltages greater than V_{CC} during user programming. The ACS70311 is backward-compatible to the ACS70310, making it a drop-in replacement.

Broken ground wire detection, clamps, power-on reset, and under/overvoltage detection provide the required diagnostics for automotive applications.

The on-board supply regulator enables the VCC pin to survive voltages of $\pm 18\text{ V}$ and the VOUT pin to survive voltages of ± 16 to -6 V for added robustness in the harsh automotive environment.

Device parameters are specified across an extended ambient automotive temperature range: -40°C to 150°C . The ACS70310/1 sensor IC is provided in an extremely thin case (1 mm thick), 4-pin SIP (single in-line package, suffix KT). The KT package is available in straight leads (suffix TN) as well as lead-formed option (suffix TH), enabling surface mount assembly and a high tolerance to mechanical vibrations. The ACS70311 is also available in a 4-pin SIP (suffix OK) package offering longer and thicker leads compared to the KT package, making it an ideal choice for current sensing modules. The OK package is available in straight leads (suffix TN) as well as lead-formed option (suffix TX). Both packages are lead (Pb) free, with 100% matte tin leadframe plating.

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ACS70310 and ACS70311

Very High Precision, Programmable Linear Hall-Effect Sensor IC with Reverse Battery Protection and High-Bandwidth (240 kHz) Analog Output for Core-Based Current Sensing

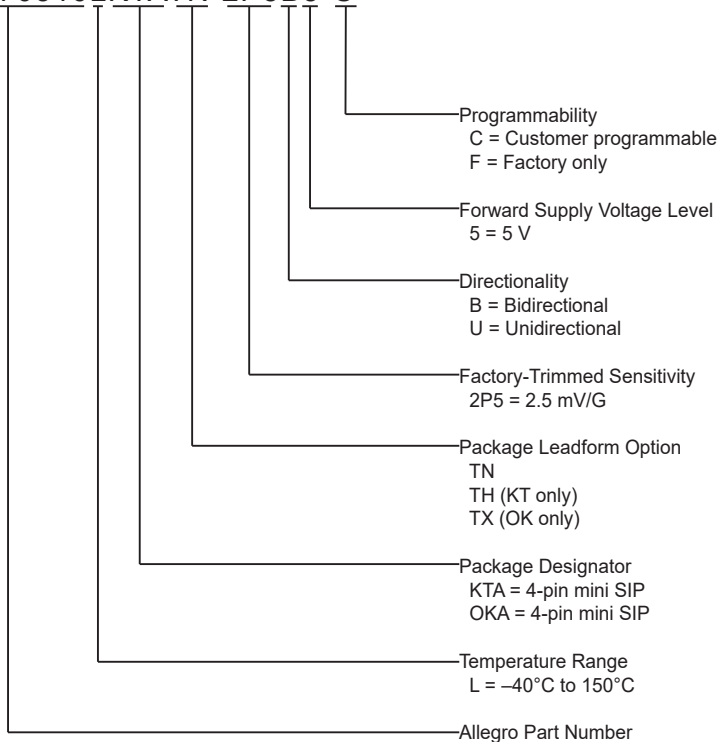
SELECTION GUIDE

Part Number [1]	Factory-Programmed Sensitivity (mV/G)	Programmable Sens Range (mV/G)	Low-Voltage Programming/ UVD Capable	Package [2]	T _A (°C)	Packing [3]
ACS70310LKTATN-001B5-C	1	0.5 to 1.2	No	4-pin SIP (suffix KT) TN leadform	-40 to 150	4000 pieces per 13-inch reel
ACS70310LKTATN-2P5B5-C	2.5	1.2 to 2.5				
ACS70310LKTATN-005B5-C	5	2.5 to 5.5				
ACS70310LKTATN-010B5-C	10	5.5 to 11.5				
ACS70311LKTATN-001B5-C	1	0.5 to 1.2	Yes			
ACS70311LKTATN-2P5B5-C	2.5	1.2 to 2.5				
ACS70311LKTATN-005B5-C	5	2.5 to 5.5				
ACS70311LKTATN-010B5-C	10	5.5 to 11.5				
ACS70311LOKATN-001B5-C	1	0.5 to 1.2	Yes	4-pin SIP (suffix OK) TN leadform		
ACS70311LOKATN-2P5B5-C	2.5	1.2 to 2.5				
ACS70311LOKATN-005B5-C	5	2.5 to 5.5				
ACS70311LOKATN-010B5-C	10	5.5 to 11.5				

[1] Characteristics are guaranteed within the sense programmable range of the corresponding part number.

[2] TH package leadform options available for the KT version. TX package leadform options available for the OK version. See Complete Selection Guide for part numbers with leadforming information.

ACS70310LKTATN-2P5B5-C



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}		18	V
Reverse Supply Voltage	V_{RCC}	$T_{J(max)}$ should not be exceeded	-18	V
Forward Output Voltage	V_{OUT}	$V_{OUT} < V_{CC} + 2\text{ V}$	16	V
Reverse Output Voltage	V_{ROUT}	Difference between V_{CC} and output should not exceed 20 V	-6	V
Output Current	I_{OUT}	Maximum survivable sink or source current on the output	± 10	mA
Forward Program Enable Voltage	V_{PROG}	$V_{PROG} < V_{CC} + 2\text{ V}$; ACS70311 only	6	V
Reverse Program Enable Voltage	V_{RPROG}	ACS70311 only	-0.5	V
Operating Ambient Temperature	T_A	L temperature range	-40 to 150	$^{\circ}\text{C}$
Storage Temperature	T_{stg}		-65 to 165	$^{\circ}\text{C}$
Maximum Junction Temperature	$T_{J(max)}$		165	$^{\circ}\text{C}$
Maximum Field Range	B	Input field range to which the part will respond	± 3000	G

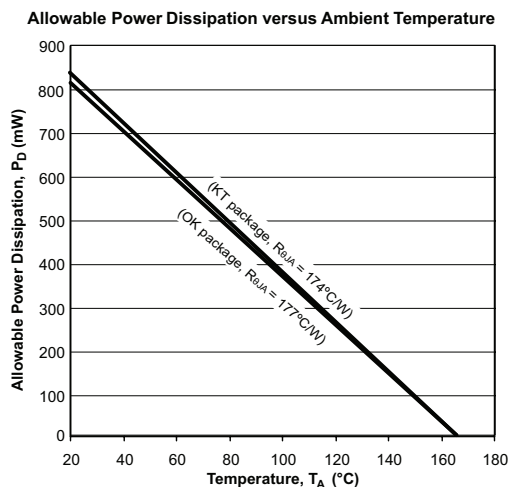
ESD RATINGS

Characteristic	Symbol	Test Conditions	Value	Unit
Human Body Model	V_{HBM}	Per JEDEC JS-001, ACS70310 devices	± 12	kV
		Per JEDEC JS-001, ACS70311 devices	± 8	kV
Charged Device Model	V_{CDM}	Per JEDEC JS-002	± 1	kV

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions [2]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Package KT, on 1-layer PCB with exposed copper limited to solder pads	174	$^{\circ}\text{C}/\text{W}$
		Package OK, on 1-layer PCB with exposed copper limited to solder pads	177	$^{\circ}\text{C}/\text{W}$

[2] Additional thermal information available on the Allegro website



PINOUT DIAGRAM AND TERMINAL LIST TABLES

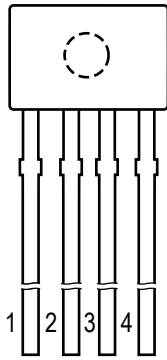


Figure 2: KT and OK Package Pinout Diagram
(Ejector pin mark on opposite side)

ACS70310 Terminal List Table

Number	Name	Function
1	VCC	Input Power Supply; also used for programming
2	VOUT	Output Signal, also used for programming
3	NC/GND	Connect to GND for optimal ESD performance
4	GND	Ground

ACS70311 Terminal List Table

Number	Name	Function
1	VCC	Input Power Supply; also used for programming
2	VOUT	Output Signal, also used for programming
3	PROG_EN	Low-Voltage Programming Enable pin; Connect to GND for optimal ESD performance
4	GND	Ground

TYPICAL APPLICATION DRAWINGS

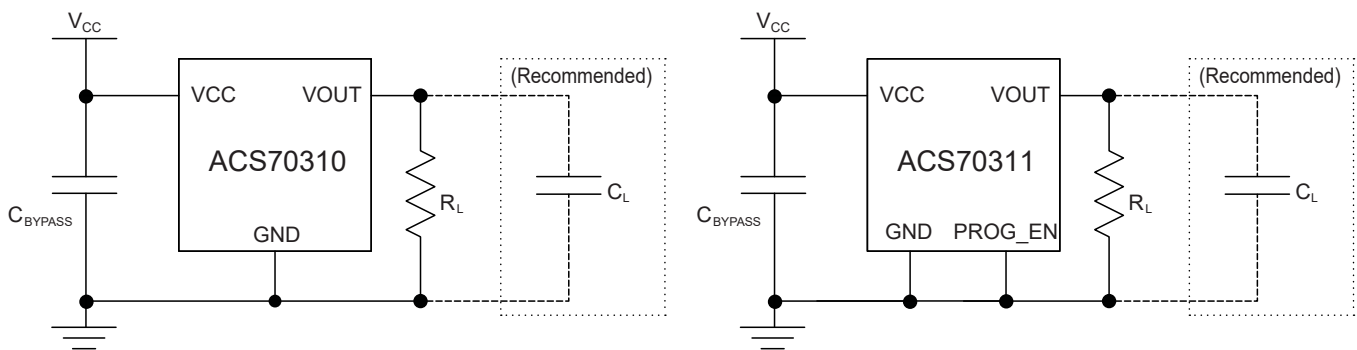


Figure 3: ACS70310/1 Typical Application Drawings

ACS70310 and ACS70311

Very High Precision, Programmable Linear Hall-Effect Sensor IC with Reverse Battery Protection and High-Bandwidth (240 kHz) Analog Output for Core-Based Current Sensing

OPERATING CHARACTERISTICS: Valid over full operating temperature range of T_A , $C_{BYPASS} = 0.1 \mu\text{F}$, and $V_{CC} = 5 \text{V}$, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}		4.5	5	5.5	V
Supply Current	I_{CC}	No load on VOUT; V_{CC} @ 4.5, 5, and 5.5 V	–	13	15	mA
Power-On Reset Voltage	V_{POR_H}	$T_A = 25^\circ\text{C}$, V_{CC} rising, 70310 Only	3.7	3.9	4.3	V
	V_{POR_L}	$T_A = 25^\circ\text{C}$, V_{CC} falling, 70310 Only	3.0	3.4	3.75	V
Power-On Reset Hysteresis	V_{POR_HYS}	$T_A = 25^\circ\text{C}$, 70310 Only	440	500	560	mV
Power-On Reset Release Time	t_{POR_R}	$T_A = 25^\circ\text{C}$, V_{CC} rising, 70310 Only	–	32	–	μs
Power-On Delay Time	t_{PO}	$T_A = 25^\circ\text{C}$, $C_{BYPASS} = \text{open}$, $C_L = 1 \text{ nF}$, 70310 Only	–	80	–	μs
Overvoltage Detection [2]	V_{OVD_H}	$T_A = 25^\circ\text{C}$	–	6.5	–	V
	V_{OVD_L}	$T_A = 25^\circ\text{C}$	–	6	–	V
Undervoltage Detection [2]	V_{UVD_H}	$T_A = 25^\circ\text{C}$, ACS70311 only	4.0	4.2	4.4	V
	V_{UVD_L}	$T_A = 25^\circ\text{C}$, ACS70311 only	3.6	3.8	4	V
UVD Hysteresis [2]	V_{UVD_HYS}	$T_A = 25^\circ\text{C}$, ACS70311 only	–	250	–	mV
UVD Enable/Disable Delay Time [2]	t_{UVD_EN}	$T_A = 25^\circ\text{C}$, ACS70311 only	–	64	–	μs
	t_{UVD_DIS}	$T_A = 25^\circ\text{C}$, ACS70311 only	–	14	–	μs
Temperature Compensation Power-On Time	t_{TC}	$T_A = 150^\circ\text{C}$, $C_{BYPASS} = \text{open}$, $C_L = 1 \text{ nF}$, Sens = 1 and 10 mV/G	–	146	–	μs
Supply Zener Clamp Voltage	V_Z	$T_A = 25^\circ\text{C}$, $I_{CC} = 30 \text{ mA}$	18	20	–	V
OUTPUT CHARACTERISTICS						
DC Output Resistance	R_{OUT}	$T_A = 25^\circ\text{C}$	2	4	8	Ω
Output Load Resistance [1]	R_L	VOUT to GND or VCC	4.7	10	–	k Ω
Output Load Capacitance	C_L	VOUT to GND	–	–	5	nF
Output Voltage Saturation	V_{SAT_H}	$T_A = 25^\circ\text{C}$, $R_L = 10 \text{ k}\Omega$ to GND, Bias = 400 G	4.75	4.8	–	V
	V_{SAT_L}	$T_A = 25^\circ\text{C}$, $R_L = 10 \text{ k}\Omega$ to VCC, Bias = 400 G	–	0.2	0.25	V
Output Voltage Clamp	V_{CLP_H}	$T_A = 25^\circ\text{C}$, $R_L = 10 \text{ k}\Omega$ to GND, Bias = 400 G	4.65	4.7	4.75	V
	V_{CLP_L}	$T_A = 25^\circ\text{C}$, $R_L = 10 \text{ k}\Omega$ to VCC, Bias = 400 G	0.25	0.3	0.36	V
Output Voltage with Broken GND	V_{BRK_L}	$T_A = 25^\circ\text{C}$, $R_L = 10 \text{ k}\Omega$ to GND, Pin 3 = open	0	100	200	mV
	V_{BRK_H}	$T_A = 25^\circ\text{C}$, $R_L = 10 \text{ k}\Omega$ to VCC, Pin 3 = open	4.8	4.9	5	V
Noise	V_{IN}	$T_A = 25^\circ\text{C}$, $C_L = 1 \text{ nF}$, Sens = 5 mV/G	–	1.2	–	mG/ $\sqrt{\text{Hz}}$
	V_{ON}	$T_A = 25^\circ\text{C}$, Sens = 5 mV/G	–	3.7	–	mV _{RMS}
Propagation Delay Time	t_{pd}	$T_A = 25^\circ\text{C}$, $C_L = 1 \text{ nF}$, $R_L = 10 \text{ k}\Omega$	–	1.2	1.65	μs
Response Time	$t_{RESPONSE}$	$T_A = 25^\circ\text{C}$, $C_L = 1 \text{ nF}$, $R_L = 10 \text{ k}\Omega$	–	2.1	3	μs
Rise Time	t_r	$T_A = 25^\circ\text{C}$, $C_L = 1 \text{ nF}$, $R_L = 10 \text{ k}\Omega$	–	1.9	–	μs
Output Slew Rate	SR	$T_A = 25^\circ\text{C}$, $C_L = 1 \text{ nF}$, $R_L = 10 \text{ k}\Omega$	410	480	550	V/ms
Bandwidth	BW	Small signal –3 dB, $C_L = 1 \text{ nF}$, $T_A = 25^\circ\text{C}$; Sens = 10 mV/G	–	240	–	kHz
Chopping Frequency	f_c	$T_A = 25^\circ\text{C}$	–	1	–	MHz

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OPERATING CHARACTERISTICS (continued): Valid over full operating temperature range of T_A , $C_{BYPASS} = 0.1 \mu F$, and $V_{CC} = 5 V$, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
QUIESCENT OUTPUT VOLTAGE ($V_{OUT(Q)}$)							
Number of Fine QVO Programming Bits	QVO_FINE		–	9	–	bit	
Quiescent Voltage Output [3]	$V_{OUT(Q)}$	Unidirectional, $T_A = 25^\circ C$	0.495	0.5	0.505	V	
		Bidirectional, $T_A = 25^\circ C$	2.495	2.5	2.505	V	
Average Quiescent Voltage Output Programming Step Size [4]	$V_{OUT(Q)Step}$	$T_A = 25^\circ C$	–	1.18	–	mV	
Average Quiescent Voltage Output Temperature Compensation Step Size	$V_{OUT(Q)TCStep}$		–	$V_{OUT(Q)Step}$	–	mV	
SENSITIVITY (Sens)							
Coarse Sensitivity Programming Bits [5]	SENS_COARSE		–	2	–	bit	
Fine Sensitivity Programming Bits	SENS_FINE		–	9	–	bit	
Sensitivity Programming Range [6]	$Sens_{PR}$	SENS_COARSE = 0, -001B5 Devices	0.5	1	1.2	mV/G	
		SENS_COARSE = 1, -2P5B5 Devices	1.2	2.5	2.5	mV/G	
		SENS_COARSE = 2, -005B5 Devices	2.5	5	5.5	mV/G	
		SENS_COARSE = 3, -010B5 Devices	5.5	10	11.5	mV/G	
Average Sensitivity Programming Step Size	$Step_{SENS}$	SENS_COARSE = 0, -001B5 Devices	–	2.87	–	$\mu V/G$	
		SENS_COARSE = 1, -2P5B5 Devices	–	6.06	–	$\mu V/G$	
		SENS_COARSE = 2, -005B5 Devices	–	13.06	–	$\mu V/G$	
		SENS_COARSE = 3, -010B5 Devices	–	27.1	–	$\mu V/G$	
Average Sensitivity Temperature Compensation Step Size	$Step_{SENSTC}$	$T_A = -40^\circ C$ to $150^\circ C$	–	$Step_{SENS}$	–	$\mu V/G$	
SENSITIVITY ERROR							
Sensitivity Error	$Sens_{ERR}$	$T_A = 25^\circ C$	–1	–	1	%	
Sensitivity Drift Over Temperature	$\Delta Sens_{TC}$	$T_A = 25^\circ C$ to $150^\circ C$	–1	–	1	%	
		$T_A = -40^\circ C$ to $25^\circ C$	–1.2	–	1.2	%	
Sensitivity Linearity Error [7]	Lin_{ERR}	Measured at $\pm 400 G$ (1, 2.5, and 5 mV/G) or $\pm 200 G$ (10 mV/G)	$\leq \pm 2 kG$	–0.5	–	0.5	%
			$\leq \pm 3 kG$	–1.1	–	1.1	%
Sensitivity Ratiometry Error	$Rat_{ERRSENS}$	$V_{CC} = 4.85$ to $5.15 V$	–0.55	–	0.55	%	
QUIESCENT VOLTAGE OUTPUT ERROR							
Quiescent Voltage Output Error	$V_{OUT(Q)ERR}$	$T_A = 25^\circ C$	–5	–	5	mV	
Quiescent Voltage Output Drift Over Temperature	$\Delta V_{OUT(Q)TC}$	$T_A = 25^\circ C$ to $150^\circ C$	–5	–	5	mV	
		$T_A = -40^\circ C$ to $25^\circ C$	–5	–	5	mV	
Quiescent Voltage Output Ratiometry Error	$V_{RatERRVOUT(Q)}$	$V_{CC} = 4.85$ to $5.15 V$	–5	–	5	mV	

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OPERATING CHARACTERISTICS (continued): Valid over full operating temperature range of T_A , $C_{BYPASS} = 0.1 \mu F$, and $V_{CC} = 5 V$, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
LIFETIME [8]							
Quiescent Voltage Output Lifetime Drift	$V_{OUT(Q)_LIFE}$	$T_A = 25^\circ C$	–	0.4	–	mV	
Sensitivity Lifetime Drift	$Sens_{ERR_LIFE}$	$T_A = 25^\circ C$	KT	–	0.5	–	%
			OK	–	0.4	–	%

[1] Using a small R_L will increase output error; this error scales with output causing offset and symmetry error, i.e. using a $R_L = 4.7 k\Omega$ will cause a 4 mV error due to the resistor divider between the $R_{L(pulldown)}$ and the internal resistance of 4 Ω at 5 V output. Keep this in mind when sizing R_L .

[2] OVD/UVD was characterized on the bench. V_{CC} ramp rate of 0.5 V/ms and 1 V/ μs for thresholds and timing respectively. UVD enabled on ACS70311 devices only.

[3] Devices programmed to the typical values are guaranteed to meet the $\Delta V_{OUT(Q)TC}$ spec.

[4] This is an average and actual step can vary. For best results, check $V_{OUT(Q)}$ after every retrim. Refer to the Quiescent Voltage Output Programming Resolution in the definition section.

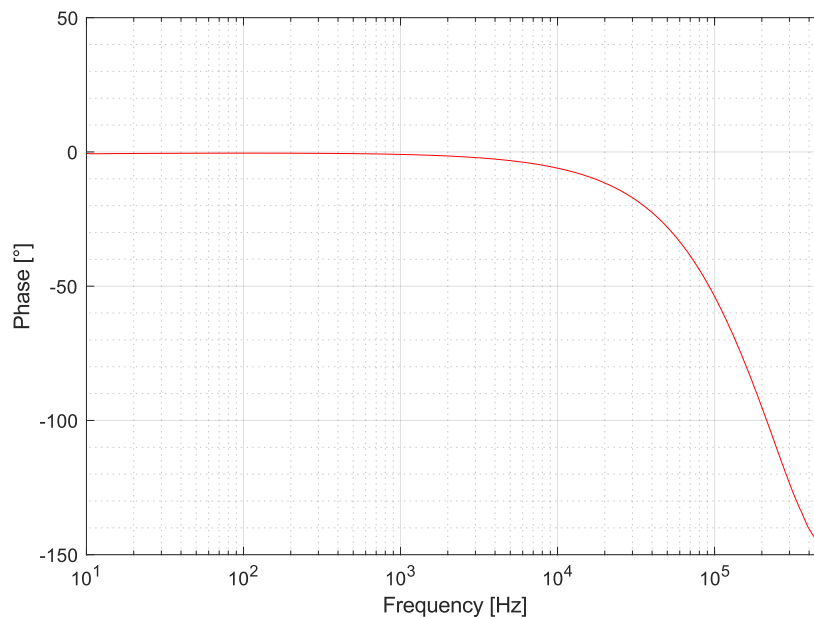
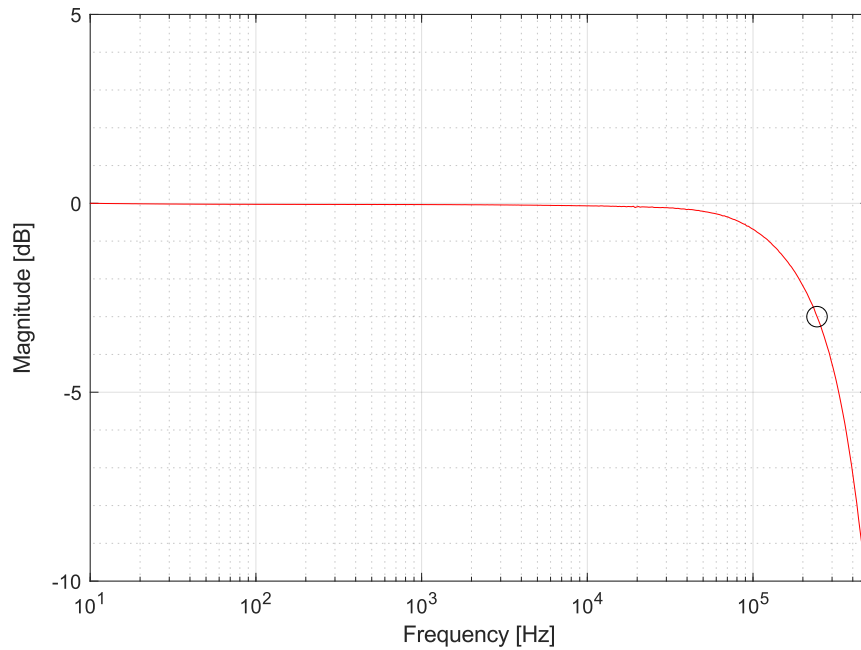
[5] Allegro guarantees limits of devices that remain within their factory-programmed SEN_COARSE and the corresponding $SENS_{PR}$ during customer programming.

[6] Device performance is guaranteed within these ranges. Typical value is the factory-programmed sensitivity.

[7] Validated by characterization and design.

[8] Lifetime drift numbers represent the average parameter drift seen during qualification.

CHARACTERISTIC PERFORMANCE
ACS70310/1 TYPICAL FREQUENCY RESPONSE



For information regarding bandwidth characterization methods used for the ACS70310/1, see the “Characterizing System Bandwidth” application note (<https://allegromicro.com/en/insights-and-innovations/technical-documents/hall-effect-sensor-ic-publications/an296169-ac720-bandwidth-testing>) on the Allegro website.

RESPONSE CHARACTERISTICS DEFINITIONS AND PERFORMANCE DATA

Response Time (t_{RESPONSE})

The time interval between a) when the applied magnetic field reaches 90% of its final value, and b) when the sensor output reaches 90% of its full-scale value.

Propagation Delay (t_{pd})

The time interval between a) when the applied magnetic field reaches 20% of its full-scale value, and b) when the sensor output reaches 20% of its full-scale value.

Rise Time (t_r)

The time interval between a) when the sensor reaches 10% of its full-scale value, and b) when it reaches 90% of its full-scale value.

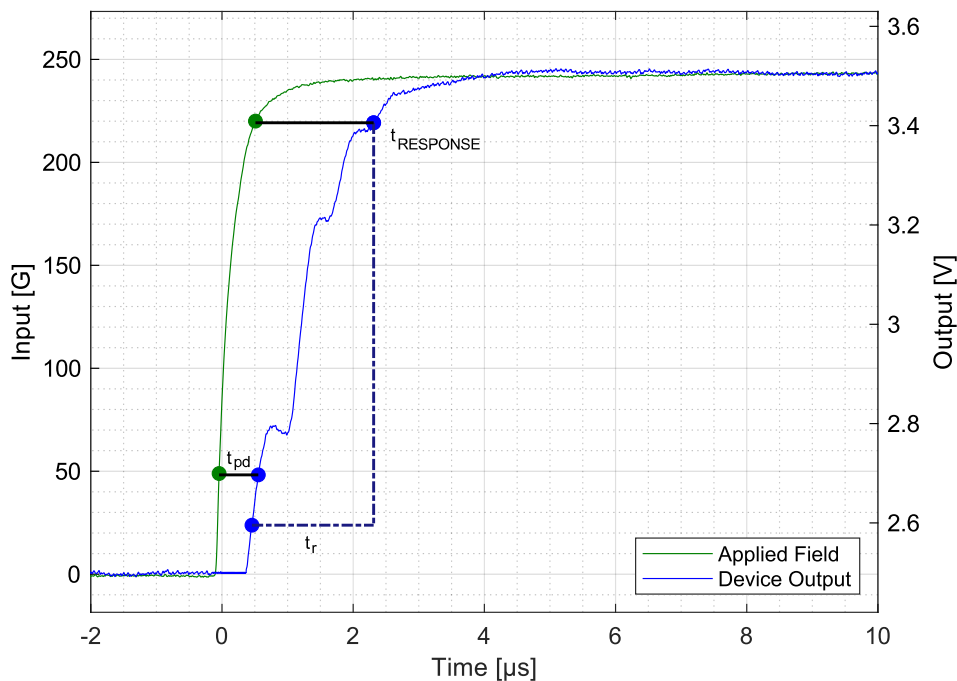
Output Slew Rate (SR)

The rate of change (V/ μs) in the output voltage from a) when the sensor reaches 10% of its full-scale value, and b) when it reaches 90% of its full-scale value.

Response Time, Propagation Delay, Rise Time, and Output Slew Rate

Applied step with 10%-90% rise time = 1 μs

Test Conditions: $T_A = 25^\circ\text{C}$, $C_{\text{BYPASS}} = 0.1 \mu\text{F}$, $C_L = 1 \text{ nF}$, $R_L = 10 \text{ k}\Omega$, 1 V output swing



Quiescent Voltage Output ($V_{OUT(Q)}$)

In the quiescent state (no significant magnetic field: $B = 0$ G), the output ($V_{OUT(Q)}$) has a constant ratio to the supply voltage (V_{CC}) throughout the entire operating ranges of V_{CC} and ambient temperature (T_A).

Before any programming, the Quiescent Voltage Output ($V_{OUT(Q)}$) has a nominal value of $V_{CC}/2$ for a bidirectional device and 0.5 V for unidirectional parts with a V_{CC} of 5 V.

Quiescent Voltage Output Programming Range

The Quiescent Voltage Output ($V_{OUT(Q)}$) can be programmed within the Quiescent Voltage Output Programming Range limits. Exceeding the specified Quiescent Voltage Output Programming Range limits will cause Quiescent Voltage Output Drift Over Temperature ($\Delta V_{OUT(Q)TC}$) to deteriorate beyond the specified values.

Average Quiescent Voltage Output Programming Step Size ($Step_{V_{OUT(Q)}}$)

The Average Quiescent Voltage Output Programming Step Size ($Step_{V_{OUT(Q)}}$) is determined using the following calculation:

$$V_{OUT(Q)Step} = \frac{V_{OUT(Q)maxcode} - V_{OUT(Q)mincode}}{2^n - 1}, \quad (1)$$

where n is the number of available programming bits in the trim range, 9 bits, $V_{OUT(Q)maxcode}$ is at decimal code 255, and $V_{OUT(Q)mincode}$ is at decimal code 256.

Quiescent Voltage Output Programming Resolution

The programming resolution for any device is half of its programming step size.

The step size of each bit can vary. For best accuracy, check $V_{OUT(Q)}$ after every trim. The devices DAC performance is screened and accounted in the factory-standard trim but becomes a possible source of error if the devices is reprogrammed beyond the Quiescent Voltage Output; programming beyond this range causes $\Delta V_{OUT(Q)TC}$ to be invalid.

Quiescent Voltage Output Drift Over Temperature ($\Delta V_{OUT(Q)TC}$)

The Quiescent Voltage Output ($V_{OUT(Q)}$) may drift from its nominal value through the operating ambient temperature (T_A). The Quiescent Voltage Output Drift Over Temperature ($\Delta V_{OUT(Q)TC}$) is defined as:

$$\Delta V_{OUT(Q)TC} = V_{OUT(Q)(T_A)} - V_{OUT(Q)(25^\circ C)} \quad (2)$$

$\Delta V_{OUT(Q)TC}$ should be calculated using the the measured value of $V_{OUT(Q)}$ at the current temperature and at 25°C.

Sensitivity (Sens) and Sensitivity Error ($Sens_{ERR}$)

The presence of a south polarity magnetic field, perpendicular to the branded surface of the package face, increases the output voltage from its quiescent value toward the supply voltage rail. The amount of the output voltage increase is proportional to the magnitude of the magnetic field applied.

Conversely, the application of a north polarity field decreases the output voltage from its quiescent value. This proportionality is specified as the magnetic sensitivity, Sens (mV/G), of the device, and it is defined as:

$$Sens = \frac{V_{OUT(BPOS)} - V_{OUT(BNEG)}}{BPOS - BNEG}, \quad (3)$$

where BPOS and BNEG are two magnetic fields with opposite polarities.

Sensitivity error is the error in percent between the factory-programmed sensitivity and the measured sensitivity value.

Factory-Programmed Sensitivity

Before any programming, Sensitivity has a nominal value that depends on the SENS_COARSE bits setting. Each ACS70310/1 variant has a different SENS_COARSE setting. The TC performance is guaranteed if the SENS_COARSE bit is in its default factory value and within the Sensitivity Programming Range corresponding to the SENS_COARSE bit.

Sensitivity Programming Range ($Sens_{PR}$)

The magnetic sensitivity (Sens) can be programmed around its initial value within the sensitivity range limits: $Sens_{PR}(min)$ and $Sens_{PR}(max)$. Exceeding the specified Sensitivity Range will cause Sensitivity Drift Over Temperature ($\Delta Sens_{TC}$) to deteriorate beyond the specified values.

Average Fine Sensitivity Programming Step Size (Step_{SENS})

This is change in the fine sensitivity parameter per code of sensf DAC. This value changes depending on SENS_COARSE. The over temperature performance of the device is guaranteed only for the factory programmed SENS_COARSE and its associated Sens_{PR}.

Sensitivity Programming Resolution

This resolution is equal to or less than $1/2 \times \text{Step}_{\text{SENS}}$. If the device is more than $1/2 \times \text{Step}_{\text{SENS}}$ but less than one $\text{Step}_{\text{SENS}}$ away from a desired trim, then an additional step in the correct direction will yield a resolution less than $1/2 \times \text{Step}_{\text{SENS}}$.

Sensitivity Drift Over Temperature ($\Delta\text{Sens}_{\text{TC}}$)

Sensitivity (sens) may drift from its expected value (Sens_EXPECTED) over the operating ambient temperature range (T_A). The Sensitivity Drift Over Temperature ($\Delta\text{Sens}_{\text{TC}}$) is defined as:

$$\Delta\text{Sens}_{\text{TC}} = \frac{\text{Sens}_{(T_A)} - \text{Sens}_{(25^\circ\text{C})}}{\text{Sens}_{(25^\circ\text{C})}} \times 100\% \quad (4)$$

Output Voltage Operating Range

The functional output voltage for optimal performance of the device is 0.5 V to 4.5 V output voltage where $V_{\text{CC}} = 5 \text{ V}$. The device can respond to magnetic fields that cause the output to go beyond these voltages, but parameters may not meet datasheet limits.

Sensitivity Linearity Error (Lin_{ERR})

The ACS70310/1 is designed to provide a linear output in response to a ramping applied magnetic field. Lin_{ERR} is valid from 0 G to $\pm 2000 \text{ G}$ input field while within the Output Voltage Operating Range. Consider two magnetic fields, B1 and B2. Ideally, the sensitivity of a device is the same for both fields, for a given supply voltage and temperature. Linearity error is present when there is a difference between the sensitivities measured at B1 and B2.

Linearity Error (%) is measured and defined as

$$\text{Lin}_{\text{ERR}} = \left(1 - \frac{\text{Sens}_{\text{B2}}}{\text{Sens}_{\text{B1}}} \right) \times 100\% \quad (6)$$

where:

$$\text{Sens}_{\text{Bx}} = \frac{|V_{\text{OUT}(\text{Bx})} - V_{\text{OUT}(\text{Q})}|}{B_x} \quad (7)$$

Ratiometry Error (Rat_{ERR})

The ACS70310/1 device features a ratiometric output. This means that the Quiescent Voltage Output ($V_{\text{OUT}(\text{Q})}$), Sensitivity (Sens), and Output Voltage Clamp (V_{CLP}) are proportional to the Supply Voltage (V_{CC}). When the supply voltage increases or decreases by a certain percentage, each characteristic also increases or decreases by the same percentage. Ratiometry Error is the difference between the measured change in the supply voltage relative to 5 V, and the measured change in each characteristic.

The Quiescent Voltage Output ratiometry error, Rat_{ERRVOUT(Q)} (%), for a given supply voltage (V_{CC}) is defined as:

$$\text{Rat}_{\text{ERRVOUT}(\text{QBI})} = \left[1 - \frac{\left(\frac{V_{\text{OUT}(\text{Q})(V_{\text{CC}})}{V_{\text{OUT}(\text{Q})(5\text{V})}} \right)}{\frac{V_{\text{CC}}}{5 \text{ V}}} \right] \times 100\% \quad (8)$$

The Quiescent Voltage Output Ratiometry Error, $V_{\text{RatERRVOUT}(\text{Q})}$ (mV), for a given supply voltage (V_{CC}) is defined as:

$$V_{\text{RATERRVOUT}(\text{Q})} = \left[\left(V_{\text{OUT}(5\text{V})} \times \frac{V_{\text{CC}}}{5\text{V}} \right) - V_{\text{OUT}(V_{\text{CC}})} \right] \quad (9)$$

The Sensitivity Ratiometry Error, Rat_{ERRSens} (%), for a given Supply Voltage (V_{CC}) is defined as:

$$\text{Rat}_{\text{ERRSens}} = \left(1 - \frac{\text{Sens}(V_{\text{CC}}) / \text{Sens}(5\text{V})}{V_{\text{CC}} / 5 \text{ V}} \right) \times 100\% \quad (10)$$

Power-On Reset Voltage (V_{POR})

On power-up, the ACS70310/1 is held in a reset state. The reset signal is disabled when V_{CC} reaches V_{POR_H} and time t_{PORR} has elapsed, allowing the output voltage to go from a high-impedance state into normal operation. During power-down, the reset signal is enabled when V_{CC} reaches V_{POR_L} , causing the output voltage to go into a high-impedance state.

Power-On Reset Release Time (t_{POR_R})

When V_{CC} rises to V_{POR_H} , the Power-On Reset counter starts. The ACS70310/1 output voltage will transition from a high-impedance state to normal operation only when the Power-On Reset Counter has reached t_{PORR} and V_{CC} has been maintained above V_{POR_H} .

Output Saturation Voltage (V_{SAT})

When output voltage clamps are disabled, the output voltage can swing to a maximum of V_{SAT_H} and to a minimum of V_{SAT_L} .

Broken Wire Voltage (V_{BRK})

If the GND pin is disconnected (broken wire event), the output voltage will go to V_{BRK_H} (if a load resistor is connected to VCC) or to V_{BRK_L} (if a load resistor is connected to GND).

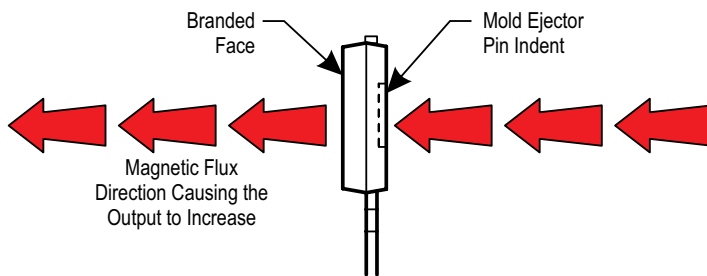


Figure 4: Magnetic Flux Polarity

Power-On Time (t_{PO})

When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field.

Power-On Time (t_{PO}) is defined as the time it takes for the output voltage to settle within $\pm 10\%$ of its steady-state value under an applied magnetic field, after the power supply has reached its minimum specified operating voltage ($V_{CC(min)}$) as shown in Figure 5.

Temperature Compensation Power-On Time (t_{TC})

After Power-On Time (t_{PO}) elapses, t_{TC} is required before a valid temperature compensated output.

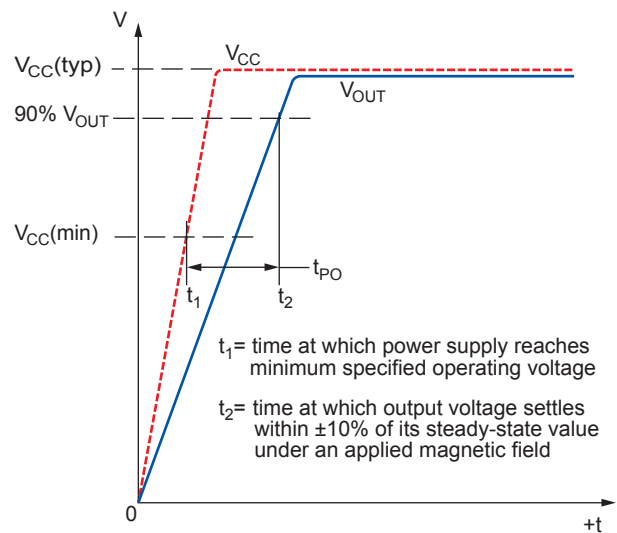


Figure 5: Power-On Time Definition

FUNCTIONAL DESCRIPTIONS

The descriptions in this section assume: Temperature = 25°C, no output load (R_L , C_L), and no magnetic field is present.

Power-On Reset (POR)

When the device is off, the output will be in a high-impedance state.

Power-On

As V_{CC} ramps up, the device output is in high-impedance until V_{CC} reaches V_{POR_H} . As V_{CC} rises above V_{POR_H} , the device output leaves the high impedance state and enters normal operating mode.

Overvoltage Detection (V_{OVD})

When V_{CC} is raised above the Overvoltage Detection enable voltage (V_{OVD_H}), the ACS70310/1 output stage enters high impedance. V_{OUT} will be pulled to V_{CC} with a pull-up R_L or pulled to GND with a pull-down R_L when V_{OVD_H} is reached. When programming the ACS70310/1, Overvoltage Detection must be active for communication. The ACS70310/1 output will resume normal operation after V_{CC} is below the Overvoltage Detection disable voltage, V_{OVD_L} . Note that Supply Voltage limits still apply for all operating characteristics.

Undervoltage Detection (V_{UVD})

When V_{CC} is dropped below the Undervoltage Detection enable voltage (V_{UVD_H}), the ACS70311 output stage drops close to GND, beyond the clamp or saturation voltage. The ACS70311 output will resume normal operation after V_{CC} is above the Undervoltage Detection disable voltage, V_{UVD_H} . Note that Supply Voltage limits still apply for all operating characteristics.

Power-Down

As V_{CC} ramps down, the device output is active until V_{CC} falls below V_{POR_L} . As V_{CC} falls below V_{POR_L} , the device output will enter a high-impedance state.

Power On/Off Profile

Figure 6 shows the analog output of the ACS70310 device at power on, entering and exiting OVD, and powering off. Where the red trace flattens out is the output entering high-impedance. If a load resistor was used, the output would be pulled to ground. Figure 7 shows the ACS70311 powering on with a pull-down resistor. The output follows V_{CC} ratiometrically after exiting POR and is pulled to ground after entering UVD.

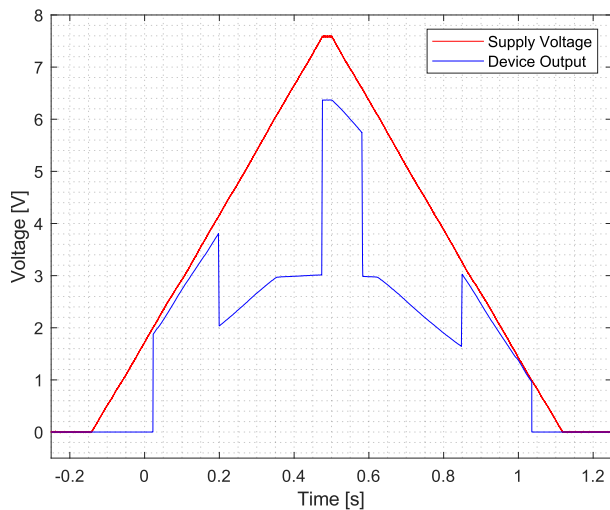


Figure 6: ACS70310 Power On/Off and OVD, no R_L

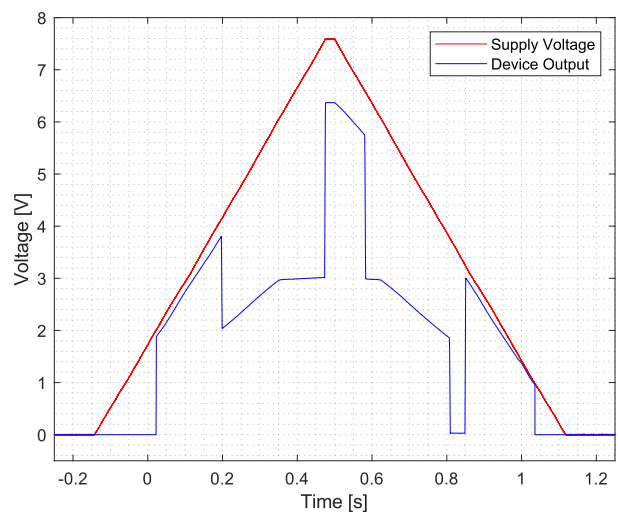


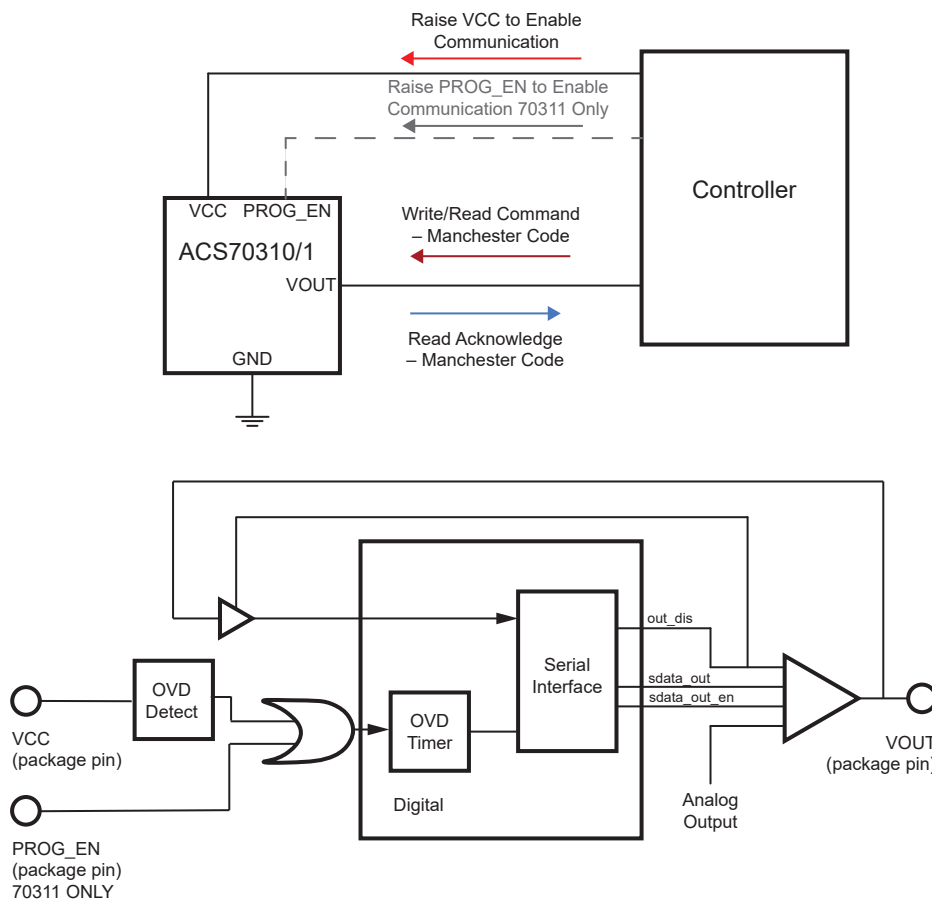
Figure 7: ACS70311 Power On/Off and UVD, $R_L = 10\text{ k}\Omega$

PROGRAMMING GUIDELINES

The serial interface uses a bidirectional communication on VOUT. Both the ACS70310 and ACS70311 will enter programming mode when V_{CC} is increased beyond V_{prgH}(VCC). The ACS70311 will also enter programming enable mode should the voltage on PROG_EN exceeds V_{prgH}(PROG_EN). The PROG_EN pin allows for low-voltage programming on the ACS70311 without

having to raise the supply voltage above 5 V. The device has an internal charge pump to generate the EEPROM pulses.

Recommended programming kits/subkits and software can be found under the Technical Documents on the ACS70310/1 product page on the www.allegromicro.com website.



sdata_out_en	out_dis	VOUT
0	0	Analog output
0	1	High-Z
1	X	sdata_out

Memory-Locking Mechanisms

The ACS70310/1 is equipped with two distinct memory-locking mechanisms:

- **Default Lock:** At power-up, all registers of the ACS70310/1 are locked by default. EEPROM and volatile memory cannot be read or written. To disable Default Lock, a specific 32-bit customer access code must be written to address 0x36 within Access Code Timeout ($t_{ACC} = 10\text{ ms}$) from power-up. After doing so, registers can be accessed. If VCC is power-cycled, the Default Lock will automatically be re-enabled. This ensures that during normal operation, memory content will not be altered due to unwanted glitches on VCC or the VOUT pin.
- **Lock Bit:** After EEPROM has been programmed by the user, the dev_lock bit can be set high and VCC power-cycled to permanently disable the ability to read or write any register. This will prevent the ability to disable Default Lock using the method described above. Note that after the dev_lock bit is set high and the VCC pin has been power-cycled, the dev_lock bit can no longer be cleared and registers can no longer be written to.

Serial Communication

The serial interface allows an external controller to read and write registers, including EEPROM, in the ACS70310/1 using a point-to-point command/acknowledge protocol. The ACS70310/1 does not initiate communication; it only responds to commands from the external controller. Each transaction consists of a command from the controller. If the command is a write, there is no acknowledgment from the ACS70310/1. If the command is a read, the ACS70310/1 responds by transmitting the requested data.

Serial interface timing parameters can be found in the Programming Levels table (Table 1). Note that the external controller must avoid sending a command frame that overlaps a Read Acknowledge frame.

The serial interface uses a Manchester-encoding-based protocol (0 = rising edge, 1 = falling edge), with address and data transmitted MSB first. Four commands are recognized by the ACS70310/1: Write Access Code, Write to Volatile Memory, Write to Non-Volatile Memory (EEPROM) and Read. One frame type, Read Acknowledge, is sent by the ACS70310/1 in response to a Read command.

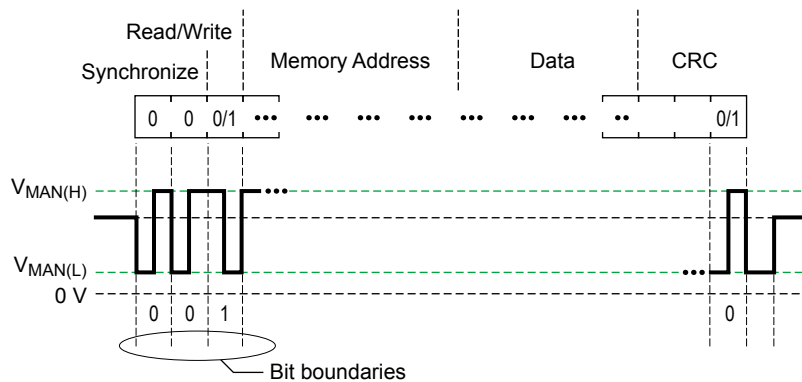


Figure 8: General Format for Serial Interface Commands

The ACS70310/1 device uses a three-wire programming interface, where VCC or PROG_EN is used to control the program enable signal, data is transmitted on VOUT, and all signals are referenced to GND. This three-wire interface makes it possible to communicate with multiple devices with shared VCC and GND lines.

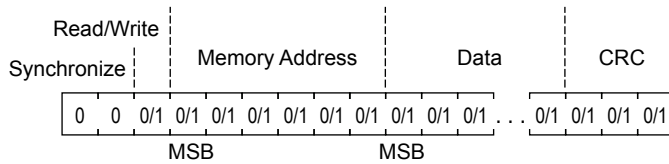
The four transactions (Write Access, Write to EEPROM, Write to Volatile Memory, and Read) are shown in the figures on the following pages. To initialize any communication, VCC or PROG_EN should be increased to a level above V_{prgH} without exceeding the pin maximum voltage. At this time, VOUT is disabled and acts as an input.

After program enable is asserted, the external controller must drive the output low in a time less than Program Time Delay, t_d . This prevents the device interpreting any false transients on

VOUT as data pulses. After the command is completed, VCC or PROG_EN is reduced below V_{prgL} , back to normal operating level. Also, the output is enabled and responds to magnetic input.

When performing a Write to EEPROM transaction, the ACS70310/1 requires a delay of t_w to store the data into the EEPROM. The device will respond with a high-to-low transition on VOUT to indicate the Write to EEPROM sequence is complete.

When sending multiple command frames, it is not necessary to toggle the program enable signal on VCC or PROG_EN. After the first command frame is completed, and VCC or PROG_EN remains at V_{prgH} , the device will ignore any subsequent pulses on the output. When the program enable signal is brought below V_{prgL} , the output will respond to the magnetic input.



Quantity of Bits	Name	Values	Description
2	Synchronization	00	Used to identify the beginning of a serial interface command
1	Read / Write	0	[As required] Write operation
		1	[As required] Read operation
6	Address	0/1	[Read/Write] Register address (volatile memory or EEPROM)
32	Data	0/1	26 data bits and 6 ECC bits. For a read command frame the data consists of 32 bits: [31:28] Don't Care, [27:26] ECC Pass/Fail, and [25:0] Data. Where bit 0 is the LSB. For a write command frame the data consists of 32 bits: [31:26] Don't Care and [25:0] Data. Where bit 0 is the LSB.
3	CRC	0/1	Bits to check the validity of frame.

Figure 9: Command Frame General Format

Table 1: Programming Parameters, $C_{BYPASS} = 0.1 \mu\text{F}$, $V_{CC} = 5 \text{ V}$

Characteristics	Symbol	Note	Min.	Typ.	Max.	Unit
V_{CC} Program Enable Voltage High	$V_{prgH}(V_{CC})$	Program enable signal high level on V_{CC}	7.3	7.6	7.9	V
V_{CC} Program Enable Voltage Low	$V_{prgL}(V_{CC})$	Program enable signal low level on V_{CC}	6.3	6.6	6.9	V
PROG_EN Program Enable Voltage High	$V_{prgH}(\text{PROG_EN})$	Program enable signal high level on PROG_EN, ACS70311 devices only	2.4	–	–	V
PROG_EN Program Enable Voltage Low	$V_{prgL}(\text{PROG_EN})$	Program enable signal low level on PROG_EN, ACS70311 devices only	–	–	1.3	V
PROG_EN Internal Pull-Down Resistor	R_{PROG}		65	100	135	$k\Omega$
Output Enable Delay	t_e	External capacitance (C_{LX}) on VOUT may increase the Output Enable Delay	100	125	150	μs
Program Time Delay	t_d		84	88	93	μs
Program Write Delay	t_w		23	24	25	ms
Manchester High Voltage	$V_{MAN(H)}$	Data pulses on VOUT	4	5	V_{CC}	V
Manchester Low Voltage	$V_{MAN(L)}$	Data pulses on VOUT	0	–	1	V
Bit Rate	t_{BITR}	Communication rate	1	30	100	kbps
Bit Time	t_{BIT}	Data bit pulse width at 30 kbps	37	39	42	μs
Access Code Timeout	t_{ACC}		11	12	13	ms

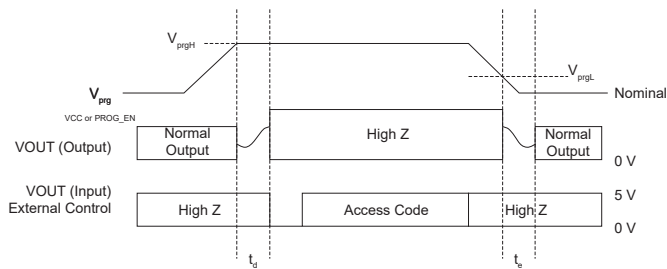


Figure 10: Write Access Code

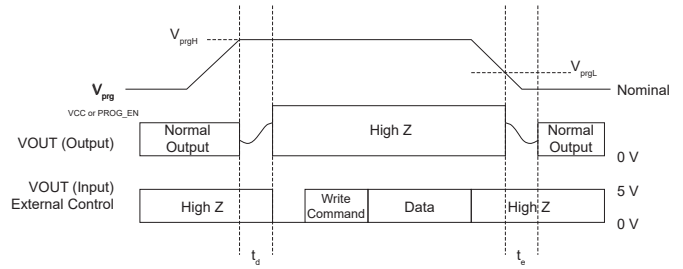


Figure 11: Write Volatile Memory

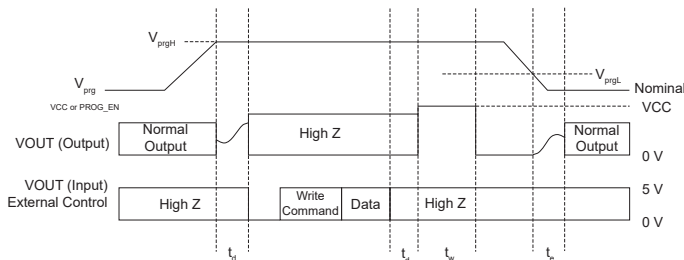


Figure 12: Write Non-Volatile Memory

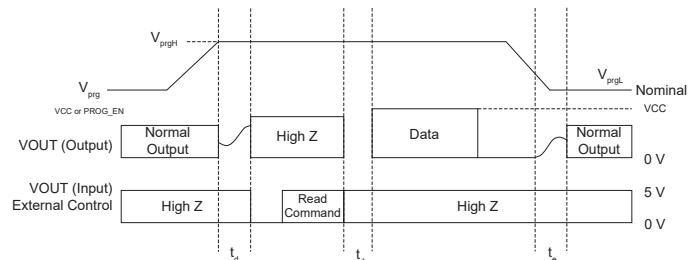
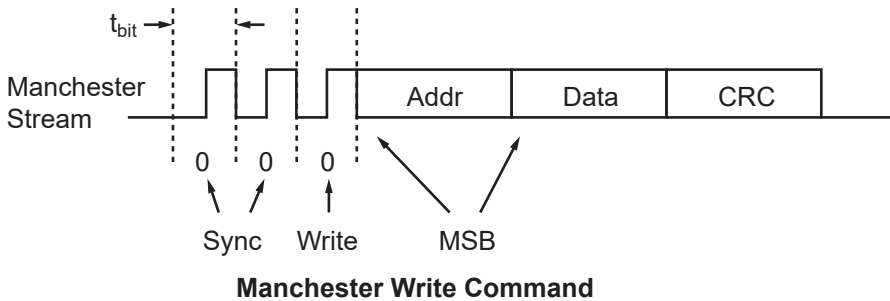


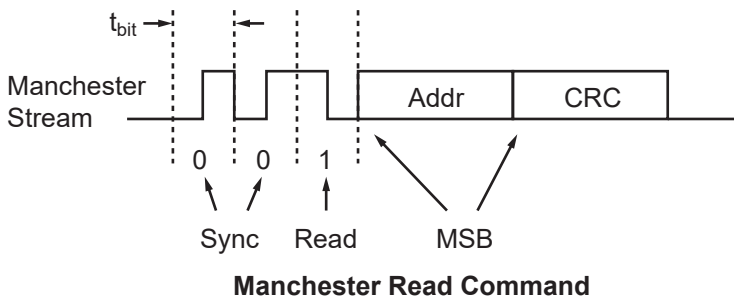
Figure 13: Read

MANCHESTER COMMUNICATION

Command Format

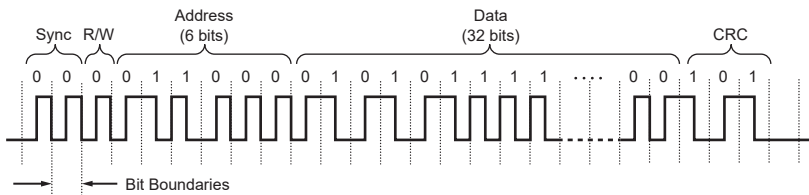


Manchester Write Command

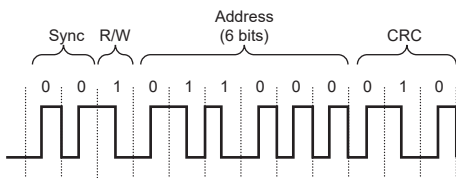


Manchester Read Command

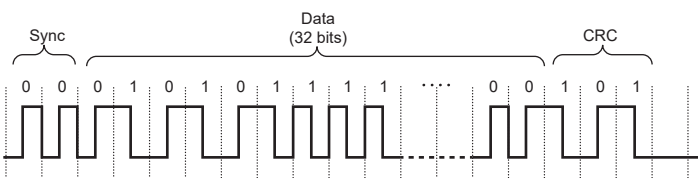
Write Command



Read Command

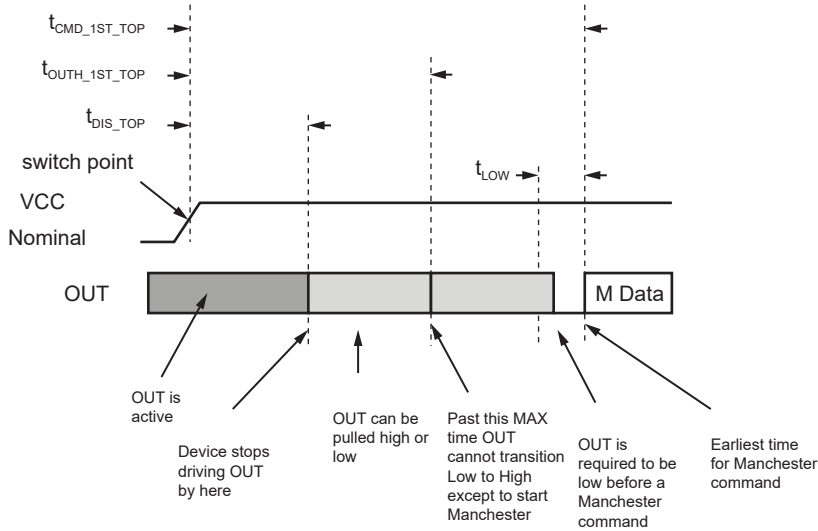


Read Acknowledge



Generic Timing

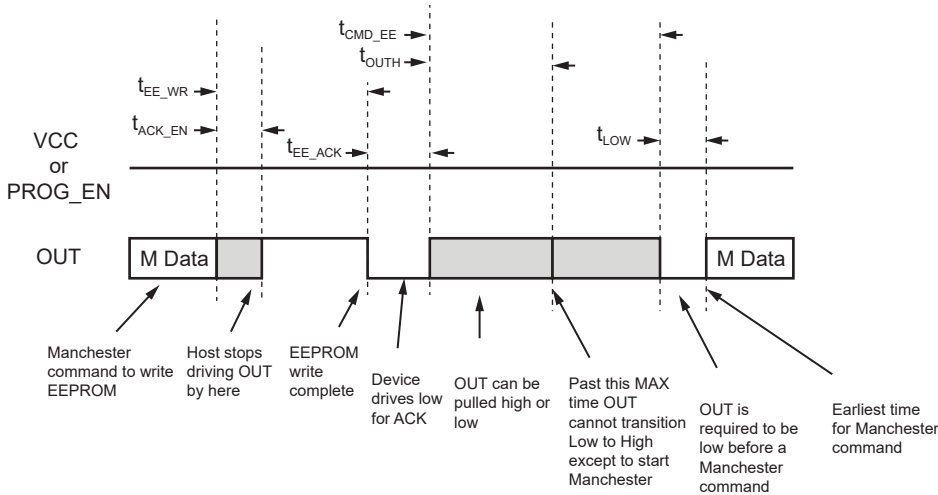
For initial portion of Manchester command



Parameter	Description	Min.	Max.
t_{sclk}	System clock period after trimming	133 ns (7.5 MHz)	167 ns (6 MHz)
t_{bit}	Bit time	1 μ s (1 MBd)	1 ms (1 kBd)
t_{DIS_TOP}	OUT pin is disabled after raising VCC	56 μ s ($512 \times t_{sclk}$)	73.5 μ s ($514 \times t_{sclk}$)
$t_{OUTH_1ST_TOP}$	The OUT pin is either pulled high or low. No low-to-high transitions are allowed after this MAX time except to start the Manchester command. This is for the 1st Manchester command after raising VCC	73.5 μ s	123 μ s
$t_{CMD_1ST_TOP}$	Time required before the 1st Manchester command can be sent after raising VCC	144 μ s	n/a
t_{LOW}	Time required to hold output low before the 1st Manchester edge	1 μ s	n/a

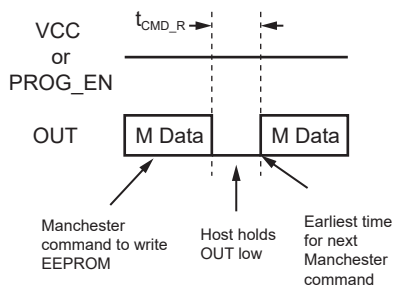
Write to EEPROM

If VCC or PROG_EN is held high at the programming voltage, multiple Manchester commands can be executed.



Parameter	Description	Min.	Max.
t_{sclk}	System clock period after trimming	133 ns (7.5 MHz)	167 ns (6 MHz)
t_{bit}	Bit time	1 μ s (1 MBd)	1 ms (1 kBd)
t_{ACK_EN}	Time for the device to drive OUT after Manchester command. Host must stop driving OUT within this time	$2 \times t_{bit}$	$2 \times t_{bit}$
t_{EE_WR}	During this time the device is writing the EEPROM	–	–
t_{EE_ACK}	Device will drive OUT low during this time	$1 \times t_{bit}$	$1 \times t_{bit}$
t_{OUTH}	The OUT pin is either pulled high or low. No low-to-high transitions are allowed after this MAX time except to start the next Manchester command	0	$1.8 \times t_{bit}$
t_{CMD_EE}	Time before the next Manchester command may be given following a write to EEPROM	$2.2 \times t_{bit}$	–
t_{LOW}	Time required to hold output low before the 1st Manchester edge	1 μ s	–

Write to Register (Not EEPROM)



Parameter	Description	Min.	Max.
t_{sclk}	System clock period after trimming.	133 ns (7.5 MHz)	167 ns (6 MHz)
t_{bit}	Bit time.	1 μ s (1 MBd)	1 ms (1 kBd)
t_{CMD_R}	Time before the next Manchester command may be given following a write to a Register.	2 μ s	n/a

Read (Controller to ACS70310/1)

The fields for the Read command are:

- Sync (2 zero bits)
- Read/Write (1 bit, must be 1 for read)
- CRC (3 bits)

Figure 14 shows the sequence for a Read command.

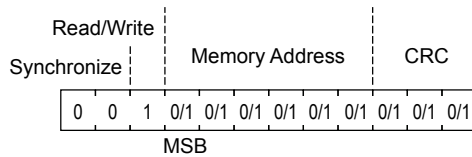


Figure 14: Read Sequence

Read Acknowledge (ACS70310/1 to Controller)

The fields for the data return frame are:

- Sync (2 zero bits)
- Data (32 bits):
 - [31:28] Don't Care
 - [27:26] ECC Pass/Fail
 - [25:0] Data

Figure 15 shows the sequence for a Read Acknowledge. Refer to the Detecting ECC Error section for instructions on how to detect Read/Write Synchronize Memory Address Data (32 bits) and ECC failure.

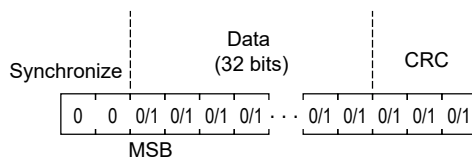


Figure 15: Read Acknowledgement Sequence

Write (Controller to ACS70310/1)

The fields for the Write command are:

- Sync (2 zero bits)
- Read/Write (1 bit, must be 0 for write)
- Address (6 bits)
- Data (32 bits):
 - [31:26] Don't Care
 - [25:0] Data
- CRC (3 bits)

Figure 16 shows the sequence for a Write command. Bits [31:26] are Don't Care because the ACS70310/1 automatically generates 6 ECC bits based on the content of bits [25:0]. These ECC bits will be stored in EEPROM at locations [31:26].

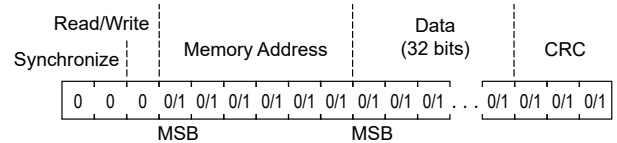


Figure 16: Write Sequence

Write Access Code (Controller to ACS70310/1)

The fields for the Access Code command are:

- Sync (2 zero bits)
- Read/Write (1 bit, must be 0 for write)
- Address (6 bits, address 0x36 for Customer Access)
- Data (32 bits, 0xC4136737 for Customer Access)
- CRC (3 bits)

Figure 17 shows the sequence for an Access Code command.

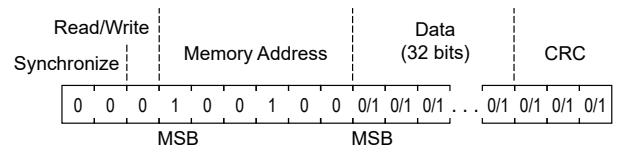


Figure 17: Write Access Code

The controller must open the serial communication with the ACS70310/1 device by sending an Access Code. It must be sent within Access Code Timeout, t_{ACC} , from power-up, or the device will be disabled for read and write access.

Access Codes Information

Name	Serial Interface Format	
	Register Address (Hex)	Data (Hex)
Customer	0x36	0xC4136737

EEPROM Error Checking and Correction (ECC)

Hamming code methodology is implemented for EEPROM checking and correction. The device has ECC enabled after power-up.

The device always returns 32 bits.

The message received from controller is analyzed by the device EEPROM driver and ECC bits are added. The first 6 received bits from device to controller are dedicated to ECC.

The Manchester serial interface uses a 3-bit cyclic redundancy check (CRC) for data-bit error checking (synchronized bits are ignored during the check). The CRC algorithm is based on the polynomial $g(x) = x^3 + x + 1$ and is initialized to 111 when first powered up. Write commands written to the slave controller are checked against the embedded CRC field.

Detecting ECC Error

If an uncorrectable error has occurred, bits 27:26 are set to 10, the VOUT pin will go to a high-impedance state, and the device will not respond to the applied magnetic field.

EEPROM ECC Errors

Bits	Name	Description
31:28	–	No meaning
27:26	ECC	00 = No Error 01 = Error detected and message corrected 10 = Uncorrectable error 11 = No meaning
25:0	D[25:0]	EEPROM data

Table 2: Customer Memory Map

Address	Register Name	Parameter Name	Description	r/w	Bits	Location
0x4	scratch_c	customer_scratch	Unused register that can be written to, as needed, for customer data storage	RW	26	25:0
0x5	cust0_c	sensf	Sensitivity, fine adjustment	RW	9	8:0
		qvof	Quiescent Output Voltage (QVO), fine adjustment	RW	9	17:9
		sensc	Coarse Sensitivity	RW [1]	2	19:18
0x6	cust1_c	rat_dis	Ratiometry disable; Sens and $V_{OUT(Q)}$ are not guaranteed if ratiometry is disabled	RW	1	2
		uni_en	Enables unidirectional output	RW	1	4
		clamp_en	Clamp enable	RW	1	5
		pol	Reverses output polarity	RW	1	6
		dev_lock	Bit to lock the serial interface from receiving data	RW	1	7
0x29	status_c	customer_access	Customer write access enabled	RO	1	0
0x36	unlock_c	customer_unlock	Write 0xC4136737 to address 0x36 within t_{ACC} to unlock the device	WO	32	31:0

[1] Overtemperature performance is no longer valid if this register is changed from factory default.

PACKAGE OUTLINE DRAWINGS

For Reference Only - Not for Tooling Use

(Reference DWG-0000426, Rev. 1)
Dimensions in millimeters - NOT TO SCALE
Dimensions exclusive of mold flash, gate burs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

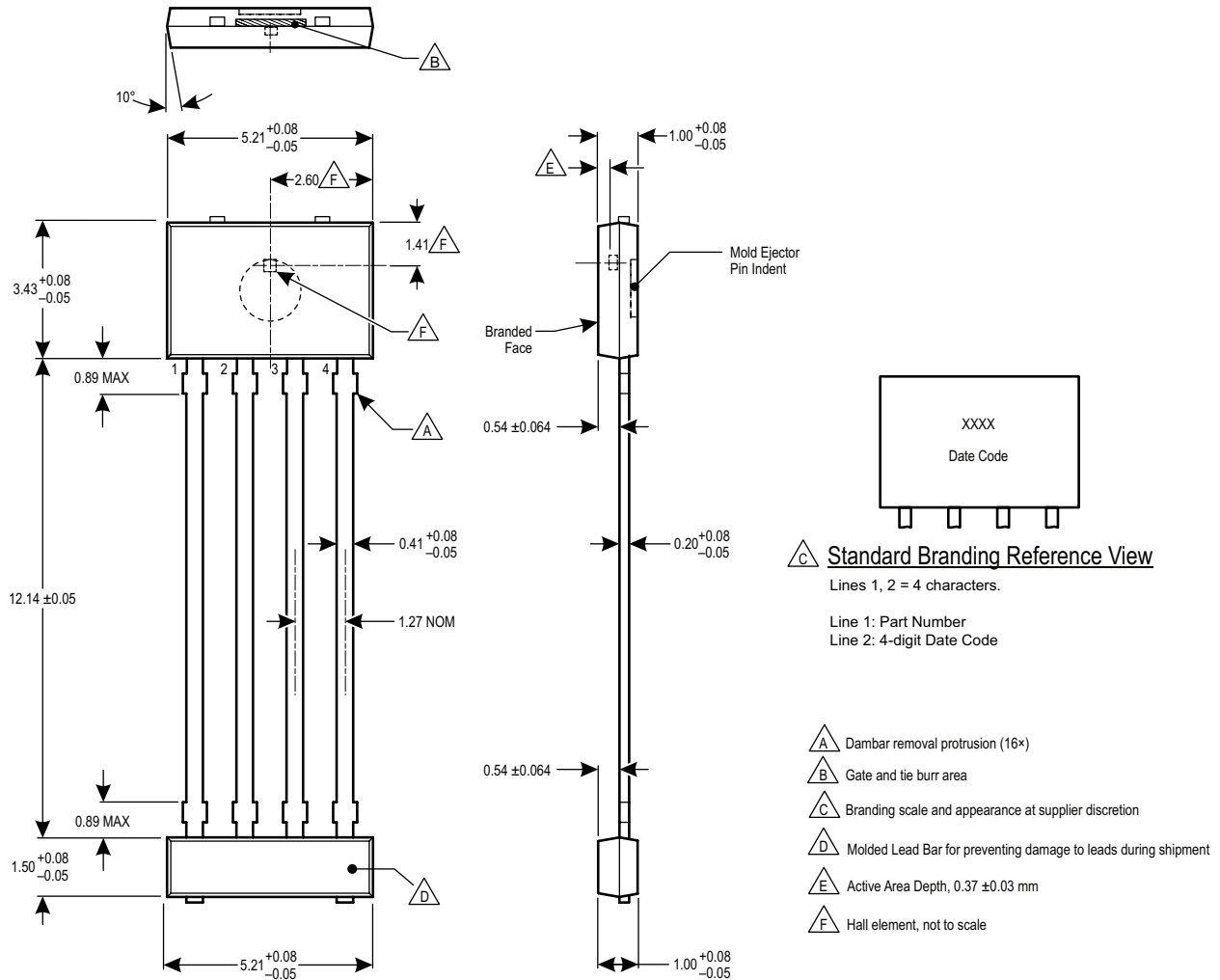


Figure 18: Package KT, 4-Pin SIP, TN Leadform

ACS70310 and ACS70311

Very High Precision, Programmable Linear Hall-Effect Sensor IC with Reverse Battery Protection and High-Bandwidth (240 kHz) Analog Output for Core-Based Current Sensing

For Reference Only - Not for Tooling Use

(Reference DWG-0000395)

Dimensions in millimeters - NOT TO SCALE

Dimensions exclusive of mold flash, gate burs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

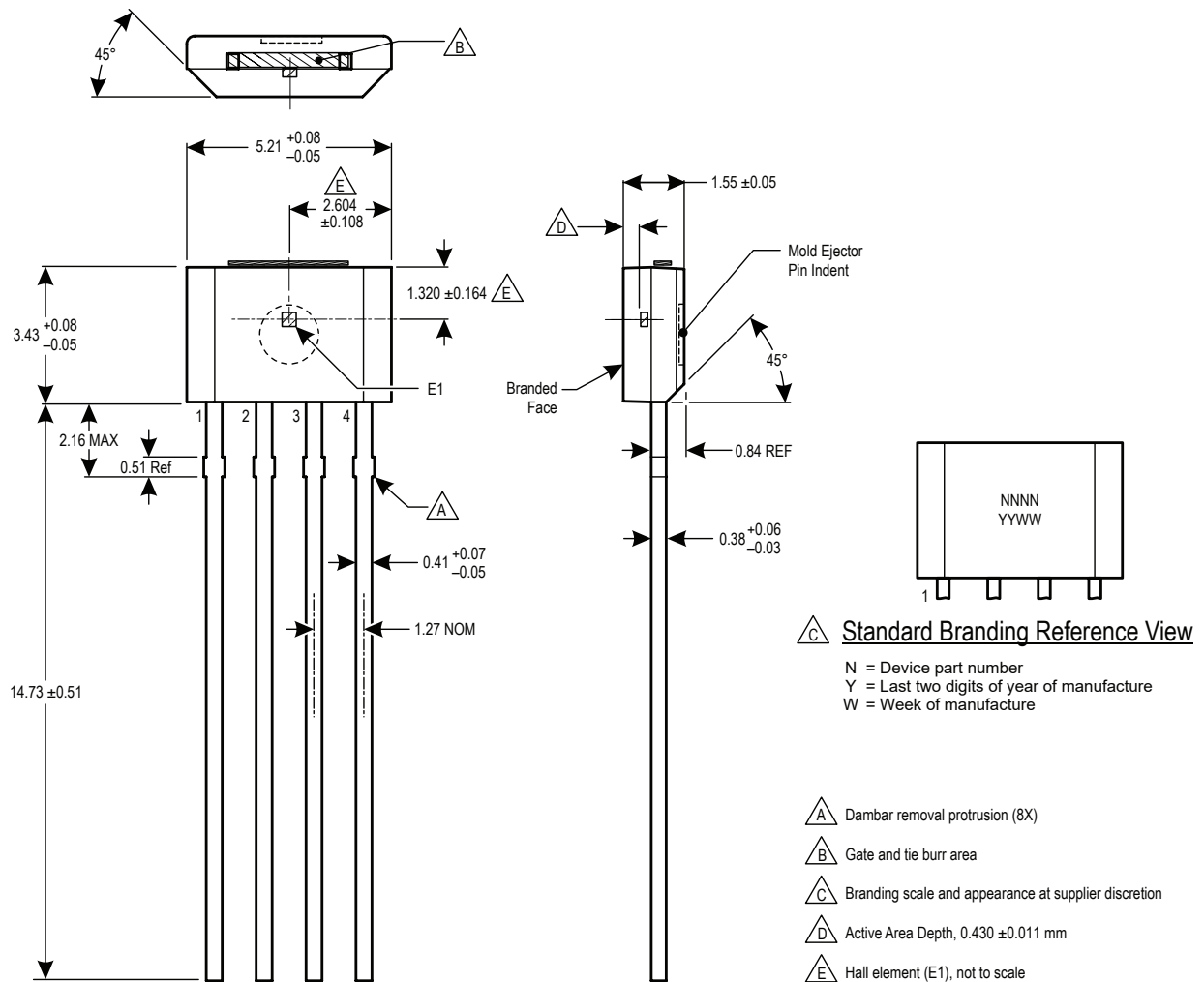
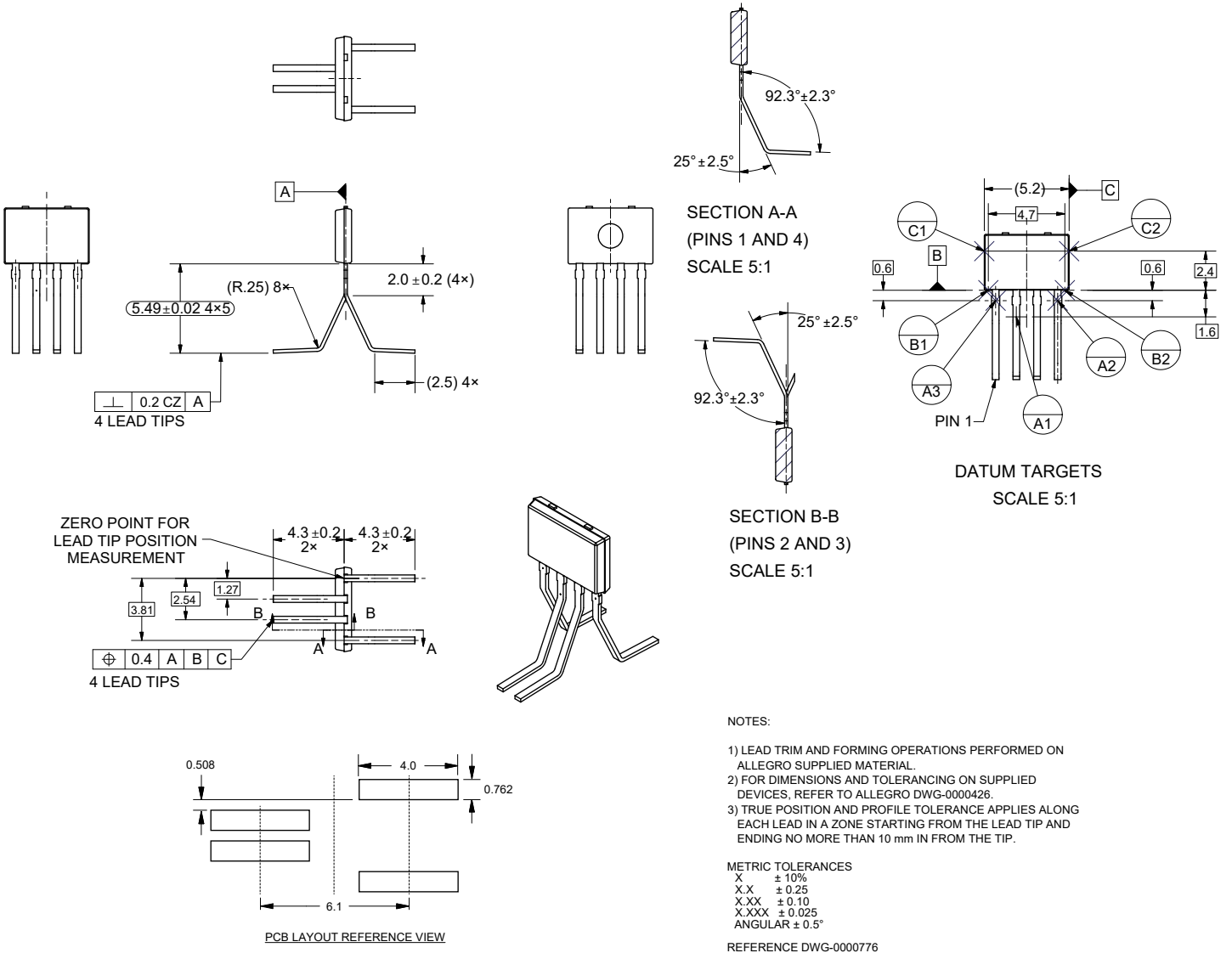


Figure 19: Package OK, 4-Pin SIP, TN Leadform



**Figure 20: Package KT, 4-Pin SIP, TH Leadform
(see Figure 18 for Hall plate location and branding)**

ACS70310 and ACS70311

Very High Precision, Programmable Linear Hall-Effect Sensor IC with Reverse Battery Protection and High-Bandwidth (240 kHz) Analog Output for Core-Based Current Sensing

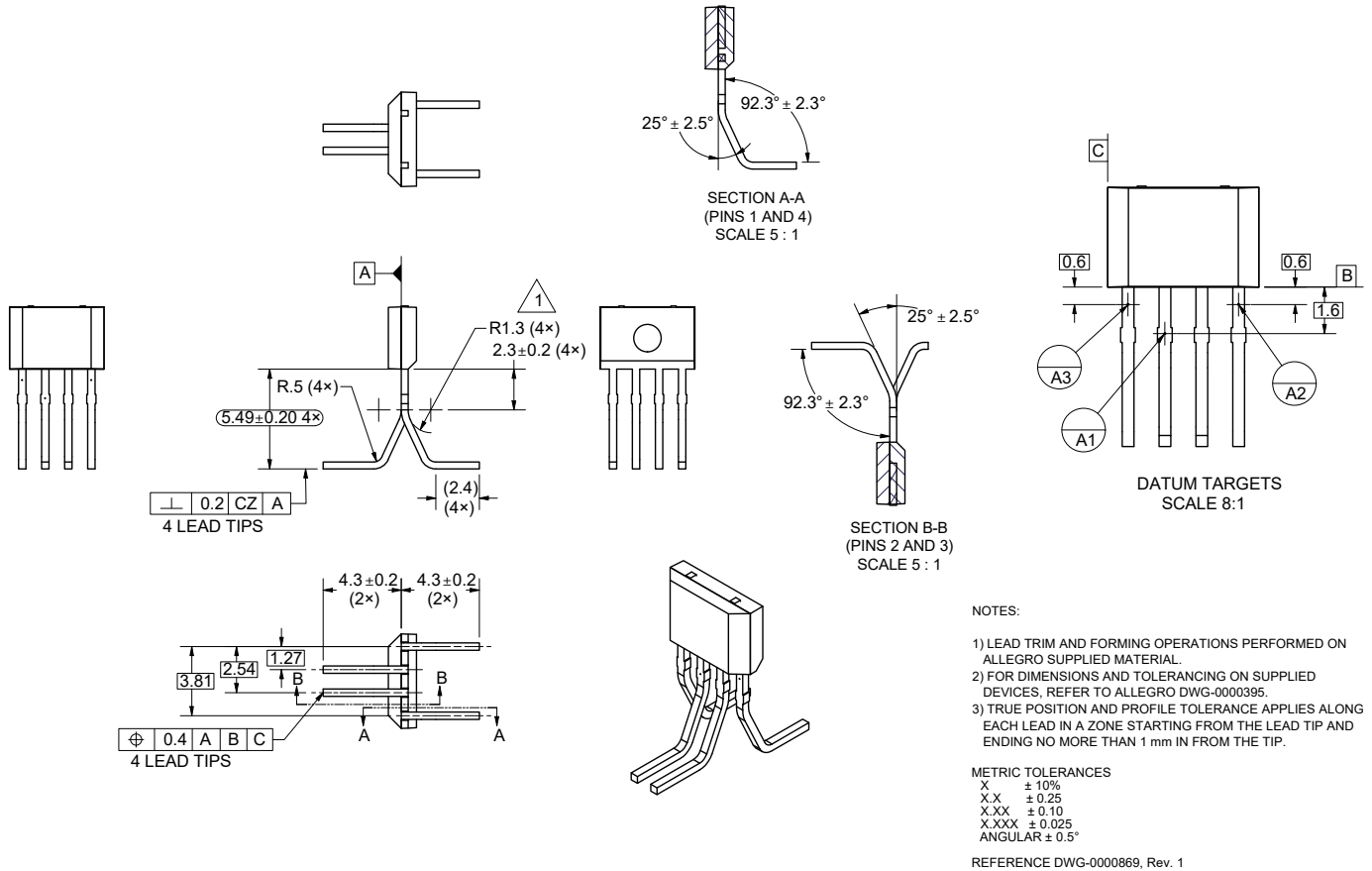


Figure 21: Package OK, 4-Pin SIP, TX Leadform

ACS70310 and ACS70311

Very High Precision, Programmable Linear Hall-Effect Sensor IC with Reverse Battery Protection and High-Bandwidth (240 kHz) Analog Output for Core-Based Current Sensing

COMPLETE SELECTION GUIDE

Part Number [1]	Factory-Programmed Sensitivity (mV/G)	Programmable Sens Range (mV/G)	Low-Voltage Programming/ UVD Capable	Package	Packing [2]	T _A (°C)
ACS70310LKTATN-001B5-C	1	0.5 to 1.2	No	4-pin SIP (suffix KT) TN leadform	4000 pieces per 13-inch reel	-40 to 150
ACS70310LKTATN-2P5B5-C	2.5	1.2 to 2.5				
ACS70310LKTATN-005B5-C	5	2.5 to 5.5				
ACS70310LKTATN-010B5-C	10	5.5 to 11.5				
ACS70311LKTATN-001B5-C	1	0.5 to 1.2	Yes			
ACS70311LKTATN-2P5B5-C	2.5	1.2 to 2.5				
ACS70311LKTATN-005B5-C	5	2.5 to 5.5				
ACS70311LKTATN-010B5-C	10	5.5 to 11.5				
ACS70310LKTATH-001B5-C	1	0.5 to 1.2	No	4-pin SIP (suffix KT) TH leadform		
ACS70310LKTATH-2P5B5-C	2.5	1.2 to 2.5				
ACS70310LKTATH-005B5-C	5	2.5 to 5.5				
ACS70310LKTATH-010B5-C	10	5.5 to 11.5				
ACS70311LKTATH-001B5-C	1	0.5 to 1.2	Yes			
ACS70311LKTATH-2P5B5-C	2.5	1.2 to 2.5				
ACS70311LKTATH-005B5-C	5	2.5 to 5.5				
ACS70311LKTATH-010B5-C	10	5.5 to 11.5				
ACS70311LOKATN-001B5-C	1	0.5 to 1.2	Yes	4-pin SIP (suffix OK) TN leadform	4000 pieces per 13-inch reel	
ACS70311LOKATN-2P5B5-C	2.5	1.2 to 2.5				
ACS70311LOKATN-005B5-C	5	2.5 to 5.5				
ACS70311LOKATN-010B5-C	10	5.5 to 11.5				
ACS70311LOKATX-001B5-C	1	0.5 to 1.2	Yes	4-pin SIP (suffix OK) TX leadform	450 pieces per 13-inch reel	
ACS70311LOKATX-2P5B5-C	2.5	1.2 to 2.5				
ACS70311LOKATX-005B5-C	5	2.5 to 5.5				
ACS70311LOKATX-010B5-C	10	5.5 to 11.5				

[1] Characteristics are guaranteed within the sense programmable range of the corresponding part number.

Revision History

Number	Date	Description
–	February 27, 2019	Initial release
1	April 10, 2019	Removed Internal Bandwidth min/max values (page 5)
2	July 11, 2019	Added ESD Ratings table (page 3)
3	July 17, 2019	Updated ESD Ratings table (page 3)
4	September 5, 2019	Updated customer memory map (page 23)
5	October 30, 2019	Updated ESD Ratings table (page 3)
6	September 21, 2020	Added ACS70311 part variant, Prog_EN operation (all pages), and TH leadform option (All pages)
7	November 9, 2020	Updated Functional Block Diagram (page 1); updated Programming Guidelines (page 13); updated EEPROM Error Checking and Correction (ECC) section (page 22); minor editorial updates
8	February 5, 2021	Updated KT package drawing
9	September 10, 2021	Added OK package variant; added Chopping Frequency characteristic (page 6); updated QVO Lifetime Drift (page 8); added Lifetime footnote (page 8); updated “ $R_L = 0\text{ k}\Omega$ ” to “ $R_L = 10\text{ k}\Omega$ ” (pages 6 and 10); added OK step response plot (page 10); updated Sensitivity Drift Through Temperature Range and Ratiometry Error sections (page 12); updated Lock Bit section (page 16); updated Customer Memory Map 0x4 description (page 24)
10	September 28, 2021	Updated Response Time, Rise Time, and Bandwidth (page 6), Typical Frequency Response plots (page 9), and Step Response plot (page 10)
11	March 3, 2022	Added Complete Selection Guide (page 28)
12	June 10, 2022	Updated programming parameters table (page 18)
13	January 9, 2023	Added OK-TX package option (pages 1-3, 28-29)
14	May 17, 2023	Updated Noise values (page 6)

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