

GaN FET Isolated Gate Driver Chipset with Power-Thru Integrated Isolated Bias Supply

FEATURES AND BENEFITS

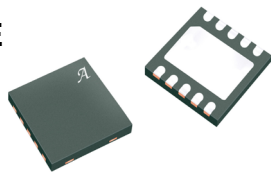
- Chipset transmits both PWM signal and bias power through a single external isolation transformer
 - No high-side bootstrap
 - No external secondary-side bias supply
- 50 ns propagation delay (with recommended transformers)
- Separate drive output pins: pull-up ($2.8\ \Omega$) and pull-down ($1.0\ \Omega$)
- Supply voltage $10.5\text{ V} < V_{\text{DRV}} < 13.2\text{ V}$
- Undervoltage lockout on primary V_{DRV} and secondary V_{SEC}
- Enable pin with fast response
- Continuous ON capability—no need to recycle IN or recharge bootstrap capacitor
- CMTI $> 100\text{ V/ns}$ dV/dt immunity (with recommended transformers)
- System creepage distance > 4 or 8 mm (with recommended transformers)

APPLICATIONS

- **AC-DC and DC-DC Converters:** Totem-pole PFC, LLC half-/full-bridge, SR drive, multi-level converters, phase-shifted full-bridge, high-side cutoff switches
- **Personal Mobility:** Chargers, on-board chargers (OBCs)
- **Industrial:** Data center, transportation, robotics, audio
- **Clean Energy:** Microinverters, string-inverters, solar

PACKAGE

Not to scale



3 mm × 3 mm
DFN-10 package
(suffix EJ)

DESCRIPTION

The AHV85000 + AHV85040 is a cost-optimized isolated gate-drive chipset for gallium-nitride (GaN) field-effect-transistor (FET) devices. When combined with one of the recommended external transformers, it provides a self-powered isolated gate drive solution, ideal for GaN FETs in multiple applications and topologies.

The chipset transmits both the pulse-width-modulated (PWM) signal and the gate bias power through the external transformer, eliminating the need for any external gate drive auxiliary bias supply or high-side bootstrap. This greatly simplifies the system design and reduces electromagnetic interference (EMI) through reduced total common-mode (CM) capacitance. It also allows the driving of a floating switch at any location in a switching power topology.

The chipset has low propagation delay and high-peak-current source/sink capability to efficiently drive GaN FETs in high-frequency designs. High common-mode transient immunity (CMTI) combined with isolated outputs for both bias power and drive make it ideal in applications requiring isolation, level-shifting, or ground separation for noise immunity.

The chipset is available in a pair of 3 mm × 3 mm, 10-pin, dual-flat no-leads (DFN-10) surface-mount packages. Several protection features are integrated, including undervoltage lockout on primary and secondary bias rails, internal pull-down on IN pin and OUTPD pin, and fast-response enable input/fault-output pin.

TYPICAL APPLICATION

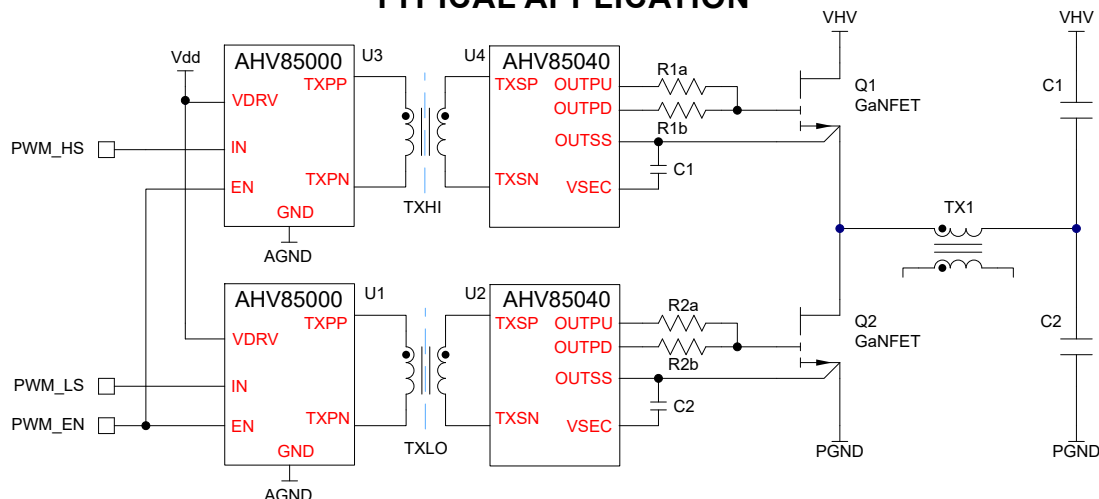


Figure 1: Typical AHV85000 + AHV85040 Chipset Half-Bridge Application—Eliminates High-Side Bootstrap

SELECTION GUIDE

| Part Number | IC Type | Switch | # of Channels | Output | Isolation | Package | Tape & Reel Detail |
|---------------|----------------|------------|---------------|----------|-----------------------------------|---|--------------------|
| AHV85000GEJSR | Primary side | E-mode GaN | 1 | Unipolar | Isolated via external transformer | 3 mm × 3 mm DFN, 10-pin low-profile surface mount | 6000 per reel |
| AHV85000GEJTD | | | | | | | 200 per reel |
| AHV85040GEJSR | Secondary side | | | | | | 6000 per reel |
| AHV85040GEJTD | | | | | | | 200 per reel |

ABSOLUTE MAXIMUM RATINGS (AHV85000, AHV85040) [1]

| Characteristic | Symbol | Notes | Rating | Unit |
|----------------------------|-------------|----------------------------------|-------------------------|------|
| Drive Supply Voltage | V_{DRV} | VDRV, with respect to GND | $V_{GND} - 0.5$ to 15 | V |
| Input Data | V_{IN} | IN, with respect to GND | $V_{GND} - 0.5$ to 15 | V |
| Enable | V_{EN} | EN, with respect to GND | $V_{GND} - 0.5$ to 15 | V |
| Select | V_{SEL} | SEL, with respect to GND | $V_{GND} - 0.5$ to 15 | V |
| Output Drive Pull-Up | V_{OUTPU} | OUTPU, with respect to OUTSS | $V_{OUTSS} - 0.5$ to 15 | V |
| Output Drive Pull-Down | V_{OUTPD} | OUTPU, with respect to OUTSS | $V_{OUTSS} - 0.5$ to 15 | V |
| Isolated Bias Supply | V_{SEC} | VSEC, with respect to OUTSS | $V_{OUTSS} - 0.5$ to 15 | V |
| Transformer Pins Primary | TXPP/TXPN | TXPP/TXPN, with respect to GND | $V_{GND} - 0.5$ to 15 | V |
| Transformer Pins Secondary | TXSP/TXSN | TXSP/TXSN, with respect to OUTSS | $V_{OUTSS} - 0.5$ to 15 | V |
| Junction Temperature | T_J | | -40 to 150 | °C |
| Storage Temperature | T_{STG} | | -40 to 150 | °C |

[1] Stresses beyond those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD RATINGS (AHV85000, AHV85040)

| Characteristic | Symbol | Test Conditions | Value | Unit |
|----------------------|-----------|-----------------|-------|------|
| Human Body Model | V_{HBM} | | ±2 | kV |
| Charged Device Model | V_{CDM} | | ±500 | V |

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

| Characteristic | Symbol | Test Conditions [1] | Value | Unit |
|--|-----------------|---|-------|------|
| Junction-to-Ambient Thermal Resistance | $R_{\theta JA}$ | Mounted on application PCB with 0.2-inch Cu heatsinking | 100 | °C/W |
| Junction-to-Case Thermal Resistance | $R_{\theta JC}$ | | 2 | °C/W |

[1] Additional thermal information available on the Allegro website.

RECOMMENDED OPERATING CONDITIONS: Valid at $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$, $10.5\text{ V} < V_{\text{DRV}} < 13.2\text{ V}$, $C_{\text{SEC}} = 47\text{ nF}$, $C_{\text{OUT}} = 1\text{ nF}$, unless otherwise stated ^[1]

| Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|-------------------------------------|--------------------|-----------------|------------------|------|------------------|--------------------|
| SUPPLY VOLTAGE PINS—AHV85000 | | | | | | |
| Drive Supply Voltage | V_{DRV} | | 10.5 | – | 13.2 | V |
| INPUT PINS—AHV85000 | | | | | | |
| Input Data | V_{IN} | | V_{GND} | – | V_{DRV} | V |
| Enable Active High | V_{EN} | | V_{GND} | – | V_{DRV} | V |
| Select | V_{SEL} | | V_{GND} | – | V_{DRV} | V |
| OUTPUT PINS—AHV85040 | | | | | | |
| Output Pull-Up | V_{OUTPU} | | 0 | – | 13.2 | V |
| Output Pull-Down | V_{OUTPD} | | 0 | – | 13.2 | V |
| Isolated Supply Referenced to OUTSS | V_{SEC} | | 0 | – | 13.2 | V |
| Junction Temperature | T_J | | –40 | – | 125 | $^{\circ}\text{C}$ |

^[1] Not cold-tested in production (-40°C); guaranteed by design and bench characterization.

VSEC PIN CAPACITOR

| Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|-------------------------|------------------|---|-------------------|------|--------------------|------|
| VSEC Pin Capacitor CSEC | C_{SEC} | External capacitance connected between VSEC and OUTSS pins; external $C_{\text{OUT}} = 1\text{ nF}$ | 10 ^[1] | 47 | 100 ^[2] | nF |

^[1] If the value of C_{SEC} is less than the recommended typical value, higher voltage ripple on C_{SEC} can result. The recommended C_{SEC} value is 10 to 20 times larger than the effective load capacitance, C_{OUT} .

^[2] Larger C_{SEC} values equate to longer startup times.

MSL RATING

| Device | MSL Rating | Maximum Floor Life at Standard Ambient (30°C/60% Relative Humidity) | Maximum Peak Reflow Temperature | Pre-Reflow Bake Requirement |
|----------------------|------------|---|---------------------------------|-----------------------------|
| AHV85000 AHV85040 | MSL-3 | 168 hours | 260°C | Per JEDEC J-STD-033C |

Per JEDEC J-STD-033C, the AHV85000 and AHV85040 devices are rated MSL-3. This MSL-3 rating means that, once the sealed production packaging is opened, the devices must be reflowed within a “floor-life” of 168 hours (1 week) if they are stored in standard ambient conditions (30°C and 60% relative humidity).

The peak reflow temperature should not exceed the maximum specified in MSL Rating table.

If the devices are exposed to the standard ambient for more than 168 hours, they must be baked before reflow to remove any excess moisture in the package and prevent damage during reflow soldering. The required bake times and temperatures are detailed in IPC/JEDEC standard J-STD-033C.

If the devices are exposed to higher temperature and/or relative humidity (RH) compared to the standard ambient of 30°C/60% RH, the floor-life becomes shortened due to the increased rate of moisture absorption. If the actual ambient conditions exceed the standard ambient, it is recommended that parts should always be baked per IEC/JEDEC J-STD-033C before reflow as a precaution to avoid potential device damage during reflow soldering.

FUNCTIONAL BLOCK DIAGRAM

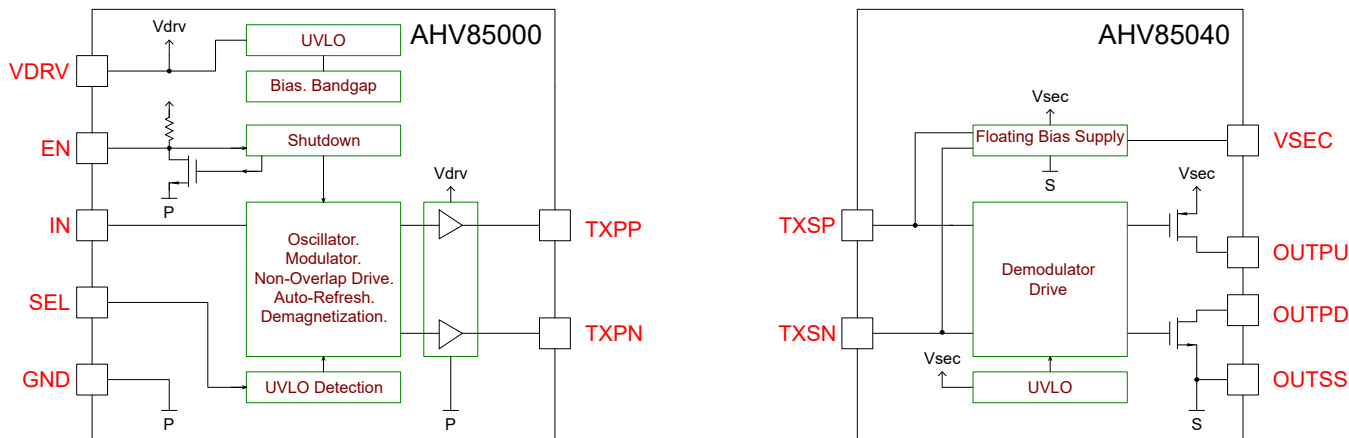
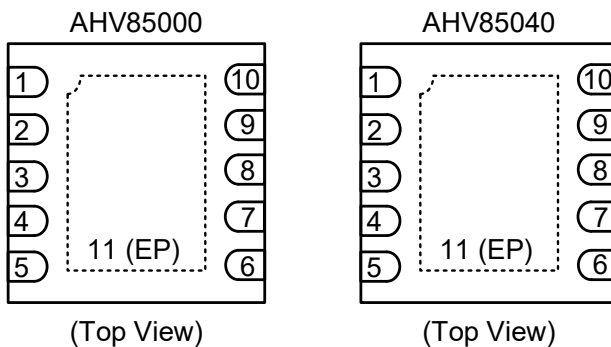


Figure 2: AHV85000 + AHV85040 Block Diagrams

PINOUT DIAGRAM AND TERMINAL LIST TABLE



(Top View)

(Top View)

Package EJ Pinout (Top View)

Terminal List Table

| AHV85000 | | | AHV85040 | | |
|----------|------|---|----------|--------------------------------|--|
| Number | Name | Function | Name | Function | |
| 1 | IN | PWM input | NC | No connect | |
| 2 | SEL | UVLO select option | OUTSS | Secondary-side ground | |
| 3 | GND | Primary-side ground | TXSP | Transformer secondary positive | |
| 4 | GND | Primary-side ground | TXSN | Transformer secondary negative | |
| 5 | GND | Primary-side ground | OUTSS | Secondary-side ground | |
| 6 | TXPN | Transformer primary negative | VSEC | Secondary supply decoupling | |
| 7 | TXPP | Transformer primary positive | OUTSS | Secondary-side ground | |
| 8 | VDRV | Primary supply rail | OUTPD | Output drive pull-down | |
| 9 | GND | Primary-side ground | OUTPU | Output drive pull-up | |
| 10 | EN | Bidirectional primary-referenced enable | OUTSS | Secondary-side ground | |
| 11 | EP | Exposed pad (GND) | EP | Exposed Pad (GND) | |

ELECTRICAL CHARACTERISTICS: Valid at $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$, $10.5\text{ V} < V_{\text{DRV}} < 13.2\text{ V}$, $C_{\text{SEC}} = 47\text{ nF}$, $C_{\text{OUT}} = 1\text{ nF}$, unless otherwise stated ^[1]

| Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|---|-------------------------|---|------|------|------|------------|
| SUPPLY CURRENTS—AHV85000 | | | | | | |
| VDRV Disable Current | $I_{\text{DRV_DIS}}$ | $V_{\text{IN}} = 0$, $V_{\text{DRV}} = 12\text{ V}$, $\text{EN} = 0$ | – | 0.4 | 0.75 | mA |
| VDRV Quiescent Current | $I_{\text{DRV_Q}}$ | $V_{\text{IN}} = 0$, $V_{\text{DRV}} = 12\text{ V}$, $\text{IN} = 0$, $\text{EN} = 1$ | – | 1.25 | 2.4 | mA |
| VDRV Switching Current | $I_{\text{DRV_SW}}$ | $f_S = 100\text{ kHz}$, $V_{\text{DRV}} = 12\text{ V}$ | – | 3 | 5.5 | mA |
| INPUT PINS—AHV85000 | | | | | | |
| Input Data – Logic Low | $V_{\text{IN(L)}}$ | | – | – | 0.8 | V |
| Input Data – Logic High | $V_{\text{IN(H)}}$ | | 2.0 | – | – | V |
| Input Data Hysteresis | $V_{\text{IN(HYS)}}$ | | – | 400 | – | mV |
| Enable Active High – Logic Low | $V_{\text{EN(L)}}$ | | – | – | 0.8 | V |
| Enable Active High – Logic High | $V_{\text{EN(H)}}$ | | 2.0 | – | – | V |
| Enable Active High – Hysteresis | $V_{\text{EN(HYS)}}$ | | – | 400 | – | mV |
| Internal On-Chip Pull-Down Resistance On IN Pin | R_{IN} | $T_A = 25^{\circ}\text{C}$ | – | 300 | – | k Ω |
| PRIMARY UNDERVOLTAGE LOCKOUT—AHV85000 | | | | | | |
| VDRV UV Threshold, Rising ^[2] | $V_{\text{DRV_UVH}}$ | SEL pin connected to VDRV | 9.5 | 10.0 | 10.5 | V |
| VDRV UV Threshold, Falling | $V_{\text{DRV_UVL}}$ | SEL pin connected to VDRV | 8.8 | 9.3 | 9.8 | V |
| VDRV UV Hysteresis | $V_{\text{DRV_UVHYS}}$ | SEL pin connected to VDRV | 0.5 | 0.7 | 0.9 | V |
| OUTPUT PINS—AHV85040 | | | | | | |
| OUTPU Pull-Up Resistance | R_{PU} | | 1.5 | 2.8 | 3.5 | Ω |
| OUTPD Pull-Down Resistance | R_{PD} | | 0.7 | 1.0 | 1.7 | Ω |
| High Level Source Current ^[3] | I_{SOURCE} | $V_{\text{SEC}} = 10\text{ V}$, $R_{\text{ext_pu}} = 0\text{ }\Omega$, $C_{\text{OUT}} = 10\text{ nF}$ | – | 2 | – | A |
| Low Level Sink Current ^[3] | I_{SINK} | $V_{\text{SEC}} = 10\text{ V}$, $R_{\text{ext_pd}} = 0\text{ }\Omega$, $C_{\text{OUT}} = 10\text{ nF}$ | – | 4 | – | A |
| SECONDARY UNDERVOLTAGE LOCKOUT—AHV85040 | | | | | | |
| VSEC UV Threshold, Rising | $V_{\text{SEC_UVH}}$ | | 3.7 | 4.4 | 5.1 | V |
| VDRV UV Threshold, Falling | $V_{\text{SEC_UVL}}$ | $T_A = 25^{\circ}\text{C}$ | 3.5 | 4.1 | 4.7 | V |
| VSEC UV Hysteresis | $V_{\text{SEC_UVHYS}}$ | $T_A = 25^{\circ}\text{C}$ | 0.1 | 0.3 | 0.6 | V |

^[1] Not cold tested in production (-40°C); guaranteed by design and bench characterization.

^[2] When V_{DRV} is below the UVLO threshold, the driver output is actively held low.

^[3] Not tested in production; guaranteed by design and bench characterization

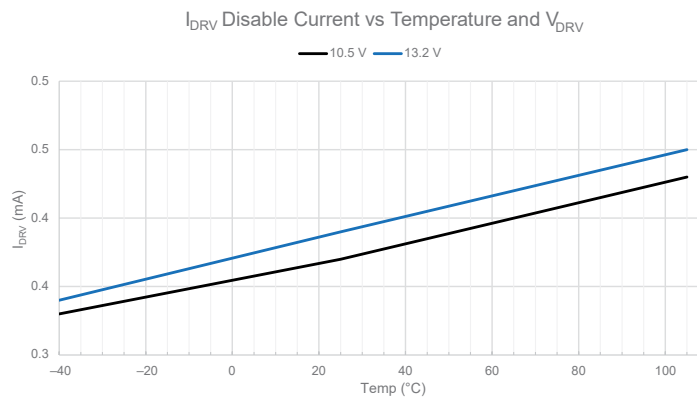
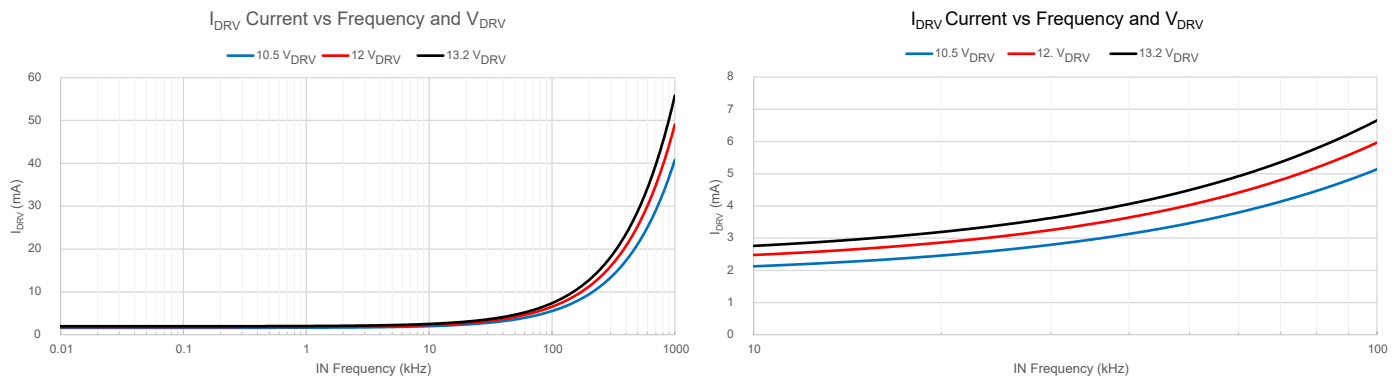
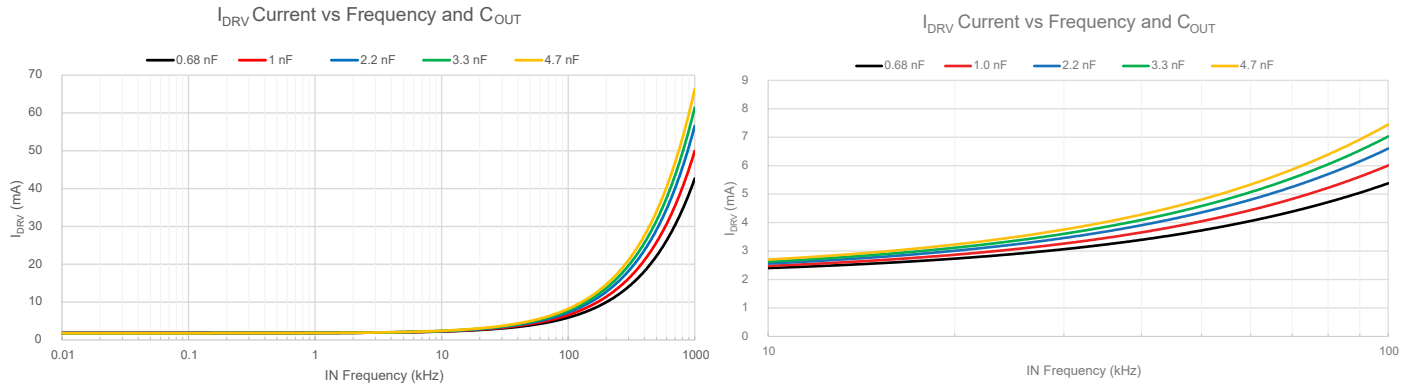
SWITCHING CHARACTERISTICS: Valid at $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$, $10.5\text{ V} < V_{\text{DRV}} < 13.2\text{ V}$, $C_{\text{SEC}} = 47\text{ nF}$, $C_{\text{OUT}} = 1\text{ nF}$, unless otherwise stated ^[1]

| Characteristics | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
|--|----------------------|--|------|------|------|---------------|
| PROPAGATION TIMES—AHV85000 + AHV85040 PLUS EXTERNAL TRANSFORMER ^[2] | | | | | | |
| Propagation Delay, High To Low | t_{PHL} | $R_{\text{ext_pu}} = R_{\text{ext_pd}} = 2\ \Omega$ | – | 50 | 100 | ns |
| Propagation Delay, Low To High | t_{PLH} | $R_{\text{ext_pu}} = R_{\text{ext_pd}} = 2\ \Omega$ | – | 50 | 100 | ns |
| RISE AND FALL TIMES—AHV85000 + AHV85040 PLUS EXTERNAL TRANSFORMER ^[2] | | | | | | |
| Rise Time | t_r | $R_{\text{ext_pu}} = 0\ \Omega$, 20–80% | – | 9 | 20 | ns |
| Fall Time | t_f | $R_{\text{ext_pd}} = 0\ \Omega$, 20–80% | – | 7 | 20 | ns |
| Shortest ON Time Allowable | $t_{\text{pw(on)}}$ | The ON time should never be less than specified minimum | 100 | – | – | ns |
| Shortest OFF Time Allowable | $t_{\text{pw(off)}}$ | The OFF time should never be less than specified minimum | 100 | – | – | ns |
| STARTUP TIME—AHV85000 + AHV85040 PLUS EXTERNAL TRANSFORMER ^[2] | | | | | | |
| Wait Time Before First IN Edge is Delivered After V_{DRV} is Within Specification | t_{START} | | – | – | 250 | μs |

^[1] Not cold tested in production (-40°C); guaranteed by design and bench characterization.

^[2] When tested with an SM91243L transformer. See the External Transformer Details section.

Typical System Characteristics Curves



FUNCTIONAL DESCRIPTION

The AHV85000 + AHV85040 is a self-powered isolated gate driver chipset that leverages Allegro's patented Power-Thru technology. The technology allows the transfer of both PWM signal and gate power across a single transformer-based isolation barrier. This eliminates the need to provide an isolated bias supply to power the isolated side of the driver, greatly simplifying the system design. Only an external transformer and decoupling capacitor on the isolated side are required.

The chipset is optimized for driving the gate of typical Schottky-gate enhancement-mode (e-mode) GaN FETs. The maximum drive capability is 30 nC at 6 V V_{GS} .

The isolated V_{SEC} bias rail on the secondary is a derived open-loop from the primary 12 V supply V_{DRV} . The V_{SEC} rail level regulates quite well versus PWM switching frequency, f_{SW} , at the IN pin, for a given fixed V_{DRV} level and for a fixed load C_{OUT} at the OUTx drive pins (the load presented by the gate of the GaN FET being driven). This is because the charge delivered per PWM cycle naturally increases in tandem with the charge consumed by the FET gate, so there is a good charge balance across a wide frequency range. While the charge is consumed by the FET gate, the secondary side decreases with falling V_{SEC} level. Therefore, the V_{SEC} rail droops as far as needed until the charge delivered matches the charge consumed.

However, the V_{SEC} rail does vary with effective loading of the gate of FET being driven; As V_{SEC} level falls, more charge is available to be delivered. For this reason, it is also very important to minimize the amount of charge diverted into any external

loads. For example, a very-low-bias-power external circuit can be powered using V_{SEC} ; however, to minimize the charge diverted away from the gate of FET, the consumption should be minimal. Similarly, if a gate-source pull-down resistor is desired on the load FET (e.g., to prevent false turn-on in the case of a manufacturing fault, such as an open-circuit gate turn-on resistor), the resistor value should be as large as possible. The recommended value is 100 k Ω , to minimize DC loading on V_{SEC} . Because DC load current converts to equivalent charge as $Q = I \times t$, DC loading effects become significantly more pronounced at lower PWM frequency, as the time duration, t , increases.

Because there is only a single magnetic isolation barrier to transfer both PWM signal and gate power, this also greatly reduces the total parasitic capacitance between the primary-side and isolated-side, to typically < 1 pF^[1] total for both signal and power channels. This is much less than the typical total parasitic capacitance value for a solution using a conventional isolated gate driver with a separate isolated DC-DC bias supply, where the capacitance contribution from the DC-DC isolation transformer could be as high as 10 pF or more. This reduction in isolation capacitance greatly reduces the level of noise injected back into the low-voltage control circuit by the high-voltage and high dv/dt switching nodes in the power-stage half-bridge legs, reduces system-level common-mode (CM) EMI, and saves on power loss that occurs through repetitive charging and discharging of this parasitic capacitance between the high bus voltage level and ground.

[1] Capacitance between the primary and the secondary is affected by the transformer used.

APPLICATIONS INFORMATION

External Transformer Details

The AHV85000 and AHV85040 chipset form the primary-side transmitter (TX) and secondary-side receiver (RX) for an isolated GaN FET gate-driver. The chipset relies on an external transformer, connected between the TX and RX ICs, to achieve the isolated transmission of both PWM signal and gate bias power to the secondary side. The required transformer consists of a simple 2-winding, 4-pin structure—a primary-referenced TX winding and a secondary-referenced RX winding.

A selection of recommended transformers follows along with the manufacturer and the orderable part number. Each transformer is designed and optimized to work with the AHV85000/AHV85040 chipset interchangeably. The desired transformer can be selected to suit system design requirements; e.g., depending on the required system creepage distance, isolation rating, and target GaN FET drive voltage and gate charge.

Recommended Transformers

| Transformer Part Number | Manufacturer | Isolation Rating | Turns Ratio |
|-------------------------|--------------|------------------|-------------|
| TBD | Bourns | Basic | 1:1 |
| SM91243L | Bourns | Reinforced | 1:1 |
| TBD | Würth | Basic | 1:1 |
| 750320380 | Würth | Reinforced | 1:1 |

Expert designers can choose to use a custom transformer design of their own. The table below lists the acceptable ranges of key transformer parameters that must be maintained to ensure compatibility with the AHV85000/AHV85040 chipset.

Required Transformer Parameters

| Transformer Parameter | Minimum | Nominal | Maximum |
|-----------------------|------------------------|----------------------|--------------|
| L_{mag} | 5 μ H | 6 μ H | 7 μ H |
| L_{leak} | — | 600 nH | 700 nH |
| Volt-Seconds | 2.5 V \times μ s | 4 V \times μ s | — |
| DCR Primary | — | 1 Ω | 1.2 Ω |
| DCR Secondary | — | 1 Ω | 1.2 Ω |
| N_p/N_s | — | 1:1 | — |
| Frequency | — | 400 kHz | 1 MHz [1] |

[1] Maximum operating frequency can be limited by thermal performance of the design.

For designs that require a higher level of secondary-side bias voltage, V_{SEC} , and hence a higher gate-drive voltage, V_{GATE} , the turns ratio of the transformer can be adjusted accordingly. It is important to adhere to the recommended maximum operating conditions of the AHV85040 IC in this case.

The transformer connections to the AHV85000 and AVH85040 ICs are:

Required Transformer Connections

| Transformer Connection | AHV85000 Pin | AHV85040 Pin |
|------------------------|--------------|--------------|
| Primary Start | TXPP | — |
| Primary End | TXPN | — |
| Secondary Start | — | TXSP |
| Secondary End | — | TXSN |

Bidirectional Enable/Disable EN Pin

EN is a bidirectional open-drain pin that requires an external resistor pull-up to the VDRV pin or a suitable logic supply > 3.3 V. The EN pin allows for management of startup and fault conditions between the PWM controller and multiple drivers, through use of a shared enable EN line. Either the PWM controller or the driver can pull the EN pin low via the EN bus, as shown in Figure 3. When the EN pin is pulled low (either externally or internally), the driver is forced into a mode where the IN pin signal is ignored and the OUT pins are disabled and actively pulled low. When the EN pin is high, typical driver operation is enabled.

In the event of an internal driver fault condition, such as UVLO or typical startup delay, the EN pin is actively pulled low internally by the driver. This driver pull-down can be detected by the PWM controller and used as a flag for an external fault or to flag that the driver is ready and PWM can commence.

The shared EN line is typically wired-AND with the controller EN pin, as shown in Figure 3. Multiple drivers can be connected in parallel with the controller on the shared EN line, such that all connected drivers hold the EN line low until all drivers and the PWM controller have released their own EN pin, ensuring smooth safe startup of the system.

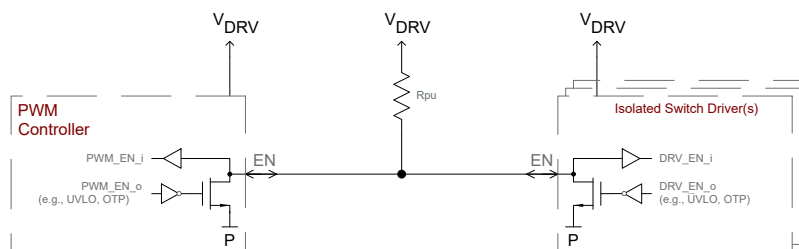


Figure 3: Example “Wired-AND” Connection Between Driver and Controller

Note that the EN pin has no internal pull-up or pull-down—the open-drain configuration relies on an external pull-up resistor for typical operation. Similarly, the EN pin must be actively pulled low externally to disable the driver. The EN pin should never be left floating. If not used, the EN pin should be connected to VDRV through a pull-up resistor in a recommended range of 10 to 100 k Ω . When being pulled low or high, the dv/dt of the EN pin should be at least 0.1 V/ μ s.

When the EN pin is pulled low, the driver output is disabled, and pulls down the OUTPD pin, regardless of the IN pin level (high or low). The driver transitions to a low-power standby mode, and the isolated VSEC bias rail is allowed to discharge. The rate of decay of V_{SEC} depends on the value of the C_{SEC} capacitor.

When the EN pin is subsequently pulled high, the driver re-enables and the isolated VSEC bias begins to recharge. Even if the IN pin is connected to a PWM signal, the OUT pins do not respond until the VSEC rail exceeds the secondary UVLO threshold. The rate of rise of V_{SEC} depends on the PWM frequency at the IN pin. The worst-case slowest rise time is when IN = 0, using the slowest internal energy-transfer mode. In this mode, the rise time is approximately 80 μ s for C_{SEC} of 47 nF to charge from zero to the rising UVLO threshold.

Startup and Shutdown Procedures

Any PWM signal applied to IN must remain low until V_{DRV} $>$ UV threshold, to avoid parasitic charging of the VDRV rail through the IN pin internal ESD structures. After V_{DRV} exceeds the UV enable threshold, a startup time delay t_{START} is required to charge VSEC and to allow all internal circuits to initialize and stabilize. During t_{START}, any IN signal inputs are ignored. The EN internal pull-down remains active during t_{START} and becomes disabled (i.e., becomes open-drain) only when V_{DRV} has reached its UVLO voltage level, all on-chip voltages are stabilized, and the internal t_{START} timer has elapsed. Thus, the EN pin can be used via a shared EN line to flag when t_{START} has elapsed and the driver is ready to respond to PWM signals at the IN pin, as outlined previously.

Typical startup waveforms are shown in Figure 4.

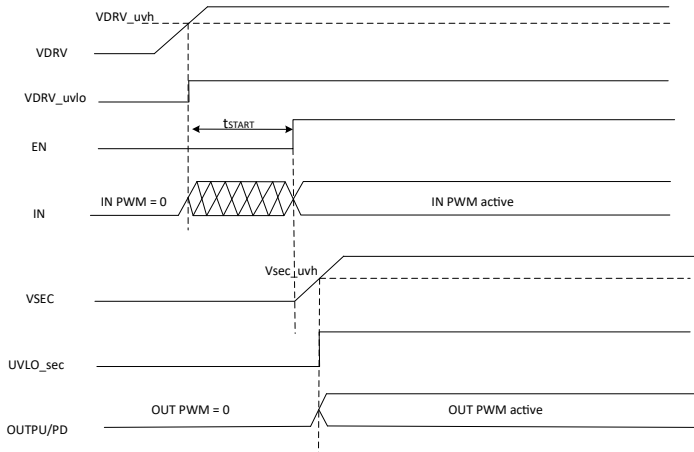


Figure 4: Startup Mechanism

Once V_{DRV} reduces below the UVLO falling threshold, the enable signal is pulled down and the driver output shuts down. The rate of decay of V_{SEC} is determined by the V_{SEC} capacitance as shown in Figure 5.

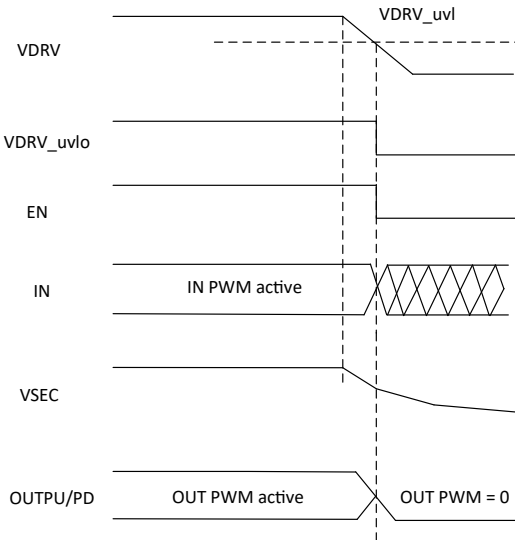


Figure 5: Shutdown Mechanism

Refresh Pulse Mechanism

If the IN-PWM signal frequency is low, or if IN is set to continuous 1 or 0, to prevent V_{SEC} voltage decay, the AHV85000 implements an internal clock of $12\ \mu\text{s}$ (t_{REFRESH}). When t_{REFRESH} elapses, the driver recharges the VSEC rail to maintain the output voltage. This condition persists until IN changes state, as shown in Figure 6.

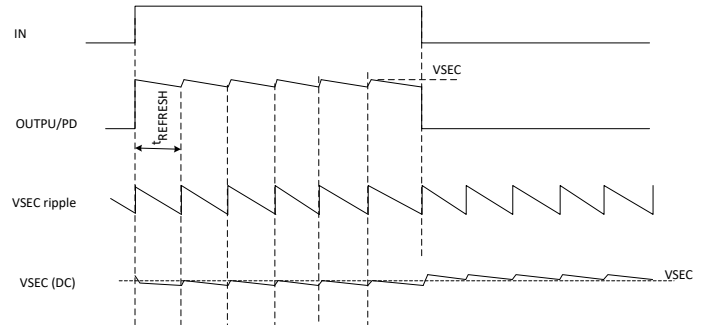


Figure 6: Refresh Mechanism

Operating Frequency

The maximum recommended PWM frequency is 1 MHz. However, the system power dissipation, application PCB layout, and ambient temperature must also be taken into account, to ensure that the internal recommended $T_{J(\text{MAX})}$ of 125°C is not exceeded.

The actual thermal performance in the end system design should always be verified, because every system is different in terms of exact PCB design and ambient airflow from natural or forced convection.

The main thermal management of the AHV85000 device is through the GND exposed pad; for the AHV85040 device, it is through the OUTSS exposed pad. It is recommended that these pads be connected to appropriate ground planes on each side and that the size of these planes be maximized to maximize thermal performance. Multiple thermal vias to larger inner-layer ground planes can also help improve thermal performance.

The effective gate capacitance, C_{OUT} , that loads the OUTx drive pins can be estimated from the GaN FET datasheet. The FET total charge $Q_{G(\text{TOT})}$ is usually specified in nC, for a given V_{GS} voltage swing.

Equation 1:

$$C_{\text{OUT}} = \frac{Q_{G(\text{TOT})}}{V_{GS}}$$

Knowing the value of C_{OUT} , the expected level of the secondary supply rail, V_{SEC} , can be estimated from Figure 7. From C_{OUT} , V_{SEC} , and the required PWM frequency f_{SW} , the total gate power can be calculated as follows:

Equation 2:

$$P_{\text{GATE}} = f_{\text{SW}} \times C_{\text{OUT}} \times V_{\text{SEC}}^2$$

In practice, the system design will likely use external gate resistors to control the FET turn-on and turn-off speed. The gate-drive

power consumption, P_{GATE} , will be dissipated by the internal driver FET resistances and external resistors, apportioned by the ratio of the resistances. The larger the value of the external resistors, the higher the power dissipation in those resistors and the lower the dissipation in the internal driver resistances. To simplify the thermal estimates, and to add in design margin, it is assumed that all of the P_{GATE} power is dissipated inside the driver package.

The internal driver stage MOSFETs consume drive power and have switching losses, so there is an efficiency factor that needs to be accounted for when estimating the internal power consumed when delivering the P_{GATE} power.

Finally, the internal isolated bias power stage consumes power. As well as the IC quiescent power consumption, there are also drive, conduction, and switching losses in the internal power FETs that drive and rectify the energy transfer through the internal isolation transformer, as well as the conduction and core losses of the transformer. These losses scale approximately linearly with PWM frequency.

V_{DRV} and C_{SEC} Design Guidelines

The output gate drive rail V_{SEC} is always less than V_{DRV} due to internal impedances and voltage drops. The V_{SEC} level depends on factors such as V_{DRV} level, C_{OUT} , and C_{SEC} . Figure 7 shows the typical output V_{SEC} level as a function of V_{DRV} and C_{OUT} , for a 50% duty cycle PWM at the IN pin. C_{OUT} is the equivalent load capacitance presented by the total gate charge of the FET being driven at the OUTx pins, as given in Equation 1.

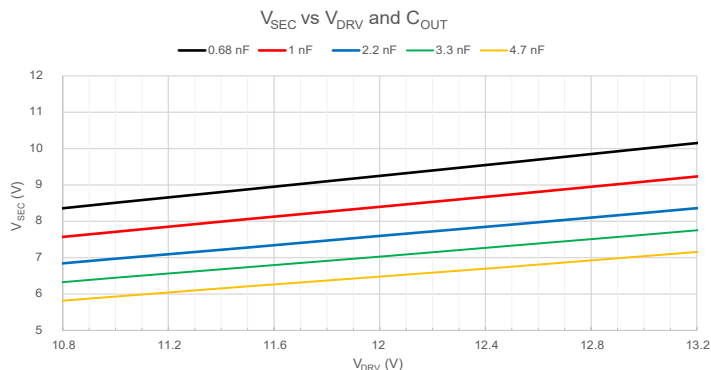


Figure 7: Typical V_{SEC} vs V_{DRV} for five C_{LOAD} capacitors; Conditions: $f_{SW} = 100$ kHz, $D = 50\%$, $C_{SEC} = 100$ nF, $X_{FMR} = SM91243L$, $T_A = 25^\circ C$

In some cases where the load FET gate charge is quite low, the V_{SEC} level may be higher than required. To reduce the V_{SEC} level to suit the FET V_{GS} requirements, the following steps can be taken:

- Make use of the recommended external Zener clamping circuit to limit the positive V_{GS} swing (with the balance appearing as a negative off-state V_{GS}). For more details, see the Bipolar Output Drive section.
- Reduce V_{DRV} level somewhat, to reduce V_{SEC} .
- Add extra load capacitance across the FET gate-source terminals; this increases the effective load gate charge and reduces V_{SEC} .
- Add some limited DC loading on the V_{SEC} rail. This can be achieved by a pull-down resistor across the FET gate-source terminals or a load resistor from the V_{SEC} pin to the OUTSS pin. The resistor value should be kept quite large to prevent an excessive overload on V_{SEC} . Begin with a large value >100 k Ω and gradually decrease the resistance until the desired V_{SEC} level is achieved.

The recommended value for C_{SEC} is approximately 10 to 20 times C_{OUT} (the equivalent gate capacitance), to give approximately 5% to 10% switching ripple on the V_{SEC} rail. Other values can be used; however, lower values result in higher ripple on V_{SEC} , and larger C_{SEC} require a longer startup time. The maximum recommended value of $C_{SEC} = 100$ nF should not be exceeded.

Because power is transferred to the secondary at a rate proportional to the PWM frequency and the gate power consumed by the load FET is also proportional to frequency, the V_{SEC} rail is relatively well regulated as PWM frequency is varied, for a given fixed V_{DRV} and fixed C_{OUT} . This is illustrated in Figure 8.

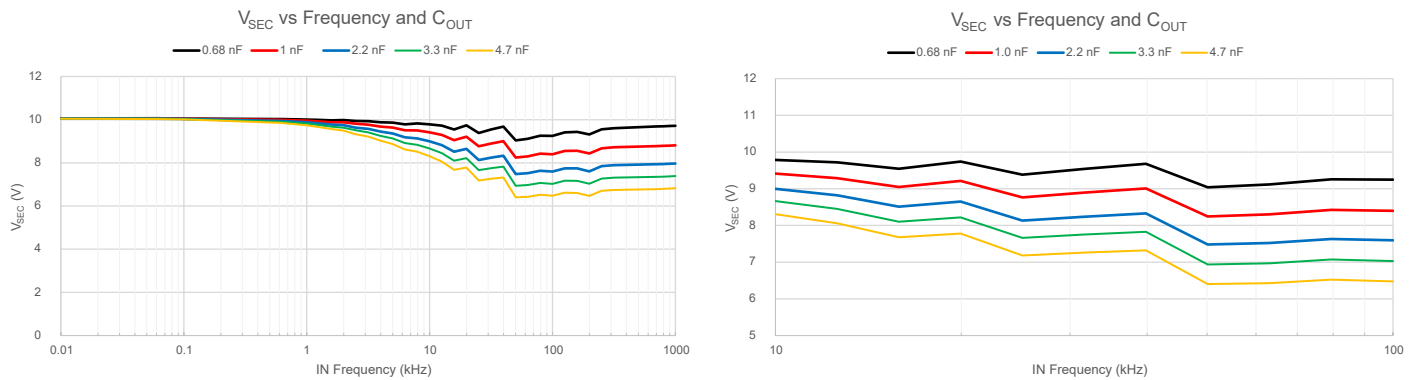


Figure 8: Secondary-Side Voltage, V_{SEC} , vs. Frequency and C_{OUT}
Conditions: $V_{DRV} = 12\text{ V}$, $C_{SEC} = 100\text{ nF}$, $X_{FMR} = \text{SM91243L}$, $T_A = 25^\circ\text{C}$

Bipolar Output Drive

The bipolar output drive is used to provide a negative gate voltage, as shown in Figure 9. This can be beneficial in protecting against false turn on due to parasitic circuits components. It can be added simply to the AHV85040 by including three extra small external components. The 5.6 V Zener diode clamps the amplitude of the positive V_{GS} swing during the on-time, with the balance of the V_{SEC} voltage appearing as a negative V_{GS} during the off-time. The 3.6 k Ω resistor in series with the Zener diode should be kept relatively large so that it does not load the V_{SEC} rail excessively. For full details, see the Allegro application note “[FET Gate Drive and Bipolar Output Applicable to AHV85110 Gate Drivers](https://www.allegromicro.com/-/media/files/application-notes/an296268-fet-gate-drive-and-bipolar-output.pdf?sc_lang=en)” (AN296268). [2]

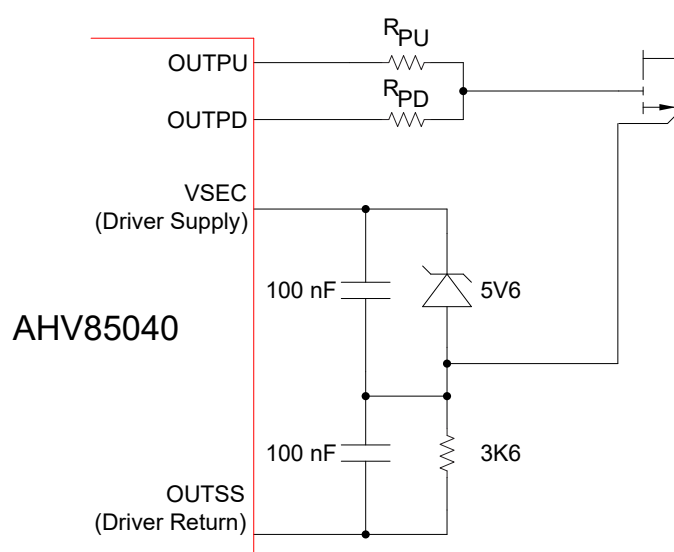


Figure 9: Bipolar Drive Implementation with External Zener Diode

[2] https://www.allegromicro.com/-/media/files/application-notes/an296268-fet-gate-drive-and-bipolar-output.pdf?sc_lang=en

Typical Application Example

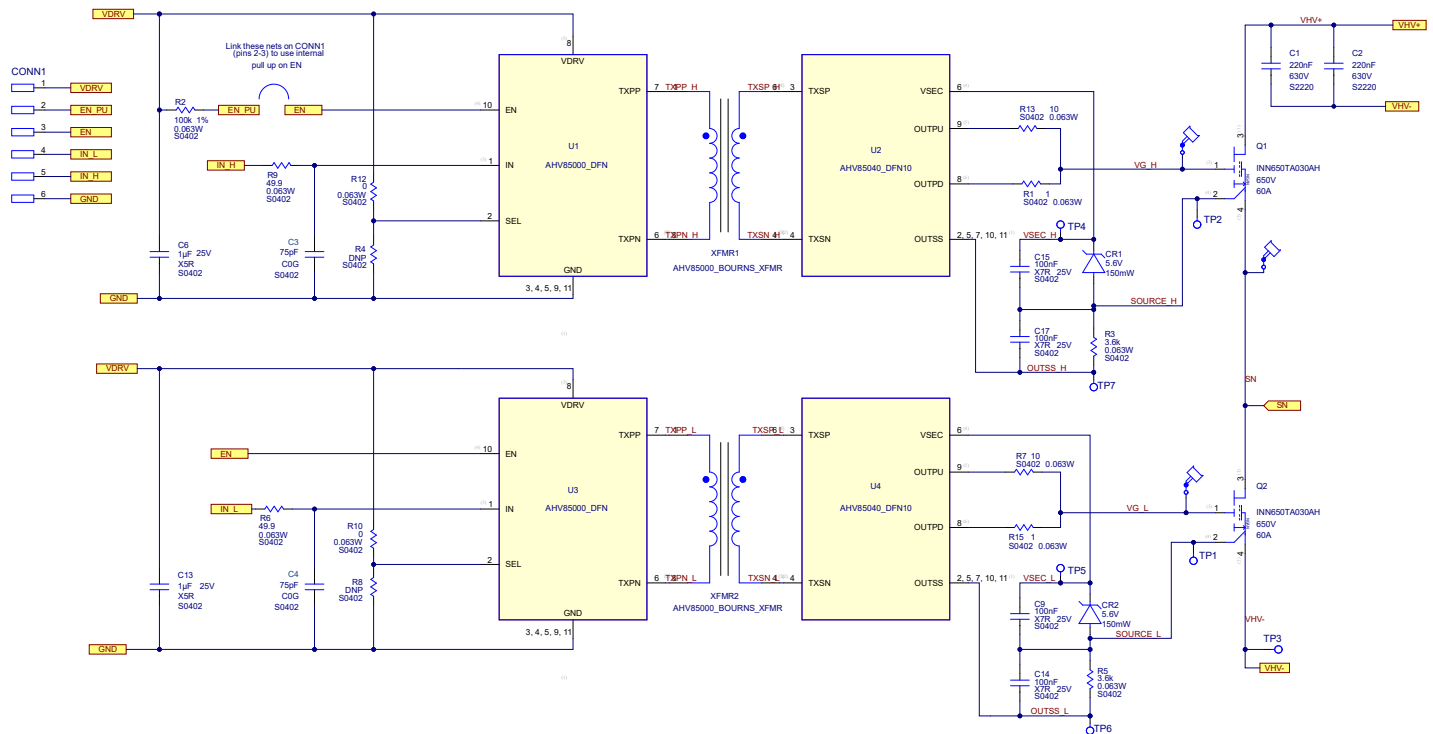


Figure 10: APEK85000-GEJ-01-T Schematic for Driving a GaN Transistor with a Bipolar Drive Arrangement

TYPICAL APPLICATIONS

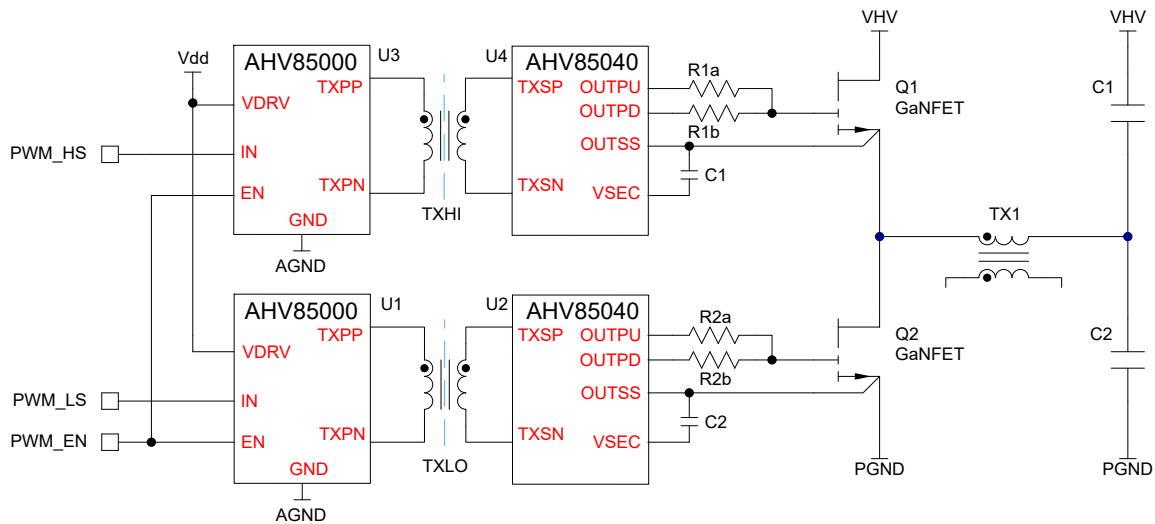


Figure 11: Half-Bridge with AHV85000 + AHV85040 Chipset as High-Side and Low-Side Drivers

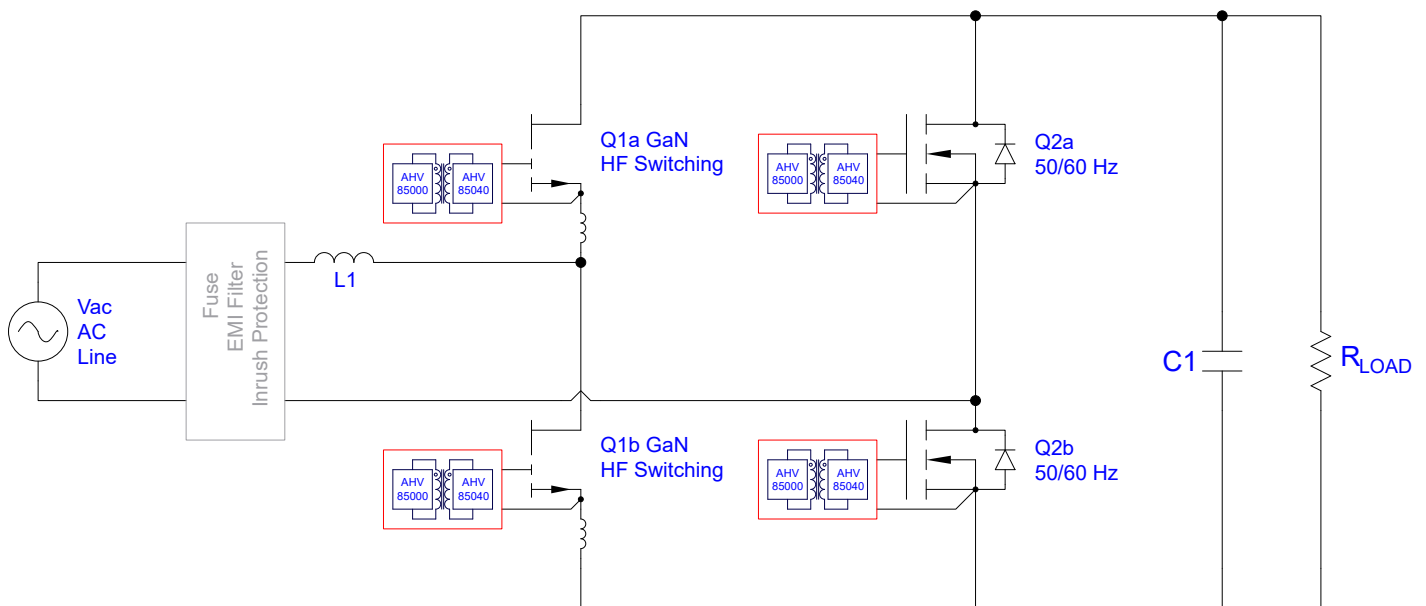


Figure 12: Totem Pole PFC with AHV85000 + AHV85040 Chipset as High-Side and Low-Side Drivers

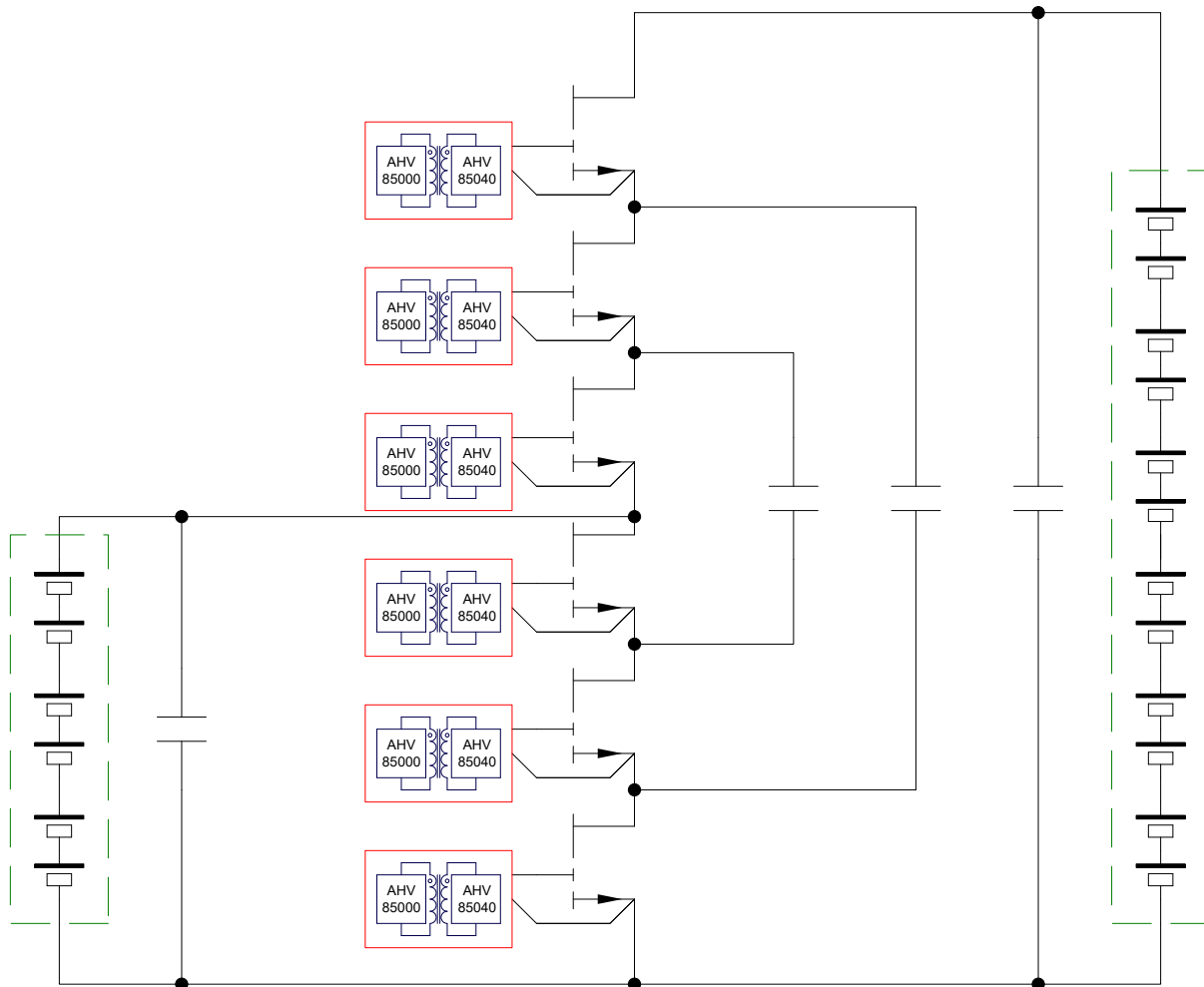


Figure 13: Multilevel Converter—Stacked Low-Voltage Switches Result in Higher Efficiency

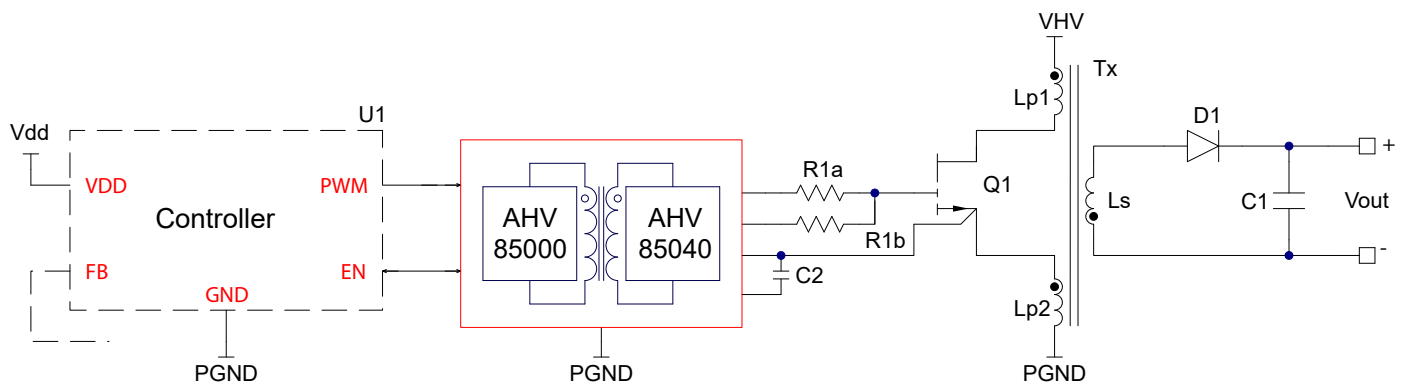


Figure 14: Center-Switched Fly-Back—AHV850x0 Driving Center-Tapped Switch (Symmetrical Bipolar Voltage Swings for Reduced Common-Mode Noise)

Layout Guidelines

- Place the AHV85040 gate driver as close as practical to the transistor. This is necessary to minimize the path of the high peak currents. This arrangement also minimizes the loop inductance and noise injection on the gate signals.
- Ensure that the resistors connected between the isolated output drive pins to the gate of the transistor are high-power rated and have high-power-surge withstanding capability.
- Decoupling capacitors must be connected close to the VDRV/GND and VSEC/OUTSS pin-pairs.
- The path connecting to the source of the transistor should be minimized to avoid large parasitic inductances.
- The layout should have good thermal relief to help dissipate heat from the gate driver to the PCB. It is recommended that vias be used to maximize thermal conductivity. The exposed pad on both ICs should be connected to an internal layer for thermal management.

Layout Example



17

Exact case and lead configuration at supplier discretion within limits shown



[4] Complete package information can be downloaded from the Allegro MicroSystems website: <https://www.allegromicro.com/en/design-support/packaging>

Revision History

| Number | Date | Description |
|--------|----------------|---|
| – | March 19, 2024 | Initial release |
| 1 | June 26, 2025 | Updated Junction-to-Case Thermal Resistance characteristic (page 2), and changed “SM91234L” to “SM91243L” (pages 6, 7, 9, 12, and 13) |

Copyright 2025, Allegro MicroSystems.

Allegro MicroSystems reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.

Allegro’s products are not to be used in any devices or systems, including but not limited to life support devices or systems, in which a failure of Allegro’s product can reasonably be expected to cause bodily harm.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

Copies of this document are considered uncontrolled documents.

For the latest version of this document, visit our website:

www.allegromicro.com