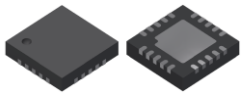
AHV85003-AHV85043

Self-Powered Isolated SiC Driver Chipset with Bipolar Output

FEATURES AND BENEFITS

- ***Power-Thru*** chipset:
  - Interfaces to external pulse transformers
  - Transmits both PWM signal and bias power
  - No high-side bootstrap or external bias-supply
- AEC-Q100 Grade 1 Qualification
- Bipolar drive, selectable regulated positive rail and configurable negative rails (secondary)
- Separate output gate pull-up & pull-down pins (6 A each)
- Miller clamp (internal)
- Supply voltage 10.5 V < V_{DRV} < 13.2 V
- UVLO on primary V_{DRV} and secondary V_{SECP} supply rails
- EN (enable) input and $\overline{FAULT}$ output pins
- Over-temperature protection (primary and secondary)
- Wide operating temperature range T_A -40°C to 125°C
- When matched with recommended external transformers:
  - Delivers up to 130nC gate charge at 25V (secondary)
  - 85 ns prop delay (typical)
  - < 50 ns skew & pulse-width-distortion
  - CMTI > 100 V/ns dv/dt immunity

PACKAGE: 20-PIN QFN 4x4 mm



DESCRIPTION

The AHV85003 and AHV85043 gate-driver chipset is optimised for driving discrete SiC FETs in applications such as automotive On-Board-Chargers (OBC), solar inverters, industrial robotics, data center power shelves, and general power supply applications. When combined with one of the recommended external transformers, it provides a self-powered isolated gate drive solution that is ideal for multiple applications and topologies. A selection of recommended third-party transformers is available, each optimised for different drive voltage, gate charge and isolation characteristics.

The chipset transmits both PWM signal and gate bias power through the external transformer, eliminating the need for any external auxiliary bias supply or high-side bootstrap. An isolated bipolar positive/negative output bias supply is generated on the isolated secondary side of the driver, eliminating the need for external circuitry to generate a split supply-rail. The bipolar output rails feature selectable regulated positive rail, and adjustable negative off-state rail for improved dv/dt immunity. This greatly simplifies the system design and reduces EMI through reduced total common-mode (CM) capacitance. It allows the driving of a floating switch in any location in a switching power topology, making it ideal for half-bridge, multi-level topologies, and any topology with a floating or high-side switch.

The chipset has fast propagation delay and high peak source/sink capability to efficiently drive SiC FETs in high-frequency designs. High CMTI combined with isolated outputs for both bias power and drive make it ideal in applications requiring isolation, level-shifting, or ground separation for noise immunity. Several protection features are integrated, including UVLO on primary and secondary bias rails, secondary bias rail over-voltage, fast-response enable input, and over-temperature shutdown. The open-drain $\overline{FAULT}$ output is de-asserted when the secondary bias rails are in regulation and no faults are detected. The chipset is available in a standard QFN-20 (4mm x 4mm) package.

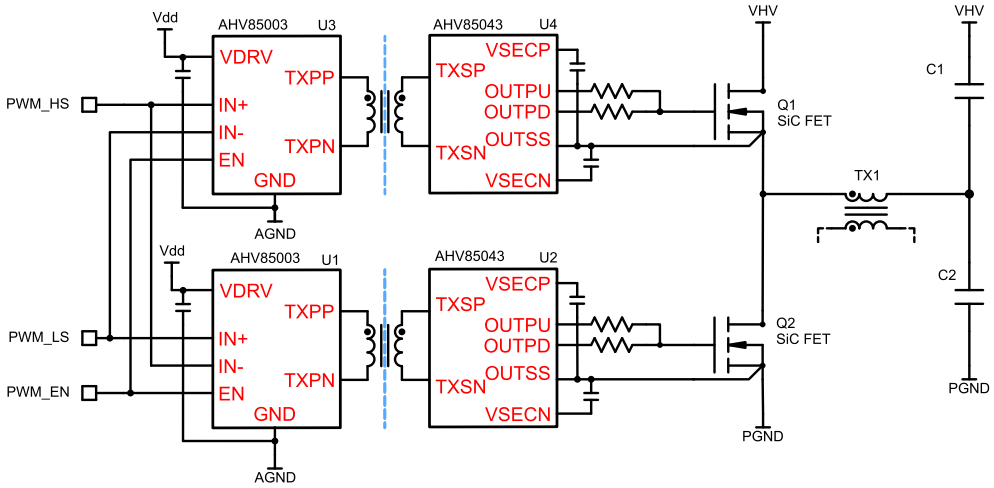


Figure 1: Simplified Typical Application Circuit

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS – AHV85003

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{DRV}	Voltages are relative to GND	-0.5 to 17	V
Input logic pins	IN+, IN-		-0.5 to +6.5	V
EN, $\overline{FAULT}$, PWRSEL pins			-0.5 to V_{DRV}	V
$\overline{FAULT}$ sink current			10	mA
TXPP/TXPN		Output pin, voltage cannot be forced Max spike voltage (<20ns) during switching activity	-5.0 to 18	V
BSP		Voltage relative to TXPP	TXPP - 0.3 to TXPP + 3.6	V
BSN		Voltage relative to TXPN	TXPN - 0.3 to TXPN + 3.6	V
Operating Ambient Temperature	T_A		–40 to 125	°C
Junction Temperature	$T_{J(max)}$		–40 to 150	
Storage Temperature	T_{stg}		–40 to 150	

ABSOLUTE MAXIMUM RATINGS – AHV85043

Driver outputs	OUTPU, OUTPD, CLAMP	Voltage relative to VSECN	Output pin, cannot be forced Max spike voltage (<20ns) during switching activity	-2.0 to +35.0	V
TXSP/TXSN Pins			VSECP refers to the regulated VSECP voltage.	-0.5 to VSECP+0.5	
Secondary bias rail	VSECP		Output pin, cannot be forced Voltage regulated at Vsecp-Vsecn	20	mA
SOURCE	V_{SOURCE}		Output pin, cannot be forced Voltage regulated at -Vsecn	20	mA
Voltage sense pin	VFBN			-0.5 to +7.5	V+
Operating Ambient Temperature	T_A			–40 to 125	°C
Junction Temperature	$T_{J(max)}$			–40 to 150	
Storage Temperature	T_{stg}			–40 to 150	
CP		Voltage relative to VSECP.		VSECP - 0.3 to VSECP + 3.6	V

Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ESD RATINGS

Characteristic	Symbol	Test Conditions	Value	Unit
Human Body Model	V_{HBM}		±2	kV
Charged Device Model	V_{CDM}		±500	V

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic [1)]	Symbol	Value	Unit
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	75 to 136	°C/W
Junction-to-Case Thermal Resistance	$R_{\theta JC}$	2	°C/W

Notes:

1) Additional thermal information available on the Allegro website.

2) Standard Board

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MSL RATING

Device	MSL Rating	Maximum Floor Life at Standard Ambient (30°C/60%RH)	Maximum Peak Reflow Temperature	Pre-Reflow Bake Requirement
AHV85003 AHV85043	MSL2	1 year	260°C	Per JEDEC J-STD-033C

Per JEDEC J-STD-033C, these devices are rated MSL2. This MSL2 rating means that once the sealed production packaging is opened, the devices must be reflowed within a “floor-life” of 1 year, if they are stored in under standard ambient conditions (30°C and 60% relative humidity (RH)). The peak reflow temperature should not exceed the maximum specified in MSL Rating table.

If the devices are exposed to the standard ambient for more than 1 year, they must be baked before reflow to remove any excess moisture in the package and prevent damage during reflow soldering. The required bake times and temperatures are detailed in IPC/JEDEC standard J-STD-033C. If the devices are exposed to higher temperature and/or RH compared to the standard ambient of 30°C/60% RH, the floor-life will be shortened due to the increased rate of moisture absorption. If the actual ambient conditions exceed the standard ambient, it is recommended that parts should always be baked per IEC/JEDEC J-STD-033C before reflow as a precaution to avoid potential device damage during reflow soldering.

SELECTION GUIDE

Part Number	Device	VSECP Setting	Package Description	Package Size (L x W x H)
AHV85003K15ESTR	Primary	15 V	20-PIN QFN	4.0 x 4.0 x 0.75 mm
AHV85043K15ESTR	Secondary	15 V	20-PIN QFN	4.0 x 4.0 x 0.75 mm
AHV85003K18ESTR	Primary	18 V	20-PIN QFN	4.0 x 4.0 x 0.75 mm
AHV85043K18ESTR	Secondary	18 V	20-PIN QFN	4.0 x 4.0 x 0.75 mm
AHV85003K20ESTR	Primary	20 V	20-PIN QFN	4.0 x 4.0 x 0.75 mm
AHV85043K20ESTR	Secondary	20 V	20-PIN QFN	4.0 x 4.0 x 0.75 mm

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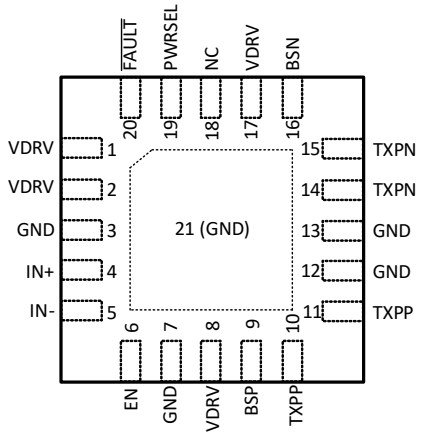
PINOUT DIAGRAM AND TABLE

AHV85003
(Top View)

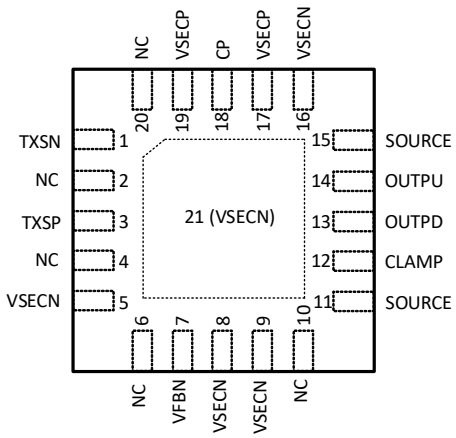


Driver Chipset Primary IC

Pinout Table

Pin name	Pin num	Brief description
VDRV	1, 2, 8, 17	Primary bias supply voltage
PWRSEL	19	Adjust power throughput
$\overline{\text{FAULT}}$	20	Fault output, open drain
GND	3, 7, 12, 13	Ground
IN+	4	Input PWM signal (positive logic)
IN-	5	Input PWM signal (negative logic)
EN	6	Enable
BSN	16	Bootstrap capacitor (wrt TXPN)
TXPP	10, 11	Positive connection to external transformer primary winding
TXPN	14, 15	Negative connection to external transformer primary winding
BSP	9	Bootstrap capacitor (wrt TXPP)
Exposed pad (GND)	21	Exposed pad (pin 21) is internally connected to GND. The exposed pad does not replace the GND pin.

AHV85043
(TOP View)

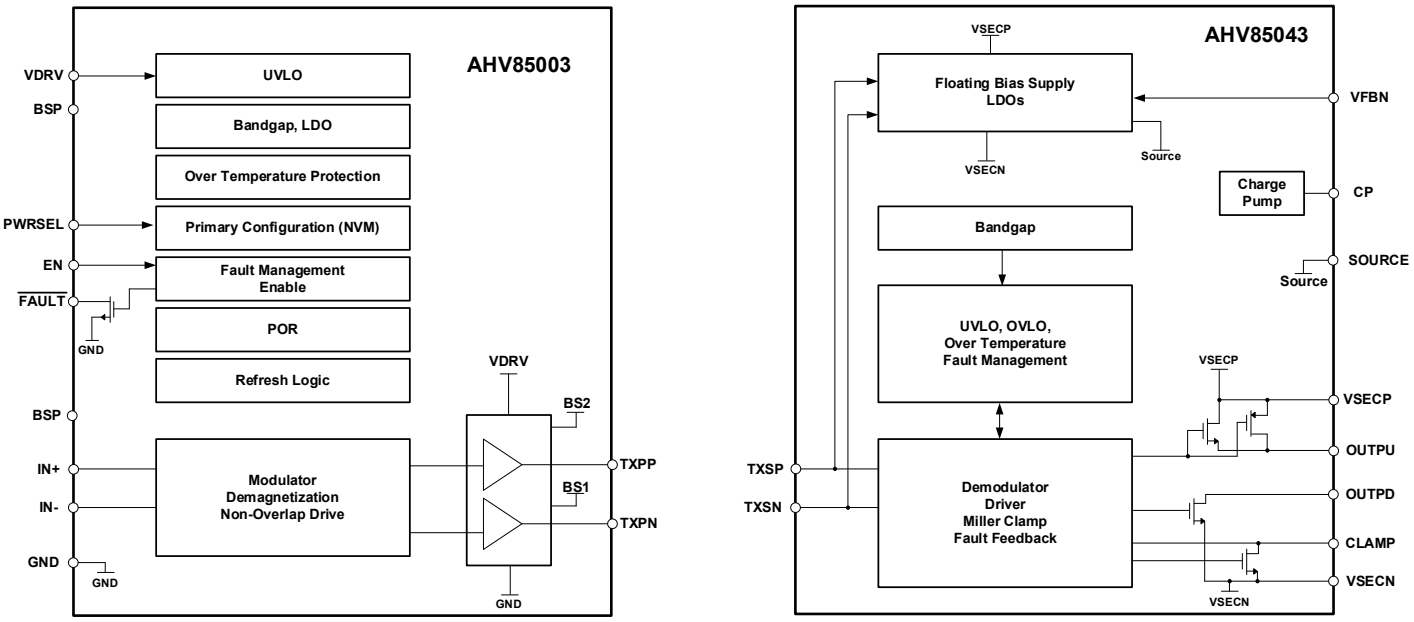


Driver Chipset Secondary IC

Pinout Table

Pin name	Pin num	Brief description
VSECP	17, 19	Positive gate drive supply rail (referenced to SOURCE), internally rectified and regulated from the power pulses at the TXSP/N pins
TXSP	3	Positive connection to external transformer secondary winding
TXSN	1	Negative connection to external transformer secondary winding
VSECN	5, 9, 8, 16	Negative gate drive supply rail (referenced to SOURCE), internally rectified and regulated from the power pulses at the TXSP/N pins
VFBN	7	Feedback input for the negative rail regulator (VSECN), connected to an external resistor divider between SOURCE and VSECN.
SOURCE	11, 15	SOURCE connection of the driven SiC FET
CLAMP	12	Miller clamp pull-down to VSECN
OUTPD	13	Output pull-down (turn-off) of the gate driver, referenced to VSECN
OUTPU	14	Output pull-up (turn-on) of the gate driver, referenced to VSECP
CP	18	Charge pump capacitor positive terminal, referenced to VSECP
Exposed pad (VSECN)	21	Exposed pad (pin 21) is internally connected to VSECN. The exposed pad does not replace the VSECN pin.

NOTE: Where multiple power and ground pins are provided (e.g. VDRV, GND, VSECP, VSECN, SOURCE), all pins must be connected



Functional Block Diagrams

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ELECTRICAL CHARACTERISTICS:

Valid at -40°C < T_J < 150°C, 10.5 V < V_{DRV} < 13.2 V, C_{SECP} = 100 nF, C_{SECN} = 100 nF, C_{OUT} = 4.7 nF, EN = high, interfaced to recommended external transformer Table 5, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Unit
ELECTRICAL CHARACTERISTICS – AHV85003						
Supply Voltage	V_{DRV}		10.5	12	13.2	V
Undervoltage Lockout	$V_{DRV(UVR)}$	V_{DRV} rising	9.5	10.0	10.5	V
	$V_{DRV(UVF)}$	V_{DRV} falling	8.5	9.0	9.5	V
Undervoltage Hysteresis	$V_{DRV(HYS)}$		0.7	1.0		V
Supply Current [2]	$I_{DRV(DIS)}$	Quiescent current, EN = Low			2.5	mA
	$I_{DRV(Q)}$	Quiescent current, EN = High, IN = Low			4.3	
	$I_{DRV(SW)}$	Switching current, EN = High, IN = 100 kHz, C_{OUT} = 0			12.5	
Input logic levels (IN+, IN-, EN)	$V_{IN(L)}$	Logic Low			0.8	V
	$V_{IN(H)}$	Logic High	2.0			
	$V_{IN(HYS)}$	Hysteresis		0.8		
	R_{IN}	Internal pull-down (IN+) or pull-up (IN-)		150		kΩ
	R_{EN}	Internal pull-down (EN)		300		
EN de-glitch	t_{EN}			50		µs
$\overline{FAULT}$	$V_{FLT(L)}$	4.5 mA sink current (1 kΩ pull-up to 5 V)			0.5	V
Over-temperature shutdown	$T_{SDP(R)}$	Primary-side sensor, rising threshold	153	163	173	°C
	$T_{SDP(F)}$	Primary-side sensor, falling threshold	130	140	150	
ELECTRICAL CHARACTERISTICS – AHV85043						
V_{SECP} regulation setpoints						
15-V option	V_{SECP_15}	With respect to SOURCE	14.25	15.0	15.75	V
18-V option	V_{SECP_18}		17.10	18.0	18.90	V
20-V option	V_{SECP_20}		19.0	20.0	21.0	V
Undervoltage Lockout	$V_{SECP(UVF)}$	V_{SECP} falling disable threshold, percentage of nominal regulation level		80%		
	$V_{SECP(UVR)}$	V_{SECP} rising enable threshold, percentage of nominal regulation level		85%		
Undervoltage de-glitch	t_{VSECUV}			20		µs
Overvoltage Lockout	$V_{SECP(OVR)}$	V_{SECP} rising disable threshold, percentage of nominal regulation level		115%		
Overvoltage de-glitch	$t_{VSECPOV}$			20		µs
Feedback reference V_{SECN}	V_{FBP}	VFBN input Referenced to V_{SECN}	0.92	1.0	1.08	V
Overvoltage Lockout	$V_{FBP(OV)}$	VFBN overvoltage		1.22		V
Output driver peak current	I_{SOURCE}	OUTPU		6		A
	I_{SINK}	OUTPD		6		
Output resistance	R_{PD}	OUTPD pull-down R_{DSON}			1	Ω
	R_{PU}	OUTPU internal PMOS pull-up R_{DSON}			10	
Clamp detection threshold	V_{CLP}	Referenced to V_{SECN}		2		V
Clamp peak current[3]	I_{CLP}			4		A
Clamp on-resistance	$R_{DSON-CLP}$				1.5	Ω
Over-temperature shutdown	$T_{SDS(R)}$	Secondary-side sensor, rising threshold	150	160	170	°C
	$T_{SDS(F)}$	Secondary-side sensor, falling threshold	130	140	150	

[1] Typical values are at T_A = 25°C and V_{DRV} = 12 V unless stated otherwise. Performance may vary for individual units, within the specified maximum and minimum limits.
[2] Supply current is for a AHV85003 + AHV85043 chipset when used with a recommended external transformer
[3] Parameter is not production-tested, guaranteed by characterization.

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ELECTRICAL CHARACTERISTICS (Continued):

Valid at -40°C < T_J < 150°C, 10.5 V < V_{DRV} < 13.2 V, C_{SECP} = 100 nF, C_{SECN} = 100 nF, C_{OUT} = 4.7 nF, EN = high, interfaced to recommended external transformer Table 5, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.[4]	Max.	Unit
TIMING CHARACTERISTICS – AHV85003 + AHV85043 + recommended external transformer						
Propagation delay	t_{PLH}	Delay from IN+ low-to-high transition to OUTPx low-to-high transition; R_{EXT_PU} = 10 Ω, C_{OUT} = 100 pF		85	135	ns
	t_{PHL}	Delay from IN+ high-to-low transition to OUTPx high-to-low transition; R_{EXT_PD} = 10 Ω, C_{OUT} = 100 pF		85	135	
Pulse-width distortion [5]	t_{PWD}	| t_{PLH} - t_{PHL} |		5	50	ns
Propagation-delay matching [4]		Part-to-part variation [4]		10		
PWM frequency [4]	f_{PWM}	Supported input frequency range at IN+/IN-. Can be operated at DC (i.e. IN+/IN- continuously low or high)	0		450	kHz
Output Rise Time	t_r	R_{EXT_PU} = 1 Ω, C_{OUT} = 1 nF, 20-80%		10		ns
Output Fall Time	t_f	R_{EXT_PD} = 1 Ω, C_{OUT} = 1 nF, 20-80%		10		

[4] Typical values are at T_A = 25°C and V_{DRV} = 12 V unless stated otherwise. Performance may vary for individual units, within the specified maximum and minimum limits.
[5] Parameter is not production-tested, verified by design/characterization.

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Functional Description

The AHV85003 and AHV85043 are the primary-side (transmitter) and secondary-side (receiver) ICs respectively, of the isolated SiC FET gate-driver chipset. The chipset interfaces to an external transformer, connected between the TX and RX ICs, which transmits both the PWM signal and the gate driver bias power for the isolated side. The required transformer consists of a simple two-winding, four-pin structure.

A selection of recommended third-party transformers is listed in Table 5. These have been fully tested and validated for use with the AHV85003 and AHV85043 chipset. The required transformer can be selected to suit different system design requirements, e.g. the required system creepage distance, isolation rating, and the target FET drive voltage and gate charge.

V_{DRV} Supply and UVLO

The AHV85003/AHV85043 chipset requires a single 12V supply (V_{DRV}) to power the driver chipset, in conjunction with the external transformer. AHV85003 is powered directly from the 12-V V_{DRV} supply on the primary side. On the isolated secondary-side, bias power for the AHV85043 is generated by internally rectifying and regulating the TXSP/TXSN pulses from the external transformer. No dedicated secondary-side bias supply is required. Under-voltage protection is provided on V_{DRV} supply to ensure proper operations. At startup, the primary circuit stays in a low-power standby mode until V_{DRV} exceeds the UVLO rising threshold $V_{DRV(UVR)}$, and no power is transferred to the secondary circuit. While running, if V_{DRV} falls below the UVLO falling threshold $V_{DRV(UVF)}$, the $\overline{FAULT}$ pin is pulled low, PWM signal and power transfer to the secondary are halted, and the internal REF regulator is disabled. When the V_{DRV} level recovers and exceeds the UVLO rising threshold $V_{DRV(UVR)}$ again, the system restarts.

Startup

When the primary supply voltage VDRV is applied to the primary side AHV85003 IC, it remains in low power mode until VDRV exceeds the UVLO threshold. Once the UVLO threshold is exceeded, the internal LDOs and regulators are enabled. If the EN input is held low, the primary side stays in a low power standby mode, with the $\overline{FAULT}$ output held low. Once EN goes high, or if EN is already high when VDRV UVLO is released, then the primary side of driver enables power transfer to the secondary, to charge the secondary-side isolated bias rails. This is achieved by sending pulses to the TXPP and TXPN pins to energize the external transformer. On the secondary-side AHV85043 IC, when the secondary-side bias rails have settled to the target regulation levels, and if no faults are detected on either the primary side or the secondary side, then the open-drain $\overline{FAULT}$ pin is allowed to go high, via the required external pull-up resistor. This indicates to the system controller that the driver is ready to accept PWM signal input. Any PWM signal inputs at the IN+/IN- pins are ignored until the internal $\overline{FAULT}$ pull-down is released.

Refresh Pulse Mechanism

In cases when PWM signal frequency is too low at the AHV85003 INx pins, or when INx is set to continuous high (1) or low (0), the AHV85003 transmits a refresh pulse to the external transformer through the TXPP and TXPN pins. On the isolated side of the external transformer, the TXSP and TXSN pins of the AHV85043 rectify these pulses, to transfer the energy to the VSECP and VSECN rails. This mechanism ensures that the VSECP and VSECN rails do not sag due to the internal bias consumption of the AHV85043, and regulation is maintained when there are no PWM signal transitions at the AHV85003 INx pins, or the transitions become infrequent due to frequency and/or duty cycle.

When INx is low or high for longer than the refresh timeout period t_{PER_REF}, the internal logic automatically generates a refresh pulse, and the refresh timer is reset. Each time an edge transition is detected on the INx pins, the refresh timer is also reset.

A benefit of the refresh pulse mechanism is that whenever INx signal to the AHV85003 is low for a continuous long period of time, for example at startup, energy is still transferred to the isolated side via the AHV85043 TXSP/TXSN pins, to charge the isolated bias rails VSECP and VSECN. As a result, no bootstrap or isolated supply is required to get the isolated side of the driver chipset started, so the chipset is ready to respond immediately to signals at the INx pins as soon as the $\overline{FAULT}$ pin pull-down is released.

A feedforward function ensures that a constant amount of power is delivered to the secondary side, independently from VDRV supply variations.

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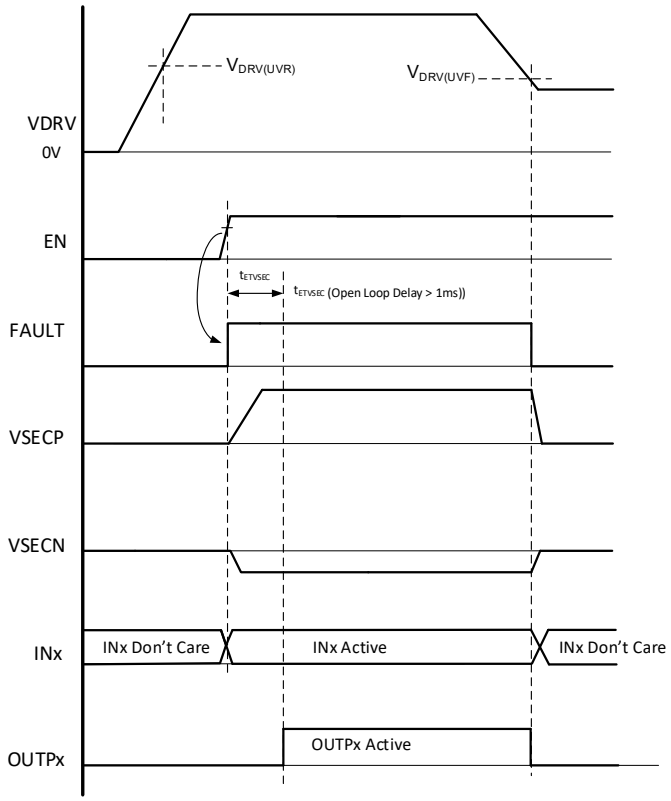

Figure 2: Startup Time and Sequence and VDRV Supply UVLO [AHV85003 + AHV85043 + recommended external transformer]

Enable Input

The AHV85003 enable (EN) pin can be pulled low to disable the TXPP and TXPN signals. This disables the PWM signal transfer to the output, and forces the AHV85003 into a low-power mode. The isolated secondary bias rails for the AHV85043 are also disabled.

The EN pin includes an internal weak pull-down, and a de-glitch filter to minimize false toggling due to noise pick-up.

The EN pin is rated up to V_{DRV} maximum, so it can be tied high to any system 5V or 3.3V logic rail, or V_{DRV}, to enable the AHV85003 driver.

Fault Output and Fault Conditions

Fault conditions, detected on either AHV85003 (primary) or AHV85043 (secondary), are reported to the AHV85003 $\overline{\text{FAULT}}$ output pin. The active-low open-drain $\overline{\text{FAULT}}$ pin requires an external pull-up resistor. The pull-up can be tied to any suitable voltage rail (i.e. 3.3V or 5V) up to V_{DRV}.

During startup, the $\overline{\text{FAULT}}$ pin is internally pulled low to flag to the external system controller that the driver is not ready to respond to PWM signals at the INx pins. Upon successful startup, with no faults detected, the $\overline{\text{FAULT}}$ pin goes high impedance to notify the system controller that driver is ready.

While running, if any faults are detected by either the primary-side AHV85003, or the secondary-side AHV85043, the $\overline{\text{FAULT}}$ pin is internally pulled low, to alert the system controller. At the same time, the AHV85043 output driver pull-up (OUTPU) is disabled, and the output driver pull-down (OUTPD) pin is held low, regardless of the signal level at the INx pins.

This open-drain configuration allows the $\overline{\text{FAULT}}$ pins of multiple driver channels to be OR-ed together, so that the $\overline{\text{FAULT}}$ bus will only go high when all driver channels are ready. Alternatively, individual driver $\overline{\text{FAULT}}$ pins can be connected to different digital input pins of the system controller, so that the specific fault source can be determined.

Fault conditions detected on the AHV85043 are transmitted to the primary side through the pulse transformer. A short filtering time is applied on the primary-side detection. If the $\overline{\text{FAULT}}$ pin functionality is not used or not required on the primary side, this pin can be left unconnected. Fault conditions are listed in Table 1.

Monitor	Function	$\overline{\text{FAULT}}$ pin
VDRV supply (AHV85003)	Undervoltage lockout	Yes
Junction (AHV85003)	Overtemperature Lockout	Yes
VSECP (AHV85043)	Undervoltage Lockout Overvoltage Lockout	Yes
VFBN (AHV85043)	VSECN Feedback (VFBN) Overvoltage Lockout	Yes
Junction (AHV85043)	Overtemperature Lockout	Yes

Table1: Fault Sources and Conditions

PWM Inputs

The AHV85003 includes two general-purpose PWM input pins IN+ and IN-. These can be driven with any type of signal, DC (continuous logic low or logic high) or any arbitrary PWM pulse train, as long as the signal timing adheres to the maximum frequency and minimum on-time and off-time specifications.

The IN+/IN- pins can be used with normal positive logic, using IN+ only, with IN- tied to GND. Or with inverted negative logic, using IN-, with IN+ tied high. Both PWM input pins are compatible with standard 3.3-V or 5-V logic signals from a system controller, and feature Schmitt-type inputs with wide hysteresis for high noise immunity. The truth table for IN+ and IN- is shown in Table 2, and example timing diagram in Figure 3.

IN+	IN-	OUTPx
0	0	0
0	1	0
1	0	1
1	1	0

Table 1: AHV85003 Truth Table for IN+ and IN- input pins

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Input pin IN+ and IN- have a 150kΩ pull-down and pull-up respectively. These built in resistors prevent the inputs from floating if they are left open. Nevertheless, any unused input must be tied low (IN-) or high (IN+) if not used in the application.

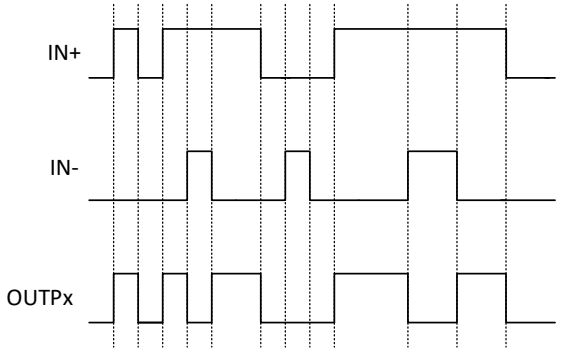

Figure 3: Logic waveforms – IN+ and IN- to OUTPx pins [AHV85003 + AHV85043 + recommended external transformer]

Isolated Secondary Bias Rails

While the positive gate drive bias rail V_{SECP} is fixed (values of +15 V, +18 V or +20 V), the negative (relative to Source) off-state gate rail, V_{SECN}, is user-adjustable through a voltage divider.

As shown in Table 3, the negative bias rail V_{SECN} can be adjusted by selecting the ratio of the two external resistors R_{nt} and R_{nb} on the V_{FBN} pin.

The values for the external divider resistors can be chosen according to the equation:

$$V_{SECN} = V_{FBN} \cdot \left(1 + \frac{R_{nt}}{R_{nb}}\right)$$

Or

$$R_{nt} = R_{nb} \cdot \left(\frac{V_{SECN}}{V_{FBN}} - 1\right)$$

Alternatively, the recommended values in Table 3 can be used to set commonly used negative voltage levels from 0 V to -5 V.

VSECN	R_{nt} (kΩ)	R_{nb} (kΩ)
-5	40.2	10.0
-4	30.1	10.0
-3	20.0	10.0
-2	10.0	10.0
-1	0	10.0
0	0	0

Table 2: AHV85311 recommended VSECN divider resistor values
Note: the total secondary voltage (V_{SECP} – V_{SECN}) must not exceed 21V

It is recommended to utilize a maximum resistor value of 47kΩ in the resistor divider, to minimize the effect of pollutants on the divider network.

For the special case where no negative gate drive rail is required (VSECN = 0 V), both divider resistors should be zero ohm, to short together the nets SOURCE-VFBN-VSECN, to disable the internal VSECN regulator. Alternatively, the SOURCE, VFBN and VSECN pins can be shorted together to disable the regulator and achieve zero negative gate drive rail.

It's recommended to add three decoupling capacitors, as shown in Figure 4. CVSN, connected between V_{SECP} and V_{SECN}. CVSP, connected between V_{SECP} and SOURCE. CVSNS connected between V_{SECN} and Source. Maximum recommended value is 1µF for each capacitor.

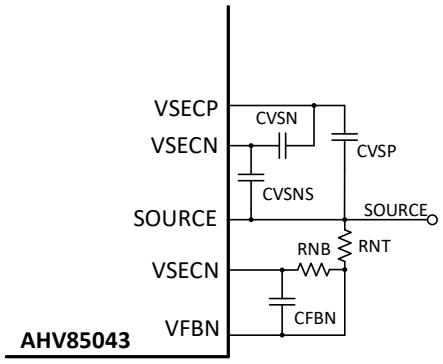

Figure 4: External resistor divider connection to program V_{SECN} regulation level

Output Driver Stage

The AHV85043 output driver stage features separate pull-up (OUTPU) and pull-down (OUTPD) pins to allow separate tuning of turn-on and turn-off speed with external gate resistors.

The pull-up structure consists of parallel N-channel and P-channel MOS-FETs. The N-channel device provides the necessary high-peak source current during the initial gate-charging phase, when the high-source current is needed most. The parallel P-channel continues to pull up during the later portion of the gate-charging phase, to bring the external gate voltage up to the V_{SECP} positive gate drive level for lowest R_{DSON} performance in the SiC FET being driven.

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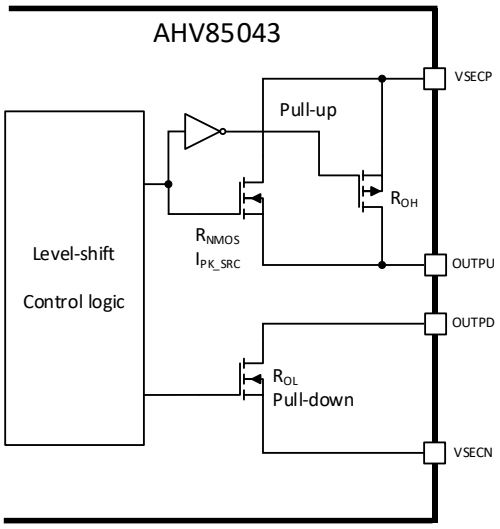

Figure 5: Output driver simplified structure [AHV85043]

The pull-down structure consists of a low R_{DSON} N-channel MOSFET for maximum peak sink current, for fast turn-off of the SiC FET.

When not powered or when the device is in a fault condition, the OUTPD is in low-impedance mode to prevent the SiC FET from turning on.

Miller Clamp

A built-in Miller clamp pull-down is provided on the AHV85043 to increase robustness to false turn-on events arising from fast dv/dt events on the SiC FET drain. The Miller clamp is activated during turn-off, after the OUTPD pin has already discharged the external SiC FET gate capacitance below the Miller clamp threshold, relative to V_{SECN}. The Miller clamp provides a low impedance path directly from the SiC FET gate to V_{SECN}, bypassing the external gate resistor. This low impedance clamp absorbs current spikes that are injected into the SiC FET gate, caused by fast dv/dt on the SiC FET drain, which forces large current spikes in the FET Miller capacitance, C_{GD}. The Miller Clamp pull-down is reset on each subsequent PWM rising edge.

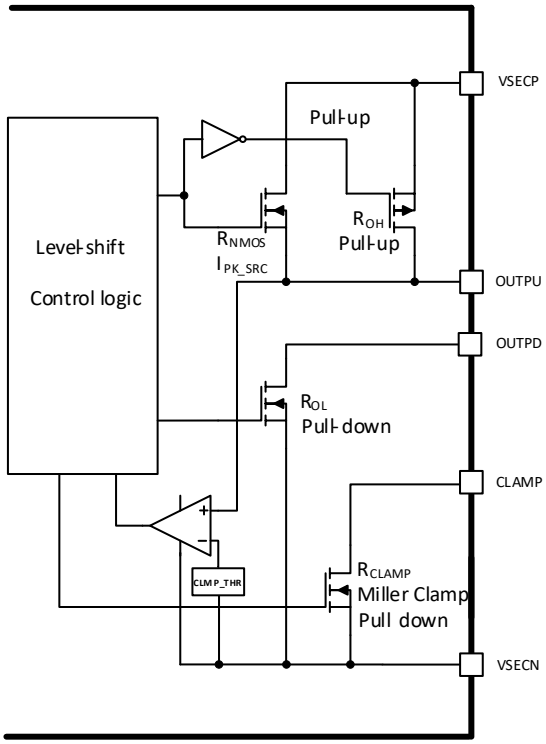

Figure 6: Miller Clamp Simplified Block Diagram [AHV85043]

Over-Temperature Shutdown

Internal over-temperature shutdown protects if the internal IC temperature of either AHV85003 or AHV85043 becomes excessive; this protection is non-latching and recovers once the internal IC temperature has cooled below the recovery level. If an over-temperature condition is detected, the AHV85043 output driver pull-up (OUTPU) is disabled, and the output driver pull-down (OUTPD) pin is held low, regardless of the signal level at the INx pins.

If the over-temperature fault is detected on the secondary-side AHV85043, the fault is communicated to the primary-side AHV85003 as described in section Fault Output.

As with all internal faults, the open drain $\overline{\text{FAULT}}$ pin will also pull low, to flag the fault condition to the system controller.

Power Select Pin PWRSEL

The AHV85003 PWRSEL pin allows the user to adjust the rate of energy transfer to the secondary side, to suit load FETs with differing levels of gate charge. Three settings are selectable, by connecting the PWRSEL pin to GND or V_{DRV} or leaving it open (floating). The PWRSEL pin setting is sampled only during startup and is in force until the VDRV pin is power cycled.

If the selected PWRSEL setting is too high compared to the level of load FET $Q_{G(TOT)}$, excess energy is delivered to the secondary, and will be dissipated in the internal regulators, resulting in higher

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package power dissipation than necessary. On the other hand, if the PWRSEL setting is too low, insufficient energy will be transferred, resulting in a drop in the secondary side supply rails (V_{SECP}, V_{SECN}) levels when the device is enabled, and PWM is applied to INx pin(s). Eventually this will cause the V_{SECP} UVLO to trigger. If this happens repeatedly, a higher PWRSEL setting should be selected. Table 4 lists the recommended maximum $Q_{G(TOT)}$ for each PWRSEL setting to assist with choosing the right setting.

PWRSEL Connection	Pulse-width range	$Q_{G(TOT)}$ maximum (nC)
GND	Low	50
Open (floating)	Medium	85
VDRV	High	130

Table 3: PWRSEL vs Qg(max) [AHV85003 + AHV85043 + recommended external transformer]

Power Dissipation and Derating

There are several factors that can contribute to the power dissipated in primary and secondary IC.

These are the power transfer selection (PWRSEL pin configuration), the PWM frequency, the settings of the secondary side power rails (VSECP, VSECN), the gate resistors (series resistor between OUTPU and OUTPD outputs and the gate of the power SiC MOSFET and the load total gate charge $Q_{G(TOT)}$.

System design must ensure that the ICs are operated within their maximum power dissipation safe operating area as a function of ambient temperature. This means that SiC FETS with lower gate charge can be driven to the higher end of the PWM frequency range, subject to package power dissipation. But if the maximum gate charge capability is used, the PWM maximum frequency must be limited, to stay within the package thermal capability.

Applications Information

Typical application

A typical application schematic for the driver chipset is shown in Figure 13. On the low-voltage primary side, the driver is supplied with a single bias supply voltage V_{DRV}, and on the isolated secondary side, no external bias supply is required – only decoupling capacitors are required.

The next sections give more detail on all the various pins and features of the driver.

Bootstrap and charge-pump capacitors

As shown in Figure 13, two external bootstrap decoupling capacitors CBSP and CBSN are required for the AHV85003 to generate floating bias rails for the internal power stage. These capacitors are connected between BSP/TXPP, and BSN/TXPN.

For the AHV85043, an external charge-pump decoupling capacitor CCHP is required to generate a floating bias rail.

Fault Output

The AHV85003 active-low open-drain $\overline{\text{FAULT}}$ pin requires an external pull-up resistor to a suitable rail. This can be any suitable 3.3V or 5V rail, or the $\overline{\text{FAULT}}$ pin can also be pulled up to the V_{DRV} pin. The pull-up resistor value recommendation is 10-100kΩ, for <1mA sink current. The user must be careful to ensure that the pull-up resistor is not too small, so that the $\overline{\text{FAULT}}$ pin does not need to sink excessive current, especially when pulled up to V_{DRV} – this could result in a low-level at the pin during pull-down that exceeds the logic-low V_{IH} at the system controller input.

The Fault Output allows wired-OR connection to multiple drivers.

Enable Input

The EN pin includes an internal 300kΩ pull-down, and an internal de-glitch filter to minimize false toggling due to noise pick-up. It's also recommended to add a low pass filter as indicated in Figure 13 in particularly noisy environments.

The EN pin is rated up to V_{DRV} maximum, so it can be tied high to any system 5V or 3.3V logic rail, or V_{DRV}, to enable the AHV85003 driver.

Both IN+ and IN- input pins have a 150kΩ pull-down (IN+) or pull-up (IN-) resistors to prevent the inputs from floating up if they are left unconnected. Nevertheless, any unused input must be tied low (IN-) or high (IN+) if not used in the application. In noisy environments, a low-pass filter as indicated in Figure 13 is recommended.

PWM Inputs and Interlock Function

The PWM input pins have a 150kΩ pull-down (IN+) to GND and 150kΩ pull-up (IN-) to the internal 3.3V bias voltage, to prevent the inputs from floating if they are left open.

If a single PWM input is used in the application, the unused input must be tied high (IN+) or low (IN-).

The two PWM input pins of the AHV85003 can also be used to provide interlock between the two series switches in a half-bridge leg, to prevent shoot through on that half-bridge leg, that would occur if both low-side and high-side switches were both turned on at the same time or had overlapping turn-on commands.

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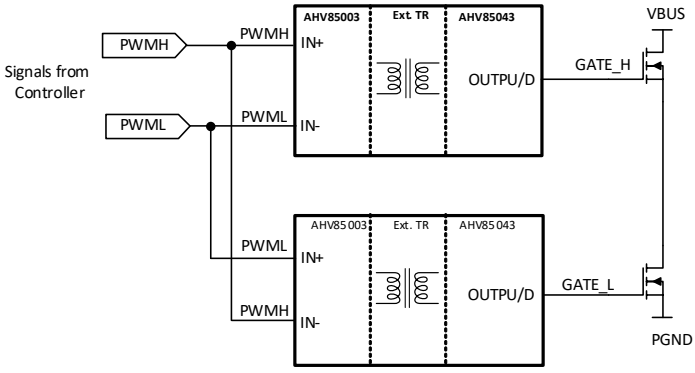

Figure 7: Interlock connection of PWML and PWMH to IN+ and IN- in a half-bridge leg for shoot-through protection [AHV85003 + AHV85043 + recommended external transformer]

As shown in Figure 7, for the low-side switch, connect IN+ to the low-side PWML signal, and connect IN- to the corresponding high-side PWMH signal for the same leg, to get interlock. For the high-side switch in that same leg, the PWM signals are connected similarly, IN+ to PWMH and IN- to PWML.

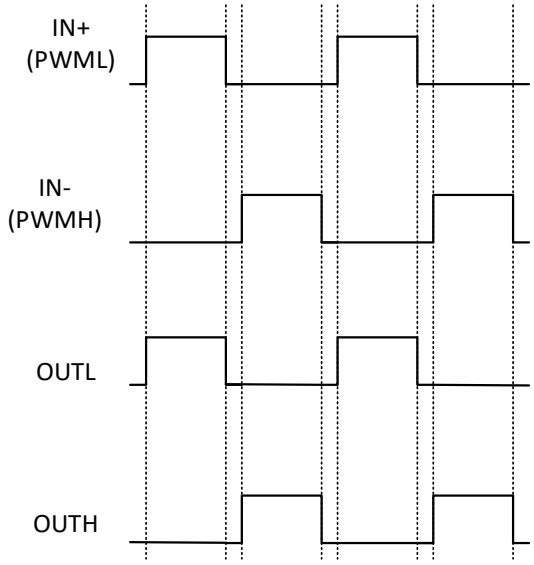

Figure 8: Half-bridge PWML and PWMH signals with dead-time generated at source by PWM controller [AHV85003 + AHV85043 + recommended external transformer]

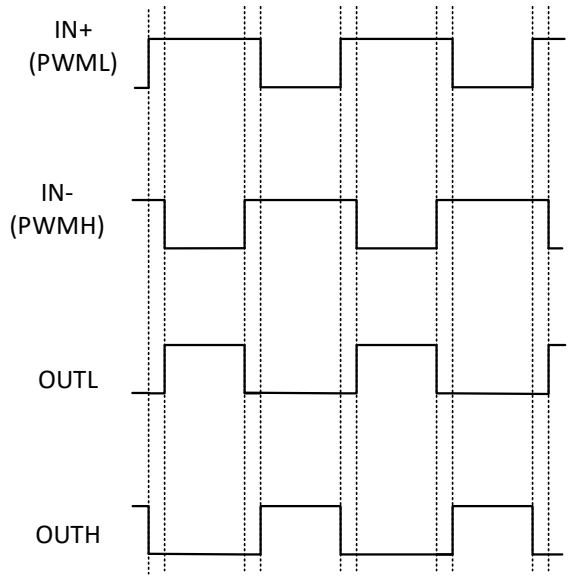

Figure 9: Half-bridge PWML and PWMH signals with deliberate overlap – dead-time generated by interlock connection [AHV85003 + AHV85043 + recommended external transformer]

Examples waveforms are shown in Figure 8 for deadtime generated at source by the PWM controller, and Figure 9 for deadtime control by use of deliberate PWM overlap.

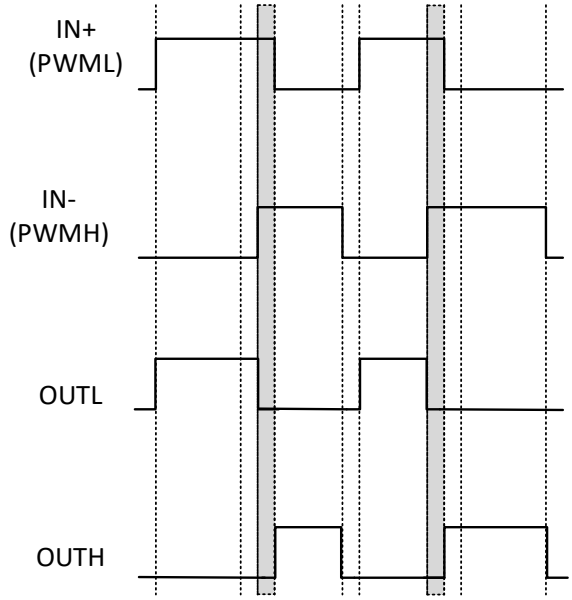

Figure 10: Half-bridge PWML and PWMH signals with erroneous overlap – shoot-through prevented by interlock connection [AHV85003 + AHV85043 + recommended external transformer]

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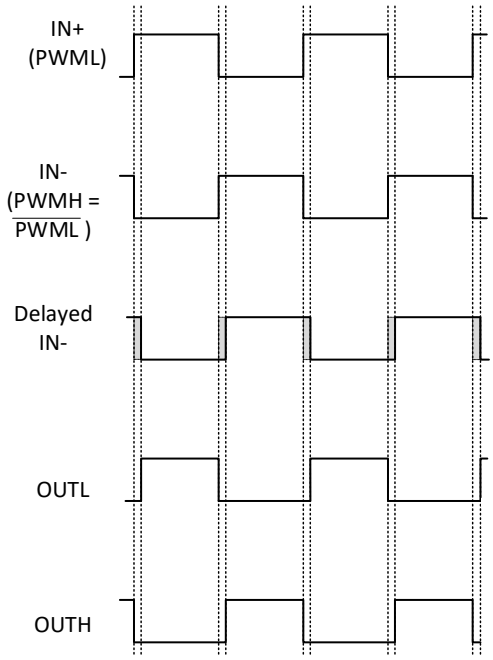

Figure 11: Half-bridge PWML and PWMH (derived from inverted PWML) signals with small RC delay applied to IN-, interlock connection introduces dead-time for shoot-through prevention. [AHV85003 + AHV85043 + recommended external transformer

If required, additional dead-time between low-side and high-side switches in a half-bridge leg can be implemented by placing a small external RC filter on the IN+ and/or IN- pins.

In Figure 11, example waveforms are shown for the generation of PWMH as the inverse of PWML (or vice versa), with virtually no dead-time. By adding a small RC delay at the driver IN- pin (or IN+ pin), and using the interlock connection between low-side and high-side half-bridge drivers, a dead-time is introduced by virtue of the short overlap between IN+ and IN- inputs, which ensures protection against cross-conduction.

Secondary Negative Bias Rails

As shown in Figure 12, the negative bias rail V_{SECN} can be adjusted by suitable choice of external resistor divider R_{nt} and R_{nb} on the VFBN pin.

The values for the external divider resistors can be chosen according to the equation:

$$V_{SECN} = V_{FBN} \cdot \left(1 + \frac{R_{nt}}{R_{nb}}\right)$$

Or

$$R_{nt} = R_{nb} \cdot \left(\frac{V_{SECN}}{V_{FBN}} - 1\right)$$

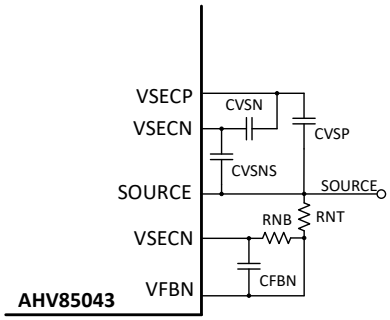

Figure 12: External resistor divider connection to set V_{SECN} regulation level [AHV85043]

Secondary Side Snubbers

The application diagram of Figure 14 shows two snubbers connected between TXSP/VSECN and TXSN/VSECN. The snubbers are required to achieve a higher common-mode transient immunity (CMTI). The values of CSNN/RSNN and CSNP/RSNP are dependent on the desired CMTI level and on the interwinding capacitance of the pulse transformer. In the transformer selection, a transformer with low interwinding capacitance should be selected to obtain high immunity levels to common mode transients.

Refer to the relevant application note for the calculation of the snubbers.

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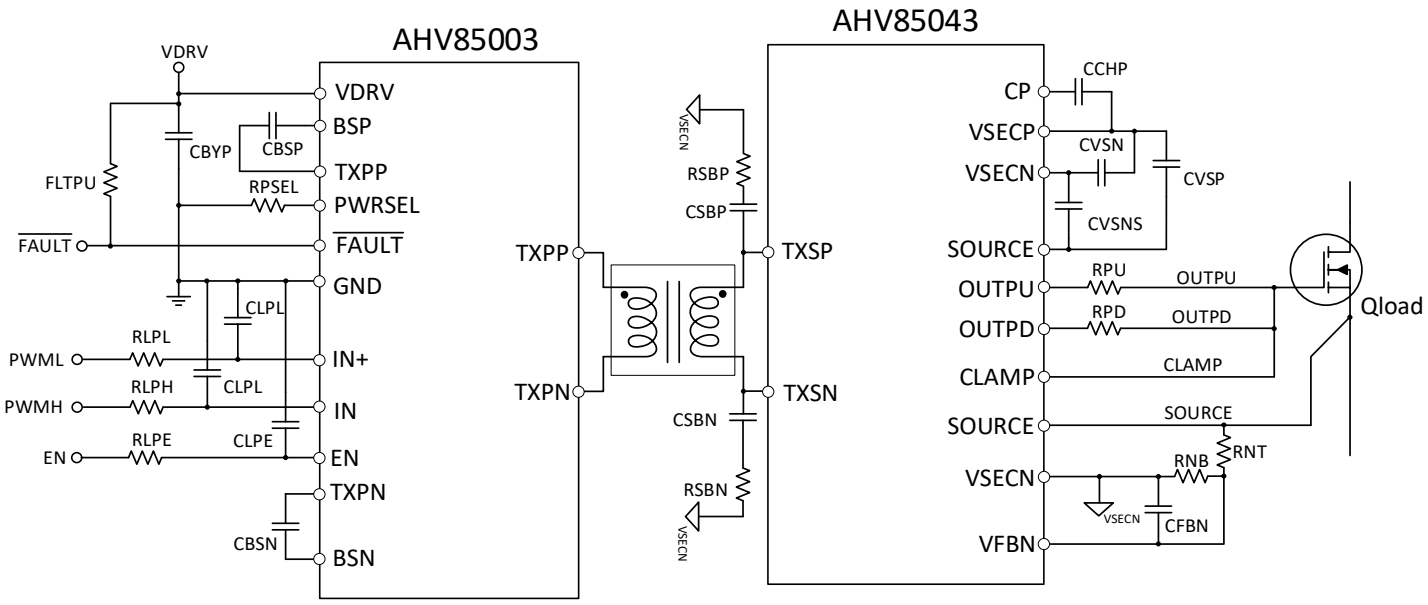

Figure 13: Typical application schematic AHV85003 + AHV85043 + external transformer

Designator	Value	Notes	Designator	Value	Notes
CBSP	22nF, 25V, X7R	Boostrap capacitor	CBSN	22nF, 25V, X7R	Bootstrap capacitor
RPSEL	0Ω	Power Selection (1)	CCHP	22nF, 25V, X7R	Charge pump capacitor
CBYP(2)	1uF, 25V, X7R	Bypass Capacitors x 3	CVSN	470nF, 25V, X7R	
FLTPU	100kΩ	FAULTb pin pull-up	CVSP	470nF, 25V, X7R	
CLPL	100pF	IN- input filter	CVSNS	470nF, 25V, X7R	
RLPL	49.9Ω	IN- input filter	RPU	See Note (3)	
CLPH	100pF	IN+ input filter	RPD	See Note (3)	
RLPH	49.9Ω	IN+ input filter	RNT	See Note (4)	Secondary Negative Rail Voltage Setting
CLPE	100pF	EN (Enable) input filter	RNB	See Note (4)	Secondary Negative Rail Voltage Setting
RLPE	49.9Ω	EN (Enable) input filter	CFBN	22pF, 25V, X7R	
CSNN	See Note (4)	Snubber (negative)	RSNN	See Note (5)	Snubber (negative)
CSNP	See Note (4)	Snubber (positive)	RSNP	See Note (5)	Snubber (positive)

Notes:

1) **Power Selection, this pin should be tied directly to VDRV, GND or left floating to select the three power transfer options. Refer to the relevant section.**
2) **One bypass capacitor should be used at each VDRV pin placed as close as possible to the device.**
3) **Gate Resistors, the value of these resistors is dependent on the system design and should be rated for surge currents**
4) **The ratio of RNT/RNB sets the level of the secondary's negative rail (VSECN).**
5) **The snubbers on the secondary side of the pulse transformer improve the CMTI performances. Please refer to the relevant application note to dimension the snubber capacitor and resistor.**
6) **For PCB layout guidelines please refer to the relevant application note.**

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Table 5 shows the commercially available transformers, tested and approved by Allegro Microsystems. To select and qualify different transformers, refer to application note ANxxxxxx.

Part number	Manufacturer	Isolation rating	Footprint (mm)	Max height (mm)
LTW4638A-P-C05TF	Sunlord	Functional	5 x 3.8	3.2

Table 4: AHV85003/AHV85043 recommended external matching transformers

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Package Information

IC package footprint QFN20 4x4 mm ES package. For additional information https://www.allegromicro.com/en/design-support/packaging

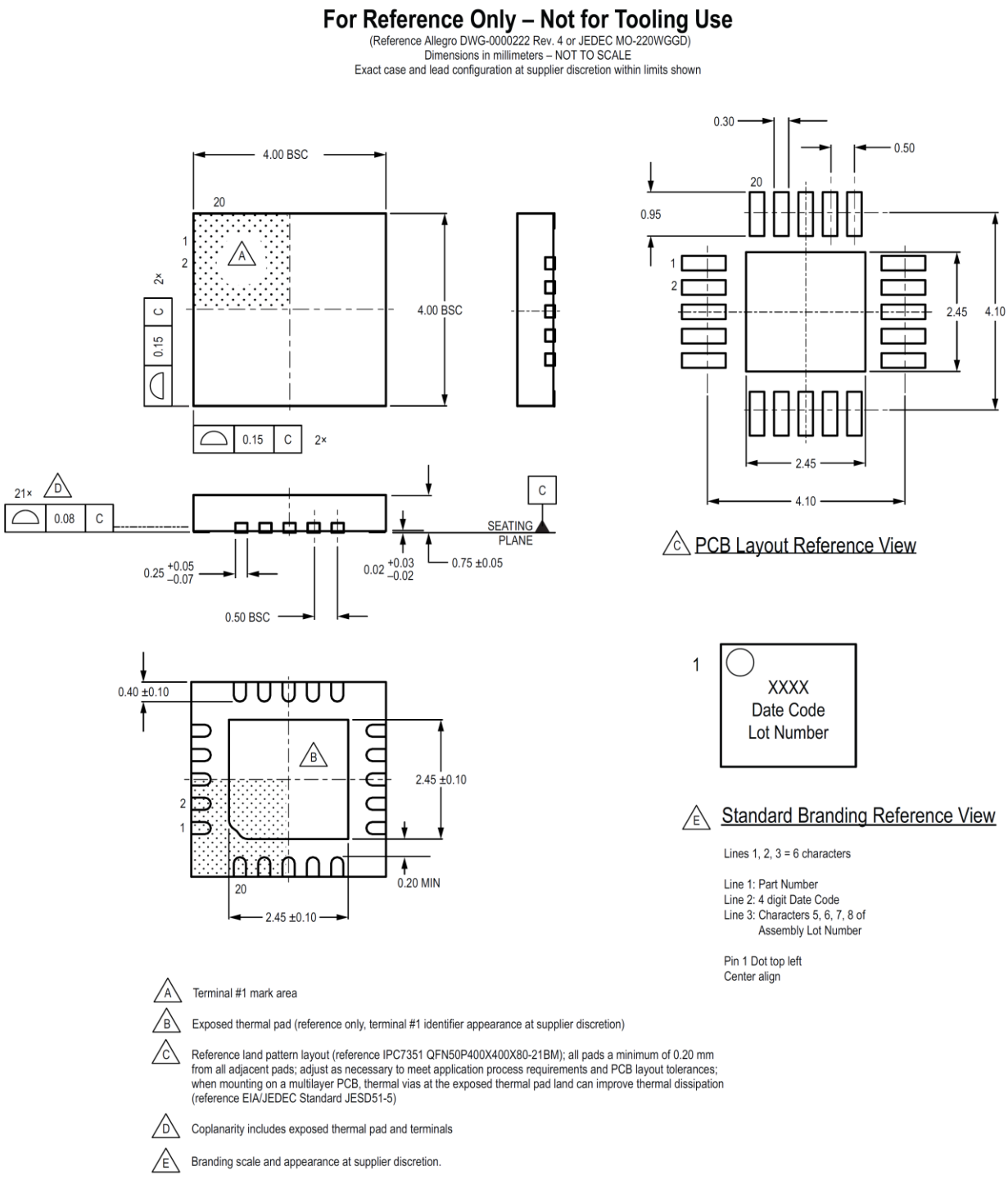

Figure 14: Package outline drawing

REVISION HISTORY

Number	Date	Description
1	9 October 2023	Preliminary QFN Datasheet (derived from AHV85311 rev 5)
2	8 November 2023	Added initial table of external transformer options; updated FAULT feedback description; updated Miller clamp block diagrams; updated timing electrical tables to split out timings for AHV85003 & AHV85043; updated functional descriptions, captions, and diagrams to better capture the separate AHV85003 & AHV85043 functionalities; added details and description of the refresh mechanism.
3	5 April 2024	Clarified that TEST pin must be connected to VSECN when not used; updated rise/fall-time load capacitor test conditions
4	23 April 2025	Reformatting all pages. Included application (schematics and components selection)
5	10 September 2025	Updated to reflect Silicon revision BA.

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