AHV85003 and AHV85043 Chipset

Self-Powered Isolated SiC Driver Chipset with Bipolar Output

Datasheet Addendum: Errata

AFFECTED PARTS

The errata described in this addendum relate to silicon revision BA for the following part numbers:

- AHV85003K15ES
- AHV85003K18ES
- AHV85003K20ES

DESCRIPTION

This addendum adds errata to the general sales datasheet (AHV85003 and AHV85043 Chipset) for this device.

This document describes a known exception to the functional behavior of the AHV85003 IC gate driver.

This document describes the functional deviation, how this deviation might affect the final user system, and the specific condition where device operation deviates from the intended functional profile.

For parameters not listed in this addendum, refer to the general sales datasheet. In the event of a conflict between this addendum and the general sales datasheet, this addendum takes precedence.

Introduction

In switching converter systems with multiswitch topologies (e.g., interleaved topologies, multileg power-factor correction [PFC]), common-mode noise (dV/dt) generated by one switch can affect another device in the system and thereby create distortion on its pulse-width modulation input (PWM_{IN}) signal.

If a dV/dt event in the system (>20 V/ns) aligns with a very-precise timing of an expected PWM transition of another device, this device might miss a turn-on or turn-off command.

Specifically, a noise-related glitch can truncate the internal transformer pulse, causing the secondary-side gate output (V_{GS}) to remain in the high state while the PWM input is in the low state. This can lead to a shoot-through event in the system lasting 3 to 4 µs.

Root Cause

- **System Level:** High dV/dt edges from adjacent switches couple common-mode current into the PWM input path of the affected driver, creating distortion on the input signal.
- **Silicon Level:** The noise glitch at the input triggers a change of polarity in the internal transformer pulse generator. This polarity change causes the actual PWM to transition and the transmission pulse is truncated. The secondary side does not recognize the state change because it fails to see a transformer pulse of sufficient magnitude/duration.

Application Impact

- **Risk:** In this condition, V_{GS} does not track with the expected transition of the PWM input. As a result, the potential for leg shoot-through exists for 3 to 4 µs.
- **Trigger Condition:** The issue occurs only when both: 1) dV/dt > 20 V/ns; and 2) the offender dV/dt perfectly aligns (for a duration of approximately tens of ns) with the expected PWM transition of another power switch.
- **Topology Risk**
  - **Low Risk—Best Fit:** Single switch converters, single half-bridge converters, static switches (SSCB, SSR)
  - **High Risk—Avoid:** Interleaved topologies, multileg converters
- For questions about topology assessment, contact Allegro MicroSystems.

Workarounds and Mitigation (Current Silicon Revision)

IMPORTANT: To ensure reliable operation with current silicon, implementation of the following measures is required:

- **External Filtering:** Place a mandatory resistor-capacitor (RC) filter on any input pins that are used in the application (i.e., EN, IN+, IN–). Ensure that the RC filter uses a 50 Ω resistor, a 330 pF capacitor, and a 15 pF capacitor (in parallel, to handle higher frequencies).
- **Slew Rate Control:** Limit the switching node dV/dt to ≤ 10 V/ns to ensure sufficient safety margin.
- **Layout:** Adhere strictly to existing layout guidelines.

Resolution Plan

Allegro is implementing a silicon-level resolution that adds a more-robust input filter to ignore noise glitches.

- **Implementation:** Improved deglitching block at the input
- **Revised Samples Availability:** Q3 FY27
- **Revised RTM:** Q4 FY27

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Revision History

Number	Date	Description
–	July 21, 2026	Initial release to Allegro website

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