

12 V Automotive Three-Phase BLDC Gate Driver with Integrated Inline Current Sense Over SPI

FEATURES AND BENEFITS

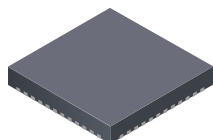
- Three-phase bridge MOSFET driver for 12 V systems
- Bootstrap gate drive for N-channel MOSFETs
- Cross-conduction protection with adjustable dead-time
- Charge pump for low supply voltage operation down to 4.5 V
- Operation at any PWM duty cycle up to and including 100%
- Strong VREG charge pump to support up to 25 mA average gate switching current, enables driving 200 nC external MOSFETs at 20 kHz for 12 V gate driver
- 4.5 to 42 V supply voltage operating range for 12 V systems
- Two programmable inline current sense amplifiers with instantaneous and average current reading through SPI
- Safe SPI-compatible serial interface for functional safety
- Bridge control by direct logic inputs or serial interface
- Battery-disconnect function
- Extensive programmable diagnostics
- Configurable diagnostics verification
- Automotive AEC-Q100 qualified
- ASIL Compliant: ASIL D safety element out-of-context developed per ISO 26262



APPLICATIONS

- 12 V automotive motor control applications:
 - Electric power steering system
 - Electro-mechanical brake system
 - Steer-by-wire system
 - Heating, cooling and pumping systems

PACKAGE



48-pin QFN
with exposed thermal pad
and wettable flank
(suffix EV)

Not to scale

DESCRIPTION

The AMD89106 is a 12 V gate driver that is capable of driving N-channel MOSFETs connected in a three-phase bridge arrangement. The device is specifically designed for 12 V automotive applications with high-power BLDC motors.

The device integrates two current sense amplifiers for inline current sensing with digital current readback through SPI. Both instantaneous and average current measurements are supported using SPI in all variants of the device. Inline current measurement has several advantages: providing the most accurate representation of the current in the motor, increasing diagnostics robustness, reducing errors and timing sensitivity during current sampling, and simplifying the control loop and PWM generation algorithms to enable precision and high-efficiency BLDC motor control.

VREG can be regulated as an output in the AMD89106. Gate drive voltage and strength are programmable for design flexibility and to help improve the EMC performance of the system while balancing system efficiency. A bootstrap capacitor is used to provide the above-battery supply required for N-channel MOSFETs with an additional above-battery charge pump to ensure that the bootstrap capacitors remain charged when held in the on-state for long periods of time at or near 100% duty cycle.

Full direct control is provided in the device over all six power MOSFETs in a three-phase bridge, allowing motors to be driven with block commutation or sinusoidal excitation including field-oriented control. The AMD89106 device supports battery disconnect by integrating a gate drive for an external battery-disconnect MOSFET. This significantly reduces the application footprint and the bill of materials. Integrated diagnostics provide indication of multiple internal faults, monitor system faults, and external power bridge faults, that can be configured to protect the external power MOSFETs from most short-circuit conditions. For safety-critical systems, the integrated diagnostic operation can be verified using the serial interface. The serial interface can be used to modify configurable settings and readback detailed diagnostic information.

The device is available in a 48-pin QFN package (suffix EV), with exposed thermal pad and wettable flank. The package is lead (Pb) free with 100% matte-tin lead frame plating.

TYPICAL APPLICATION

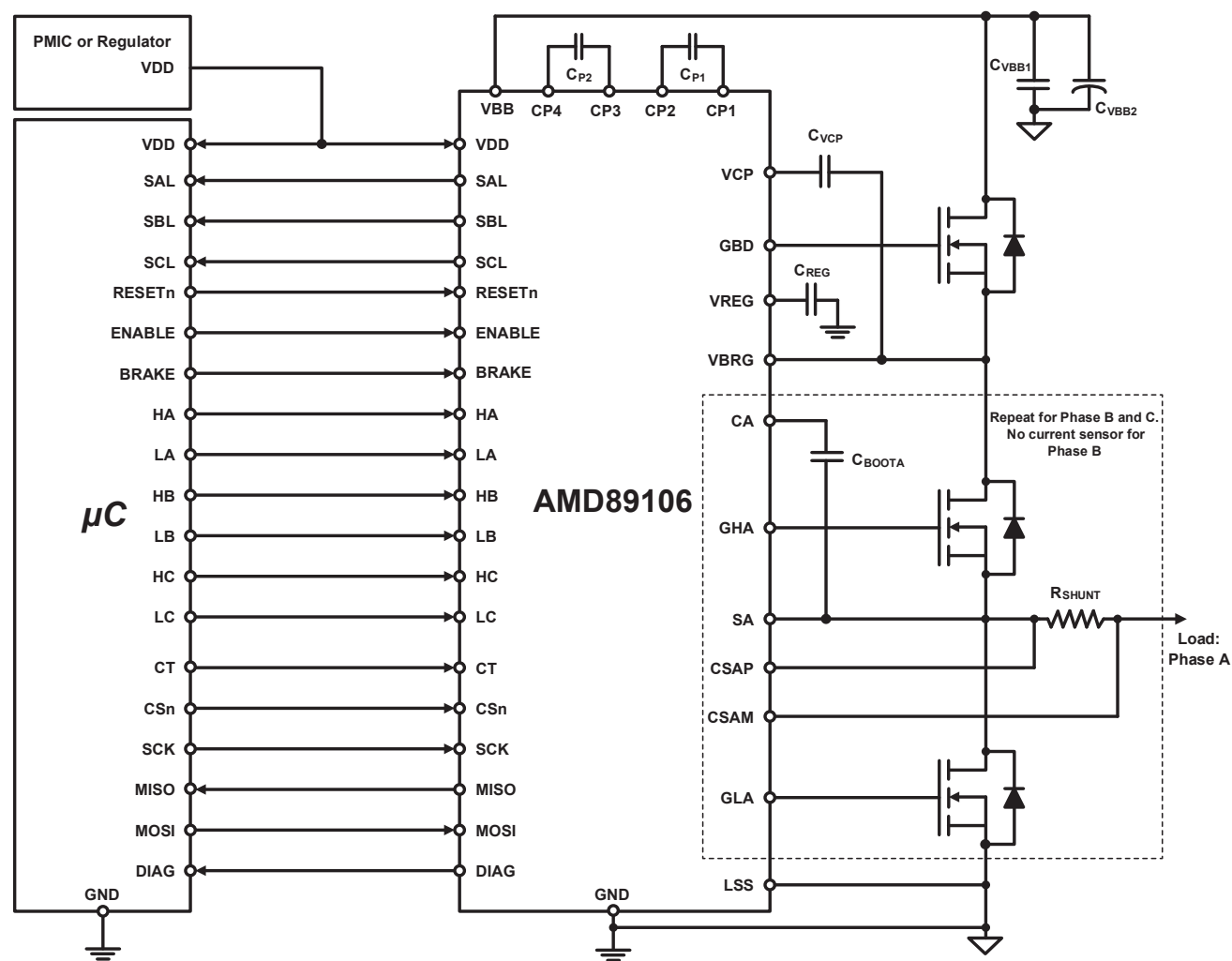


Figure 1: Typical Application

PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference DWG-0000378, Rev. 7)

Dimensions in millimeters

NOT TO SCALE

Exact case and lead configuration at supplier discretion within limits shown

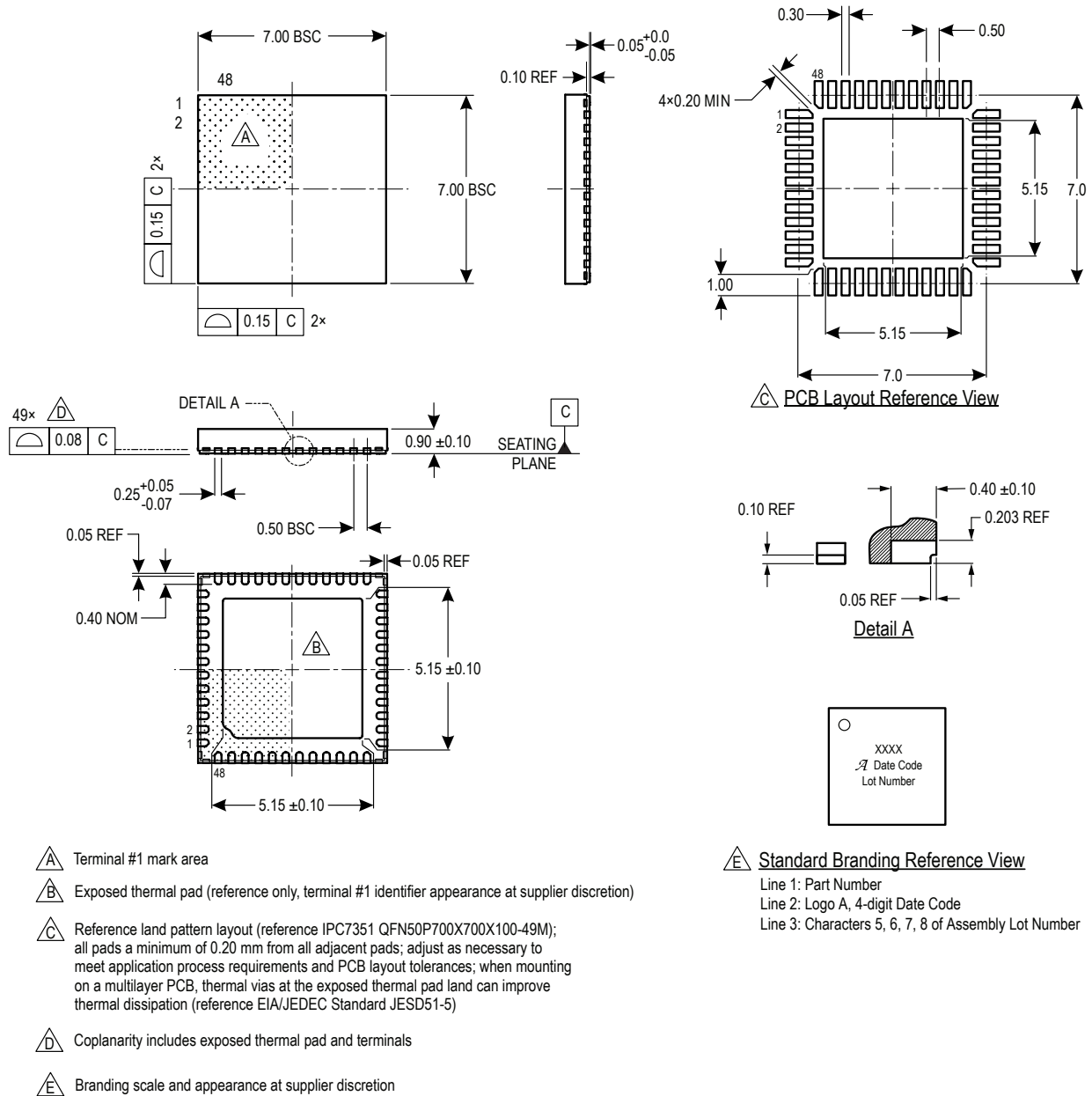


Figure 2: EV Package, 48-Pin QFN with Exposed Thermal Pad and Wettable Flank

REVISION HISTORY

Number	Date	Description
–	September 15, 2026	Initial release of short-form to web

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