The APS11450 three-wire planar Hall-effect sensor integrated circuits (ICs) were developed in accordance with ISO 26262:2011 as a hardware safety element out of context with ASIL B capability (pending assessment) for use in automotive safety-related systems when integrated and used in the manner prescribed in the applicable safety manual and datasheet. The enhanced three-wire interface provides interconnect open/short diagnostics and a fault state to communicate diagnostic information while maintaining compatibility with legacy three-wire systems. The continuous background diagnostics are transparent to the host system and result in a reduced fault tolerant time.

The APS11450 product options include magnetic switch points, temperature coefficient, hysteresis, and response to north or south magnetic fields (unipolar switch) or both (bipolar latch or omnipolar switch). The response can be matched to SmCo, NdFeB, or low-cost ferrite magnets. For situations where a functionally equivalent three-wire latch device is preferred, refer to the APS12450.

**TYPICAL APPLICATIONS**

- Automotive and industrial safety systems
- Limit switches and safety interlocks
- Sun roof/convertible top/tailgate/liftgate position
- Brake/clutch pedals
- Transmission pawl, fork, piston, valve, gear position detection
- Door locks/latches
- User controls

---

**DESCRIPTION**

The APS11450 three-wire planar Hall-effect sensor integrated circuits (ICs) were developed in accordance with ISO 26262:2011 as a hardware safety element out of context with ASIL B capability (pending assessment) for use in automotive safety-related systems when integrated and used in the manner prescribed in the applicable safety manual and datasheet. The enhanced three-wire interface provides interconnect open/short diagnostics and a fault state to communicate diagnostic information while maintaining compatibility with legacy three-wire systems. The continuous background diagnostics are transparent to the host system and result in a reduced fault tolerant time.

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*Continued on the next page...*
APS11450 Three-Wire Hall-Effect Switch with Advanced Diagnostics

DESCRIPTION (continued)
APS11450 sensors are engineered to operate in the harshest environments with minimal external components. They are qualified beyond the requirements of AEC-Q100 Grade 0 and will survive extended operation at 175°C junction temperature.

These monolithic ICs include on-chip reverse-battery protection, overvoltage protection (e.g., 40 V load dump), ESD protection, overtemperature detection, and an internal voltage regulator for operation directly from an automotive battery bus. These integrated features reduce the end-product bill-of-materials (BOM) and assembly cost.

Package options include industry-standard surface-mount SOT (LH) and through-hole SIP (UA) packages. Both packages are RoHS-compliant and lead (Pb) free with 100% matte-tin-plated leadframes.

---

SELECTION GUIDE [1]

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package</th>
<th>Packing</th>
<th>Output Polarity (B &gt; B_{OP})</th>
<th>Temperature Coefficient</th>
<th>Magnetic Operate Point, B_{OP} (typ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>APS11450LLHALX-0SLA</td>
<td>3-pin SOT23W surface mount</td>
<td>13-in. reel, 10,000 pieces/reel</td>
<td>Low</td>
<td>0%/°C</td>
<td>35 G</td>
</tr>
<tr>
<td>APS11450LLHALT-0SLA</td>
<td>3-pin SOT23W surface mount</td>
<td>7-in. reel, 3000 pieces/reel</td>
<td>Low</td>
<td>–0.12%/°C</td>
<td>180 G</td>
</tr>
<tr>
<td>APS11450LUAA-0SLA</td>
<td>3-pin SIP through-hole</td>
<td>bulk, 500 pieces/bag</td>
<td>Low</td>
<td>–0.12%/°C</td>
<td>280 G</td>
</tr>
<tr>
<td>APS11450LLHALX-2SLC</td>
<td>3-pin SOT23W surface mount</td>
<td>13-in. reel, 10,000 pieces/reel</td>
<td>Low</td>
<td>–0.2%/°C</td>
<td>280 G</td>
</tr>
<tr>
<td>APS11450LLHALT-2SLC</td>
<td>3-pin SOT23W surface mount</td>
<td>7-in. reel, 3000 pieces/reel</td>
<td>Low</td>
<td>–0.2%/°C</td>
<td>280 G</td>
</tr>
<tr>
<td>APS11450LLHALX-3SLC</td>
<td>3-pin SOT23W surface mount</td>
<td>13-in. reel, 10,000 pieces/reel</td>
<td>Low</td>
<td>–0.2%/°C</td>
<td>280 G</td>
</tr>
<tr>
<td>APS11450LLHALT-3SLC</td>
<td>3-pin SOT23W surface mount</td>
<td>7-in. reel, 3000 pieces/reel</td>
<td>Low</td>
<td>–0.2%/°C</td>
<td>280 G</td>
</tr>
<tr>
<td>APS11450LLHALX-3SLD</td>
<td>3-pin SOT23W surface mount</td>
<td>13-in. reel, 10,000 pieces/reel</td>
<td>Low</td>
<td>–0.2%/°C</td>
<td>280 G</td>
</tr>
<tr>
<td>APS11450LLHALT-3SLD</td>
<td>3-pin SOT23W surface mount</td>
<td>7-in. reel, 3000 pieces/reel</td>
<td>Low</td>
<td>–0.2%/°C</td>
<td>280 G</td>
</tr>
</tbody>
</table>

### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Notes</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage [2]</td>
<td>$V_{\text{DC}}$</td>
<td></td>
<td>35</td>
<td>V</td>
</tr>
<tr>
<td>Reverse Supply Voltage</td>
<td>$V_{\text{RCC}}$</td>
<td></td>
<td>–30</td>
<td>V</td>
</tr>
<tr>
<td>Forward Output Voltage</td>
<td>$V_{\text{OUT}}$</td>
<td></td>
<td>30</td>
<td>V</td>
</tr>
<tr>
<td>Reverse Output Voltage</td>
<td>$V_{\text{ROUT}}$</td>
<td></td>
<td>–0.3</td>
<td>V</td>
</tr>
<tr>
<td>Output Current Sink</td>
<td>$I_{\text{OUT(SINK)}}$</td>
<td>VCC to VOUT</td>
<td>12</td>
<td>mA</td>
</tr>
<tr>
<td>Maximum Junction Temperature</td>
<td>$T_{J(\text{MAX})}$</td>
<td>For 500 hours</td>
<td>165</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>$T_{\text{stg}}$</td>
<td></td>
<td>–65 to 170</td>
<td>°C</td>
</tr>
</tbody>
</table>

[2] This rating does not apply to extremely short voltage transients such as load dump and/or ESD. Those events have individual ratings specific to the respective transient voltage event. Contact your local field applications engineer for information on EMC test results.
PINOUT DIAGRAMS AND TERMINAL LIST

LH Package, 3-Pin SOT23W Pinout

UA Package, 3-Pin SIP Pinout

Terminal List Table

<table>
<thead>
<tr>
<th>Name</th>
<th>Pin Number</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>VOUT</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>GND</td>
<td>3</td>
<td>2</td>
</tr>
</tbody>
</table>

Supply voltage  
Output  
Ground
## OPERATING CHARACTERISTICS:

Valid over full operating voltage and ambient temperature ranges for $T_J < T_J(max)$, unless otherwise specified.

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>SUPPLY AND STARTUP</td>
<td>$V_{CC}$</td>
<td>Operating, $T_J &lt; 165^\circ C$</td>
<td>3.0</td>
<td>–</td>
<td>30</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$I_{CC}$</td>
<td>–</td>
<td>–</td>
<td>4.5</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$t_{on}$</td>
<td>$V_{CC} &gt; V_{CC}(min)$, $B &lt; B_{RP}(min) - 10 , G$,$B &gt; B_{OP}(max) + 10 , G$</td>
<td>–</td>
<td>–</td>
<td>150</td>
<td>μs</td>
</tr>
<tr>
<td></td>
<td>POS</td>
<td>$t &lt; t_{on}(max)$</td>
<td>$V_{OUT(FAULT)}$</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>OUTPUT RISE TIME</td>
<td>$t_{RISE}$</td>
<td>–</td>
<td>2</td>
<td>4</td>
<td>15</td>
<td>μs</td>
</tr>
<tr>
<td>OUTPUT FALL TIME</td>
<td>$t_{FALL}$</td>
<td>–</td>
<td>2</td>
<td>4</td>
<td>15</td>
<td>μs</td>
</tr>
<tr>
<td>OUTPUT OFF VOLTAGE</td>
<td>$V_{OUT(LOW)}$</td>
<td>Output ratio metric to $V_{PU}$; $V_{PU} = V_{CC}$, $\tau &lt; 3 , μs$, $I_{OUT} &lt; 12 , mA$</td>
<td>10</td>
<td>20</td>
<td>30</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td>$V_{OUT(HIGH)}$</td>
<td>Overshoot percentage relative to $V_{PU}$ (see Figure 8); $V_{PU} = V_{CC}$, $\tau &lt; 3 , μs$, $I_{OUT} &lt; 12 , mA$</td>
<td>70</td>
<td>80</td>
<td>90</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td>$t_{VOUT(H)OVER}$</td>
<td>Duration of output voltage overshoot ($V_{OUT(H)OVER}$)</td>
<td>–</td>
<td>2</td>
<td>–</td>
<td>%</td>
</tr>
</tbody>
</table>

## TRANSIENT PROTECTION CHARACTERISTICS:

Valid for $T_A = 25^\circ C$ and $C_{BYP} = 0.1 \, μF$, unless otherwise specified.

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>PROTECTION</td>
<td>$V_Z$</td>
<td>$I_{CC}(max) + 3 , mA$</td>
<td>35</td>
<td>–</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>REVERSE SUPPLY ZENER CLAMP VOLTAGE</td>
<td>$V_{RCC}$</td>
<td>$I_{CC} = -1 , mA$</td>
<td>–</td>
<td>–</td>
<td>–30</td>
<td>V</td>
</tr>
<tr>
<td>REVERSE SUPPLY CURRENT</td>
<td>$I_{RCC}$</td>
<td>$V_{RCC} = -30 , V$</td>
<td>–</td>
<td>–</td>
<td>–5</td>
<td>mA</td>
</tr>
</tbody>
</table>

[1] Typical data is at $T_A = 25^\circ C$ and $V_{CC} = 12 \, V$ and is for design information only.

[2] $V_{CC}$ represents the voltage between the VCC pin and the GND pin.

[3] Power-On Time ($t_{ON}$) is measured from $V_{CC} = V_{CC}(min)$ to 50% of the output transition from $V_{PU}$ to final value. Adding a bypass capacitor will increase Power-On Time.

[4] The overshoot specification pertains only to conditions where the overshoot is greater than the $V_{OUT(H)OVER}$ specification.

[5] $\tau$ is the time constant of the RC circuit; $\tau = R_{PU} \times C_{OUT}$.

[6] The diagnostics fault retry repeats continuously until a fault condition is no longer observed. See Diagnostics Mode Operation section for details.
MAGNETIC CHARACTERISTICS: Valid over full operating voltage and ambient temperature ranges for $T_J < T_J(\text{max})$, unless otherwise specified

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Sensitivity Temperature Coefficient</td>
<td>$T_{C_{SENS}}$</td>
<td>Relative to sensitivity at 25°C</td>
<td>(A) Flat</td>
<td>–</td>
<td>0</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(B) SmCo</td>
<td>–</td>
<td>–0.035</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(C) NdFeB</td>
<td>–</td>
<td>–0.12</td>
<td>–</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(D) Ferrite</td>
<td>–</td>
<td>–0.2</td>
<td>–</td>
</tr>
<tr>
<td>Analog Signal Bandwidth</td>
<td>$f_{(3\text{dB})}$</td>
<td></td>
<td></td>
<td>–</td>
<td>10</td>
<td>–</td>
</tr>
</tbody>
</table>

| Operate Point | $B_{OP}$ | APS11450-0SxA | $T_A = –40°C$ | 128 | 184 | 240 | G |
| | | APS11450-2SxC | $T_A = 25°C$ | 125 | 180 | 235 | G |
| | | APS11450-3SxC | $T_A = 150°C$ | 106 | 153 | 200 | G |
| | | APS11450-3SxD | $T_A = –40°C$ | 230 | 286 | 342 | G |
| | | APS11450-3SxC | $T_A = 25°C$ | 230 | 280 | 335 | G |
| | | APS11450-3SxC | $T_A = 150°C$ | 190 | 235 | 280 | G |
| | | APS11450-3SxD | $T_A = –40°C$ | 260 | 316 | 379 | G |
| | | APS11450-3SxD | $T_A = 25°C$ | 230 | 280 | 335 | G |
| | | APS11450-3SxD | $T_A = 150°C$ | 173 | 210 | 251 | G |

| Release Point | $B_{RP}$ | APS11450-0SxA | $T_A = –40°C$ | 5 | 25 | – | G |
| | | APS11450-2SxC | $T_A = 25°C$ | 72 | 128 | 184 | G |
| | | APS11450-2SxC | $T_A = 150°C$ | 70 | 125 | 180 | G |
| | | APS11450-3SxC | $T_A = –40°C$ | 59 | 105 | 150 | G |
| | | APS11450-3SxC | $T_A = 25°C$ | 174 | 230 | 286 | G |
| | | APS11450-3SxC | $T_A = 150°C$ | 170 | 225 | 280 | G |
| | | APS11450-3SxD | $T_A = –40°C$ | 143 | 190 | 235 | G |
| | | APS11450-3SxD | $T_A = 25°C$ | 128 | 169 | 210 | G |

| Hysteresis | $B_{HYS}$ | APS11450-0SxA | – | 10 | 25 | G |
| | | APS11450-2SxC, APS11450-3SxC | 40 | 55 | 70 | G |
| | | APS11450-3SxD | 25 | 55 | 75 | G |

[1] Typical data is at $T_A = 25°C$ and $V_{CC} = 12$ V, unless otherwise noted; for design information only.
[2] 1 G (gauss) = 0.1 mT (millitesla).

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package Thermal Resistance</td>
<td>$R_{JA}$</td>
<td>Package LH, on 1-layer PCB based on JEDEC standard</td>
<td>228</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Package LH, on 2-layer PCB with 0.463 in.² of copper area each side</td>
<td>110</td>
<td>°C/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Package UA, on 1-layer PCB with copper limited to solder pads</td>
<td>165</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

*Additional thermal information available on the Allegro website.
CHARACTERISTIC PERFORMANCE DATA

$V_{OUT(HIGH)}$ vs. $T_A$

$V_{OUT(HIGH)}$ vs. $V_{CC}$

$V_{OUT(LOW)}$ vs. $T_A$

$V_{OUT(LOW)}$ vs. $V_{CC}$

$t_{DIAG}$ vs. $T_A$

$t_{DIAG}$ vs. $V_{CC}$
CHARACTERISTIC PERFORMANCE DATA (continued)

- **I_{CC} vs. T_A**
  - Supply Current, I_{CC} (mA)
  - Ambient Temperature, T_A (°C)
  - V_{CC} (V)
  - Different lines represent different V_{CC} values:
    - 3 V
    - 12 V
    - 24 V
    - 35 V

- **I_{CC} vs. V_{CC}**
  - Supply Current, I_{CC} (mA)
  - Supply Voltage, V_{CC} (V)
  - Ambient Temperature, T_A (°C)
  - Different lines represent different T_A values:
    - 0°C
    - 40°C
    - 75°C
    - 150°C

- **t_{on} vs. T_A**
  - Power-on Time, t_{on} (µs)
  - Ambient Temperature, T_A (°C)

- **t_{RISE} & t_{FALL} vs. T_A**
  - Rise & Fall Time (µs)
  - Ambient Temperature, T_A (°C)
CHARACTERISTIC PERFORMANCE DATA
APS11450–0SxA

- $B_{DIP(A)}$ vs. $T_A$
- $B_{DIP(A)}$ vs. $V_{CC}$
- $B_{HYS(A)}$ vs. $T_A$
- $B_{HYS(A)}$ vs. $V_{CC}$
CHARACTERISTIC PERFORMANCE DATA
APS11450–2SxC

B_{OP(2S_C)} vs. T_A

B_{OP(2S_C)} vs. V_{CC}

B_{RP(2S_C)} vs. T_A

B_{RP(2S_C)} vs. V_{CC}

B_{HYS(2S_C)} vs. T_A

B_{HYS(2S_C)} vs. V_{CC}
CHARACTERISTIC PERFORMANCE DATA

APS11450–3SxC

$B_{OP}(3S_C)$ vs. $T_A$

$B_{OP}(3S_C)$ vs. $V_{CC}$

$B_{RP}(3S_C)$ vs. $T_A$

$B_{RP}(3S_C)$ vs. $V_{CC}$

$B_{HYS}(3S_C)$ vs. $T_A$

$B_{HYS}(3S_C)$ vs. $V_{CC}$
CHARACTERISTIC PERFORMANCE DATA
APS11450-3SxD

B_{OP(3S_D)} vs. T_A

B_{OP(3S_D)} vs. V_CC

B_{OP(3S_D)} vs. T_A

B_{OP(3S_D)} vs. V_CC

B_{RPHYS(3S_D)} vs. T_A

B_{RPHYS(3S_D)} vs. V_CC

B_{OPHYS(3S_D)} vs. T_A

B_{OPHYS(3S_D)} vs. V_CC

B_{RPHYS(3S_D)} vs. T_A

B_{RPHYS(3S_D)} vs. V_CC

B_{RPHYS(3S_D)} vs. T_A

B_{RPHYS(3S_D)} vs. V_CC

B_{RPHYS(3S_D)} vs. T_A

B_{RPHYS(3S_D)} vs. V_CC
FUNCTIONAL DESCRIPTION

Operation

The output of these devices switches when a magnetic field perpendicular to the Hall-effect sensor exceeds the operate point threshold ($B_{OP}$). When the magnetic field is reduced below the release point ($B_{RP}$), the device output switches to the alternate state. The output state (polarity) and magnetic field polarity depends on the selected device options.

For unipolar south, an increasing south field is required; likewise for unipolar north, an increasing north field is required to exceed $B_{OP}$. The output state is a configuration option. In omnipolar mode, the device will switch on and off with either magnetic polarities, while latching will require both polarities.

The difference between operate ($B_{OP}$) and release ($B_{RP}$) points is the hysteresis ($B_{HYS}$). Hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise. The user can program the desired hysteresis level.

Figure 1 shows the output switching behavior relative to increasing and decreasing magnetic field. On the horizontal axis, the B+ direction indicates increasing south polarity magnetic field strength. Figure 2 shows the sensing orientation of the magnetic field, relative to the device package.

The APS11450 Hall-effect switch can be configured to respond to a north or south magnetic field, including both unipolar and omnipolar configurations, as well as the output polarity.

Figure 1 shows the potential unipolar and omnipolar options and output polarity options of the APS11450 that can be configured. The direction of the applied magnetic field is perpendicular to the branded face of the APS11450 (see Figure 2).
Figure 1: Hall switch magnetic and output polarity options
B- indicates increasing north polarity magnetic field strength, and B+ indicates increasing south polarity magnetic field strength.

Figure 2: Magnetic Sensing Orientations
APS11450 LH (Panel A), APS11450 UA (Panel B)
The APS11450 was developed in accordance with ISO 26262:2011 as a hardware safety element out of context with ASIL B capability (pending assessment) for use in automotive safety-related systems when integrated and used in the manner prescribed in the applicable safety manual and datasheet.

**Diagnostics Mode Operation**

The APS11450 features a proprietary diagnostics routine that meets ASIL B safety requirements (pending assessment). This internal diagnostics routine continuously runs in the background, monitoring all key subsystems of the IC. These subsystems are shown in Table 1 and Figure 3. The diagnostic scheme runs at high speed and provides minimal impact on device performance. Signal path diagnostics are injected and measured in less than 2 μs, while all other diagnostics are running in real time in the background. The Hall element biasing circuit and voltage regulator are checked for valid operation, and the digital and non-volatile memory blocks are checked for valid device configuration.

The signal path monitoring system verifies two internal state transitions (B_{OP} and B_{RP} within limits) under normal operation. In cases when these output transitions do not occur, or if another internal fault is detected, the output will go to the fault state (see “Three-Wire Diagnostic Output” section).

In the event of an internal fault, the device will continuously run the diagnostics routine every 2 ms (t_{DIAGF}). The periodic recovery attempt sequence allows the device to continually check for the presence of a fault and return to normal operation if the fault condition clears.

In the case where the fault is no longer present, the output will resume normal operation. However, if the fault is persistent, the device will not exit fault mode and the output voltage will continue to be V_{OUT(FAULT)}.

When a system rating higher than ASIL B is required, additional external safety measures may be employed (e.g., sensor redundancy and rationality checks, etc.). Refer to the device safety manual for additional details about the diagnostics.

**Table 1: Diagnostics Coverage**

<table>
<thead>
<tr>
<th>Feature</th>
<th>Coverage</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Hall plate</td>
<td>Connectivity and biasing of Hall plate</td>
</tr>
<tr>
<td>2 Signal path</td>
<td>Signal path and Schmitt trigger</td>
</tr>
<tr>
<td>3 Voltage regulator</td>
<td>Regulator voltage for normal operation</td>
</tr>
<tr>
<td>4 Digital subsystem</td>
<td>Digital subsystem and non-volatile memory</td>
</tr>
<tr>
<td>5 Entire system</td>
<td>Overtemperature and redundancies for single point failures</td>
</tr>
<tr>
<td>6 Output</td>
<td>Output verified through valid regulations states (external monitor)</td>
</tr>
</tbody>
</table>

**Figure 3: Diagnostics Coverage Block Diagram**
Power-On Behavior

During Power-on, the output voltage is in the fault state ($V_{\text{OUT (FAULT)}}$), which is the pull-up voltage ($V_{\text{PU}}$), until the device is ready to respond appropriately to the input magnetic field ($t > t_{\text{ON}}$). If the device powers-on with the field within the hysteresis band, the output will switch from $V_{\text{OUT (FAULT)}}$ to the off state ($V_{\text{OUT (HIGH)}}$) with standard output polarity as shown in Figure 4. For inverted output polarity operation, the output will switch from $V_{\text{OUT (FAULT)}}$ to $V_{\text{OUT (LOW)}}$ (not shown).

Temperature Coefficient and Magnet Selection

The APS11450 allows the user to select the magnetic temperature coefficient to compensate for drifts of SmCo, NdFeB, and ferrite magnets over temperature, as indicated in the Magnetic Characteristics specifications table. This compensation improves the magnetic system performance over the entire temperature range. For example, the magnetic field strength from NdFeB decreases as the temperature increases from 25°C to 150°C. This lower magnetic field strength means that a lower switching threshold is required to maintain switching at the same distance from the magnet to the sensor. Correspondingly, higher switching thresholds are required at cold temperatures, as low as –40°C, due to the higher magnetic field strength from the NdFeB magnet. The APS11450 compensates the switching thresholds over temperature as described above. It is recommended that system designers evaluate their magnetic circuit over the expected operating temperature range to ensure the magnetic switching requirements are met.

A sample calculation is provided in the "Applications Information" section.
Three-Wire Diagnostic Output

Three-wire diagnostic output enables the user to identify various fault conditions external to the IC, in addition to the internal fault detection. The output low (V_{OUT(LOW)}) and high (V_{OUT(HIGH)}) states are ratiometric to the pull-up voltage, with low and high states being 20% and 80% respectively. For example, a V_{CC} and V_{PULL-UP} of 5 V, the output state levels will be 1.0 V and 4.0 V ±0.5 V. The output RC time constant (τ) must be less than 3 μs (e.g., R_{PU} = 3 kΩ and C_{OUT} = 1 nF), and V_{PU} must be equal to V_{CC} (recommend pulling up V_{OUT} directly to V_{CC}).

Under normal operation (Figure 5), the output switches between the V_{OUT(LOW)} (20%) and V_{OUT(HIGH)} (80%) states.

With various opens and shorts on any of the IC pins, the output will no longer be controlled by the IC. The output itself may continue to switch, depending on the external connectivity fault; however, the output level(s) observed will deviate from the 20% and 80% (of V_{PU}) output levels.

If an internal fault is detected via diagnostics monitoring, the output will be set to the fault state, V_{OUT(FAULT)}, which is equal to the pull-up voltage, V_{PU}.

Any output voltage levels outside of the valid V_{OUT(HIGH)} and V_{OUT(LOW)} ranges indicates a fault as shown in Figure 6. The observed voltage on V_{OUT} relative to potential fault conditions are summarized in Table 2.

The output relative to the fault condition is summarized in Table 2 below.

Table 2: Fault Conditions and Resulting Output Level

<table>
<thead>
<tr>
<th>Fault</th>
<th>Output Level</th>
</tr>
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<tbody>
<tr>
<td>No Fault</td>
<td>20% or 80% of V_{PU}, respectively</td>
</tr>
<tr>
<td>Short, VCC-VOUT</td>
<td>V_{CC}</td>
</tr>
<tr>
<td>Short, VOUT-GND</td>
<td>GND</td>
</tr>
<tr>
<td>Short, VCC-GND</td>
<td>V_{PU}</td>
</tr>
<tr>
<td>Open, VCC</td>
<td>V_{PU}</td>
</tr>
<tr>
<td>Open, VOUT</td>
<td>V_{PU}</td>
</tr>
<tr>
<td>Open, GND</td>
<td>V_{PU}</td>
</tr>
<tr>
<td>Internal Fault</td>
<td>V_{PU}</td>
</tr>
</tbody>
</table>

Note: V_{OUT(FAULT)} ≤ V_{PULL-UP} and V_{PULL-UP} = V_{CC}.  

![Figure 5: The APS11450 diagnostic output under normal operation (no fault detected)](image)

![Figure 6: APS11450 valid (normal) and fault condition output levels](image)
Fault Detection and Retry

The fault detection diagnostics runs continuously in the background during normal operation after the device has powered-on. In the event a fault is detected, the output will immediately change to the $V_{\text{OUT(FAULT)}}$ state. The diagnostics will continue to retry the diagnostics approximately every 2 ms. If the fault recovers, the output will return to normal operation. See Figure 7.

Output Overshoot

When the output switches from $V_{\text{OUT(LOW)}}$ to $V_{\text{OUT(HIGH)}}$, depending upon the RC circuit, a small overshoot can occur ($V_{\text{OUT(HOVER)}}$). $V_{\text{OUT(HOVER)}}$ is specified as a percentage of $V_{\text{PULL-UP}}$ (and/or $V_{\text{CC}}$, which need to be the same). Therefore with an RC Time Constant ($\tau$) of 3 $\mu$s (see the “Applications Information” section), a nominal overshoot of 2% is possible. With $V_{\text{PULL-UP}}$ at 5.0 V, the output may overshoot by 0.1 V, for less than 5 $\mu$s ($t_{\text{OUT(HOVER)}}$). Figure 7 demonstrates output edge profile.

For example, with a 5 V pull-up, if $V_{\text{OUT(HIGH)}}$ is at the upper limit (90%), $V_{\text{OUT(HIGH)}}$ will be 4.5 V. With a $\tau$ of 3 $\mu$s at room temperature, the output can briefly reach 4.6 V until it settles to 4.5 V. Since $V_{\text{OUT(HIGH)}}$ is valid between 70% and 90%, or 3.5 and 4.5 V, this condition is not out of specification. The Output Off Voltage Overshoot specification pertains only to conditions where the overshoot is greater than the $V_{\text{OUT(HIGH)MAX}}$ specification.

Figure 7: Fault Detection and Retry

**Output Switches according to external magnetic field**

OUTPUT

$V_{\text{OUT(HOVER)}}$

$V_{\text{OUT(LOW)}}$

$V_{\text{OUT(HIGH)}}$

DIAG CHECK

* 4x Diagnostic Cycles completed every 0.025 ms (nom.)

** Diagnostic Fault Retry Time interval is 2 ms (nom.)

Failure Detected

Diag Retry**

Device Recovers

2 ms

2 ms

Figure 8: Output Overshoot
APPLICATIONS INFORMATION

Typical Applications

For the LH and UA packages, an external bypass capacitor, \( C_{BYP} \), should be connected (in close proximity to the Hall sensor) between the supply and ground of the device to reduce both external noise and noise generated by the chopper stabilization technique. As is shown in Figure 9, a 0.1 \( \mu \)F bypass capacitor is typical, with an optional output capacitor, \( C_{OUT} \) (recommended 1 nF).

The time constant of the RC circuit (\( \tau \)) on output must be less than 3 \( \mu \)s, where:

\[
\tau = R_{PULLUP} \times C_{OUT}
\]

\[
= 3 \text{ k}\Omega \times 1 \text{ nF}
\]

\[
= 3 \mu\text{s}
\]

The resistor, \( R_{PULLUP} \), must be between 2 and 30 k\( \Omega \).

Figure 9: Typical Applications Circuits

Diagnostic Output

Temperature Compensation

To calculate the typical effect of the \( T_{SENS} \) on \( B_{OP} \) (or \( B_{RP} \)), simply multiply the \( B_{OP} \) at the starting temperature by \( T_{SENS} \) and the change in temperature.

Sample \( B_{OP} \) calculation for \( T_{SENS} \) compensation from 25°C to 150°C, for \( T_{SENS} = -0.12\%/\degree \text{C} \), and \( B_{OP(25C)} = 180 \text{ G} \):

\[
\Delta T_A = 150\degree \text{C} - 25\degree \text{C} = 125\degree \text{C}
\]

\[
B_{OP(150C)} = B_{OP(25C)} + (B_{OP(25C)} \times T_{SENS} \times \Delta T_A)
\]

\[
= 180 \text{ G} + (180 \text{ G} \times -0.12\%/\degree \text{C} \times 125\degree \text{C})
\]

\[
= 180 \text{ G} + (-27 \text{ G})
\]

\[
= 153 \text{ G}
\]

The following application circuit conditions are required

- The \( \tau \) of the RC on output must be < 3 \( \mu \)s.
- \( 2 \text{ k}\Omega < R_{RC} < 30 \text{ k}\Omega \).
- \( V_{PU} = V_{CC} \) (recommend pulling VOUT up to VCC).

* The following application circuit conditions are required

- The \( \tau \) of the RC on output must be < 3 \( \mu \)s.
- \( 2 \text{ k}\Omega < R_{RC} < 30 \text{ k}\Omega \).
- \( V_{PU} = V_{CC} \) (recommend pulling VOUT up to VCC).
Extensive applications information on magnets and Hall-effect sensors is available in:

- *Hall-Effect IC Applications Guide*, AN27701
- *Guidelines For Designing Subassemblies Using Hall-Effect Devices*, AN27703.1
- *Soldering Methods for Allegro’s Products – SMT and Through-Hole*, AN26009

All are provided on the Allegro website:

[www.allegromicro.com](http://www.allegromicro.com)
Chopper Stabilization Technique

A limiting factor for switch point accuracy when using Hall-effect technology is the small-signal voltage developed across the Hall plate. This voltage is proportionally small relative to the offset that can be produced at the output of the Hall sensor. This makes it difficult to process the signal and maintain an accurate, reliable output over the specified temperature and voltage range. Chopper stabilization is a proven approach used to minimize Hall offset.

The technique, dynamic quadrature offset cancellation, removes key sources of the output drift induced by temperature and package stress. This offset reduction technique is based on a signal modulation-demodulation process. “Figure 10: Model of Chopper Stabilization Circuit (Dynamic Offset Cancellation)” illustrates how it is implemented.

The undesired offset signal is separated from the magnetically induced signal in the frequency domain through modulation. The subsequent demodulation acts as a modulation process for the offset causing the magnetically induced signal to recover its original spectrum at baseband while the DC offset becomes a high-frequency signal. Then, using a low-pass filter, the signal passes while the modulated DC offset is suppressed. Allegro’s innovative chopper-stabilization technique uses a high-frequency clock.

The high-frequency operation allows a greater sampling rate that produces higher accuracy, reduced jitter, and faster signal processing. Additionally, filtering is more effective and results in a lower noise analog signal at the sensor output. Devices such as the APS11450 that use this approach have an extremely stable quiescent Hall output voltage, are immune to thermal stress, and have precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process which allows the use of low offset and low noise amplifiers in combination with high-density logic and sample-and-hold circuits.

Figure 10: Model of Chopper Stabilization Circuit (Dynamic Offset Cancellation)
POWER DERATING

The device must be operated below the maximum junction temperature, \(T_J\) (max). Reliable operation may require derating supplied power and/or improving the heat dissipation properties of the application.

Thermal Resistance (junction to ambient), \(R_{\text{JA}}\), is a figure of merit summarizing the capability of the application and the device to dissipate heat from the junction (die), through all paths to ambient air. \(R_{\text{JA}}\) is dominated by the Effective Thermal Conductivity, \(K\), of the printed circuit board which includes adjacent devices and board layout. Thermal resistance from the die junction to case, \(R_{\text{JC}}\), is a relatively small component of \(R_{\text{JA}}\). Ambient air temperature, \(T_A\), and air motion are significant external factors in determining a reliable thermal operating point.

The following three equations can be used to determine operation points for given power and thermal conditions.

\[
P_D = V_{\text{IN}} \times I_{\text{IN}} \quad (1)
\]

\[
\Delta T = P_D \times R_{\text{JA}} \quad (2)
\]

\[
T_J = T_A + \Delta T \quad (3)
\]

For example, given common conditions: \(T_A = 25^\circ\text{C}\), \(V_{\text{CC}} = 12\text{ V}\), \(I_{\text{CC}} = 4\text{ mA}\), and \(R_{\text{JA}} = 110^\circ\text{C}/\text{W}\) for the LH package, then:

\[
P_D = V_{\text{CC}} \times I_{\text{CC}} = 12\text{ V} \times 4\text{ mA} = 48\text{ mW}
\]

\[
\Delta T = P_D \times R_{\text{JA}} = 48\text{ mW} \times 110^\circ\text{C}/\text{W} = 5.28^\circ\text{C}
\]

\[
T_J = T_A + \Delta T = 25^\circ\text{C} + 5.28^\circ\text{C} = 31.28^\circ\text{C}
\]

Determining Maximum \(V_{\text{CC}}\)

For a given ambient temperature, \(T_A\), the maximum allowable power dissipation as a function of \(V_{\text{CC}}\) can be calculated. \(P_D\) (max) represents the maximum allowable power level without exceeding \(T_J\) (max) at a selected \(R_{\text{JA}}\) and \(T_A\).

Example: \(V_{\text{CC}} = 3\text{ V}\), \(I_{\text{CC}} = 4\text{ mA}\), and \(R_{\text{JA}} = 228^\circ\text{C}/\text{W}\) for the LH package using equation 1, the largest possible amount of dissipated power is:

\[
P_D = V_{\text{IN}} \times I_{\text{IN}}
\]

\[
P_D = 3\text{ V} \times 4\text{ mA} = 12\text{ mW}
\]

Finally, using equation 1, solve for maximum allowable \(V_{\text{CC}}\) for the given conditions:

\[
V_{\text{CC}} (\text{est}) = P_D (\text{max}) \div I_{\text{CC}} (\text{max}) = 91\text{ mW} \div 4\text{ mA} = 22.8\text{ V}
\]

The result indicates that, at \(T_A\), the application and device can dissipate adequate amounts of heat at voltages \(\leq V_{\text{CC}} (\text{est})\). If the application requires \(V_{\text{CC}} > V_{\text{CC}} (\text{est})\) then \(R_{\text{JA}}\) must by improved. This can be accomplished by adjusting the layout, PCB materials, or by controlling the ambient temperature.

Determining Maximum \(T_A\)

In cases where the \(V_{\text{CC}}\) (max) level is known, and the system designer would like to determine the maximum allowable ambient temperature \(T_A\) (max), for example, in a worst-case scenario with conditions \(V_{\text{CC}}\) (max) = 40 V, \(I_{\text{CC}}\) (max) = 4 mA, and \(R_{\text{JA}} = 228^\circ\text{C}/\text{W}\) for the LH package using equation 1, the largest possible amount of dissipated power is:

\[
P_D = V_{\text{IN}} \times I_{\text{IN}}
\]

\[
P_D = 40\text{ V} \times 4\text{ mA} = 160\text{ mW}
\]

Then, by rearranging equation 3 and substituting with equation 2:

\[
T_A (\text{max}) = T_J (\text{max}) - \Delta T
\]

\[
T_A (\text{max}) = 165^\circ\text{C} - (160\text{ mW} \times 228^\circ\text{C}/\text{W})
\]

\[
T_A (\text{max}) = 165^\circ\text{C} - 36.5^\circ\text{C} = 128.5^\circ\text{C}
\]

In another example, the maximum supply voltage is equal to \(V_{\text{CC}}\) (min). Therefore, \(V_{\text{CC}}\) (max) = 3 V and \(I_{\text{CC}}\) (max) = 4 mA. By using equation 1 the largest possible amount of dissipated power is:

\[
P_D = V_{\text{IN}} \times I_{\text{IN}}
\]

\[
P_D = 3\text{ V} \times 4\text{ mA} = 12\text{ mW}
\]

Then, by rearranging equation 3 and substituting with equation 2:

\[
T_A (\text{max}) = T_J (\text{max}) - \Delta T
\]

\[
T_A (\text{max}) = 165^\circ\text{C} - (12\text{ mW} \times 228^\circ\text{C}/\text{W})
\]

\[
T_A (\text{max}) = 165^\circ\text{C} - 11.6^\circ\text{C} = 126.2^\circ\text{C}
\]

The example above indicates that at \(V_{\text{CC}} = 3\text{ V}\) and \(I_{\text{CC}} = 4\text{ mA}\), the \(T_A\) (max) can be as high as 162.3°C without exceeding \(T_J\) (max). However the \(T_A\) (max) rating of the device is 150°C; the device performance is not guaranteed above \(T_A = 150^\circ\text{C}\).
Three-Wire Hall-Effect Switch with Advanced Diagnostics

APS11450

Package LH, 3-Pin SOT23W

For Reference Only – Not for Tooling Use
(Reference Allegro DWG-0000628, Rev. 1)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

For Reference Only – Not for Tooling Use
(Reference Allegro DWG-0000628, Rev. 1)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

Branded Face

Standard Branding Reference View
Line 1 = 3 characters
Line 1: Last 3 digits of Part Number
Branding scale and appearance at supplier discretion
Package UA, 3-Pin SIP, Matrix HD Style

For Reference Only – Not For Tooling Use
(Reference DWG-0000404, Rev. 1)
NOT TO SCALE
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

Ejector pin flash
protrusion
Mold gate and tie bar
protrusion zone

R0.25 MAX (2×)
0.10 MAX
45° (2×)
5° (2×)
0.56 MAX
1.52 ±0.05
1.68 MAX

Mold gate and tie bar
protrusion zone
Including gate and
tie bar burrs

Hall Element
(not to scale)
Sensor element location tolerance
Standard ±0.20

Sensor element location tolerance
Standard ±0.20

0.50 ±0.08 Active Area Depth

Ejector pin flash
protrusion

0.10 MAX

0.41 ±0.03
0.06

0.79 REF

45°
10° (3×)

0.05 NOM
0.05 NOM

1.02 MAX
0.51 REF

0.10 MAX
0.10 MAX

0.05 NOM

1.27 NOM (2×)
4.09 +0.08
–0.05

3.00 ±0.05
2.04 NOM

0.56 MAX

3.02 +0.08
–0.05

1.44 NOM

5°
0.06 ±0.05
–0.00

0.15 MAX

0.43 ±0.05
(3×)

Dambar Trim Detail

Standard Branding Reference View
A = Supplier emblem
N = Last three digits of device part number
Branding scale and appearance at supplier discretion.
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www.allegromicro.com

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<th>Number</th>
<th>Date</th>
<th>Description</th>
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<tr>
<td>–</td>
<td>January 31, 2019</td>
<td>Initial release</td>
</tr>
<tr>
<td>1</td>
<td>April 23, 2019</td>
<td>Updated ASIL status</td>
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<tr>
<td>2</td>
<td>September 17, 2021</td>
<td>Added “-3SLD” part variant (pages 2, 6, and 12); updated package drawings (pages 23-24)</td>
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