APS12800

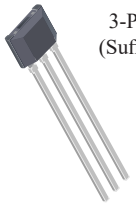
Two-Wire Hall-Effect Latch with Advanced Diagnostics

FEATURES AND BENEFITS

- Functional safety
  - Developed in accordance with ISO 26262
  - Designed to meet ASIL B requirements
  - Integrated background diagnostics for:
    - Signal path
    - Regulator
    - Hall plate and bias
    - Overtemperature detection
    - Nonvolatile memory
  - Defined fault state
- Multiple product options
  - Magnetic polarity, switch points, and hysteresis
  - Temperature coefficient
  - Output polarity
- Reduces module bill-of-materials (BOM) and assembly cost
  - ASIL B sensor can replace redundant sensors
  - Integrated overvoltage clamp and reverse-battery diode
- Automotive-grade ruggedness and fault tolerance
  - Extended AEC-Q100 Grade 0 qualification
  - Operation to 175°C junction temperature
  - 3 to 30 V operating voltage range
  - ±8 kV HBM ESD
  - Overtemperature indication

PACKAGES

3-Pin SOT23W
(Suffix LH)



3-Pin SIP
(Suffix UA)

Not to scale

DESCRIPTION

The APS12800 is a two-wire planar Hall-effect sensor integrated circuit (IC) developed in accordance with ISO 26262. It includes internal diagnostics and a fault state that support a functional safety level of ASIL B when integrated and used in conjunction with the appropriate system-level control. The two-wire interface provides interconnect open/short diagnostics and a fault state to communicate diagnostic information while maintaining compatibility with legacy two-wire systems. The continuous background diagnostics are transparent to the host system and results in a reduced fault tolerant time.

The APS12800 product options include magnetic switch points, temperature coefficient, magnetic and output polarity. The switch points are configured for a stable or flat temperature response. Additional temperature response characteristics for NdFeB or low-cost ferrite magnets may be available by contacting Allegro MicroSystems. For situations where a functionally equivalent two-wire switch device is preferred, refer to the APS11800.

Continued on next page...

APPLICATIONS

- Automotive and industrial safety systems
- Seat/window motors
- Sun roof/convertible top/liftgate/tailgate actuation
- Brake and clutch by wire actuators
- Engine management actuators
- Electronic power steering
- Transmission shift actuators

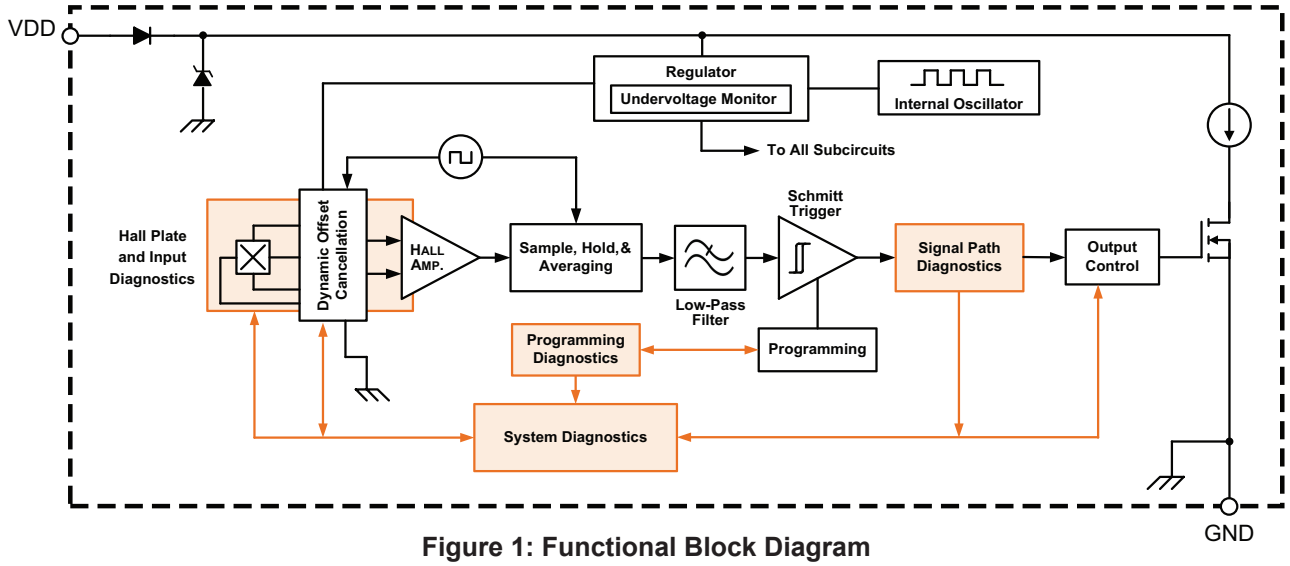


Figure 1: Functional Block Diagram

DESCRIPTION (continued)

APS12800 sensors are engineered to operate in the harshest environments with minimal external components. They are qualified beyond the requirements of AEC-Q100 Grade 0 and will survive extended operation at 175°C junction temperature.

These monolithic ICs include on-chip reverse-battery protection, overvoltage protection (e.g., 40 V load dump), ESD protection, overtemperature detection, and an internal voltage regulator for operation directly from an automotive 12 V battery system. These integrated features reduce the end-product bill-of-materials (BOM) and assembly cost.

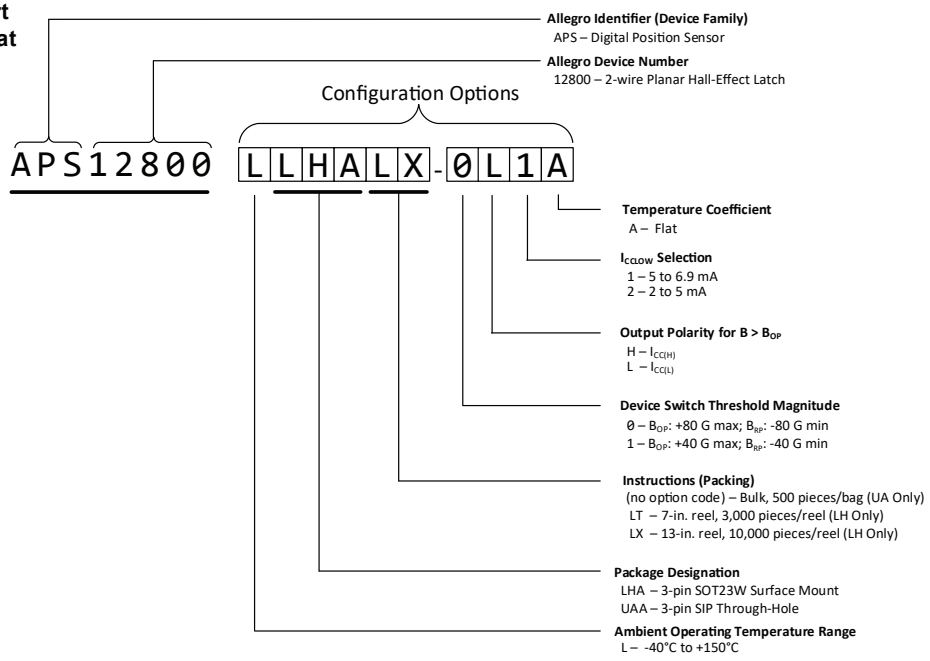
Package options include industry-standard surface-mount SOT (LH) and through-hole SIP (UA) packages. Both packages are RoHS-compliant and lead (Pb) free with 100% matte-tin-plated leadframes

SELECTION GUIDE

Part Number [1]	Package	Packing	Magnetic Temperature Coefficient	Output Polarity for B > B_{OP}	Device Latch Threshold (G)	$I_{CC(L)}$ Selection (mA)
APS12800LLHALT-0H1A	3-pin SOT23-W surface mount	7-inch reel, 3000 pieces/reel	Flat	$I_{CC(H)}$	B_{OP}: +80 max B_{RP}: –80 max	5 to 6.9
APS12800LLHALX-0H1A	3-pin SOT23-W surface mount	13-inch reel, 10000 pieces/reel				
APS12800LUAA-0H1A	3-pin SIP through-hole	Bulk, 500 pieces/bag	Flat	$I_{CC(H)}$	B_{OP}: +80 max B_{RP}: –80 max	5 to 6.9
APS12800LUAATN-0H1A	3-pin SIP through-hole	13-inch reel, 4000 pieces/reel				
APS12800LUAA-0H2A [2]	3-pin SIP through-hole	Bulk, 500 pieces/bag	Flat	$I_{CC(H)}$	B_{OP}: +80 max B_{RP}: –80 max	2 to 5
APS12800LUAATN-0H2A [2]	3-pin SIP through-hole	13-inch reel, 4000 pieces/reel				

[1] Contact Allegro MicroSystems for options not listed in the selection guide.
[2] Contact Allegro MicroSystems for availability.

Complete Part Number Format



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ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage [1]	V_{CC}		45	V
Reverse Supply Voltage [1]	V_{RCC}		–30	V
Maximum Junction Temperature	$T_{J(MAX)}$		165	°C
		1000 hours	175	
Storage Temperature	T_{stg}		–65 to 170	°C

[1] This rating does not apply to extremely short voltage transients such as Load Dump and/or ESD. Those events have individual ratings, specific to the respective transient voltage event.

ESD PERFORMANCE

Characteristic	Symbol	Notes	Rating	Unit
AEC-Q100 ESD	$V_{ESD(HBM)}$	Human Body Model AEC-Q100-002	±8	kV

TRANSIENT PROTECTION CHARACTERISTICS: Valid for T_A = 25°C and C_{BYP} = 0.1 µF (unless otherwise specified)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Forward Supply Zener Clamp Voltage	V_Z	$I_{CC(max)}$ + 3 mA	44	–	–	V
Reverse Supply Zener Clamp Voltage	V_{RCC}	I_{CC} = –1 mA	–	–	–30	V
Reverse Supply Current	I_{RCC}	V_{RCC} = –30 V	–	–	–5	mA

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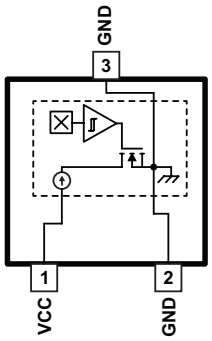
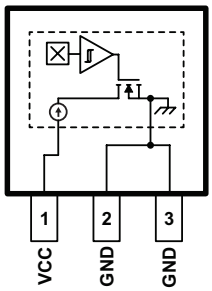
PINOUT DIAGRAMS AND TERMINAL LISTS



Package LH, 3-Pin SOT23W Pinout



Package UA, 3-Pin SIP Pinout

Terminal List Table

Symbol	Pin Number		
	LH Package	UA Package	Description
VCC	1	1	Supply Voltage
GND	2*	2	Ground
GND	3*	3	Ground

* Pins 2 and 3 are tied together internally and the device will operate with either pin 2 or 3 grounded externally; however, grounding both pins externally is recommended for EMC robustness.

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OPERATING CHARACTERISTICS: Valid over full operating voltage and ambient temperature ranges for $T_J < T_J$ (max), and C_{BYP} = 0.1 µF, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit
Supply Voltage	V_{CC}	Operating; min. V_{CC} for magnetically actuated output	3	–	30	V
Undervoltage Lockout	V_{UVLO}	Voltage threshold at which the device output is set to POS during power down	–	2.3	–	V
Shutdown Voltage	V_{SD}	Sensor output shuts down	–	1.8	–	V
Supply Current	$I_{CC(L)}$	I_{CCLOW} Selection = 2	2	–	5	mA
		I_{CCLOW} Selection = 1	5	–	6.9	mA
	$I_{CC(H)}$		12	–	17	mA
	I_{FAULT}	Safe current state; indicates device diagnostics have detected a fault condition; see Table 1	–	–	1.8	mA
Output Slew Rate	dI/dt	Standard circuit; C_{BYP} = 100 nF, C_L [2] = 20 pF, R_{SENSE} = 100 Ω	–	0.4	–	mA/µs
		Min. circuit; C_{BYP} = 10 nF, C_L [2] = 20 pF, R_{SENSE} = 100 Ω	–	4	–	mA/µs
Power-On Time [3]	t_{PO}	On power up only; time starts when supply voltage exceeds $V_{CC(min)}$	–	–	70	µs
Power-On State [4]	POS	Output state during power on; valid only when $V_{CC} \geq V_{CC(min)}$	$I_{CC(H)}$	–	–	mA
Chopping Frequency	f_C		–	800	–	kHz
Diagnostic Characteristics						
Fault Reaction Time	t_{DIAG}	C_{BYP} = 0.1 µF, R_{SENSE} = 100 Ω	–	44	–	µs
Diagnostic Fault Retry Time	t_{DIAGF}		–	2	–	ms
Overtemperature Shutdown	T_{JF}	Temperature increasing	–	205	–	°C
Overtemperature Hysteresis	T_{HYS}		–	25	–	°C

[1] Typical data is at T_A = 25°C and V_{CC} = 12 V, unless otherwise noted; for design information only.
[2] C_L – measurement probe capacitance.
[3] Measured from $V_{CC} \geq V_{CC(min)}$ to valid output.
[4] Power-on state is defined only when V_{CC} slew rate > 6 V/ms.

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MAGNETIC CHARACTERISTICS: Valid over full operating voltage and ambient temperature ranges for $T_J < T_J(max)$ and C_{BYP} = 0.01 µF, unless otherwise specified

Characteristics	Symbol	Magnetic Switch Point Option	Temperature Coefficient	Test Conditions	Min.	Typ. [8]	Max.	Unit [9]
Operate Point	B_{OP}	-0	A – Flat	T_A = –40°C to 150°C	5	–	80	G
		-1	A – Flat	T_A = –40°C to 150°C	5	–	40	G
Release Point	B_{RP}	-0	A – Flat	T_A = –40°C to 150°C	–80	–	–5	G
		-1	A – Flat	T_A = –40°C to 150°C	–40	–	–5	G
Hysteresis	B_{HYS}	-0	A – Flat	T_A = –40°C to 150°C	40	–	110	G
		-1	A – Flat	T_A = –40°C to 150°C	15	40	65	G
Symmetry	B_{SYM}	All	All	$B_{OP} + B_{RP}$	–30	–	30	G
Switch Point Temperature Coefficient		All	A – Flat	T_A = –40°C to 150°C	–	0	–	%/°C
Jitter [10]	–	-1	A – Flat		–	0.25	–	%

[8] Typical data is at T_A = 25°C and V_{CC} = 12 V, unless otherwise noted; for design information only.
[9] Magnetic flux density, B, is indicated as a negative value for north-polarity magnetic fields, and a positive value for south-polarity magnetic fields.
[10] Output edge repeatability as a percentage of the period.

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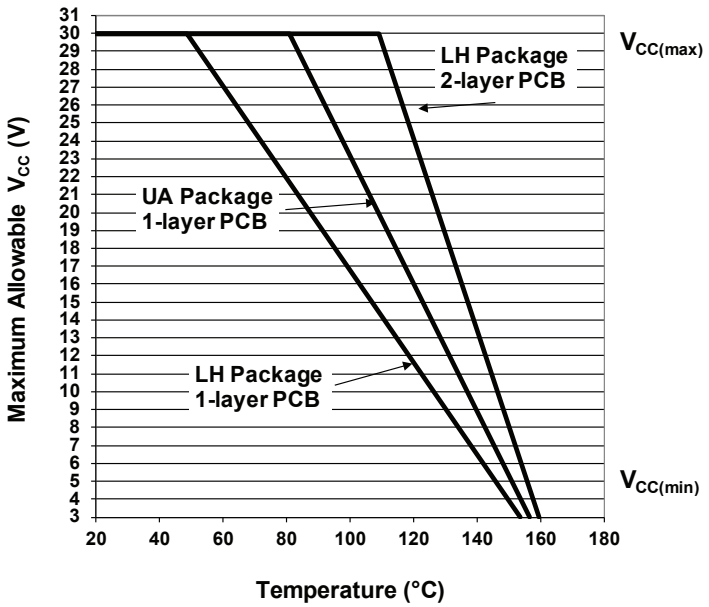
THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Notes	Rating	Unit
Package Thermal Resistance	$R_{\theta JA}$	Package LH, 1-layer PCB with copper limited to solder pads	228	°C/W
		Package LH, 2-layer PCB with 0.463 in.^{2} of copper area, each side connected by thermal vias	110	°C/W
		Package UA, 1-layer PCB with copper limited to solder pads	165	°C/W

Power Derating Curve



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FUNCTIONAL DESCRIPTION

Operation

The output of these devices switches when a magnetic field perpendicular to the Hall-effect sensor exceeds the operate point threshold (B_{OP}). When the magnetic field is reduced below the release point, B_{RP}, the device output switches to the alternate state. The output state (polarity) and magnetic field polarity depends on the selected device options. For unipolar south, an increasing south field is required; likewise, for unipolar north, an increasing north field is required to exceed B_{OP}. The output state is a configuration option.

The difference in magnetic operate and release points is the hysteresis, B_{HYS}, of the device. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise. Figure 3 shows the output switching behavior relative to increasing and decreasing magnetic field. On the horizontal axis, the B+ direction indicates increasing south polarity magnetic field strength. Figure 2 shows the sensing orientation of the magnetic field, relative to the device package.

The difference between operate (B_{OP}) and release (B_{RP}) points is the hysteresis, B_{HYS}. Hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

Figure 3 shows the potential unipolar and omnipolar options and output polarity options the APS12800 can be configured for. The direction of the applied magnetic field is perpendicular to the branded face of the APS12800.

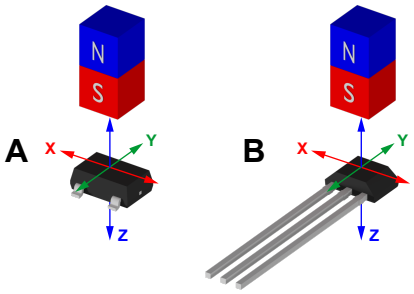

Figure 2: Magnetic Sensing Orientations
LH Package (Panel A), UA Package (Panel B)

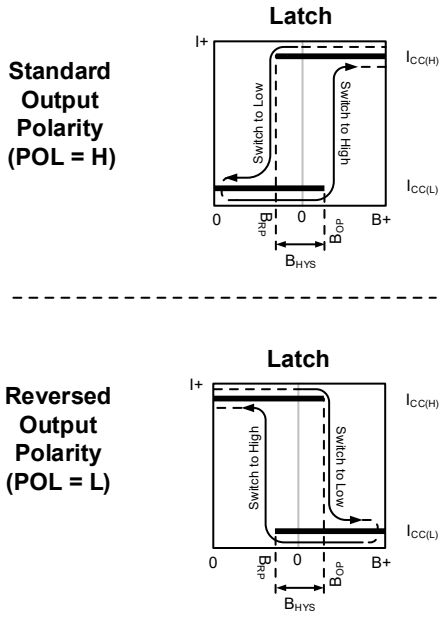

Figure 3: Hall Latch Output State vs. Magnetic Field

B- indicates increasing north polarity magnetic field strength, and B+ indicates increasing south polarity magnetic field strength.

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Power-On/Off Behavior

During power up when V_{CC} reaches $V_{CC(min)}$, the output will enter Power-On State and stay there until t_{PO} expires. The t_{PO} timer starts as soon as V_{CC} exceeds $V_{CC(min)}$; once t_{PO} expires, the device output is determined by the B_{OP}/B_{RP} specifications. (Note the minimum allowed power V_{CC} slew rate is 6 V/ms to ensure that V_{CC} has reached $V_{CC(min)}$ within t_{PO}).

After the device is powered up, if V_{CC} drops below $V_{CC(min)}$, the output state will continue to function; however, B_{OP}/B_{RP} specifications are not be guaranteed over temperature and process corners when $V_{UVLO} < V_{CC} < V_{CC(min)}$. As soon as V_{CC} exceeds $V_{CC(min)}$, B_{OP}/B_{RP} limits will be guaranteed over process and temperature. See Figure 4. If V_{CC} continues to drop below the UVLO threshold, the device output will be forced to POS ($I_{CC(H)}$) and will remain there as long as $V_{PD} < V_{CC} \leq V_{CC(min)}$. Once V_{CC} has dropped below V_{UVLO}, the device will go through power-up sequence once V_{CC} is restored. If V_{CC} continues to drop below V_{PD}, the device will power down and the output will not be functional until V_{CC} is restored to be $>V_{CC(min)}$.

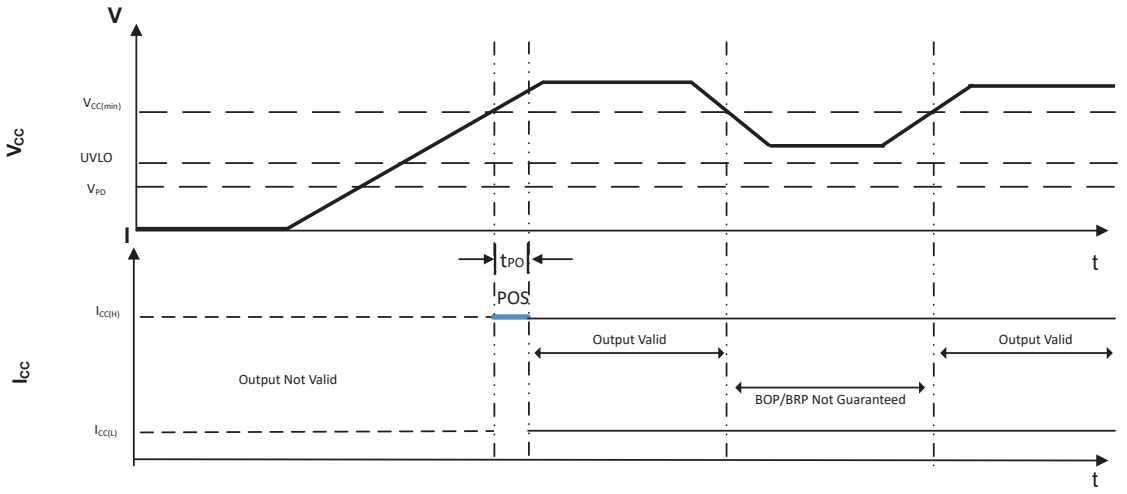

Figure 4: Device power up and subsequent restart after falling below $V_{CC(min)}$ but not below V_{UVLO}

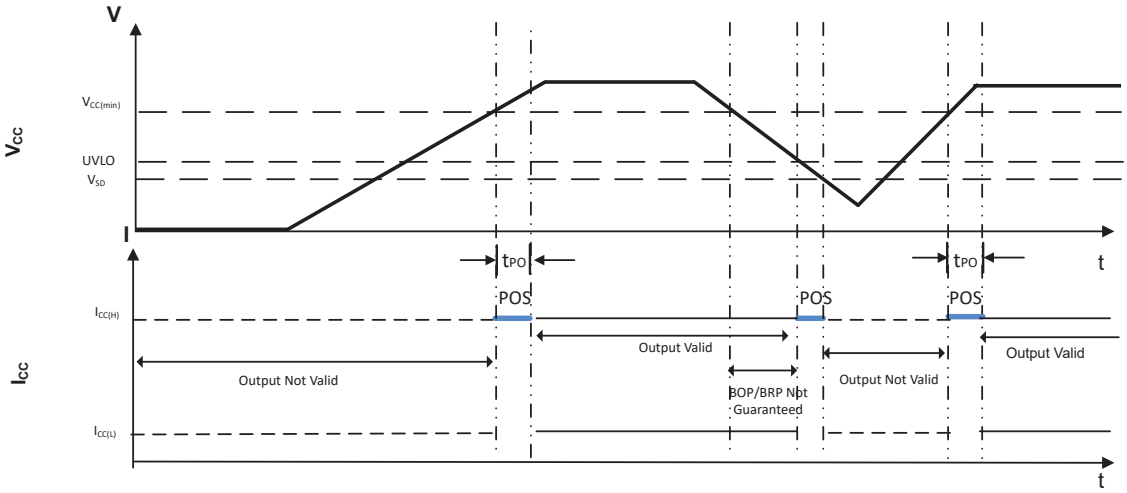

Figure 5: Device power up and subsequent reset after V_{CC} falls below V_{UVLO}

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Two-Wire Interface

The regulated current output is configured for two-wire applications, requiring one less wire for operation than latches with the traditional open-collector output. Additionally, the two-wire interface provides basic diagnostics to the system by monitoring the supply current. During normal operation, the supply current should operate in the specified ranges; see Figure 6. Any current level not within the specified operating ranges for $I_{CC(H)}$ or $I_{CC(L)}$ indicates a fault condition.

There are a couple specific fault conditions indicated by $I_{CC} = I_{FAULT}$. If the device junction temperature exceeds T_{JF}, average supply current will be in the I_{FAULT} region. Additionally, if the any of the device internal diagnostics described in Table 1 detect a fault, the output will go to I_{FAULT}. A supply current greater than the specified maximum for the high level ($I_{CC} > I_{CC(H)(max)}$), typically indicates a short condition. If $I_{CC} < I_{FAULT(min)}$ typically indicates an open-circuit condition.

This unique two-wire interface protocol is backward compatible with legacy systems using two-wire latches. Additionally, the low fault mode supply current resulting from an internal fault will fall outside of the low and high supply current ranges and can be similarly identified as a sensor fault.

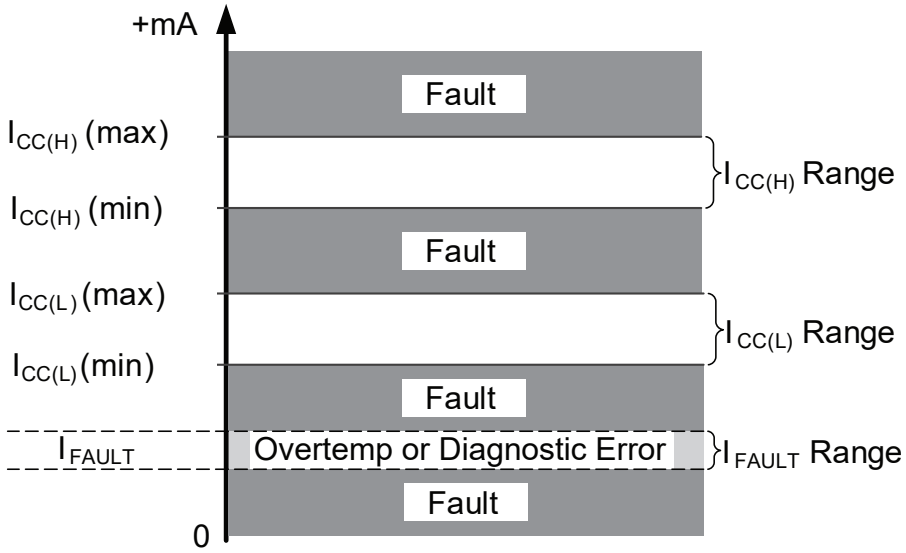

Figure 6: Two Wire Interface Output

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Functional Safety

The APS12800 was developed in accordance with the international standard for automotive functional safety, ISO 26262. Designed to meet ASIL B requirements when integrated and used in conjunction with the appropriate system-level control in the manner prescribed in the APS12800 Safety Manual.

The APS12800 features a proprietary diagnostics routine to support ASIL B safety requirements; see Table 1 and Figure 7. This internal diagnostics routine continuously runs in the background, monitoring all key subsystems of the IC. The diagnostic scheme runs at high speed and provides minimal impact on device performance.

The Hall element biasing circuit and voltage regulator are checked for valid operation, and the digital and nonvolatile memory blocks are checked for valid device configuration.

All diagnostics are running in real time in the background, allowing for a fault reaction time of approximately 44 µs. The signal path monitoring system verifies two internal state transitions (B_{OP} and B_{RP} within limits) under normal operation. In cases when these output transitions do not occur, or if another internal fault is detected, the output will go to the safe state.

In the event of an internal fault, the device will continuously run the diagnostics routine every 2 ms (t_{DIAGF}). The periodic recovery attempt sequence allows the device to continually check for the presence of a fault and return to normal operation if the fault condition clears.

In the case where the fault is no longer present, the output will resume normal operation. However, if the fault is persistent, the device will not exit fault mode and I_{CC} will continue to be I_{FAULT}. See Figure 8.

When a system rating higher than ASIL B is required, additional external safety measures may be employed (e.g., sensor redundancy and rationality checks, etc.). Refer to the device safety manual for additional details about the diagnostics.

Table 1: Diagnostics Coverage

	Feature	Coverage
1	Hall plate	Connectivity and biasing of Hall plate
2	Signal path	Signal path and Schmitt trigger
3	Voltage regulator	Regulator voltage for normal operation
4	Digital subsystem	Digital subsystem and non-volatile memory
5	Entire system	Overtemperature and redundancies for single point failures
6	Output	Output verified with external monitors

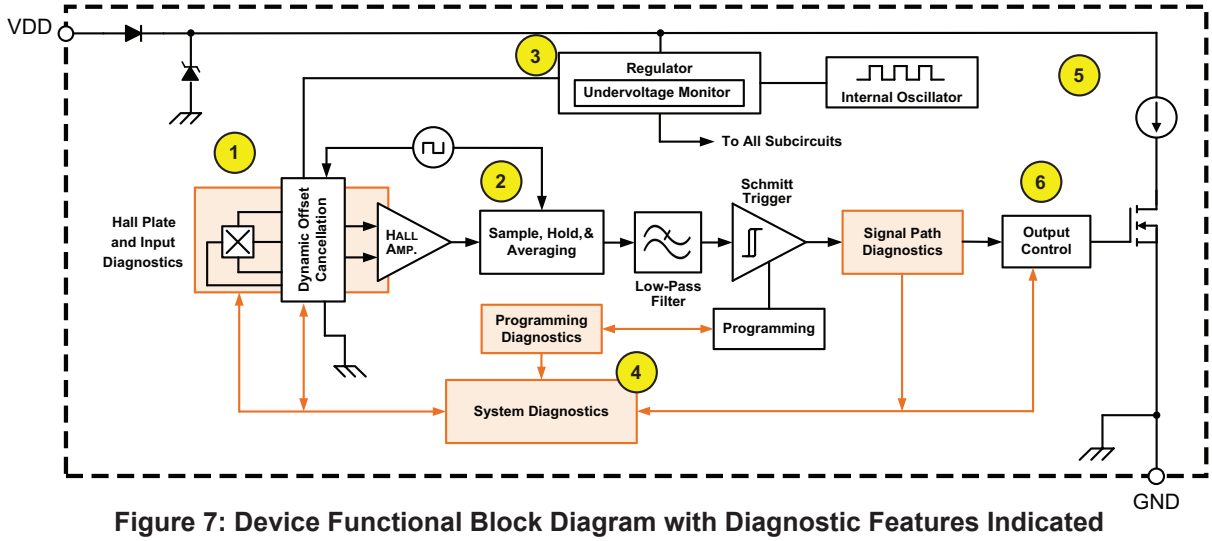

Figure 7: Device Functional Block Diagram with Diagnostic Features Indicated

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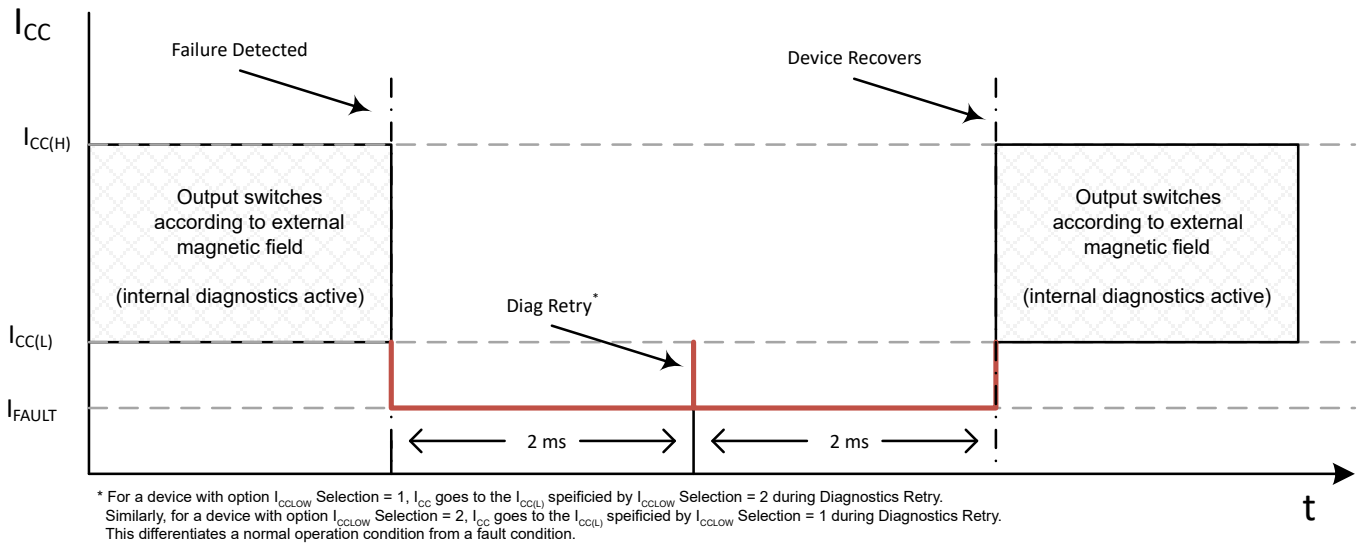

Figure 8: Diagnostic mode operation and timing during normal operation and during a fault condition

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APPLICATIONS INFORMATION

Typical Applications

For the LH and UA, an external bypass capacitor, C_{BYP}, should be connected as close as possible to the Hall sensor between the supply and ground to reduce noise. See Figure 9.

Temperature Coefficient and Magnet Selection

The APS12800 incorporates circuitry to compensate the magnetic switch points over the operating temperature range. This feature is referred to as the magnetic switch point temperature coefficient. The default option is for flat stable response over temperature. If the application requires compensation for temperature drifts common with NdFeB and ferrite magnets, contact Allegro MicroSystems. It is recommended that system designers evaluate their magnetic circuit over the expected operating temperature range to ensure the magnetic switching requirements are met.

Extensive applications information on magnets and Hall-effect sensors is available in:

- *Hall-Effect IC Applications Guide, AN27701,*
- *Hall-Effect Devices: Guidelines For Designing Subassemblies Using Hall-Effect Devices AN27703.1*
- *Soldering Methods for Allegro's Products – SMT and Through-Hole, AN26009*
- Functional Safety Challenges to the Automotive Supply Chain (http://www.allegromicro.com/en/Design-Center/Technical-Documents/General-Semiconductor-Information/Functional-Safety-Challenges-Automotive-Supply-Chain.aspx)

All are provided on the Allegro website:

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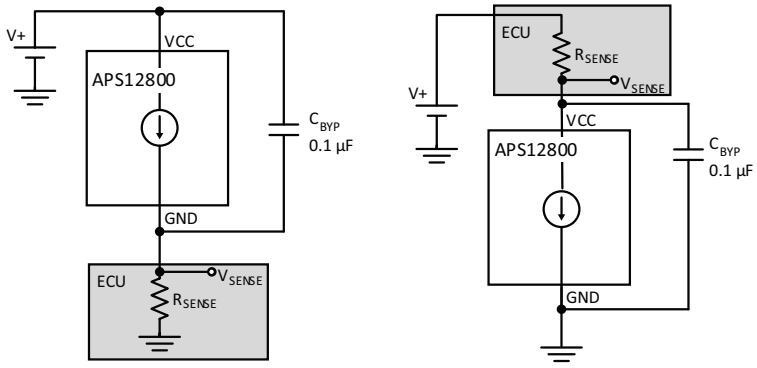

(A) Low-Side Sensing **(B) High-Side Sensing**

Figure 9: Typical Application Circuits

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CHOPPER STABILIZATION

A limiting factor for switch point accuracy when using Hall-effect technology is the small-signal voltage developed across the Hall plate. This voltage is proportionally small relative to the offset that can be produced at the output of the Hall sensor. This makes it difficult to process the signal and maintain an accurate, reliable output over the specified temperature and voltage range. Chopper stabilization is a proven approach used to minimize Hall offset.

The technique, dynamic quadrature offset cancellation, removes key sources of the output drift induced by temperature and package stress. This offset reduction technique is based on a signal modulation-demodulation process. Figure 10: Model of Chopper Stabilization Circuit (Dynamic Offset Cancellation) illustrates how it is implemented.

The undesired offset signal is separated from the magnetically induced signal in the frequency domain through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetically induced signal to recover its original spectrum at baseband while the DC offset becomes a high-frequency signal. Then, using a low-pass filter, the signal passes while the modulated DC offset is suppressed.

Allegro's innovative chopper stabilization technique uses a high-frequency clock. The high-frequency operation allows a greater sampling rate that produces higher accuracy, reduced jitter, and faster signal processing. Additionally, filtering is more effective and results in a lower noise analog signal at the sensor output. Devices such as the APS12800 that use this approach have a stable quiescent Hall output voltage, are immune to thermal stress, and have precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process which allows the use of low-offset and low-noise amplifiers in combination with high-density logic and sample-and-hold circuits.

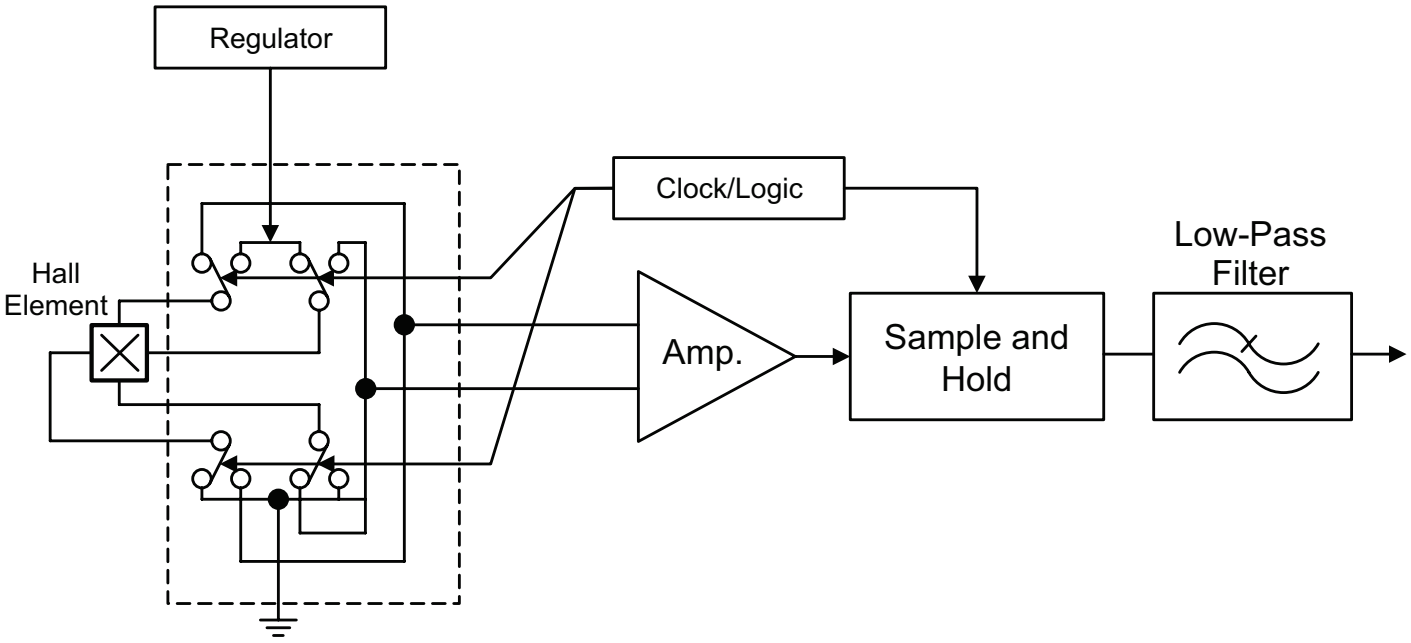

Figure 10: Model of Chopper Stabilization Circuit (Dynamic Offset Cancellation)

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POWER DERATING

The device must be operated below the maximum junction temperature, T_J (max). Reliable operation may require derating supplied power and/or improving the heat dissipation properties of the application.

Thermal Resistance (junction to ambient), $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to ambient air. $R_{\theta JA}$ is dominated by the Effective Thermal Conductivity, K, of the printed circuit board which includes adjacent devices and board layout. Thermal resistance from the die junction to case, $R_{\theta JC}$, is a relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors in determining a reliable thermal operating point.

The following three equations can be used to determine operation points for given power and thermal conditions.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions: T_A = 25°C, V_{CC} = 12 V, I_{CC} = 17 mA, and $R_{\theta JA}$ = 110°C/W for the LH package, then:

$$P_D = V_{CC} \times I_{CC} = 12\ V \times 17\ mA = 204\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 204\ mW \times 110°C/W = 22.44°C$$

$$T_J = T_A + \Delta T = 25°C + 22.44°C = 47.44°C$$

Determining Maximum V_{CC}

For a given ambient temperature, T_A, the maximum allowable power dissipation as a function of V_{CC} can be calculated. P_D (max) represents the maximum allowable power level without exceeding T_J (max) at a selected $R_{\theta JA}$ and T_A.

Example: V_{CC} at T_A = 150°C, package UA, using low-K PCB. Using the worst-case ratings for the device, specifically: $R_{\theta JA}$ = 165°C/W, T_J (max) = 165°C, V_{CC} (max) = 24 V, and I_{CC} (max) = 17 mA, calculate the maximum allowable power level, P_D (max). First, using equation 3:

$$\Delta T\ (max) = T_J\ (max) - T_A = 165°C - 150°C = 15°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, from equation 2:

$$P_D\ (max) = \Delta T\ (max) \div R_{\theta JA} = 15°C \div 165°C/W = 91\ mW$$

Finally, using equation 1, solve for maximum allowable V_{CC} for the given conditions:

$$V_{CC}\ (est) = P_D\ (max) \div I_{CC}\ (max) = 91\ mW \div 17\ mA = 5.4\ V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages ≤ V_{CC} (est).

If the application requires $V_{CC} > V_{CC(est)}$ then $R_{\theta JA}$ must by improved. This can be accomplished by adjusting the layout, PCB materials, or by controlling the ambient temperature.

Determining Maximum T_A

In cases where the V_{CC} (max) level is known, and the system designer would like to determine the maximum allowable ambient temperature T_A (max), for example, in a worst-case scenario with conditions V_{CC} (max) = 24 V, I_{CC} (max) = 17 mA, and $R_{\theta JA}$ = 228°C/W for the LH package using equation 1, the largest possible amount of dissipated power is:

$$P_D = V_{IN} \times I_{IN}$$

$$P_D = 24\ V \times 17\ mA = 408\ mW$$

Then, by rearranging equation 3 and substituting with equation 2:

$$T_A\ (max) = T_J\ (max) - \Delta T$$

$$T_A\ (max) = 165°C - (408\ mW \times 228°C/W)$$

$$T_A\ (max) = 165°C - 93°C = 72°C$$

Finally, note that the T_A (max) rating of the device is 150°C and performance is not guaranteed above this temperature for any power level.

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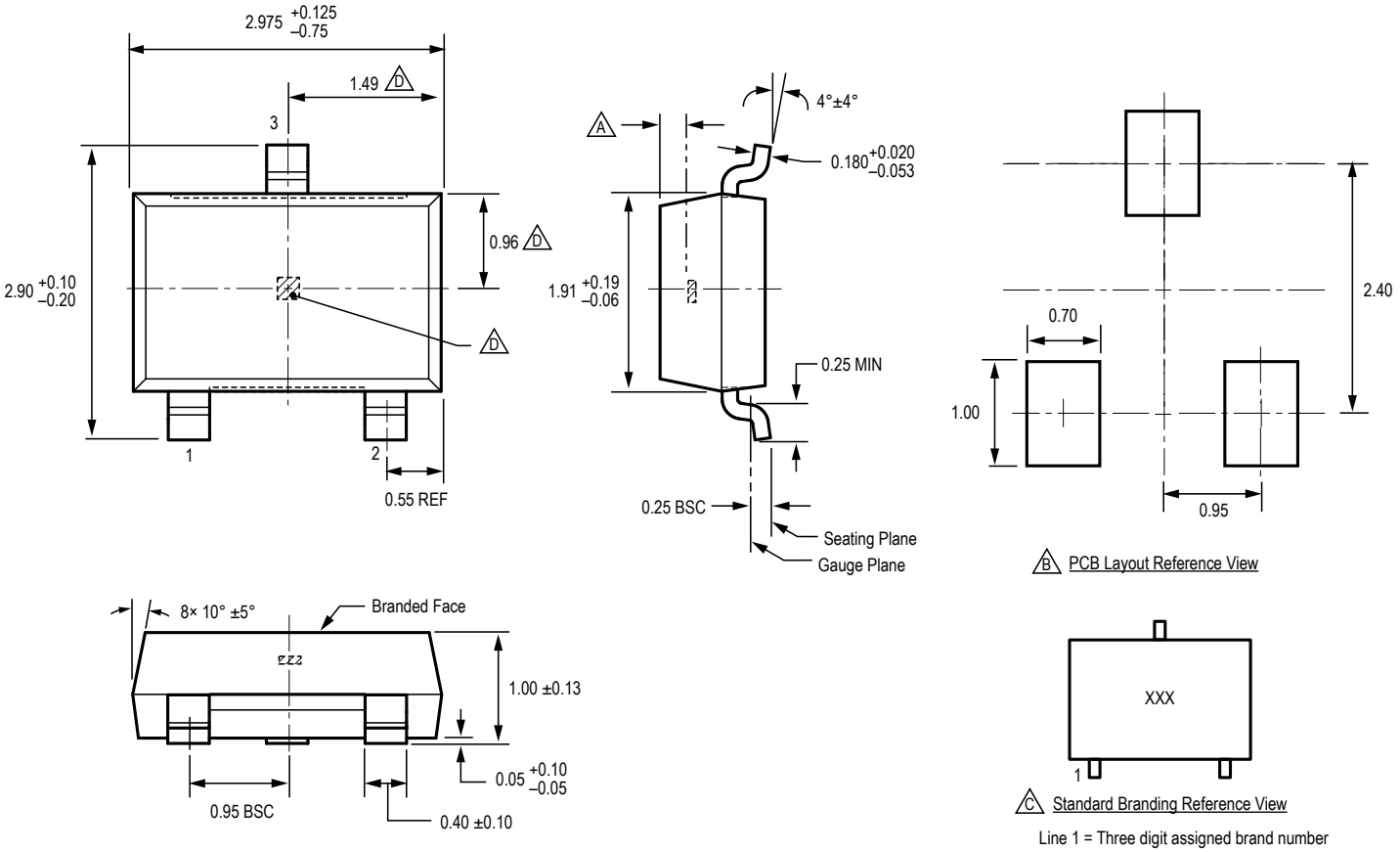
PACKAGE OUTLINE DRAWINGS



For reference only; not for tooling use (reference DWG-0000628, Rev. 1).
Dimensions in millimeters.
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions.
Exact case and lead configuration at supplier discretion within limits shown.

A Active Area Depth, 0.28 ±0.04 mm

B Reference land pattern layout
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

D Hall element, not to scale

Figure 11: Package LH, 3-Pin SOT23W

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NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

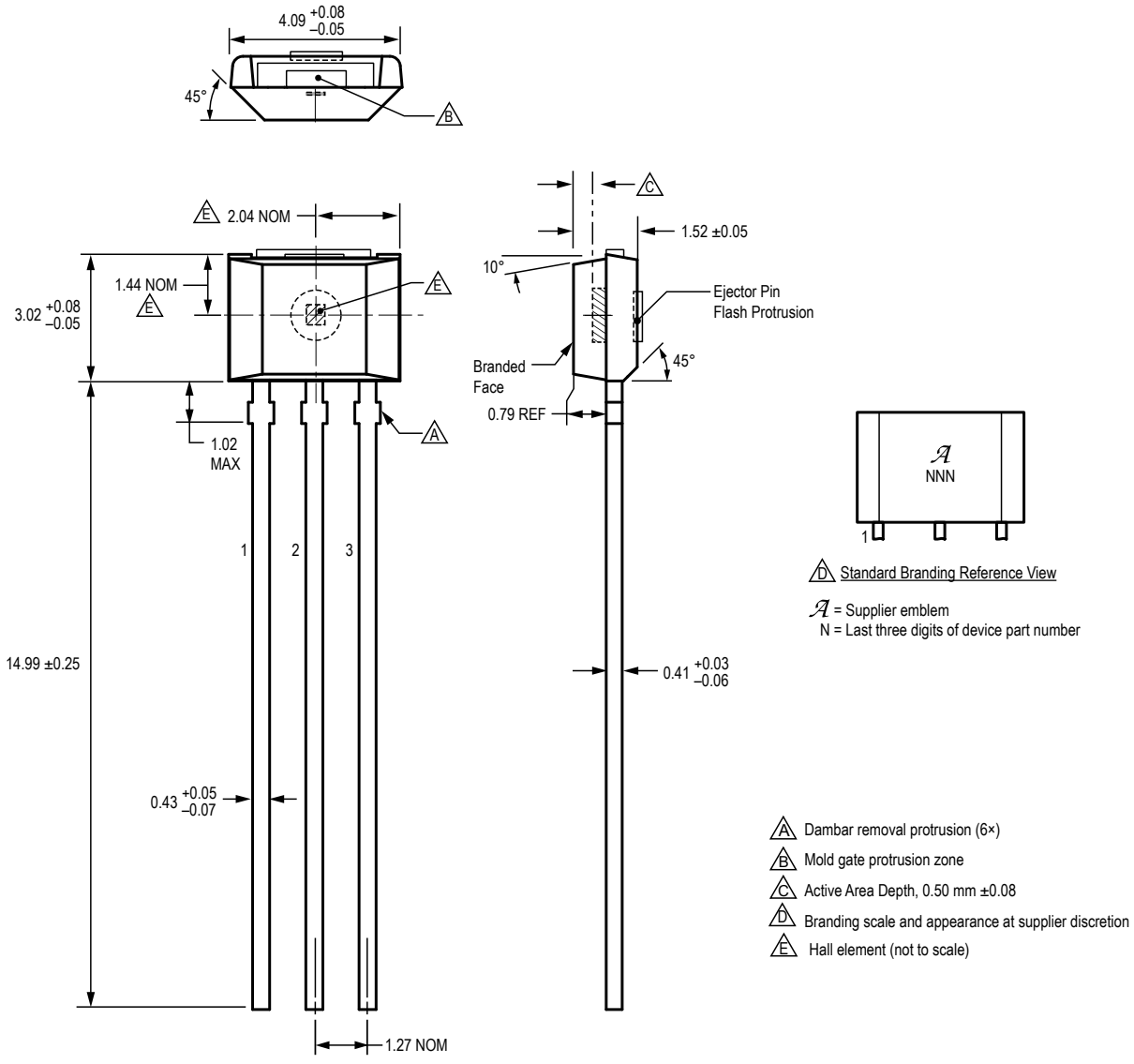

Figure 12: Package UA, 3-Pin SIP

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Revision History

Number	Date	Description
–	March 24, 2020	Initial release
1	January 23, 2024	Updated ISO 26262 status

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