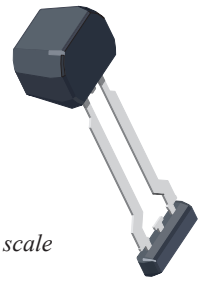
ATS19200

High-Accuracy Hall-Effect Wheel Speed Gear Tooth Sensor IC

FEATURES AND BENEFITS

- **Integrated back-bias magnet** for ease of design-in with ferromagnetic gear targets
- **Integrated capacitor** in a single overmolded package provides greater EMC robustness
- **Advanced threshold switching algorithm** supporting pitch and duty cycle high accuracy over operating air gap range
- **ASIL B(D) rating** based on integrated diagnostics and certified safety design process
- **EEPROM** offers device traceability throughout the production process
- **Two-wire current source output** supporting speed and ASIL protocol

PACKAGE: 3-pin SIP (suffix SN)



Not to scale

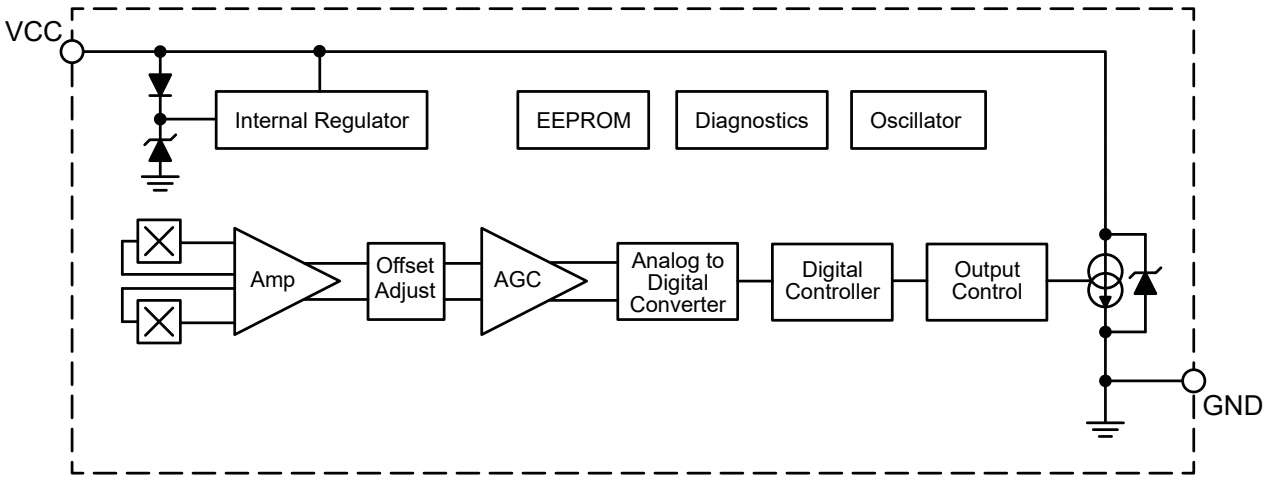
DESCRIPTION

The ATS19200 is an optimized Hall-effect integrated circuit (IC), rare-earth pellet, and high-temperature ceramic capacitor in a single overmolded package, reducing the need for external EMC protection. The ATS19200 provides a user-friendly solution for true zero-speed digital gear tooth sensing in two-wire applications.

The single integrated circuit incorporates a dual element Hall-effect sensor IC and signal processing circuitry that switches in response to differential magnetic signals created by a rotating ferromagnetic target. The device contains a sophisticated compensating circuit to eliminate magnetic and system offsets. Digital tracking of the analog signal is used to achieve high accuracy for pitch and duty cycle. Advanced calibration algorithms are used to adjust the device gain and offset at power-up, resulting in air gap independent switchpoints, which greatly improves output accuracy and mitigates the effect of system anomalies such as target vibration and sudden changes in air gap.

Integrated diagnostics are used to detect an IC failure which impacts the output protocol's accuracy, providing coverage compatible with ASIL B(D) compliance. Built-in EEPROM scratch memory offers traceability of the device throughout the IC's production process.

The ATS19200 is provided in a lead (Pb) free 3-pin back-biased SIP package (suffix SN) with tin leadframe plating. The ATS19200 provides a user-friendly solution for true zero-speed digital gear tooth sensing in two-wire applications, such as automotive or two-wheeler braking systems.



Functional Block Diagram

SELECTION GUIDE

Part Number	Power-On State	ASIL	Packing*
ATS19200LSNATN-L-A	$I_{CC(LOW)}$	Enabled	800 pieces per 13-inch reel
ATS19200LSNATN-H-A	$I_{CC(HIGH)}$	Enabled	
ATS19200LSNATN-L	$I_{CC(LOW)}$	Disabled	
ATS19200LSNATN-H	$I_{CC(HIGH)}$	Disabled	

*Contact Allegro™ for additional packing options

SPECIFICATIONS

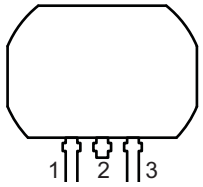
ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{CC}		28	V
Reverse Supply Voltage	V_{RCC}		–18	V
Operating Ambient Temperature	T_A	Range L, refer to Power Derating Curve	–40 to 150	°C
Maximum Junction Temperature	$T_{J(max)}$		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

INTERNAL DISCRETE CAPACITOR RATINGS

Characteristic	Symbol	Notes	Rating	Units
Nominal Capacitance	C_{SUPPLY}	Connected between VCC and GND	2.2	nF

PINOUT DIAGRAM AND TERMINAL LIST



Package SN, 3-Pin SIP Pinout Diagram

Terminal List Table

Number	Name	Function
1	VCC	Supply voltage
2	VCC	Supply voltage
3	GND	Ground

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OPERATING CHARACTERISTICS: V_{CC} and T_A within specification, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit [2]
ELECTRICAL CHARACTERISTICS						
Supply Voltage [3]	V_{CC}	Operating, $T_J < T_J$(max)	4	–	24	V
Undervoltage Lockout	$V_{CC(UV)}$	V_{CC} 0 → 5 V or 5 → 0 V	–	3.5	3.95	V
Reverse Supply Current [4]	I_{RCC}	$V_{CC} = V_{RCC\ (MAX)}$	–10	–	–	mA
Supply Zener Clamp Voltage	$V_{ZSUPPLY}$	$I_{CC} = I_{CC\ (HIGH)}$ + 3 mA, T_A = 25°C	28	–	–	V
Supply Zener Current	$I_{ZSUPPLY}$	T_A = 25°C, V_{CC} = 28 V	–	–	19	mA
Supply Current	$I_{CC(LOW)}$	Low-current state	5.9	–	8.4	mA
	$I_{CC(HIGH)}$	High-current state	12	–	16	mA
Supply Current Ratio	$I_{CC(HIGH)}$ / $I_{CC(LOW)}$	Ratio of high current to low current	1.9	–	–	–
ASIL Safety Current	I_{RESET}	-A variant	1.0	–	3.3	mA
POWER-ON STATE CHARACTERISTICS						
Power-On State	POS	-H variant	–	$I_{CC(HIGH)}$	–	mA
		-L variant	–	$I_{CC(LOW)}$	–	mA
OUTPUT STAGE						
Output Rise Time	t_r	Corresponds to measured output slew rate, from 10% to 90% I_{CC} level C_{SUPPLY}, R_{SENSE} = 100 Ω	0	–	1.5	µs
Output Fall Time	t_r	Corresponds to measured output slew rate, from 90% to 10% I_{CC} level C_{SUPPLY}, R_{SENSE} = 100 Ω	0	–	1.5	µs
PERFORMANCE CHARACTERISTICS						
Operating Frequency	f_{OP}		0	–	5	kHz
Operate Point	B_{OP}	% of peak-to-peak B_{SIG}, AG_{OP} within specification	–	60	–	%
Release Point	B_{RP}	% of peak-to-peak B_{SIG}, AG_{OP} within specification	–	40	–	%

Continued on the next page…

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OPERATING CHARACTERISTICS (continued): V_{CC} and T_A within specification, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit [2]
FUNCTIONAL CHARACTERISTICS						
Operational Air Gap Range	AG_{OP}	Using Allegro Reference Target 60-0, duty cycle within specification	0.5	–	2.5	mm
Extended Operational Air Gap Range	AG_{EXT}	Using Allegro Reference Target 60-0, output switching (no missed edges), duty cycle not guaranteed	–	–	3	mm
Allowable User-Induced Differential Offset	$B_{DIFFEXT}$	Operation within specification	±60	–	–	G
Output Duty Cycle	D	Using Reference Target 60-0, static air gap, AG within specification	40	–	60	%
Maximum Sudden Signal Amplitude Change	$B_{SEQ(n+1)}$ / $B_{SEQ(n)}$	No missed output edge. Instantaneous symmetric magnetic signal amplitude change, measured as a percentage of peak-to-peak B_{SIG} (see Figure 1).	–	0.6	–	–
Allowable Differential Signal Amplitude Variation	$B_{SEQ(min)}$ / $B_{SEQ(max)}$	Overall symmetric magnetic signal amplitude ratio of B_{SIG}	–	0.2	–	–

[1] Typical values are at T_A = 25°C and V_{CC} = 12 V. Performance may vary for individual units, within the specified maximum and minimum limits.
[2] 1 G (gauss) = 0.1 mT (millitesla).
[3] Maximum voltage must be adjusted for power dissipation and junction temperature; see Power Derating section.
[4] Negative current is defined as conventional current coming out of (sourced from) the specified device terminal.

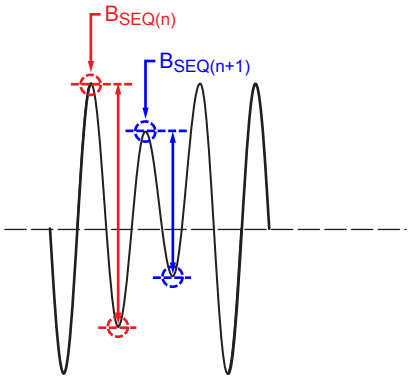

Figure 1: Differential Signal Variation

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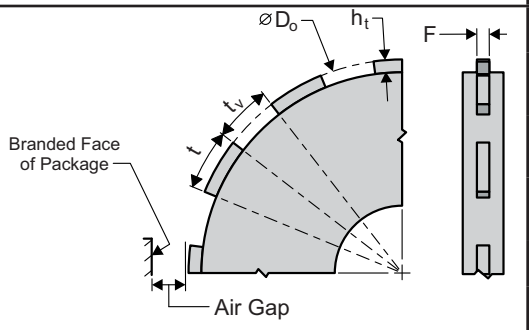
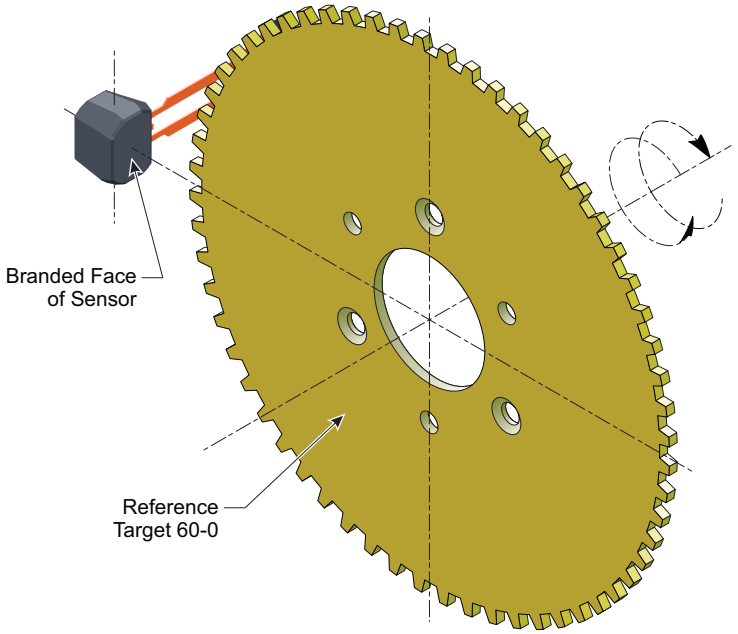
Reference Target 60-0 (60 Tooth Target)

Characteristics	Symbol	Test Conditions	Typ.	Units	Symbol Key
Outside Diameter	D_o	Outside diameter of target	120	mm	
Face Width	F	Breadth of tooth, with respect to branded face	6	mm	
Circular Tooth Length	t	Length of tooth, with respect to branded face	3	deg.	
Circular Valley Width	t_v	Length of valley, with respect to branded face	3	deg.	
Tooth Whole Depth	h_t		3	mm	
Material		Low Carbon Steel	–	–	



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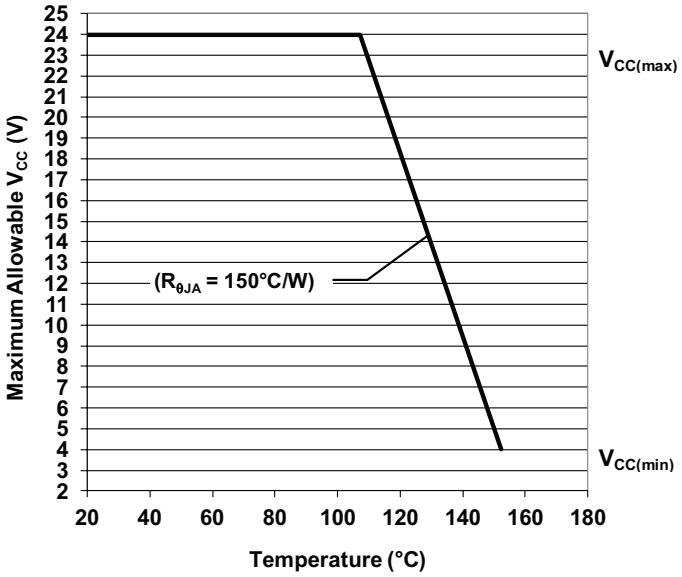
THERMAL CHARACTERISTICS: May require derating at maximum conditions; see Power Derating section

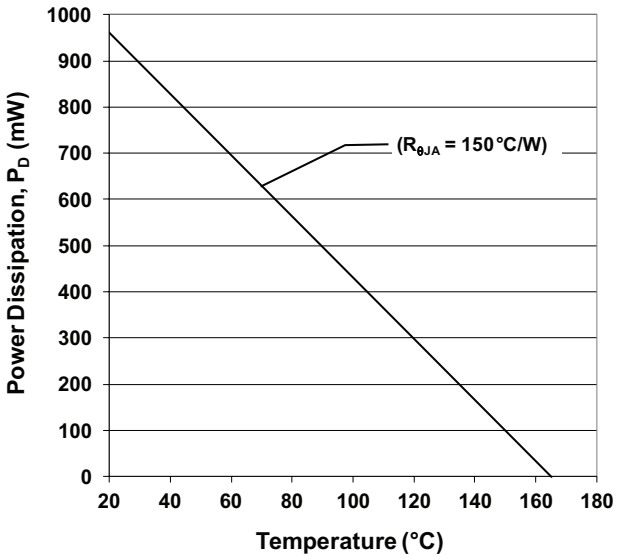
Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Single layer PCB, with copper limited to solder pads	150	°C/W

*Additional thermal information available on the Allegro website

Power Derating Curve



Power Dissipation versus Ambient Temperature



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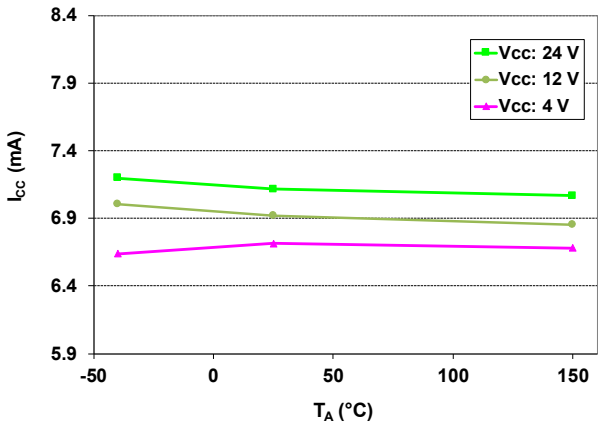
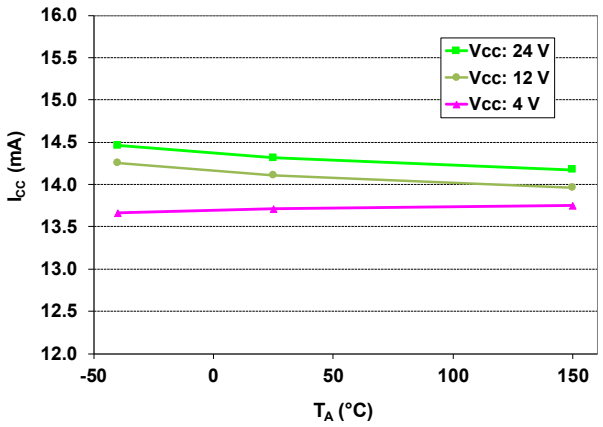
CHARACTERISTIC PERFORMANCE PLOTS

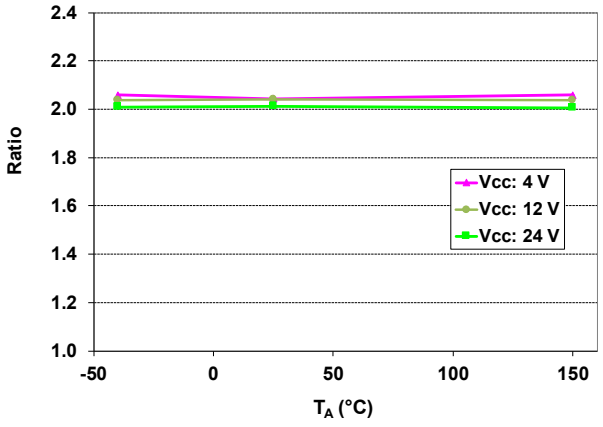
Supply Current (LOW) versus Ambient Temperature



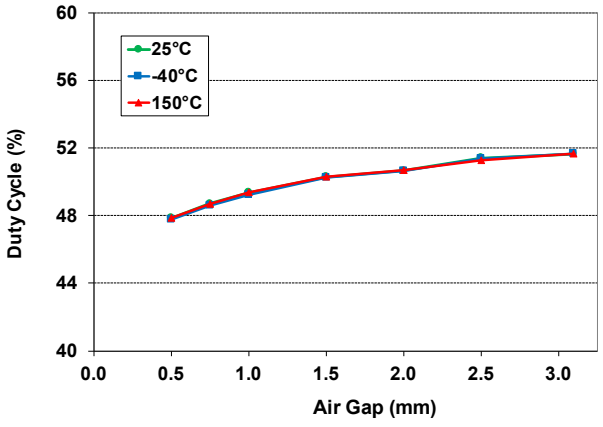
Supply Current (HIGH) versus Ambient Temperature



Supply Current Ratio versus Ambient Temperature



Average Duty Cycle versus Air Gap
Pin 1 to 3 Rotation of Allegro Reference Target



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FUNCTIONAL DESCRIPTION

Sensing Technology

The ATS19200 sensor IC contains a single-chip differential Hall-effect circuit, a back-biasing pellet, and a flat ferrous pole piece (a precisely-mounted magnetic field concentrator that homogenizes the flux passing through the Hall chip). As shown in Figure 2, the circuit supports two Hall elements, which sense the magnetic profile of the ferromagnetic gear target simultaneously, but at different points (spaced at a 1.75 mm pitch), generating a differential internal analog voltage, V_{PROC}, that is processed for precise switching of the digital output signal.

The Hall IC is self-calibrating and also integrates a temperature compensated amplifier and offset cancellation circuitry. Its voltage regulator provides supply noise rejection throughout the operating voltage range. Changes in temperature do not greatly affect this device due to the stable amplifier design and the offset rejection circuitry. The Hall transducers and signal processing electronics are integrated on the same silicon substrate, using a proprietary BiCMOS process.

Target Profiling During Operation

Under normal operating conditions, the IC is capable of providing digital information that is representative of the mechanical features of a rotating gear. The waveform diagram in Figure 3 presents the automatic translation of the mechanical profile, through the magnetic profile that it induces, to the digital output signal of the ATS19200. No additional optimization is needed and minimal processing circuitry is required. This ease of use reduces design time and incremental assembly costs for most applications.

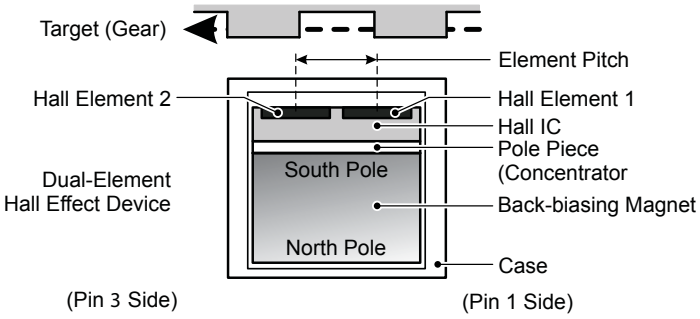

Figure 2: Relative Motion of the Target is Detected by the Dual Hall Elements Mounted on the Hall IC.

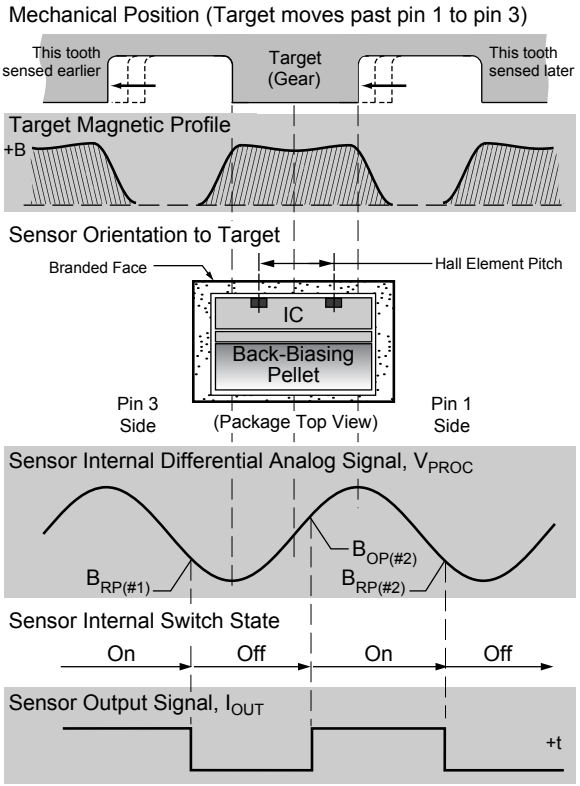

Figure 3: The Magnetic Profile Reflects the Geometry of the Target, Allowing the ATS19200 to Present an Accurate Digital Output Response (-H variant shown).

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Diagnostics

The regulated current output is configured for two-wire applications, requiring one less wire for operation than do switches with the traditional open-collector output. Additionally, the system designer inherently gains diagnostics because there is always output current flowing, which should be in either of two narrow ranges, shown in Figure 4 as $I_{CC(HIGH)}$ and $I_{CC(LOW)}$. Any current level not within these ranges indicates a fault condition. If $I_{CC} > I_{CC(HIGH)}(max)$, then a short condition exists, and if $I_{CC} < I_{CC(LOW)}(min)$, then an open condition exists. Any value of I_{CC} between the allowed ranges for $I_{CC(HIGH)}$ and $I_{CC(LOW)}$ indicates a general fault condition, excepting currents indicating ASIL Safety Current.

The sensor IC contains diagnostic circuitry that will continuously monitor occurrences of failure defects within the IC. Refer to Figure 5 for the output protocol of the ASIL safe state, which is enabled for "-A" variants.

Refer to the Safety Manual for additional details on the ASIL Safe State Output Protocol.

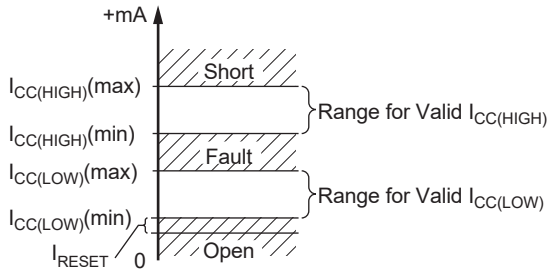

Figure 4: Diagnostic Characteristics of Supply Current Values.

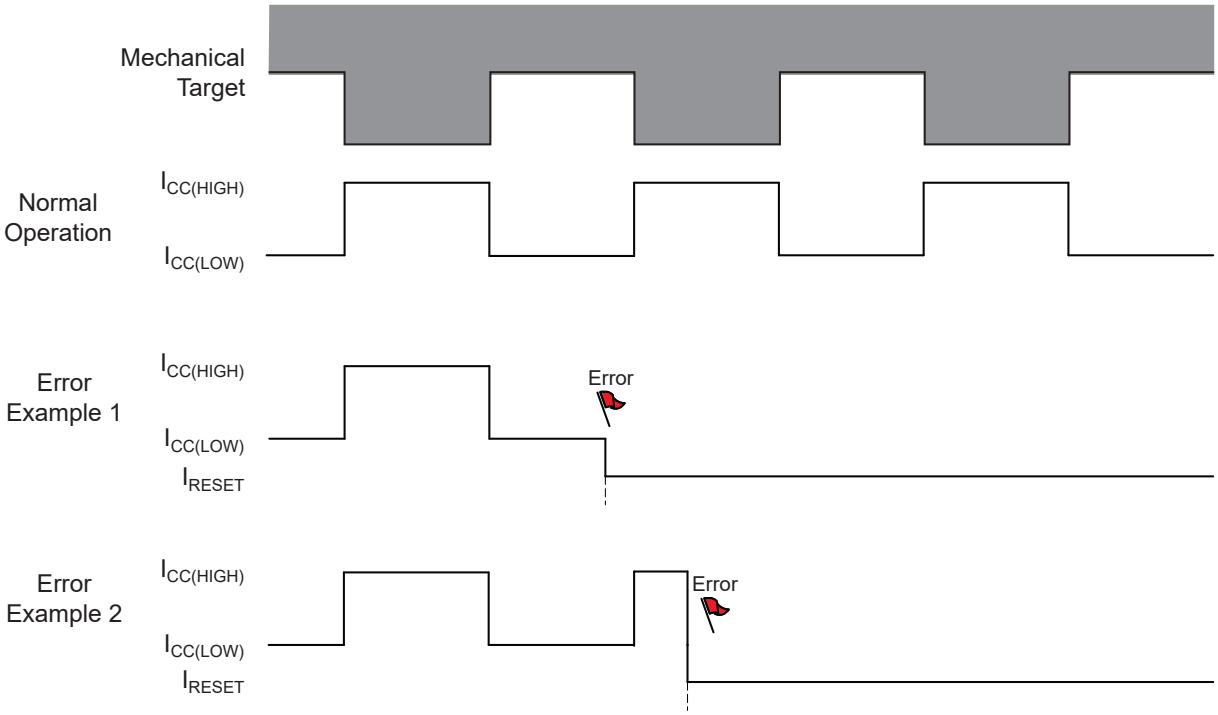

Figure 5: Output Protocol with ASIL Safety Current, "-A" Variant

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Determining Output Signal Polarity

In Figure 3, the top panel, labeled *Mechanical Position*, represents the mechanical features of the target gear and orientation to the device. The bottom panel, labeled *Device Output Signal*, displays the square waveform corresponding to the digital output signal (current amplitude) that results from a rotating gear configured as shown in Figure 6. Referring to the target side nearest the face of the sensor IC, the direction of rotation is: perpendicular to the leads, across the face of the device, from the pin 1 side to the pin 3 side.

With the -H variant, this results in the IC output switching from $I_{CC(HIGH)}$ to $I_{CC(LOW)}$ as the leading edge of a tooth (a rising mechanical edge, as detected by the IC) passes the package face. The output polarity is inverted for the -L variant.

If the direction of rotation is reversed, so that the gear rotates from the pin 3 side to the pin 1 side, then the output polarity inverts from that of the pin 1 to 3 rotation.

To read the output signal as a voltage (V_{SENSE}), a sense resistor (R_{SENSE}) can be placed on either the VCC signal or on the GND signal. As shown in Figure 7, when R_{SENSE} is placed on the GND signal, the output signal voltage ($V_{SENSE(LowSide)}$) is in phase with I_{CC}. When R_{SENSE} is placed on the VCC signal, the output signal voltage ($V_{SENSE(HighSide)}$) is inverted relative to I_{CC}.

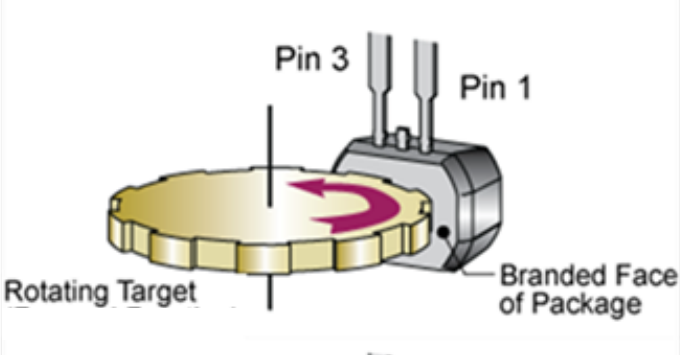

Figure 6: Left-to-Right, Pin 1 to Pin 3 Direction of Target Rotation.

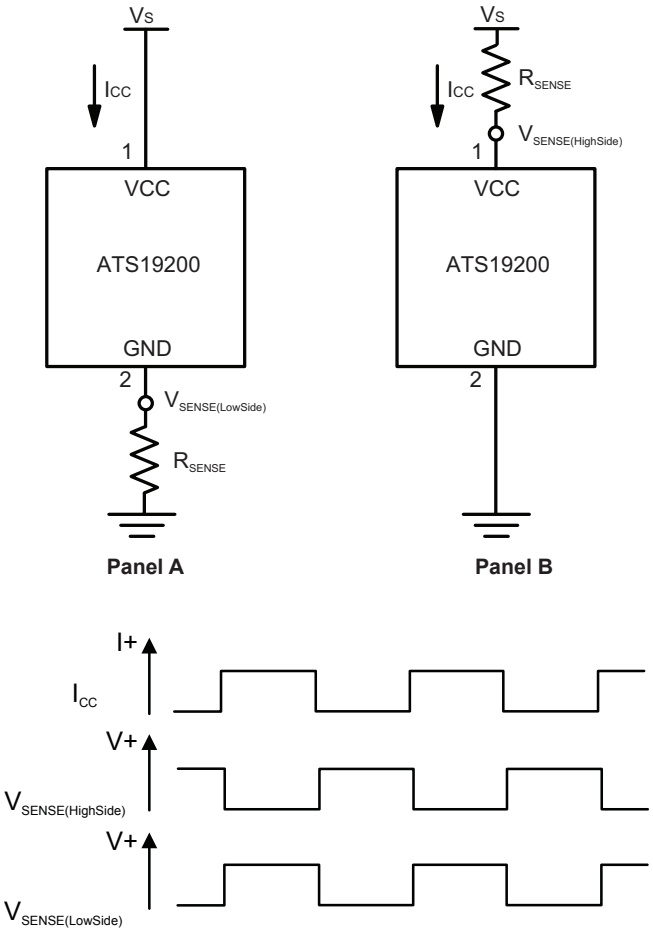

Figure 7: Alternative Polarity Configurations Using Two-Wire Sensing.

The Output Polarity States table provides the permutations of output voltage relative to I_{CC}, given alternative locations for R_{SENSE}. Panel A shows the low-side ($V_{SENSE(LowSide)}$) sensing configuration, and panel B shows the high-side ($V_{SENSE(HighSide)}$) configuration. As shown in panel C, $V_{SENSE(LowSide)}$ is in phase with I_{CC}, and $V_{SENSE(HighSide)}$, is inverted.

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POWER DERATING

The device must be operated below the maximum junction temperature of the device ($T_{J(max)}$). Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro website.)

The Package Thermal Resistance ($R_{\theta JA}$) is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity (K) of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case ($R_{\theta JC}$) is relatively small component of $R_{\theta JA}$. Ambient air temperature (T_A) and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: T_A= 25°C, V_{CC} = 12 V, I_{CC} = 6 mA, and $R_{\theta JA}$ = 150°C/W, then:

$$P_D = V_{CC} \times I_{CC} = 12\ V \times 6\ mA = 72\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 72\ mW \times 150°C/W = 10.8°C$$

$$T_J = T_A + \Delta T = 25°C + 10.8°C = 35.8°C$$

A worst-case estimate, $P_{D(max)}$, represents the maximum allowable power level ($V_{CC(max)}$, $I_{CC(max)}$), without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A

Example: Reliability for V_{CC} at T_A=150°C, package SN, using a single-layer PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$ =150°C/W, $T_{J(max)}$ =165°C, and $I_{CC(max)}$ = 16 mA.

Calculate the maximum allowable power level, $P_{D(max)}$. First, invert equation 3:

$$\Delta T_{max} = T_{J(max)} - T_A = 165\,°C - 150\,°C = 15\,°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15°C \div 150°C/W = 100\ mW$$

Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_{D(max)} \div I_{CC(max)} = 100\ mW \div 16\ mA = 6.3\ V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages ≤$V_{CC(est)}$.

Compare $V_{CC(est)}$ to $V_{CC(max)}$. If $V_{CC(est)} \leq V_{CC(max)}$, then reliable operation between $V_{CC(est)}$ and $V_{CC(max)}$ requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \geq V_{CC(max)}$, then operation between $V_{CC(est)}$ and $V_{CC(max)}$ is reliable under these conditions.

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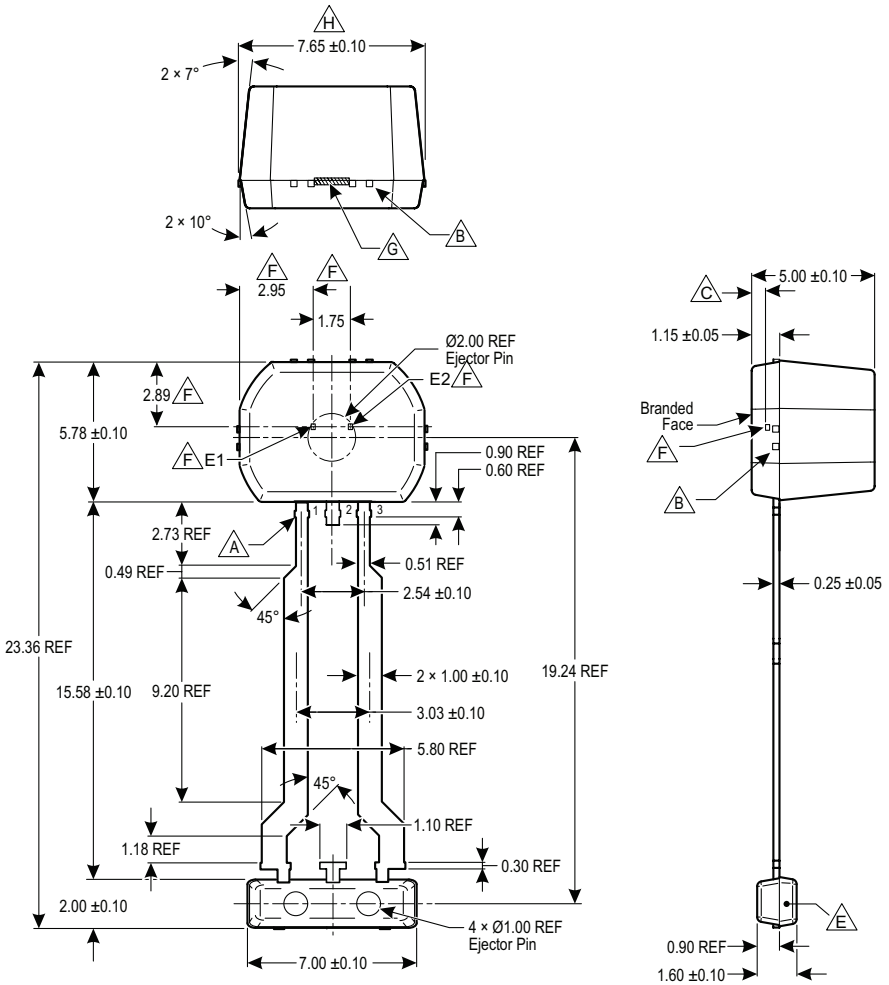
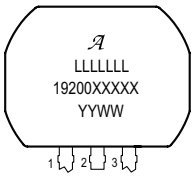
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference DWG-9206, Rev.2)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown





D **Standard Branding Reference View**

Lines 1, 2, 3, 4: Up to 10 characters, centered

Line 1: Logo A
Line 2: Characters 5, 6, 7, 8, 9, 10, 11 of Assembly Lot Number
Line 3: Part Number:
5 digit part number (19200),
0-5 character part variant (XXXXX)
Line 4: 4 digit Date Code

Notes:

A Dambar removal protrusion (12×)
B Tie bars (8×)
C Active Area Depth, 0.40 ±0.05 mm
D Branding scale and appearance at supplier discretion
E Molded lead bar for preventing damage to leads during shipment
F Hall elements (E1 and E2); not to scale
G Gate location
H Dimension does not include tie bar protrusion, which can add up to 0.30 mm to the total width

Figure 8: Package SN, 3-Pin SIP

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Revision History

Number	Date	Description
–	November 26, 2018	Initial release
1	January 14, 2020	Updated Allowable Differential Signal Amplitude Variation characteristic (page 4)
2	March 25, 2021	Updated “ASIL B” to “ASIL B(D)” (page 1)

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