

XtremeSense™ TMR Current Sensor with Ultra-Low Noise and <1% Total Error

FEATURES AND BENEFITS

- Integrated contact current sensing for low to medium current ranges:
 - 0 to 20 A □ 0 to 50 A
 - ±20 A □ ±50 A
 - 0 to 30 A □ 0 to 65 A
 - ±30 A □ ±65 A
- Integrated current carrying conductor (CCC)
- Linear analog output voltage
- Total error output: ±1.0% FS
- 1 MHz bandwidth
- Response time: ~300 ns
- UL/IEC 62368-1 and UL1577 certification
 - Rated isolation voltage: 2.5 kV_{RMS}
 - Working voltage for basic isolation: 701 V_{RMS}
 - Working voltage for reinforced isolation: 344 V_{RMS}
- IEC 61000-4-5 certified
- Low noise: 9.5 to 19.0 mA_{RMS} @ f_{BW} = 100 kHz
- Supply voltage: 3.0 to 3.6 V
- Filter function to reduce noise on output pin
- Immunity to common mode fields: -40 dB
- Overcurrent detection
 - Out of range currents
- AEC-Q100 grade 1
- 8-lead SOIC package



TÜV Certificate No.:
R 72226133 0001



UL Certificate No.:
UL-CA-2201235-0

DESCRIPTION

The CT417 is a high bandwidth and ultra-low noise integrated contact current sensor that uses Allegro patented XtremeSense™ TMR technology to enable high accuracy current measurements for many consumer, enterprise, and industrial applications. The device supports eight current ranges where the integrated current carrying conductor (CCC) will handle up to 65 A of current and generates a current measurement as a linear analog output voltage. The device achieves a total output error of less than ±1.0% full-scale (FS).

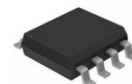
The device has a 300 ns output response time while the current consumption is ~6.0 mA and is immune to common mode fields. The CT417 has an integrated overcurrent detection (OCD) circuitry to identify out of range currents (OCD) with the result output to the fault-bar ($\overline{\text{FLT}}$) pin. The $\overline{\text{FLT}}$ is an open drain, active low digital signal that is activated by the CT417 to alert the microcontroller that a fault condition has occurred.

The CT417 is offered in an industry-standard 8-lead SOIC package that is green and RoHS compliant.

APPLICATIONS

- Solar/power inverters
- UPS, SMPS, and telecom power supplies
- Motor control
- Power utility meter
- Overcurrent fault protection

PACKAGE:



8-lead SOIC

Not to scale

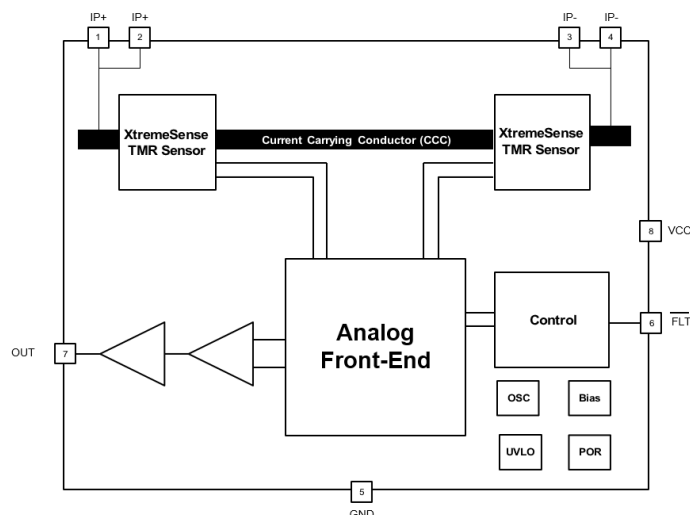


Figure 1: CT417 Functional Block Diagram for 8-lead SOIC Package

SELECTION GUIDE

Part Number	Current Range (I _P MAX) (A)	Sensitivity (mV/A)	Operating Temperature Range (°C)	Package	Packing
CT417-HSN820MR	±20	50	-40 to 125	8-lead SOIC 4.89 mm × 6.00 mm × 1.62 mm	Tape and Reel
CT417-HSN830MR	±30	33.3			
CT417-HSN850MR	±50	20			
CT417-HSN865MR	±65	15.4			
CT417-HSN820DR	20	100			
CT417-HSN830DR	30	66.7			
CT417-HSN850DR	50	40			
CT417-HSN865DR	65	30.8			
AEC-Q100 GRADE 1					
CT417-ASN820MR	±20	50	Grade 1 -40 to 125	8-lead SOIC 4.89 mm × 6.00 mm × 1.62 mm	Tape and Reel
CT417-ASN830MR	±30	33.3			
CT417-ASN850MR	±50	20			
CT417-ASN865MR	±65	15.4			
CT417-ASN820DR	20	100			
CT417-ASN830DR	30	66.7			
CT417-ASN850DR	50	40			
CT417-ASN865DR	65	30.8			

EVALUATION BOARD SELECTION GUIDE

Part Number	Current Range (A)	Operating Temperature Range (°C)
CTD417-20DC	0 to 20	-40 to 125
CTD417-20AC	±20	
CTD417-30DC	0 to 30	
CTD417-30AC	±30	
CTD417-50DC	0 to 50	
CTD417-50AC	±50	
CTD417-65DC	0 to 65	
CTD417-65AC	±65	

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ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage Strength	V_{CC}		-0.3 to 6.0	V
Analog Input/Output Pins Maximum Voltage	$V_{I/O}$		-0.3 to $V_{CC} + 0.3$ [2]	V
Current Carrying Conductor Maximum Current	$I_{CCC(MAX)}$	$T_A = 25^\circ\text{C}$	70	A
Dielectric Surge Strength Test Voltage	V_{SURGE}	IEC 61000-4-5: Tested ± 5 Pulses at 2/60 seconds, 1.2 μs (rise) and 50 μs (width)	6.0 (min)	kV
Surge Strength Test Current	I_{SURGE}	Tested ± 5 Pulses at 3/60 seconds, 8.0 μs (rise) and 20 μs (width)	3.0 (min)	kA
Electrostatic Discharge Protection Level	ESD	Human Body Model (HBM) per JESD22-A114	± 2.0	kV
		Charged Device Model (CDM) per JESD22-C101	± 0.5	kV
Junction Temperature	T_J		-40 to 150	$^\circ\text{C}$
Storage Temperature	T_{STG}		-65 to 155	$^\circ\text{C}$
Lead Soldering Temperature	T_L	10 seconds	260	$^\circ\text{C}$

[1] Stresses exceeding the absolute maximum ratings may damage the CT417 and may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

[2] The lower of $V_{CC} + 0.3$ V or 6.0 V.

RECOMMENDED OPERATING CONDITIONS [1]

Characteristic	Symbol	Notes	Min.	Typ.	Max.	Unit
Supply Voltage Range	V_{CC}		3.0	3.3	3.6	V
Output Voltage Range	V_{OUT}		0	-	V_{CC}	V
Output Current	I_{OUT}		-	-	± 1.0	mA
Operating Ambient Temperature	T_A	Extended Industrial	-40	25	125	$^\circ\text{C}$
		Automotive	-40	25	125	$^\circ\text{C}$

[1] The Recommended Operating Conditions table defines the conditions for actual operation of the CT417. Recommended operating conditions are specified to ensure optimal performance to the specifications. Allegro does not recommend exceeding them or designing to absolute maximum ratings.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	Value	Unit
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	Junction-to-ambient thermal resistance is a function of application and board layout and is determined in accordance to JEDEC standard JESD51 for a four (4) layer 2s2p FR-4 printed circuit board (PCB) with 2 oz. of copper (Cu) and 4 oz. of copper (Cu) or more for 65 A. Special attention must be paid not to exceed junction temperature $T_{J(MAX)}$ at a given ambient temperature T_A .	25	$^\circ\text{C/W}$
Junction-to-Case Thermal Resistance	$R_{\theta JC}$		15	$^\circ\text{C/W}$

ISOLATION RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Rated Isolation Voltage	V_{ISO}	Agency Tested per IEC 62368 [1] for 60 seconds. Production Tested at V_{ISO} for 1 second per IEC 62368.	2.5	kV_{RMS}
		Agency Tested per UL1577 for 60 seconds. Production Tested at V_{ISO} for 1 second per UL1577.	2.5	kV_{RMS}
Working Voltage for Basic Isolation	V_{WORK_ISO}	Tested per IEC 62368 [1].	991	V_{PK}
			701	V_{RMS}
Working Voltage for Reinforced Isolation	V_{WORK_RI}	Tested per IEC 62368 [1].	487	V_{PK}
			344	V_{RMS}
Creepage Distance	D_{CR}	Minimum distance along package body from IP pins to I/O pins.	4.96	mm
Clearance Distance	D_{CL}	Minimum distance through air from IP pins to I/O pins.	4.63	mm
Distance Through Isolation	D_{ISO}	Minimum internal distance through isolation	110	μm
Comparative Tracking Index	CTI	Material Group II	400 to 599	V

[1] IEC 62368 is the succeeding standard to IEC 60950-1 (Edition 2) for isolation testing specifications and as such it will be compliant to the latter standard.

APPLICATION DIAGRAM

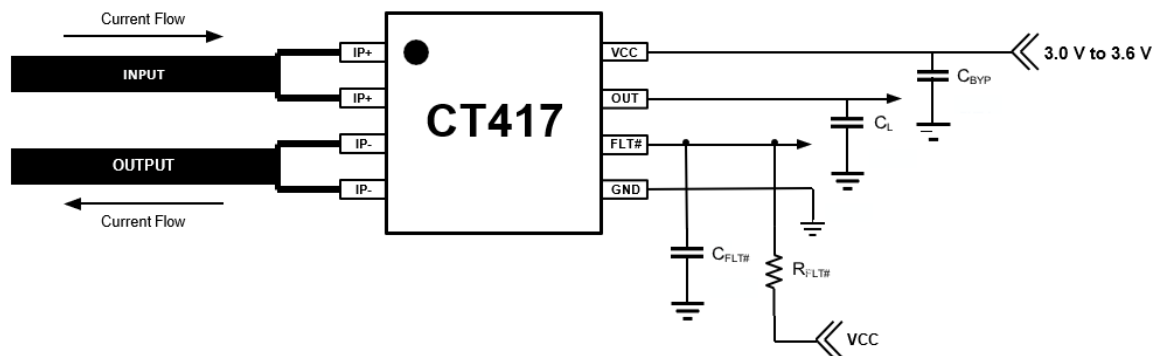


Figure 2: CT417 Application Block Diagram

Table 1: Recommended External Components

Component	Description	Vendor and Part Number	Parameter	Min.	Typ.	Max.	Unit
C_{BYP}	1.0 μF , X5R or Better	Murata GRM155C81A105KA12	C1	–	1.0	–	μF
$C_{FLT\#}$	1.0 nF, X5R or Better	Murata GRM0335C1E102JA01	C2	–	1.0	–	nF
$R_{FLT\#}$	10 k Ω Pull-Up Resistor	Various	R1	–	10	–	k Ω

PINOUT DIAGRAM AND TERMINAL LIST

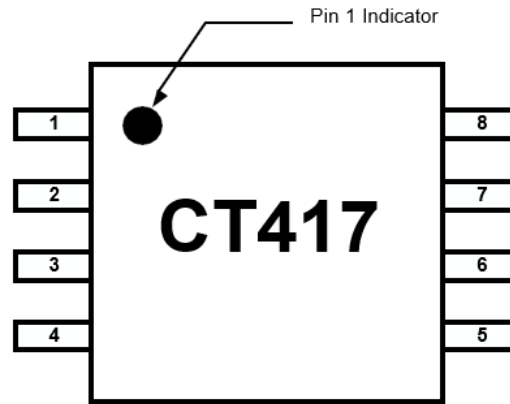


Figure 3: CT417 Pinout Diagram for 8-lead SOIC Package (Top-Down View)

Terminal List

Number	Name	Function
1, 2	IP+	Input primary conductor (positive).
3, 4	IP-	Output primary conductor (negative).
5	GND	Ground.
6	FLT	Active low output fault signal (open drain output) to indicate that the following parameters are outside of normal operational bounds: <ul style="list-style-type: none"> • Overcurrent Detection • UVLO If not used, then a 1.0 nF capacitor must be connected from the pin to ground.
7	OUT	Analog output voltage that represents the measured current.
8	VCC	Supply voltage.

ELECTRICAL CHARACTERISTICS: Valid for $V_{CC} = 3.0$ to 3.6 V, $C_{BYP} = 1.0$ μ F, and $T_A = -40^\circ\text{C}$ to 125°C , typical values are $V_{CC} = 3.3$ V and $T_A = 25^\circ\text{C}$, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
POWER SUPPLIES						
Supply Current	I_{CC}	$f_{BW} = 1$ MHz, no load, $I_P = 0$ A	–	6.0	9.0	mA
OUT Maximum Drive Capability [1]	I_{OUT}	OUT covers 10% to 90% of V_{CC} span	–1.0	–	+1.0	mA
OUT Capacitive Load [1]	C_{L_OUT}		–	–	100	pF
OUT Resistive Load [1]	R_{L_OUT}		–	100	–	k Ω
Primary Conductor Resistance [1]	R_{IP}		–	0.5	–	m Ω
Power Supply Rejection Ratio [1]	PSRR		–	35	–	dB
Sensitivity Power Supply Rejection Ratio [1]	SPSRR		–	35	–	dB
Offset Power Supply Rejection Ratio [1]	OPSRR		–	40	–	dB
ANALOG OUTPUT (OUT)						
OUT Voltage Linear Range, Typical	V_{OUT}	$V_{SIG_AC} = \pm 1.00$ V, $V_{SIG_DC} = +2.00$ V	0.65	–	2.65	V
Output High Saturation Voltage	V_{OUT_SAT}	V_{OUT} , $T_A = 25^\circ\text{C}$	$V_{CC} - 0.30$	$V_{CC} - 0.25$	–	V
Common Mode Field Rejection Ratio [1]	CMFRR		–	–40	–	dB
			–	0.5	–	mA/G
FAULT OUTPUT (FLT)						
FLT Voltage Low	$V_{FLT\#_OL}$	$I_{FLT\#_OUT} \leq 20$ mA	0	–	0.5	V
High-Impedance Output Leakage Current	$I_{LEAK_FLT\#}$	$V_{FLT\#_OH} = V_{CC}$	–	5	–	μ A
FLT Pull-Up Resistor	R_{PU}		–	100	–	k Ω
TIMINGS						
Power-On Time [1]	t_{ON}	$V_{CC} \geq 2.50$ V	–	100	200	μ s
Rise Time [1]	t_{RISE}	$I_P = I_{RANGE(MAX)}$, $T_A = 25^\circ\text{C}$, $C_L = 100$ pF	–	200	–	ns
Response Time [1]	$t_{RESPONSE}$	$I_P = I_{RANGE(MAX)}$, $T_A = 25^\circ\text{C}$, $C_L = 100$ pF	–	300	–	ns
Propagation Delay [1]	t_{DELAY}	$I_P = I_{RANGE(MAX)}$, $T_A = 25^\circ\text{C}$, $C_L = 100$ pF	–	250	–	ns
FLT Response Time	$t_{FLT\#}$		–	250	–	ns
PROTECTION						
Undervoltage Lockout	V_{UVLO}	Rising V_{DD}	–	2.50	–	V
		Falling V_{DD}	–	2.45	–	V
UVLO Hysteresis	V_{UV_HYS}		–	50	–	mV
Overcurrent Detection (OCD) for DC Current (Unipolar)	I_{OCD_U}	Rising I_P	–	$1.1 \times I_{RANGE(MAX)}$	–	A
		Falling I_P	–	$0.9 \times I_{RANGE(MAX)}$	–	A
Overcurrent Detection (OCD) for AC Current (Bipolar)	I_{OCD_B}	Rising I_P	–	$1.1 \times I_{RANGE(MAX)}$	–	A
		Falling I_P	–	$0.9 \times I_{RANGE(MAX)}$	–	A
Overcurrent Detection Hysteresis	I_{OCD_HYS}		–	$0.2 \times I_{RANGE(MAX)}$	–	A

[1] Guaranteed by design and characterization; not tested in production.

ELECTRICAL CHARACTERISTICS

$V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, and $C_{BYP} = 1.0\ \mu\text{F}$ (unless otherwise specified)

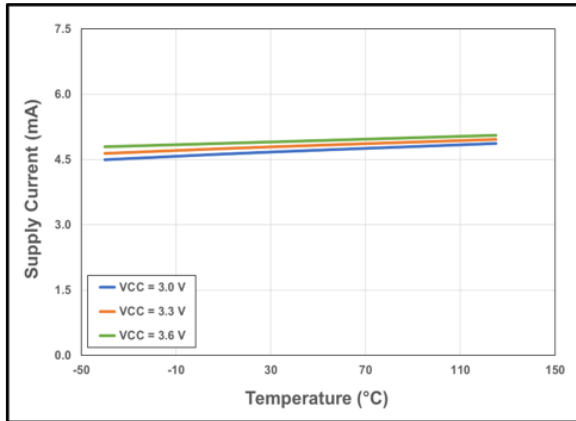


Figure 4: CT417 Supply Current vs. Temperature vs. Supply Voltage

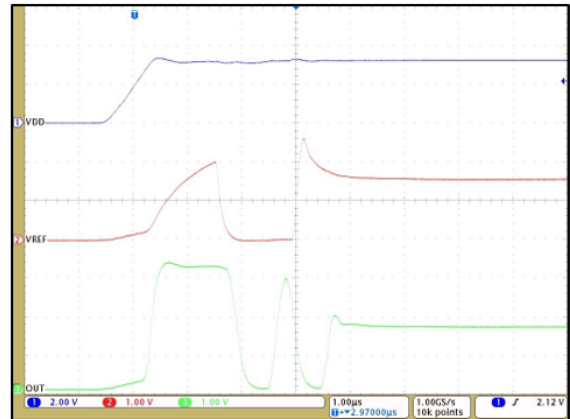


Figure 5: CT417 Startup Waveforms for $V_{OQ} = 1.65\text{ V}$ (AC Current)

ELECTRICAL CHARACTERISTICS (continued)

$V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, and $C_{BYP} = 1.0\ \mu\text{F}$ (unless otherwise specified)

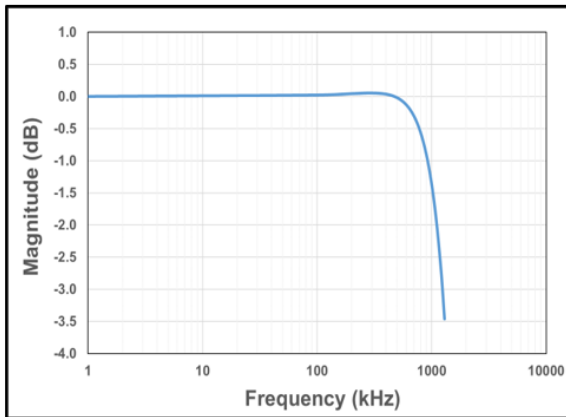


Figure 6: CT417 Bandwidth with $C_{FILTER} = 1.0\ \text{pF}$

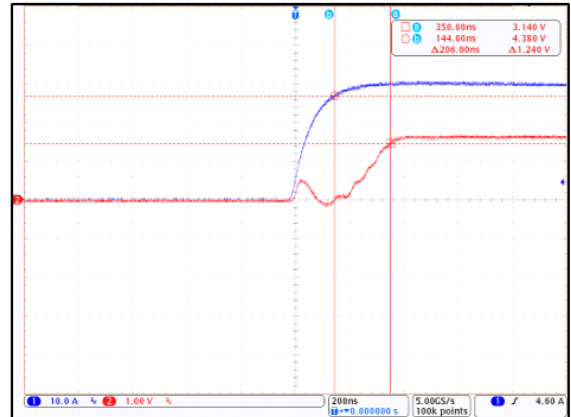


Figure 7: CT417 Response Time; $I_P = 30\ \text{A}_{PK}$ and $C_L = 100\ \text{pF}$

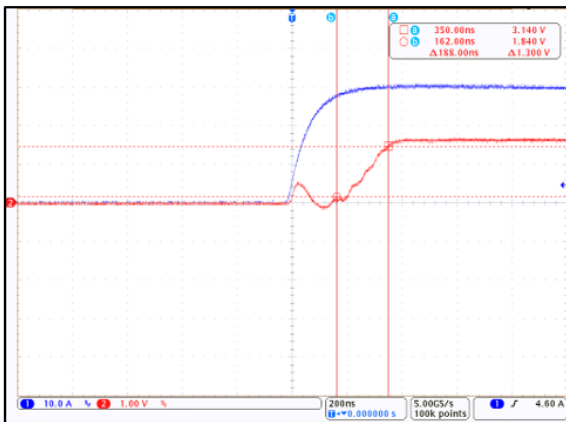


Figure 8: CT417 Rise Time; $I_P = 30\ \text{A}_{PK}$ and $C_L = 100\ \text{pF}$

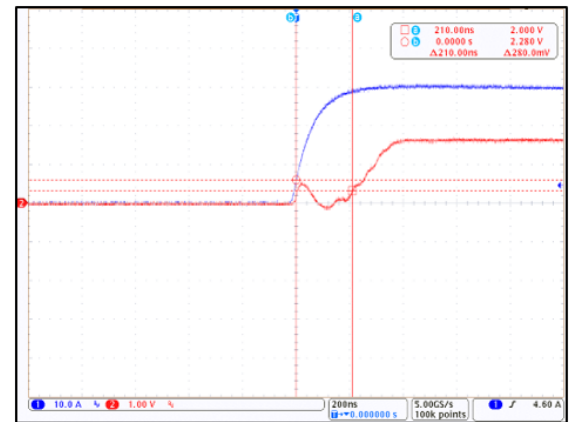


Figure 9: CT417 Propagation Delay; $I_P = 30\ \text{A}_{PK}$ and $C_L = 100\ \text{pF}$

ELECTRICAL CHARACTERISTICS (continued)

$V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, and $C_{BYP} = 1.0\ \mu\text{F}$ (unless otherwise specified)

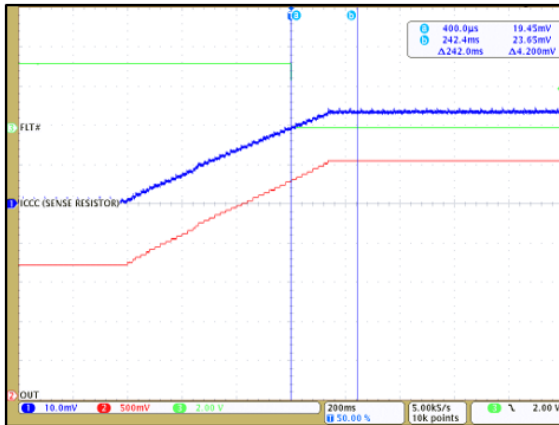


Figure 10: CT417 OCD enabled at 110% of 30 A_{PK} and FLT# is Low

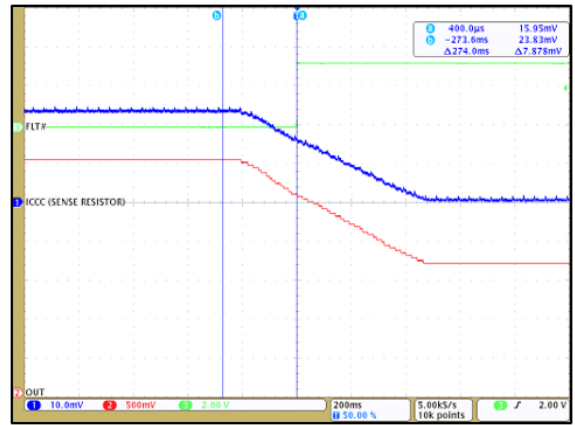


Figure 11: CT417 OCD disabled at 90% of 30 A_{PK} and FLT# is High

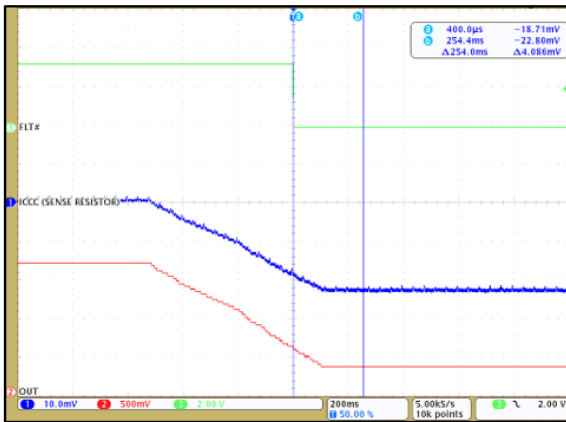


Figure 12: CT417 OCD enabled at -110% of -30 A_{PK} and FLT# is Low

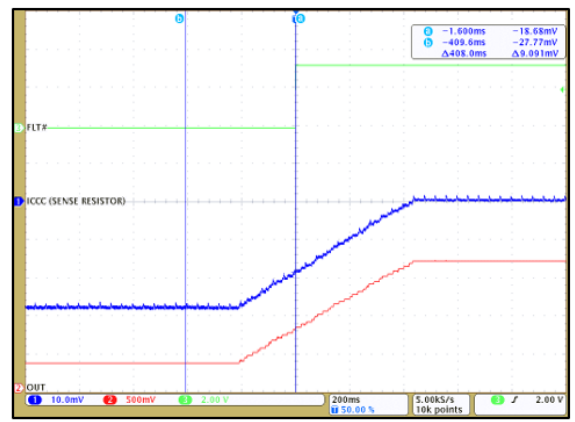


Figure 13: CT417 OCD disabled at -90% of -30 A_{PK} and FLT# is High

CT417-xSN820DR: 0 to 20 A – ELECTRICAL CHARACTERISTICS: Valid for $V_{CC} = 3.0$ to 3.6 V, $C_{BYP} = 1.0$ μ F, and $T_A = -40^\circ\text{C}$ to 125°C , typical values are $V_{CC} = 3.3$ V and $T_A = 25^\circ\text{C}$, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Current Range	I_{RANGE}		0	–	20	A
Voltage Output Quiescent	V_{OQ}	$T_A = 25^\circ\text{C}$, $I_P = 0$ A	0.645	0.650	0.655	V
Sensitivity	S	$I_{RANGE(MIN)} < I_P < I_{RANGE(MAX)}$	–	100	–	mV/A
Bandwidth [1]	f_{BW}	Small Signal = –3 dB	–	1.0	–	MHz
Noise [1]	e_N	$T_A = 25^\circ\text{C}$, $f_{BW} = 100$ kHz	–	9.5	–	mA_{RMS}
OUT ACCURACY PERFORMANCE						
Total Output Error	E_{OUT}	$I_P = I_{P(MAX)}$ @ $T_A = 25^\circ\text{C}$	–	± 1.0	–	% FS
	E_{OUT_H}	$I_P = I_{P(MAX)}$ @ $T_A = 25^\circ\text{C}$ to 125°C	–	± 1.0	± 2.5	% FS
	E_{OUT_C}	$I_P = I_{P(MAX)}$ @ $T_A = -40^\circ\text{C}$ to 25°C	–	± 1.0	± 3.0	% FS
Non-Linearity Error [1]	E_{LIN}	$I_P = I_{P(MAX)}$, $T_A = -40^\circ\text{C}$ to 125°C	–	± 0.1	–	% FS
Sensitivity Error [1]	E_{SENS}	$I_P = I_{P(MAX)}$, $T_A = -40^\circ\text{C}$ to 125°C	–	± 0.2	–	% FS
Offset Voltage [1]	V_{OFFSET}	$I_P = 0$ A, $T_A = -40^\circ\text{C}$ to 125°C	–	± 5.2	–	mV
			–	± 0.3	–	% FS
LIFETIME DRIFT						
Total Output Error Lifetime Drift [1]	E_{TOT_DRIFT}	$I_P = I_{P(MAX)}$	–	± 1.0	–	% FS

[1] Guaranteed by design and characterization; not tested in production.

ELECTRICAL CHARACTERISTICS FOR CT417-xSN820DR

$V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, and $C_{BYP} = 1.0\ \mu\text{F}$ (unless otherwise specified)

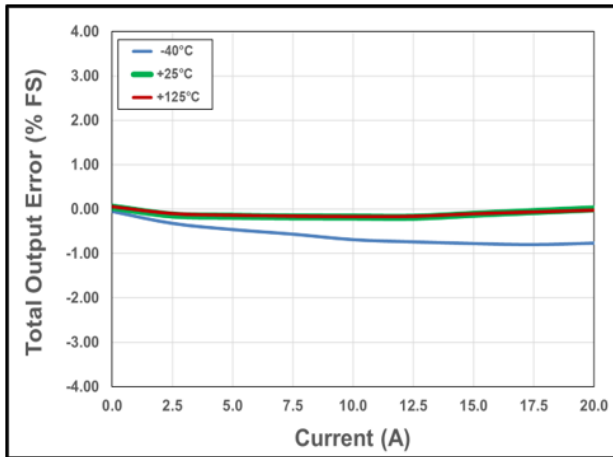


Figure 14: Total Output Error vs. Current vs. Temperature

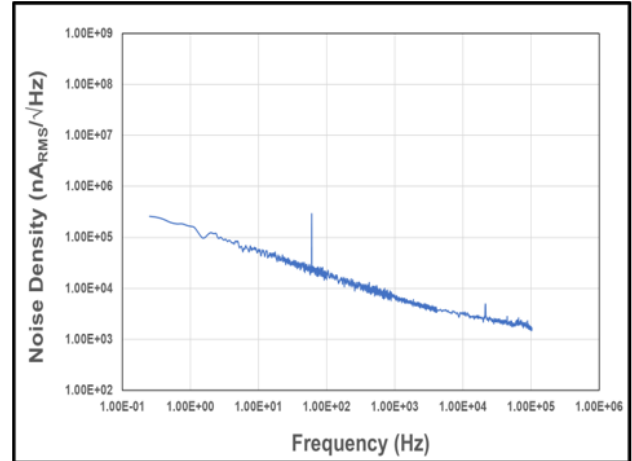


Figure 15: Noise Density vs. Frequency

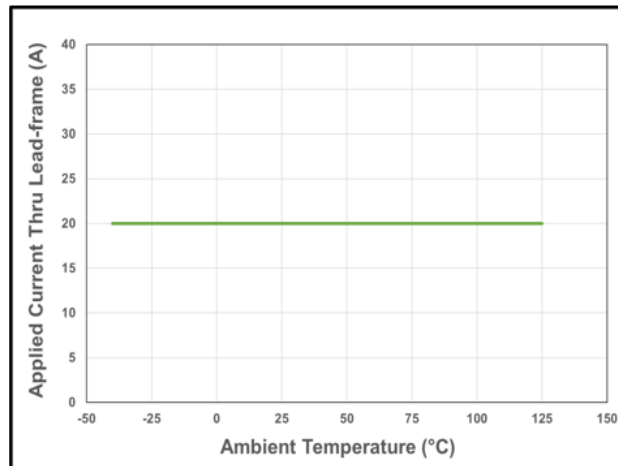


Figure 16: CT417 Current Derating Curve for 20 A_{DC}

CT417-xSN820MR: ±20 A – ELECTRICAL CHARACTERISTICS: Valid for $V_{CC} = 3.0$ to 3.6 V, $C_{BYP} = 1.0$ μ F, and $T_A = -40^\circ\text{C}$ to 125°C , typical values are $V_{CC} = 3.3$ V and $T_A = 25^\circ\text{C}$, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Current Range	I_{RANGE}		-20	-	20	A
Voltage Output Quiescent	V_{OQ}	$T_A = 25^\circ\text{C}$, $I_P = 0$ A	1.645	1.650	1.655	V
Sensitivity	S	$I_{RANGE(MIN)} < I_P < I_{RANGE(MAX)}$	-	50	-	mV/A
Bandwidth [1]	f_{BW}	Small Signal = -3 dB	-	1.0	-	MHz
Noise [1]	e_N	$T_A = 25^\circ\text{C}$, $f_{BW} = 100$ kHz	-	11.0	-	mA_{RMS}
OUT ACCURACY PERFORMANCE						
Total Output Error	E_{OUT}	$I_P = I_{P(MAX)}$ @ $T_A = 25^\circ\text{C}$	-	± 1.0	-	% FS
	E_{OUT_H}	$I_P = I_{P(MAX)}$ @ $T_A = 25^\circ\text{C}$ to 125°C	-	± 1.0	± 2.5	% FS
	E_{OUT_C}	$I_P = I_{P(MAX)}$ @ $T_A = -40^\circ\text{C}$ to 25°C	-	± 1.0	± 3.0	% FS
Non-Linearity Error [1]	E_{LIN}	$I_P = I_{P(MAX)}$, $T_A = -40^\circ\text{C}$ to 125°C	-	± 0.1	-	% FS
Sensitivity Error [1]	E_{SENS}	$I_P = I_{P(MAX)}$, $T_A = -40^\circ\text{C}$ to 125°C	-	± 0.3	-	% FS
Offset Voltage [1]	V_{OFFSET}	$I_P = 0$ A, $T_A = -40^\circ\text{C}$ to 125°C	-	± 7.9	-	mV
			-	± 0.4	-	% FS
LIFETIME DRIFT						
Total Output Error Lifetime Drift [1]	E_{TOT_DRIFT}	$I_P = I_{P(MAX)}$	-	± 1.0	-	% FS

[1] Guaranteed by design and characterization; not tested in production.

ELECTRICAL CHARACTERISTICS FOR CT417-xSN820MR

$V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, and $C_{BYP} = 1.0\ \mu\text{F}$ (unless otherwise specified)

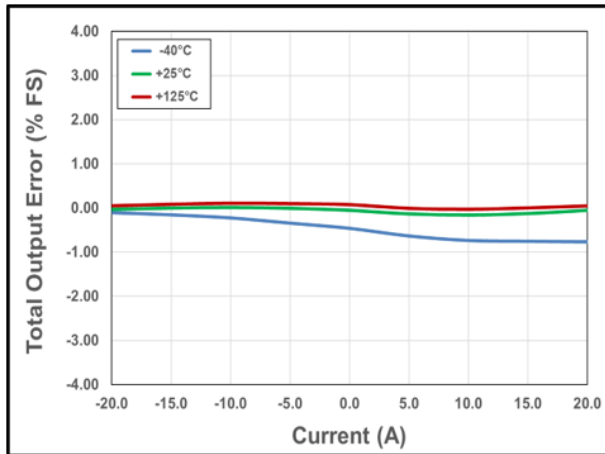


Figure 17: Total Output Error vs. Current vs. Temperature

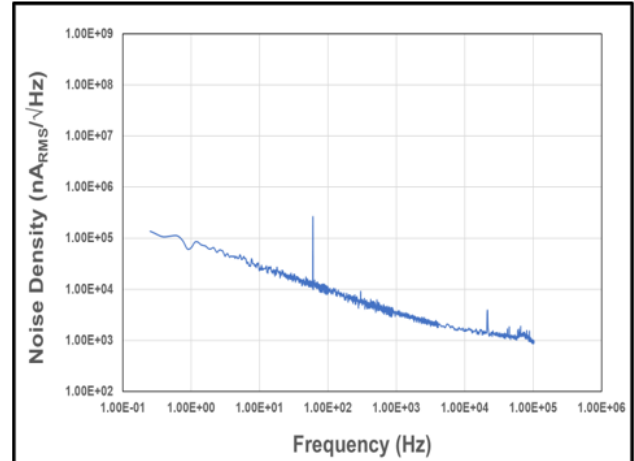


Figure 18: Noise Density vs. Frequency

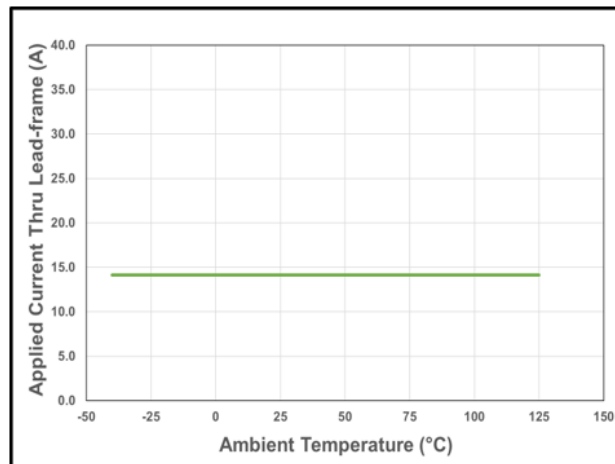


Figure 19: CT417 Current Derating Curve for 20 A_{PK} (14.1 A_{DC})

CT417-xSN830DR: 0 to 30 A – ELECTRICAL CHARACTERISTICS: Valid for $V_{CC} = 3.0$ to 3.6 V, $C_{BYP} = 1.0$ μ F, and $T_A = -40^\circ\text{C}$ to 125°C , typical values are $V_{CC} = 3.3$ V and $T_A = 25^\circ\text{C}$, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Current Range	I_{RANGE}		0	–	30	A
Voltage Output Quiescent	V_{OQ}	$T_A = 25^\circ\text{C}$, $I_P = 0$ A	0.645	0.650	0.655	V
Sensitivity	S	$I_{RANGE(MIN)} < I_P < I_{RANGE(MAX)}$	–	66.7	–	mV/A
Bandwidth [1]	f_{BW}	Small Signal = -3 dB, $C_{FILTER} = 5$ pF	–	1.0	–	MHz
Noise [1]	e_N	$T_A = 25^\circ\text{C}$, $f_{BW} = 100$ kHz	–	10.0	–	mA_{RMS}
OUT ACCURACY PERFORMANCE						
Total Output Error	E_{OUT}	$I_P = I_{P(MAX)}$ @ $T_A = 25^\circ\text{C}$	–	± 1.0	–	% FS
	E_{OUT_H}	$I_P = I_{P(MAX)}$ @ $T_A = 25^\circ\text{C}$ to 125°C	–	± 1.0	± 2.5	% FS
	E_{OUT_C}	$I_P = I_{P(MAX)}$ @ $T_A = -40^\circ\text{C}$ to 25°C	–	± 1.0	± 3.0	% FS
Non-Linearity Error [1]	E_{LIN}	$I_P = I_{P(MAX)}$, $T_A = -40^\circ\text{C}$ to 125°C	–	± 0.1	–	% FS
Sensitivity Error [1]	E_{SENS}	$I_P = I_{P(MAX)}$, $T_A = -40^\circ\text{C}$ to 125°C	–	± 0.3	–	% FS
Offset Voltage [1]	V_{OFFSET}	$I_P = 0$ A, $T_A = -40^\circ\text{C}$ to 125°C	–	± 4.4	–	mV
			–	± 0.2	–	% FS
LIFETIME DRIFT						
Total Output Error Lifetime Drift [1]	E_{TOT_DRIFT}	$I_P = I_{P(MAX)}$	–	± 1.0	–	% FS

[1] Guaranteed by design and characterization; not tested in production.

ELECTRICAL CHARACTERISTICS FOR CT417-xSN830DR

$V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, and $C_{BYP} = 1.0\ \mu\text{F}$ (unless otherwise specified)

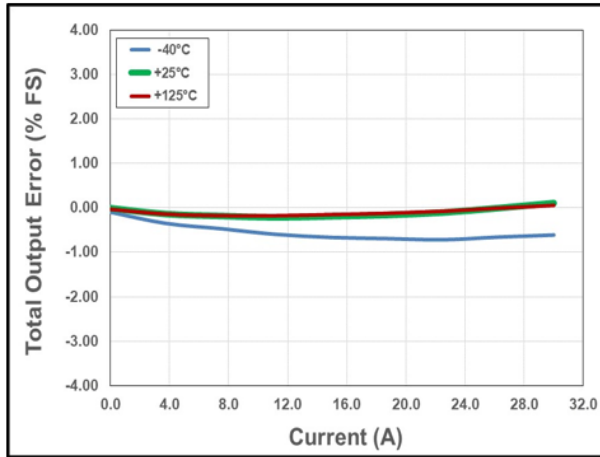


Figure 20: Total Output Error vs. Current vs. Temperature

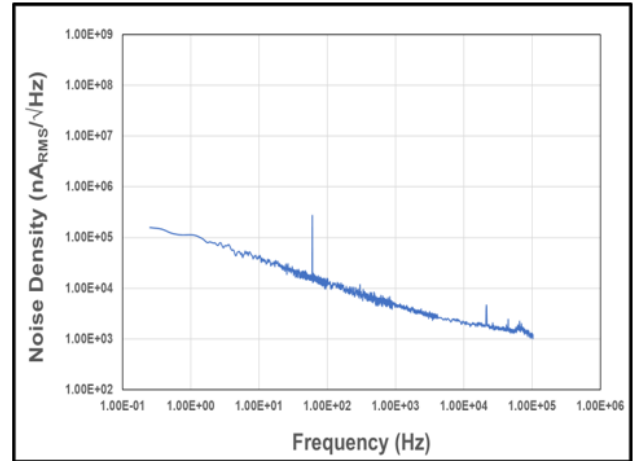


Figure 21: Noise Density vs. Frequency

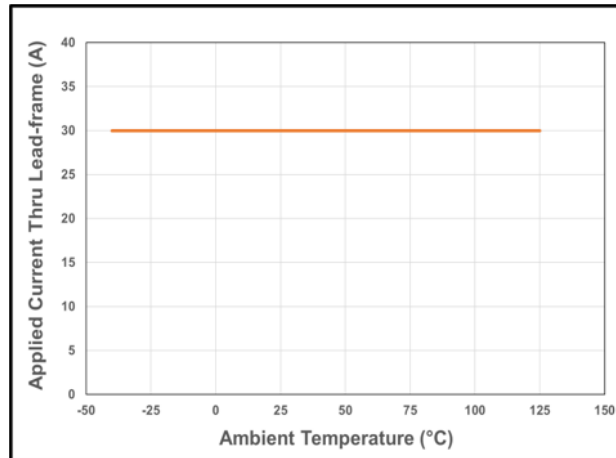


Figure 22: CT417 Current Derating Curve for 30 A_{DC}

CT417-xSN830MR: ±30 A – ELECTRICAL CHARACTERISTICS: Valid for $V_{CC} = 3.0$ to 3.6 V, $C_{BYP} = 1.0$ μ F, and $T_A = -40^\circ\text{C}$ to 125°C , typical values are $V_{CC} = 3.3$ V and $T_A = 25^\circ\text{C}$, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Current Range	I_{RANGE}		-30	-	30	A
Voltage Output Quiescent	V_{OQ}	$T_A = 25^\circ\text{C}$, $I_P = 0$ A	1.645	1.650	1.655	V
Sensitivity	S	$I_{RANGE(MIN)} < I_P < I_{RANGE(MAX)}$	-	33.3	-	mV/A
Bandwidth [1]	f_{BW}	Small Signal = -3 dB, $C_{FILTER} = 5$ pF	-	1.0	-	MHz
Noise [1]	e_N	$T_A = 25^\circ\text{C}$, $f_{BW} = 100$ kHz	-	12.5	-	mA_{RMS}
OUT ACCURACY PERFORMANCE						
Total Output Error	E_{OUT}	$I_P = I_{P(MAX)}$ @ $T_A = 25^\circ\text{C}$	-	± 1.0	-	% FS
	E_{OUT_H}	$I_P = I_{P(MAX)}$ @ $T_A = 25^\circ\text{C}$ to 125°C	-	± 1.0	± 2.5	% FS
	E_{OUT_C}	$I_P = I_{P(MAX)}$ @ $T_A = -40^\circ\text{C}$ to 25°C	-	± 1.0	± 3.0	% FS
Non-Linearity Error [1]	E_{LIN}	$I_P = I_{P(MAX)}$, $T_A = -40^\circ\text{C}$ to 125°C	-	± 0.1	-	% FS
Sensitivity Error [1]	E_{SENS}	$I_P = I_{P(MAX)}$, $T_A = -40^\circ\text{C}$ to 125°C	-	± 0.3	-	% FS
Offset Voltage [1]	V_{OFFSET}	$I_P = 0$ A, $T_A = -40^\circ\text{C}$ to 125°C	-	± 6.6	-	mV
			-	± 0.3	-	% FS
LIFETIME DRIFT						
Total Output Error Lifetime Drift [1]	E_{TOT_DRIFT}	$I_P = I_{P(MAX)}$	-	± 1.0	-	% FS

[1] Guaranteed by design and characterization; not tested in production.

ELECTRICAL CHARACTERISTICS FOR CT417-xSN830MR

$V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, and $C_{BYP} = 1.0\ \mu\text{F}$ (unless otherwise specified)

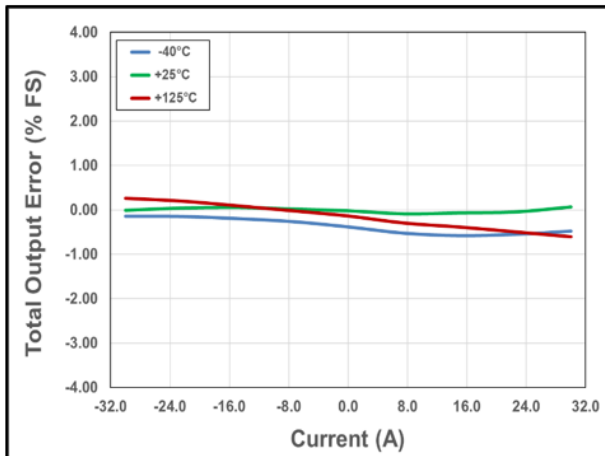


Figure 23: Total Output Error vs. Current vs. Temperature

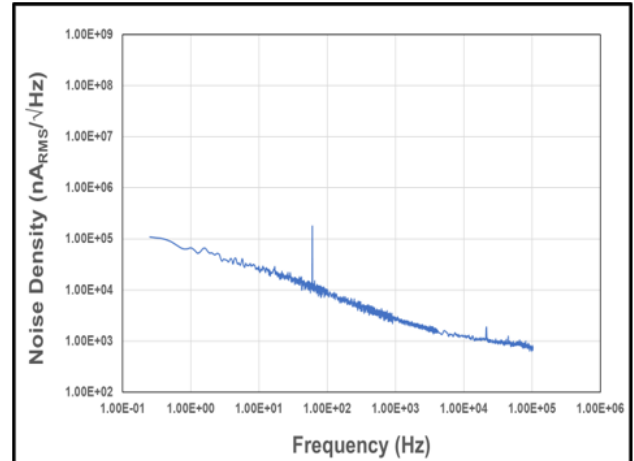


Figure 24: Noise Density vs. Frequency

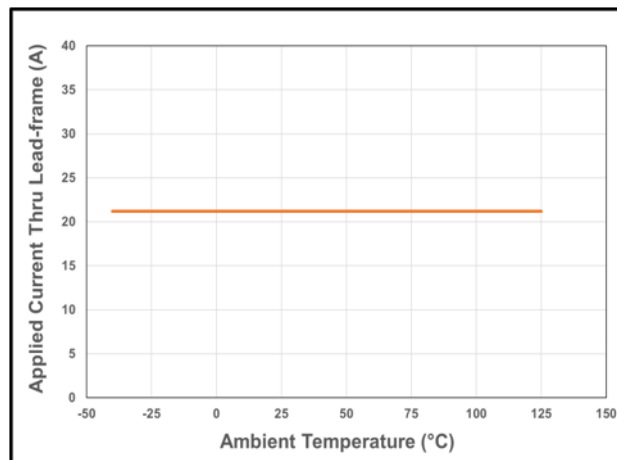


Figure 25: CT417 Current Derating Curve for 30 A_{PK} (21.2 A_{DC})

CT417-xSN850DR: 0 to 50 A – ELECTRICAL CHARACTERISTICS: Valid for $V_{CC} = 3.0$ to 3.6 V, $C_{BYP} = 1.0$ μ F, and $T_A = -40^\circ\text{C}$ to 125°C , typical values are $V_{CC} = 3.3$ V and $T_A = 25^\circ\text{C}$, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Current Range	I_{RANGE}		0	–	50	A
Voltage Output Quiescent	V_{OQ}	$T_A = 25^\circ\text{C}$, $I_P = 0$ A	0.645	0.650	0.655	V
Sensitivity	S	$I_{RANGE(MIN)} < I_P < I_{RANGE(MAX)}$	–	40	–	mV/A
Bandwidth [1]	f_{BW}	Small Signal = –3 dB	–	1.0	–	MHz
Noise [1]	e_N	$T_A = 25^\circ\text{C}$, $f_{BW} = 100$ kHz	–	11.0	–	mA_{RMS}
OUT ACCURACY PERFORMANCE						
Total Output Error	E_{OUT}	$I_P = I_{P(MAX)}$ @ $T_A = 25^\circ\text{C}$	–	± 1.0	–	% FS
	E_{OUT_H}	$I_P = I_{P(MAX)}$ @ $T_A = 25^\circ\text{C}$ to 125°C	–	± 1.0	± 2.5	% FS
	E_{OUT_C}	$I_P = I_{P(MAX)}$ @ $T_A = -40^\circ\text{C}$ to 25°C	–	± 1.0	± 3.0	% FS
Non-Linearity Error [1]	E_{LIN}	$I_P = I_{P(MAX)}$, $T_A = -40^\circ\text{C}$ to 125°C	–	± 0.2	–	% FS
Sensitivity Error [1]	E_{SENS}	$I_P = I_{P(MAX)}$, $T_A = -40^\circ\text{C}$ to 125°C	–	± 0.7	–	% FS
Offset Voltage [1]	V_{OFFSET}	$I_P = 0$ A, $T_A = -40^\circ\text{C}$ to 125°C	–	± 8.8	–	mV
			–	± 0.4	–	% FS
LIFETIME DRIFT						
Total Output Error Lifetime Drift [1]	E_{TOT_DRIFT}	$I_P = I_{P(MAX)}$	–	± 1.0	–	% FS

[1] Guaranteed by design and characterization; not tested in production.

ELECTRICAL CHARACTERISTICS FOR CT417-xSN850DR

$V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, and $C_{BYP} = 1.0\ \mu\text{F}$ (unless otherwise specified)

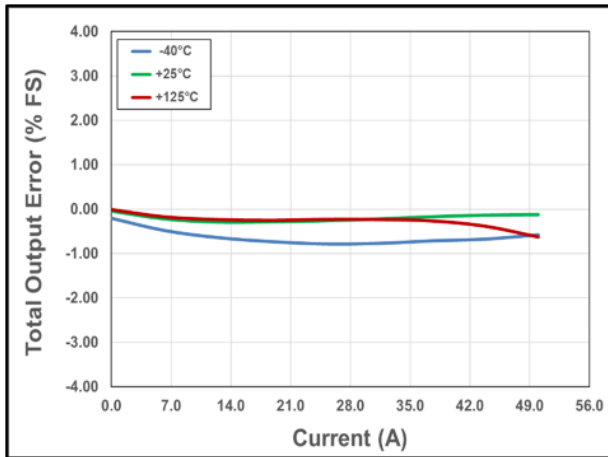


Figure 26: Total Output Error vs. Current vs. Temperature

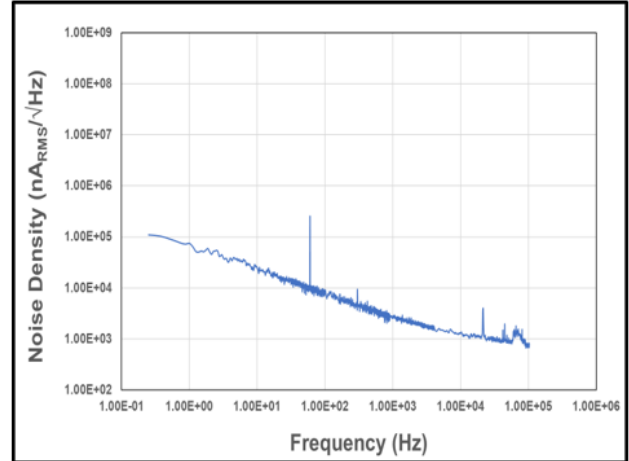


Figure 27: Noise Density vs. Frequency

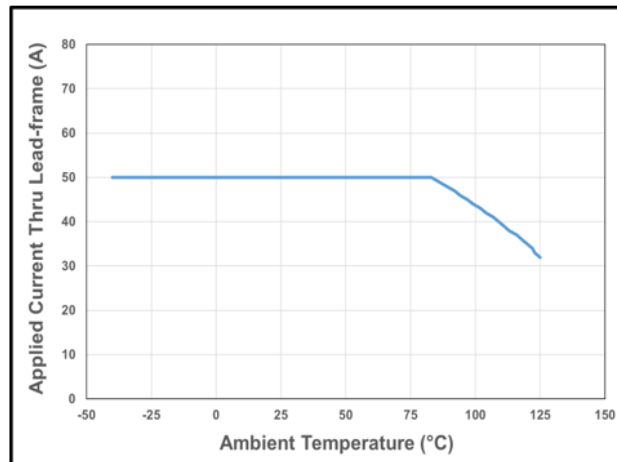


Figure 28: CT417 Current Derating Curve for 50 A_{DC}

CT417-xSN850MR: ±50 A – ELECTRICAL CHARACTERISTICS: Valid for $V_{CC} = 3.0$ to 3.6 V, $C_{BYP} = 1.0$ μ F, and $T_A = -40^\circ\text{C}$ to 125°C , typical values are $V_{CC} = 3.3$ V and $T_A = 25^\circ\text{C}$, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Current Range	I_{RANGE}		-50	-	50	A
Voltage Output Quiescent	V_{OQ}	$T_A = 25^\circ\text{C}$, $I_P = 0$ A	1.645	1.650	1.655	V
Sensitivity	S	$I_{RANGE(MIN)} < I_P < I_{RANGE(MAX)}$	-	20	-	mV/A
Bandwidth [1]	f_{BW}	Small Signal = -3 dB	-	1.0	-	MHz
Noise [1]	e_N	$T_A = 25^\circ\text{C}$, $f_{BW} = 100$ kHz	-	19.0	-	mA_{RMS}
OUT ACCURACY PERFORMANCE						
Total Output Error	E_{OUT}	$I_P = I_{P(MAX)}$ @ $T_A = 25^\circ\text{C}$	-	± 1.0	-	% FS
	E_{OUT_H}	$I_P = I_{P(MAX)}$ @ $T_A = 25^\circ\text{C}$ to 125°C	-	± 1.0	± 2.5	% FS
	E_{OUT_C}	$I_P = I_{P(MAX)}$ @ $T_A = -40^\circ\text{C}$ to 25°C	-	± 1.0	± 3.0	% FS
Non-Linearity Error [1]	E_{LIN}	$I_P = I_{P(MAX)}$, $T_A = -40^\circ\text{C}$ to 125°C	-	± 0.1	-	% FS
Sensitivity Error [1]	E_{SENS}	$I_P = I_{P(MAX)}$, $T_A = -40^\circ\text{C}$ to 125°C	-	± 0.5	-	% FS
Offset Voltage [1]	V_{OFFSET}	$I_P = 0$ A, $T_A = -40^\circ\text{C}$ to 125°C	-	± 6.0	-	mV
			-	± 0.3	-	% FS
LIFETIME DRIFT						
Total Output Error Lifetime Drift [1]	E_{TOT_DRIFT}	$I_P = I_{P(MAX)}$	-	± 1.0	-	% FS

[1] Guaranteed by design and characterization; not tested in production.

ELECTRICAL CHARACTERISTICS FOR CT417-xSN850MR

$V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, and $C_{BYP} = 1.0\ \mu\text{F}$ (unless otherwise specified)

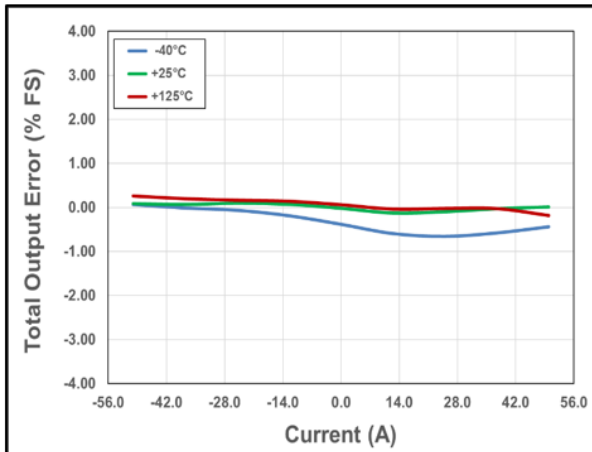


Figure 29: Total Output Error vs. Current vs. Temperature

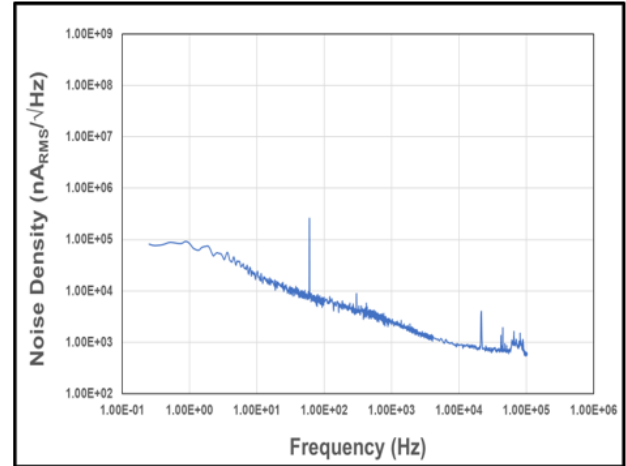


Figure 30: Noise Density vs. Frequency

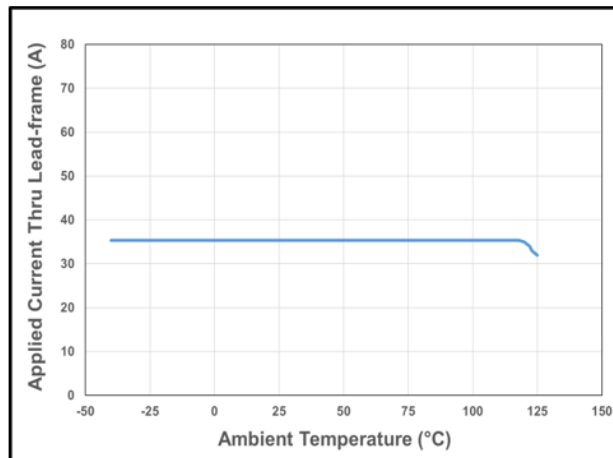


Figure 31: CT417 Current Derating Curve for 50 A_{PK} (35.4 A_{DC})

CT417-xSN865DR: 0 to 65 A – ELECTRICAL CHARACTERISTICS: Valid for $V_{CC} = 3.0$ to 3.6 V, $C_{BYP} = 1.0$ μ F, and $T_A = -40^\circ\text{C}$ to 125°C , typical values are $V_{CC} = 3.3$ V and $T_A = 25^\circ\text{C}$, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Current Range	I_{RANGE}		0	–	65	A
Voltage Output Quiescent	V_{OQ}	$T_A = 25^\circ\text{C}$, $I_P = 0$ A	0.645	0.650	0.655	V
Sensitivity	S	$I_{RANGE(MIN)} < I_P < I_{RANGE(MAX)}$	–	30.8	–	mV/A
Bandwidth [1]	f_{BW}	Small Signal = -3 dB, $C_{FILTER} = 5$ pF	–	1.0	–	MHz
Noise [1]	e_N	$T_A = 25^\circ\text{C}$, $f_{BW} = 100$ kHz	–	11.5	–	mA_{RMS}
OUT ACCURACY PERFORMANCE						
Total Output Error	E_{OUT}	$I_P = I_{P(MAX)}$ @ $T_A = 25^\circ\text{C}$	–	± 1.0	–	% FS
	E_{OUT_H}	$I_P = I_{P(MAX)}$ @ $T_A = 25^\circ\text{C}$ to 125°C	–	± 1.0	± 2.5	% FS
	E_{OUT_C}	$I_P = I_{P(MAX)}$ @ $T_A = -40^\circ\text{C}$ to 25°C	–	± 1.0	± 3.0	% FS
Non-Linearity Error [1]	E_{LIN}	$I_P = I_{P(MAX)}$, $T_A = -40^\circ\text{C}$ to 125°C	–	± 0.2	–	% FS
Sensitivity Error [1]	E_{SENS}	$I_P = I_{P(MAX)}$, $T_A = -40^\circ\text{C}$ to 125°C	–	± 0.2	–	% FS
Offset Voltage [1]	V_{OFFSET}	$I_P = 0$ A, $T_A = -40^\circ\text{C}$ to 125°C	–	± 3.0	–	mV
			–	± 0.1	–	% FS
LIFETIME DRIFT						
Total Output Error Lifetime Drift [1]	E_{TOT_DRIFT}	$I_P = I_{P(MAX)}$	–	± 1.0	–	% FS

[1] Guaranteed by design and characterization; not tested in production.

ELECTRICAL CHARACTERISTICS FOR CT417-xSN865DR

$V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, and $C_{BYP} = 1.0\ \mu\text{F}$ (unless otherwise specified)

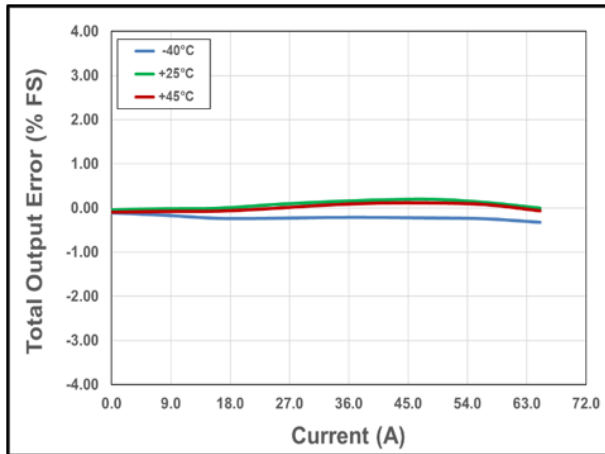


Figure 32: Total Output Error vs. Current vs. Temperature

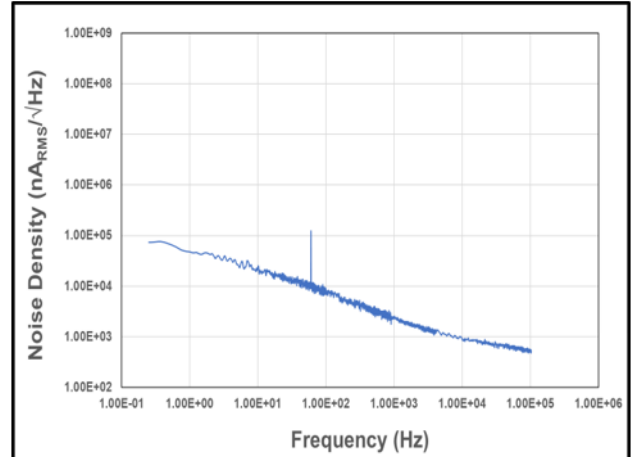


Figure 33: Noise Density vs. Frequency

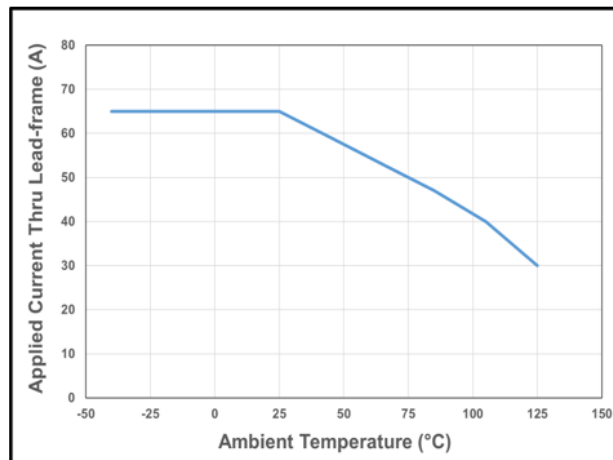


Figure 34: CT417 Current Derating Curve for 65 A_{DC}

CT417-xSN865MR: ±65 A – ELECTRICAL CHARACTERISTICS: Valid for $V_{CC} = 3.0$ to 3.6 V, $C_{BYP} = 1.0$ μ F, and $T_A = -40^\circ\text{C}$ to 125°C , typical values are $V_{CC} = 3.3$ V and $T_A = 25^\circ\text{C}$, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Current Range	I_{RANGE}		-65	-	65	A
Voltage Output Quiescent	V_{OQ}	$T_A = 25^\circ\text{C}$, $I_P = 0$ A	1.645	1.650	1.655	V
Sensitivity	S	$I_{RANGE(MIN)} < I_P < I_{RANGE(MAX)}$	-	15.4	-	mV/A
Bandwidth [1]	f_{BW}	Small Signal = -3 dB, $C_{FILTER} = 5$ pF	-	1.0	-	MHz
Noise [1]	e_N	$T_A = 25^\circ\text{C}$, $f_{BW} = 100$ kHz	-	19.0	-	mA_{RMS}
OUT ACCURACY PERFORMANCE						
Total Output Error	E_{OUT}	$I_P = I_{P(MAX)}$ @ $T_A = 25^\circ\text{C}$	-	± 1.0	-	% FS
	E_{OUT_H}	$I_P = I_{P(MAX)}$ @ $T_A = 25^\circ\text{C}$ to 125°C	-	± 1.0	± 2.5	% FS
	E_{OUT_C}	$I_P = I_{P(MAX)}$ @ $T_A = -40^\circ\text{C}$ to 25°C	-	± 1.0	± 3.0	% FS
Non-Linearity Error [1]	E_{LIN}	$I_P = I_{P(MAX)}$, $T_A = -40^\circ\text{C}$ to 125°C	-	± 0.2	-	% FS
Sensitivity Error [1]	E_{SENS}	$I_P = I_{P(MAX)}$, $T_A = -40^\circ\text{C}$ to 125°C	-	± 0.3	-	% FS
Offset Voltage [1]	V_{OFFSET}	$I_P = 0$ A, $T_A = -40^\circ\text{C}$ to 125°C	-	± 4.0	-	mV
			-	± 0.1	-	% FS
LIFETIME DRIFT						
Total Output Error Lifetime Drift [1]	E_{TOT_DRIFT}	$I_P = I_{P(MAX)}$	-	± 1.0	-	% FS

[1] Guaranteed by design and characterization; not tested in production.

ELECTRICAL CHARACTERISTICS FOR CT417-xSN865MR

$V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, and $C_{BYP} = 1.0\ \mu\text{F}$ (unless otherwise specified)

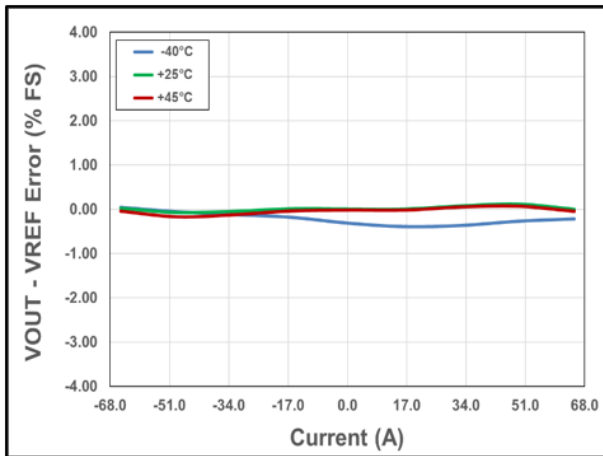


Figure 35: Total Output Error vs. Current vs. Temperature

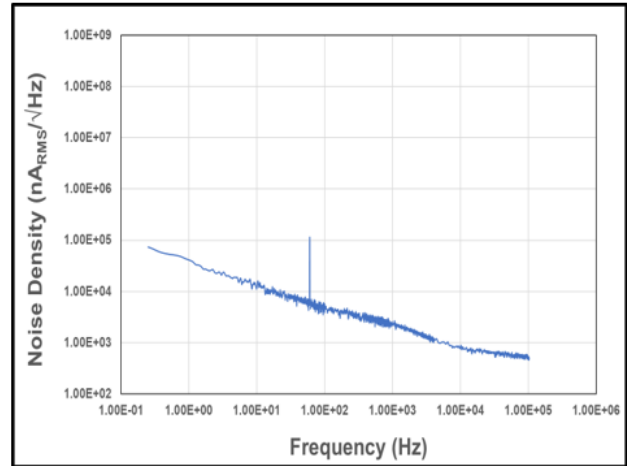


Figure 36: Noise Density vs. Frequency

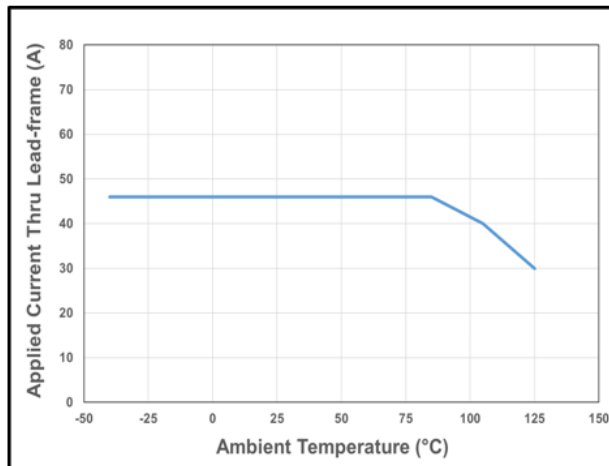


Figure 37: CT417 Current Derating Curve for 65 A_{PK} (46.0 A_{DC})

FUNCTIONAL DESCRIPTION

Overview

The CT417 is a high accuracy contact current sensor with an integrated current-carrying conductor that handles up to 65 A. It has high sensitivity and a wide dynamic range with excellent accuracy (low total output error) across temperature. This current sensor supports eight current ranges:

- 0 to 20 A
- ±20 A
- 0 to 30 A
- ±30 A
- 0 to 50 A
- ±50 A
- 0 to 65 A
- ±65 A

When current is flowing through the current-carrying conductor, the XtremeSense TMR sensors inside the chip senses the field which in turn generates differential voltage signals that then goes through the Analog Front-End (AFE) to output a current measurement with less than ±1.0% full-scale total output error (E_{OUT}).

The chip is designed to enable a fast response time of 300 ns for the current measurement from the OUT pin as the bandwidth for the CT417 is 1.0 MHz. Even with a high bandwidth, the chip consumes a minimal amount of power.

Linear Output Current Measurement

The CT417 provides a continuous linear analog output voltage which represents the current measurement. The output voltage range of OUT is from 0.65 to 2.65 V with a V_{OQ} of 0.65 V and 1.65 V for unidirectional and bidirectional currents, respectively. Figure 38 illustrates the output voltage range of the OUT pin as a function of the measured current.

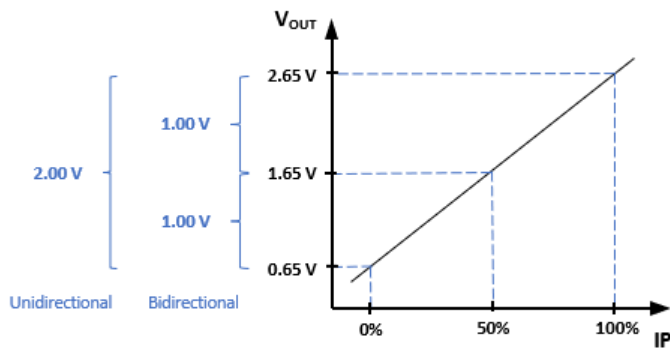


Figure 38: Linear Output Voltage Range (OUT) vs. Measured Current (IP)

Sensitivity

Sensitivity (S) is a change in the CT417 output in response to a change in 1 A of current flowing through the current-carrying conductor. It is defined by the product of the magnetic circuit sensitivity (G/A, where 1.0 G = 0.1 mT) and the chip linear amplifier gain (mV/G). Therefore, the result of this gives a sensitivity unit of mV/A. The CT417 is factory-calibrated to optimize the sensitivity for the full scale of the device dynamic range.

Total Output Error

The Total Output Error (E_{OUT}) is the maximum deviation of the sensor output from the ideal sensor transfer curve over the full temperature range relative to the sensor full scale.

The Total Output Error is measured by performing a full-scale primary current (IP) sweep and measuring V_{OUT} at multiple points.

$$E_{OUT} = 100 * \frac{\max(V_{OUT_IDEAL}(I) - V_{OUT}(I))}{F.S.}$$

The Ideal Transfer Curve is calculated based on datasheet parameters as described below.

$$V_{OUT_IDEAL}(I_P) = V_{OQ} + S * I_P$$

E_{OUT} incorporates all sources of error and is a function of the sensed current (I_P) from the current sensor.

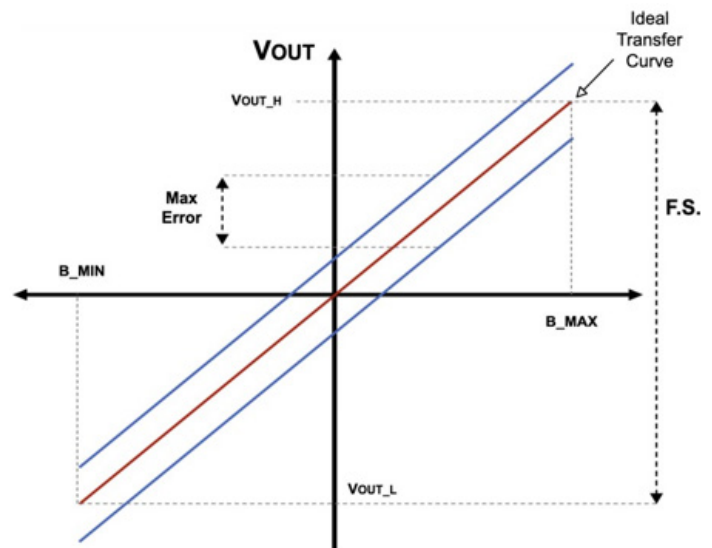


Figure 39: Total Output Error (E_{OUT}) vs. Sensed Current (I_P)

The CT417 achieves a total output error (E_{OUT}) that is less than $\pm 3.0\%$ of Full-Scale (FS) over supply voltage and temperature. It is designed with innovative and proprietary TMR sensors and circuit blocks to provide very accurate current measurements regardless of the operating conditions.

Sensitivity Error

The sensitivity error (E_{SENS}) is the sensitivity temperature drift error for unipolar or DC current. It is calculated using the equation below:

$$E_{SENS} = 100 \times \left(\frac{S_{MEASURED}}{S} - 1 \right)$$

For bipolar or AC current, the E_{SENS} is calculated by dividing the equation by 2.

Power-On Time (t_{ON})

Power-On Time (t_{ON}) of 100 μs is the amount of time required by CT417 to start up, fully power the chip, and becoming fully operational from the moment the supply voltage is applied to it. This time includes the ramp-up time and the settling time (within 10% of steady-state voltage under an applied magnetic field) after the power supply has reached the minimum V_{CC} .

Response Time ($t_{RESPONSE}$)

Response Time ($t_{RESPONSE}$) of 300 ns for the CT417 is the time interval between the following terms:

1. When the primary current signal reaches 90% of its final value,
2. When the chip reaches 90% of its output corresponding to the applied current.

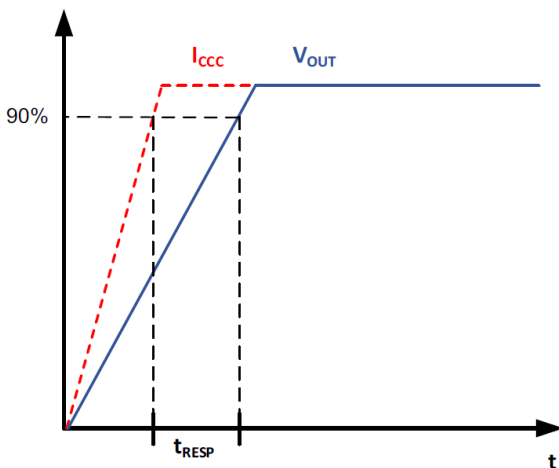


Figure 40: CT417 Response Time Curve

Rise Time (t_{RISE})

Rise Time (t_{RISE}) is the time interval of when it reaches 10% and 90% of the full-scale output voltage. The t_{RISE} of the CT417 is 200 ns.

Propagation Delay (t_{DELAY})

Propagation Delay (t_{DELAY}) is the time difference between these two events:

1. When the primary current reaches 20% of its final value
2. When the chip reaches 20% of its output corresponding to the applied current.

The CT417 has a propagation delay of 250 ns.

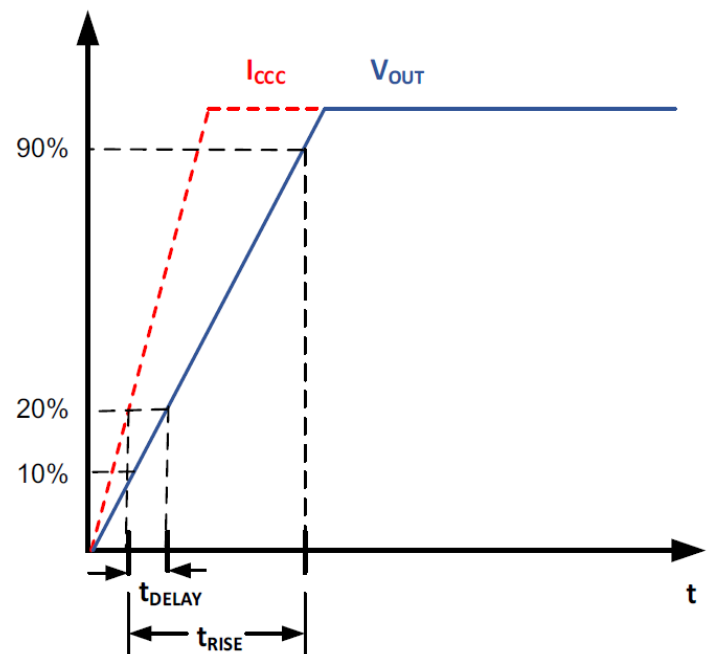


Figure 41: CT417 Propagation Delay and Rise Time Curve

Undervoltage Lockout (UVLO)

The Undervoltage Lockout protection circuitry of the CT417 is activated when the supply voltage (V_{CC}) falls below 2.45 V. The CT417 remains in a low quiescent state until V_{CC} rises above the UVLO threshold (2.50 V). In this condition where V_{CC} is less than 2.45 V and UVLO is triggered, the output from the CT417 is not valid, and the \overline{FLT} pin will go low. Once V_{CC} rises above 2.50 V then the UVLO is cleared, and the \overline{FLT} pin will be high.

Immunity to Common Mode Fields

The CT417 is housed in a custom plastic package that uses a U-shaped leadframe to reduce the common mode fields generated as current flows through the current-carrying conductor. With the U-shaped leadframe, the stray fields cancel one another thus reducing electromagnetic interference (EMI).

Also, a good PCB layout of the CT417 will optimize performance and reduce EMI. See the Applications Information section in this datasheet for recommendations on PCB layout.

Creepage and Clearance

Two important terms as it relates to isolation provided by the package are: creepage and clearance. Creepage is defined as the shortest distance across the surface of the package from one side the leads to the other side of the leads. The definition for clearance is the shortest distance between the leads of opposite side through the air. Figure 42 illustrates the creepage and clearance for the SOIC-8 package of the CT417.

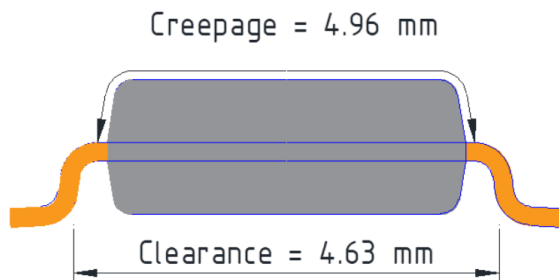


Figure 42: The Creepage and Clearance for the CT417 SOIC-8 package

Application

The CT417 is an integrated contact current sensor that can be used in many applications from measuring current in power supplies to motor control to overcurrent fault protection. It is a plug-and-play solution in that no calibration is required, and it outputs

to a microcontroller a simple linear analog output voltage which corresponds to a current measurement value.

It is designed to support an operating voltage range of 3.3 to 3.6 V, but it is ideal to use a 3.3 V power supply where the output tolerance is less than $\pm 5\%$.

Bypass Capacitor

A single 1.0 μF capacitor is needed for the VCC pin to reduce the noise from the power supply and other circuits. This capacitor should be placed as close as possible to the CT417 to minimize inductance and resistance between the two devices.

$\overline{\text{FLT}}$ Resistor and Capacitor

For the CT417, the $\overline{\text{FLT}}$ pin is an open drain output. It requires a pull-up resistor value of 100 k Ω to be connected from the pin to V_{CC} and also a 1.0 nF capacitor to be connected from the pin to ground.

If the $\overline{\text{FLT}}$ pin function is not needed in the application, then a 1.0 nF capacitor must be connected from the pin to ground.

Fault# Interrupt ($\overline{\text{FLT}}$)

The CT417 generates an active low digital fault signal via the $\overline{\text{FLT}}$ pin to interrupt the microcontroller to indicate a fault event has been triggered. It is an open drain output and requires a pull-up resistor with a value of 100 k Ω tied to VCC and a 1.0 nF capacitor is connected to ground. A fault signal will interrupt the host system for these events:

- OCD
- UVLO

The $\overline{\text{FLT}}$ signal will be asserted low whenever one of the above fault events occur. In the case of an UVLO event, the $\overline{\text{FLT}}$ pin will stay low until the fault is cleared and then go high.

If the $\overline{\text{FLT}}$ is not used, then a 1.0 nF capacitor must be connected from the pin to ground.

Recommended PCB Layout

Since the CT417 can measure up to 65 A of current, special care must be taken in the printed circuit board (PCB) layout of the CT417 and the surrounding circuitry. It is recommended that the CCC pins be connected to as much copper area as possible. It is also recommended that 2 oz. or heavier copper be used for PCB traces when the CT417 is used to measure up to 30 A of current. Additional layers of the PCB should also be used to carry current and be connected using the arrangement of vias. Figure 43 and Figure 44 show the recommended the PCB layout for the 20 A and 30 A variants of CT417. For the 65 A variant, it is recommended that 4 oz. of copper be used for the PCB traces.

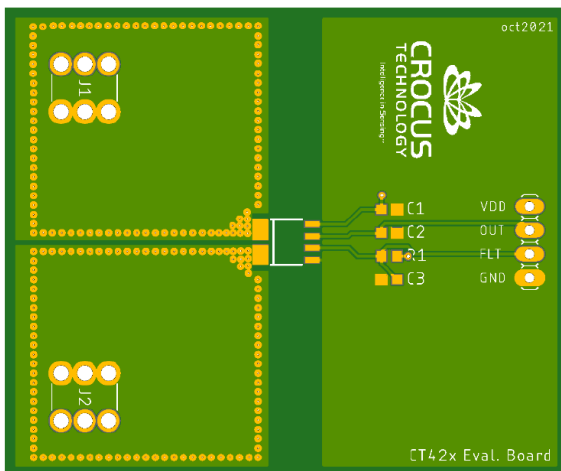


Figure 43: Recommended PCB Layout (Top Layer) for the 20 A to 65 A variants of the CT417

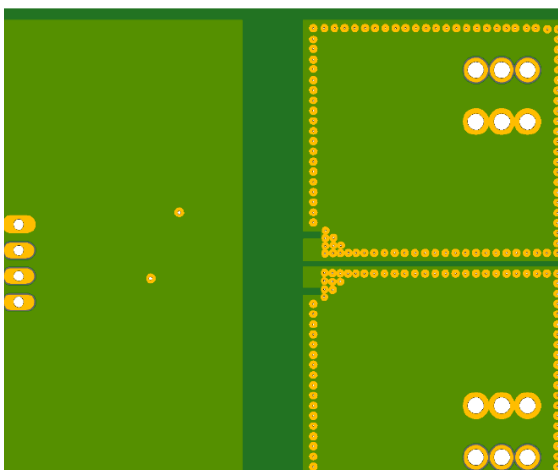


Figure 44: Recommended PCB Layout (Bottom Layer) for the 20 A to 65 A variants of the CT417

PACKAGE OUTLINE DRAWING

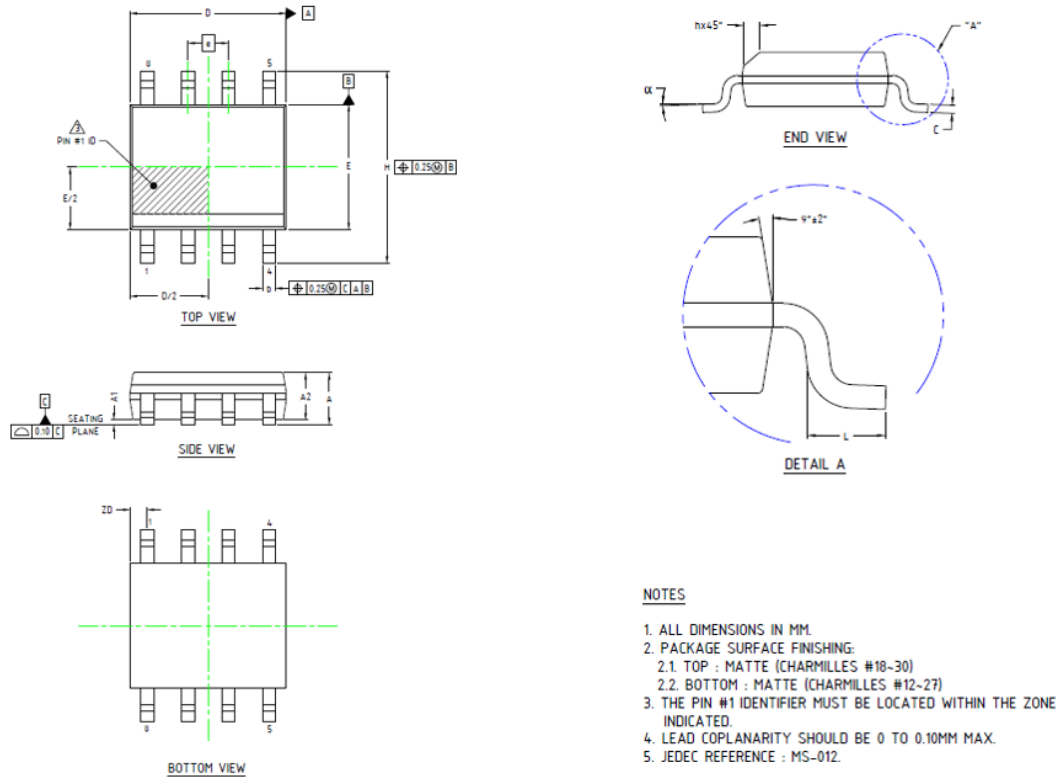
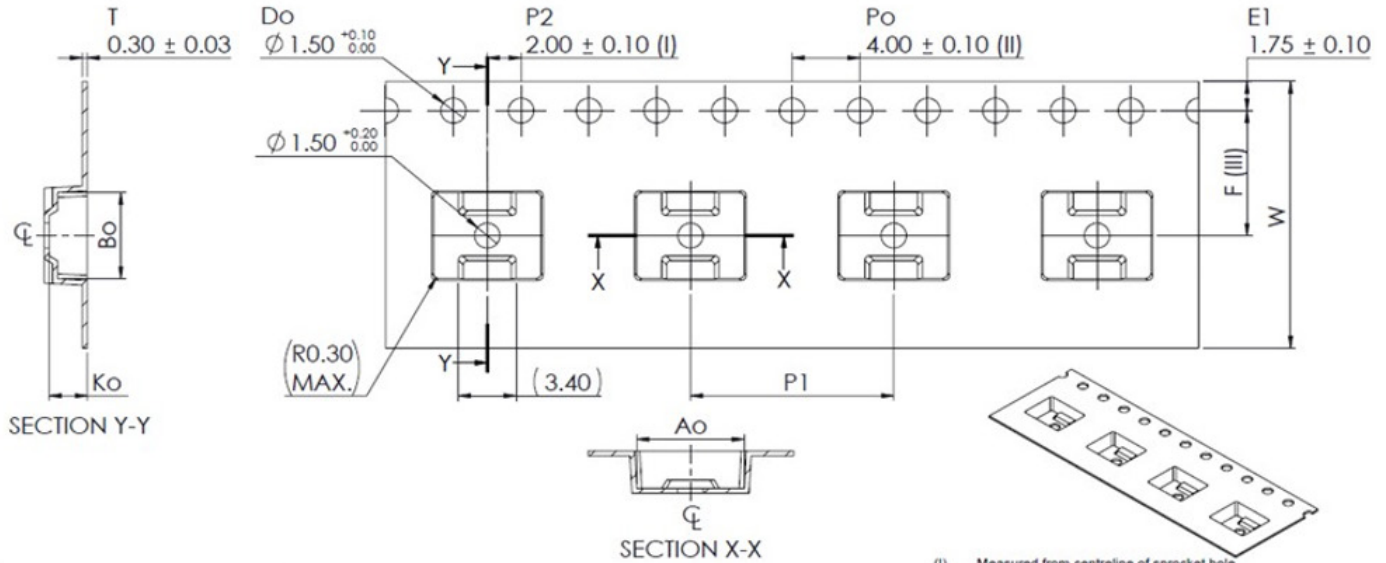


Figure 45: SOIC-8 Package Drawing and Dimensions

Table 2: CT417 SOIC-8 Package Dimensions

Symbol	Dimensions in Millimeters (mm)		
	Min.	Typ.	Max.
A1	0.10	0.18	0.25
b	0.36	0.41	0.46
C	0.19	0.22	0.25
D	4.80	4.89	4.98
E	3.81	3.90	3.99
e	1.27 BSC		
H	5.80	6.00	6.20
h	0.25	0.37	0.50
L	0.41	–	1.27
A	1.52	1.62	1.72
α	0°	–	8°
ZD	0.53 REF		
A2	1.37	1.47	1.57

TAPE AND REEL POCKET DRAWING AND DIMENSIONS



Ao	6.35	+/- 0.10
Bo	5.13	+/- 0.10
Ko	2.25	+/- 0.15
K1	1.75	+/- 0.10
F	7.50	+/- 0.10
P1	12.00	+/- 0.10
W	16.00	+0.30 / -0.10

- (I) Measured from centreline of sprocket hole to centreline of pocket.
- (II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
- (III) Measured from centreline of sprocket hole to centreline of pocket.
- (IV) Other material available.
- (V) Dimension with () is used for design reference purposes, No measurement required.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

Figure 46: Tape and Pocket Drawing for SOIC-8 Package

PACKAGE INFORMATION

Table 3: CT417 Package Information

Part Number	Package Type	# of Leads	Package Quantity	Lead Finish	MSL Rating [2]	Operating Temperature (°C) [3]	Device Marking [4]
CT417-HSN820DR	SOIC	8	2000	Sn	3	-40 to 125	CT417 S820DR YYWWLL
CT417-ASN820DR	SOIC	8	2000	Sn	3	-40 to 125	CT417A S820DR YYWWLL
CT417-HSN820MR	SOIC	8	2000	Sn	3	-40 to 125	CT417 S820MR YYWWLL
CT417-ASN820MR	SOIC	8	2000	Sn	3	-40 to 125	CT417A S820MR YYWWLL
CT417-HSN830DR	SOIC	8	2000	Sn	3	-40 to 125	CT417 S830DR YYWWLL
CT417-ASN830DR	SOIC	8	2000	Sn	3	-40 to 125	CT417A S830DR YYWWLL
CT417-HSN830MR	SOIC	8	2000	Sn	3	-40 to 125	CT417 S830MR YYWWLL
CT417-ASN830MR	SOIC	8	2000	Sn	3	-40 to 125	CT417A S830MR YYWWLL
CT417-HSN850DR	SOIC	8	2000	Sn	3	-40 to 125	CT417 S850DR YYWWLL
CT417-ASN850DR	SOIC	8	2000	Sn	3	-40 to 125	CT417A S850DR YYWWLL
CT417-HSN850MR	SOIC	8	2000	Sn	3	-40 to 125	CT417 S850MR YYWWLL
CT417-ASN850MR	SOIC	8	2000	Sn	3	-40 to 125	CT417A S850MR YYWWLL
CT417-HSN865DR	SOIC	8	2000	Sn	3	-40 to 125	CT417 S865DR YYWWLL
CT417-ASN865DR	SOIC	8	2000	Sn	3	-40 to 125	CT417A S865DR YYWWLL
CT417-HSN865MR	SOIC	8	2000	Sn	3	-40 to 125	CT417 S865MR YYWWLL
CT417-ASN865MR	SOIC	8	2000	Sn	3	-40 to 125	CT417A S865MR YYWWLL

[1] RoHS is defined as semiconductor products that are compliant to the current EU RoHS requirements. It also will meet the requirement that RoHS substances do not exceed 0.1% by weight in homogeneous materials. Green is defined as the content of chlorine (Cl), bromine (Br), and antimony trioxide based flame retardants satisfy JS709B low halogen requirements of $\leq 1,000$ ppm.

[2] MSL Rating = Moisture Sensitivity Level Rating as defined by JEDEC standard classifications.

[3] Package will withstand ambient temperature range of -40°C to 125°C and storage temperature range of -65°C to 150°C .

[4] Device Marking for CT417 is defined as CT417 S8xxZR YYWWLL where the first 2 lines = part number, YY = year, WW = work week, and LL = lot code.

DEVICE MARKING

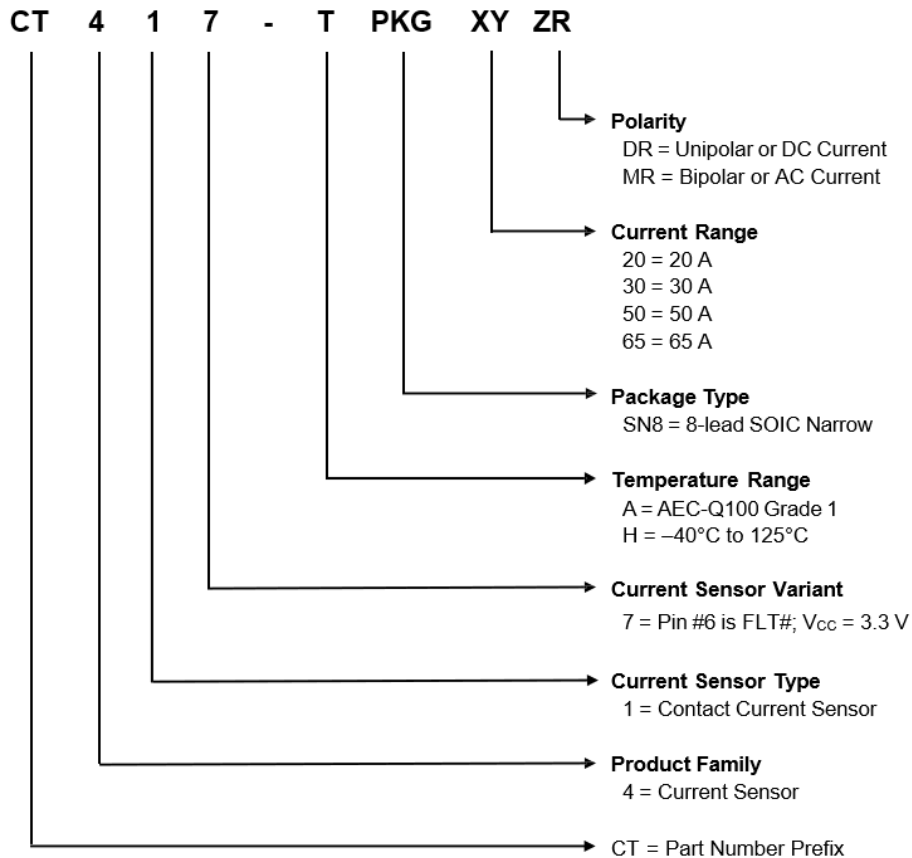


Figure 47: CT417 Device Marking for 8-lead Package

Table 4: CT417 Device Marking Definition for 8-lead SOIC Package

Row No.	Code	Definition
3	•	Pin 1 Indicator
1	CT417	Allegro Part Number
1	A	AEC-Q100 Qualified
2	P	Package Type
2	N	Number of Pins
2	XX	Current Range
2	ZR	Polarity
3	YY	Calendar Year
3	WW	Work Week
3	LL	Lot Code

PART ORDERING NUMBER LEGEND



Revision History

Number	Date	Description
2	November 2, 2023	Document rebranded and minor editorial updates

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