ACSEVB-LX8

LX Package Bare Evaluation Board User Guide

DESCRIPTION

Bare evaluation boards offer a method for evaluating Allegro current sensors in a lab environment. This document describes the use of the LX Package Bare Evaluation Board. This evaluation board (ACSEVB-LX8, TED-0004673) is intended for use with any LX package (8-pin flat PSOF custom package) Allegro Hall-based or TMR-based current sensors.

FEATURES OF THE BARE BOARD

- Enhanced thermal performance
  - □ 6-layer PCB with 2 oz copper weight on all layers
  - □ Nonconductive-filled via-in-pad
  - □ High-performance FR4 material with 180°C glass transition temperature
- Flexible layout for user installed connection points
  - □ Standard Keystone test points
  - □ SMA/SMB connector
  - □ 2-pin headers
- Integrated current-loop resistance can be measured directly on the evaluation board after test-point installation; voltage drop can be measured for approximating power loss in the package.

BARE EVALUATION BOARD CONTENTS

- **NOTE:** It is the responsibility of the user to assemble the board with the desired current sensor and supporting circuitry. This board does not come populated with an Allegro current sensor or other components.
- Recommended supporting circuitry for all compatible current sensors is listed in the Supporting Circuitry section.

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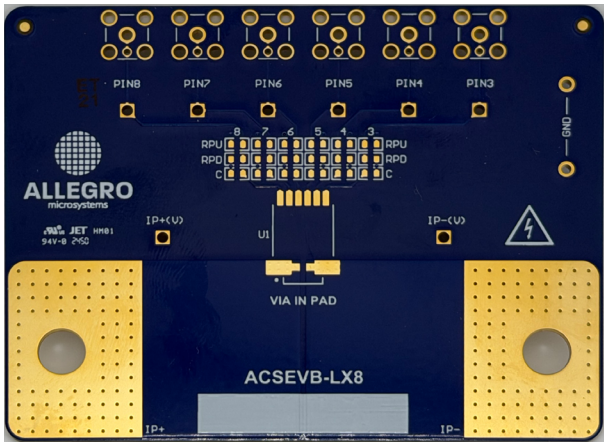
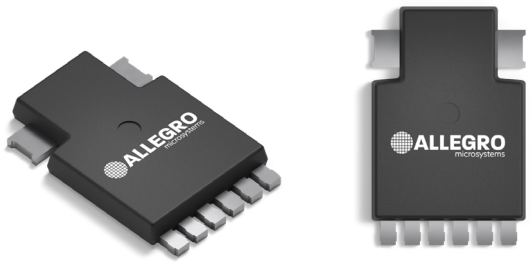


Figure 1: LX Bare Evaluation Board



Not to scale

Figure 2: 8-pin Flat PSOF Package (Suffix LX)

USING THE EVALUATION BOARD

Evaluation Board Procedure

SETTING UP THE EVALUATION BOARD

Upon receiving the evaluation board, it is the responsibility of the user to populate the evaluation board with the desired Allegro current sensor. It is also the responsibility of the user to install test points, SMA/SMB connectors, header connectors, and supporting circuitry, as needed.

CONNECTING TO THE EVALUATION BOARD

The most reliable way to connect measurement instruments to the evaluation board is to use SMB/SMA or 2-pin header connectors along with coaxial cables. This configuration is the most resilient to external coupling, is the most mechanically stable, and is the preferred way to measure a high-speed signal.

Keystone test points provide a convenient way to connect any instrument but are recommended for DC setups only.

Evaluation Board Detailed Description

1. U1 is the LX package footprint (pin 1 is on bottom left side of the package footprint; see the small white dot to the left of the package footprint).
2. U1 pins allow the option to connect:
   - ♦ RPU: pull-up resistor to VCC
   - ♦ RPD: pull-down resistor to GND
   - ♦ C: decoupling or load capacitor to GND

NOTE: All passive components are 0603 package size.

3. Optional through-hole test points (Keystone 5005 test points, e.g., Digikey# 36-5005-ND)
4. Optional standard SMB or SMA connection points (e.g., Digikey# 1868-1429-ND)
5. Optional 2-pin 100 mil header connector (note: either SMB or header can be assembled)
6. Primary current cables mounting positions (positive current flow direction is left to right)
7. Optional 2-pin 100 mil header connector for voltage drop measurement across the integrated current loop of the current sensor
8. RB1, RB2, RB3, and RB4: rubber bumper mounting positions (e.g., Digikey# SJ61A6-ND)

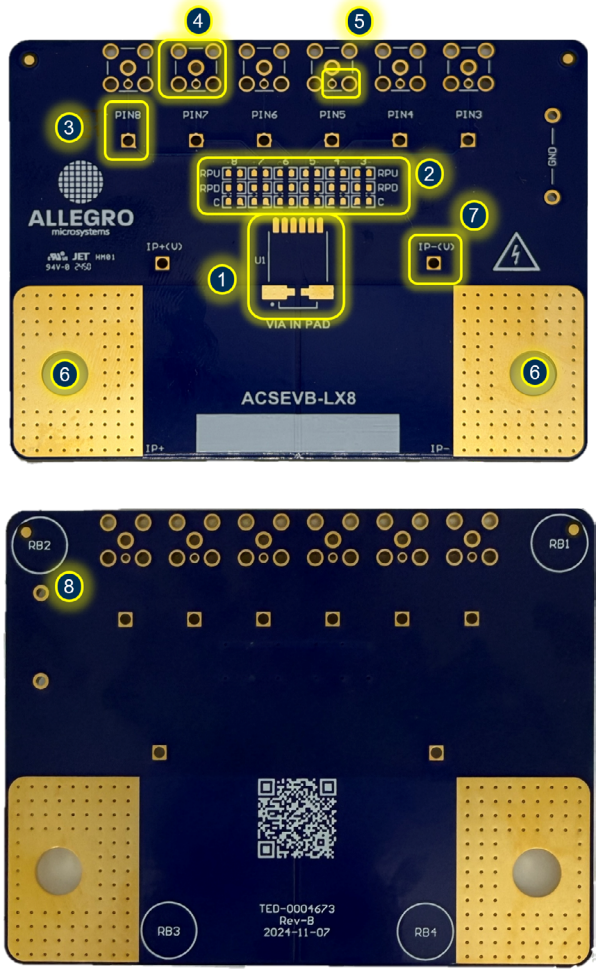


Figure 3: LX Bare Evaluation Board Reference Image

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EVALUATION BOARD PERFORMANCE DATA

Introduction

Self-heating due to the flow of current in the package IP conductor should be considered during the design of any current sensing system. The sensor, printed circuit board (PCB), and contacts to the PCB generate heat and act like a heat sink when current moves through the system.

The thermal response is highly dependent on PCB layout, copper thickness, cooling techniques, and the profile of the injected current. The current profile includes peak current value, current on-time, and duty cycle.

Placing vias under the copper pads of the Allegro current sensor evaluation board minimizes the current path resistance and improves heat-sinking to the PCB, while vias outside of the pads limit the current path to the top of the PCB trace and have worse heat-sinking performance under the part (see Figure 4 and Figure 5). The ACSEVB-LX8 includes vias in pad, which are recommended to improve thermal performance.

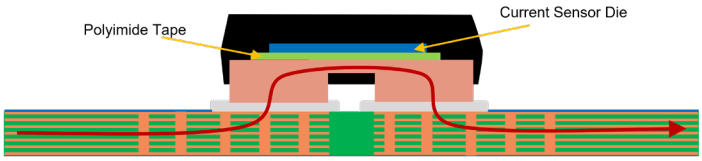

Figure 4: Vias Under Copper Pads

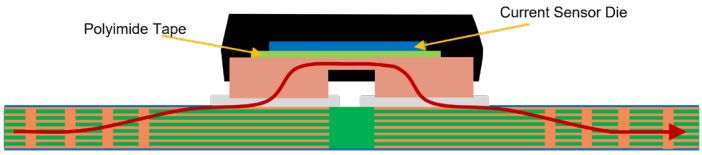

Figure 5: No Vias Under Copper Pads

The thermal capacity of the LX package should be verified by the end user in the application-specific conditions. The maximum junction temperature, $T_{J(max)}$ (165°C), should not be exceeded. Measuring the temperature of the top of the package is a close approximation of the die temperature.

Thermal Characterization

The plot in Figure 6 shows the measured internal temperature of the LX package (this is the approximate temperature of the device die) versus time in seconds at an ambient temperature, T_A, of 25°C. The plot shows several applied currents; current was applied for 300 seconds or until the internal temperature reached the maximum junction temperature 165°C. Figure 6 demonstrates that 200 A maximum continuous DC current can be used without exceeding 165°C. Figure 7 demonstrates that 150 A maximum continuous DC current can be used at an ambient temperature of 85°C without exceeding 165°C. Finally, Figure 8 demonstrates that 100 A maximum continuous DC current can be used at an ambient temperature of 125°C without exceeding 165°C.

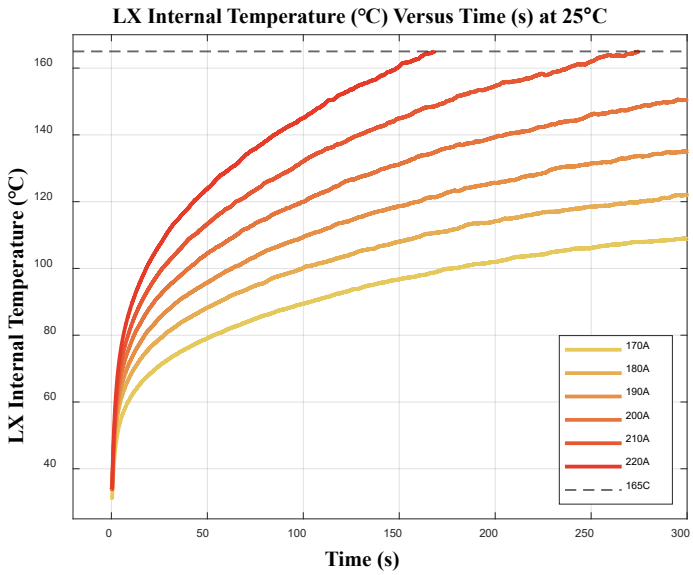

Figure 6: LX Internal Temperature vs. Time at 25°C

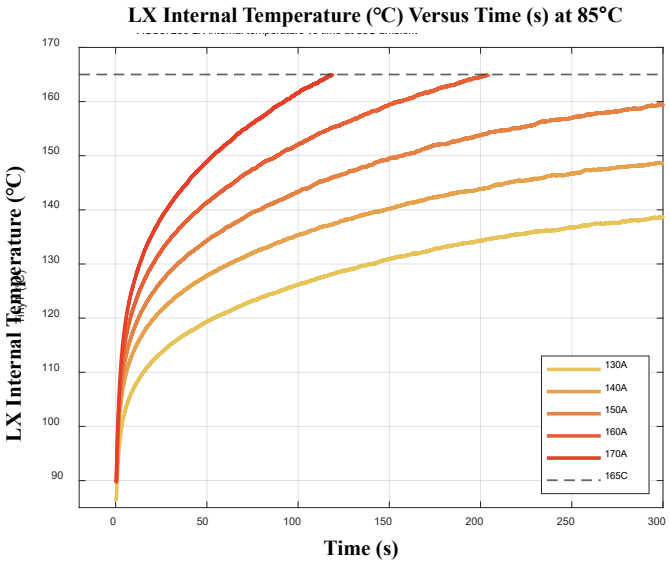

Figure 7: LX Internal Temperature vs. Time at 85°C

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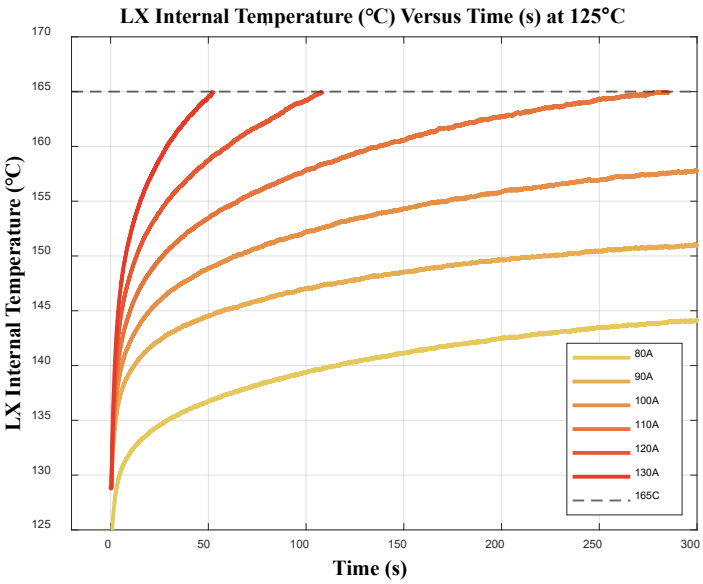

Figure 8: LX Internal Temperature vs. Time at 125°C

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SCHEMATIC

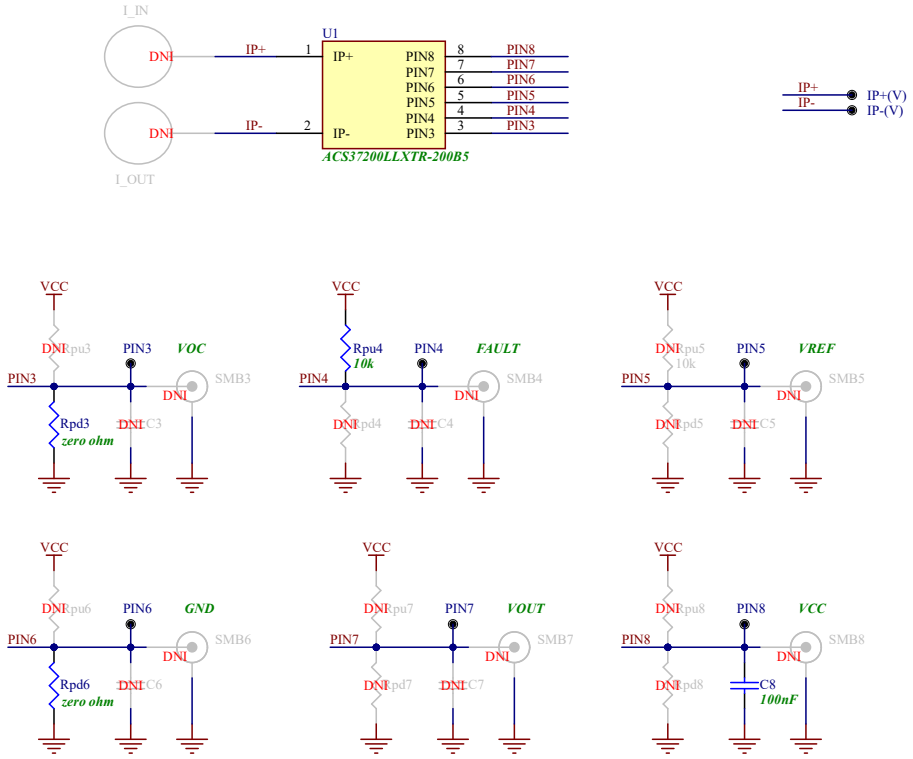

Figure 9: LX Bare Evaluation Board Schematic

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LAYOUT

The LX bare evaluation board has the option for a 2-pin 100 mil header connector, which allows the integrated current-loop resistance to be measured directly from the evaluation board. The voltage drop sensing is routed in the first internal layer (as not to reduce the isolation specification of the package). As a consequence, the voltage drop includes the parasitic resistance of the vias between the top layer and the first interior layer. The following images are not to scale.

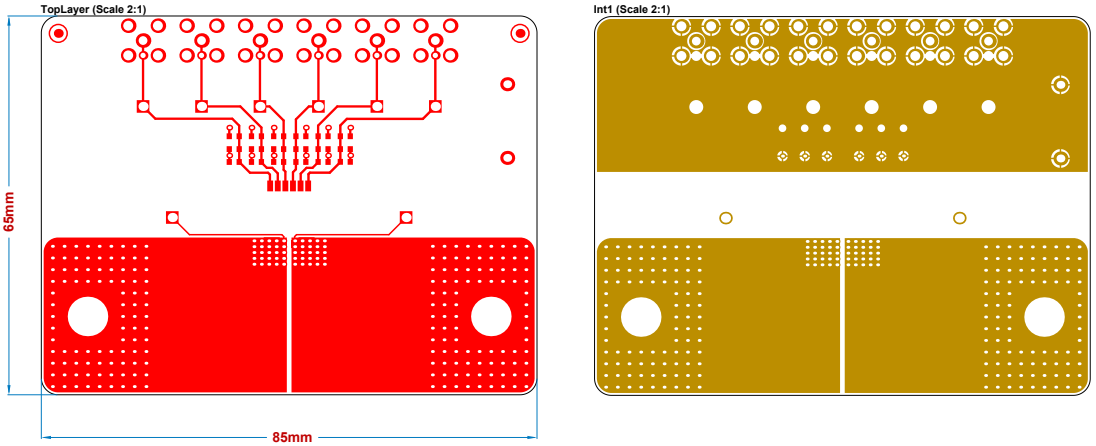

Figure 10: LX Bare Evaluation Board Top Layer (left) and Interior Layer 1 (right)

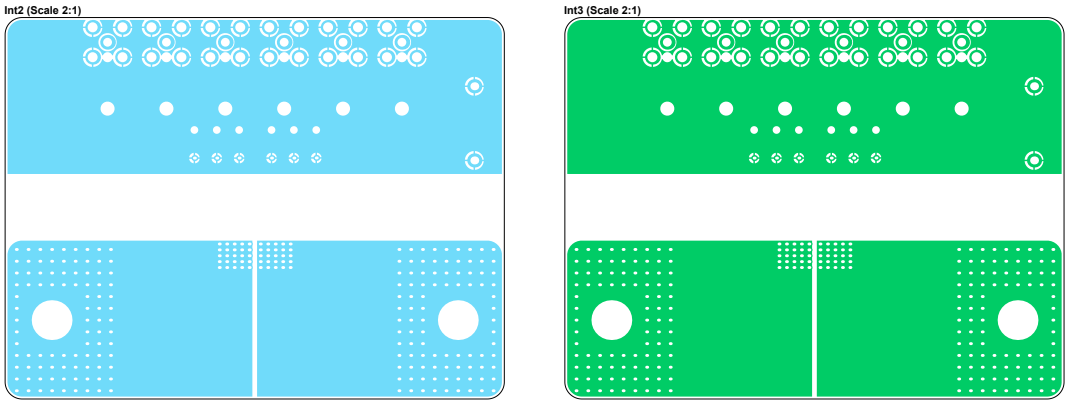

Figure 11: LX Bare Evaluation Board Interior Layer 2 (left) and Interior Layer 3 (right)

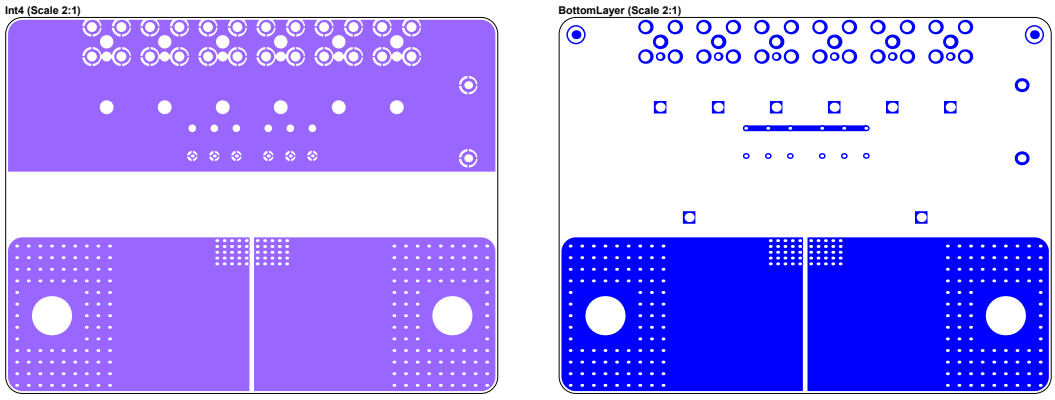

Figure 12: LX Bare Evaluation Board Interior Layer 4 (left) and Bottom Layer (right)

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Revision History

Number	Date	Description
–	January 16, 2026	Initial release

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