APM81815 Evaluation Board User Guide

DESCRIPTION

The APM81815 evaluation board is designed to help system designers evaluate the operation and performance of the APM81815, 80 V, 1.5 A synchronous buck regulator module. The APM81815 evaluation board output voltage can be configured by a jumper configuration of VS1 and VS2.

FEATURES

- APM81815 synchronous buck regulator
- V_{IN} operating range from 5 V to 72 V
- V_{OUT} selectable through jumper configuration
- Low electromagnetic interference (EMI) design
- 20 µA no-load quiescent current.

EVALUATION BOARD CONTENTS

- APEK81815 evaluation board

Figure 1: APEK81815 Evaluation Board

Table of Contents

Table 1: APM81815 Evaluation Board Configurations

Configuration Name	Part Number	Output Current
APM81815	APEK81815KNB-01-T	1.5 A

Table 2: General Specifications

Specification	Min	Typ	Max	Units
Input Operating Voltage	5	–	72	V
Output Current	–	–	1.5	A
Switching Frequency	–	2.1	–	MHz
EN High Threshold	1.15	1.2	1.25	V
EN Input Hysteresis	–	150	–	mV

USING THE EVALUATION BOARD

This section provides an overview of the connections and configuration options of the APM81815 evaluation board. For each group of connections highlighted in Figure 2, a detail section follows. The default jumper positions are highlighted in blue. The APM81815 datasheet contains detailed information about the use and functionality of each pin. The datasheet should be consulted for more detailed information than is contained in this user guide.
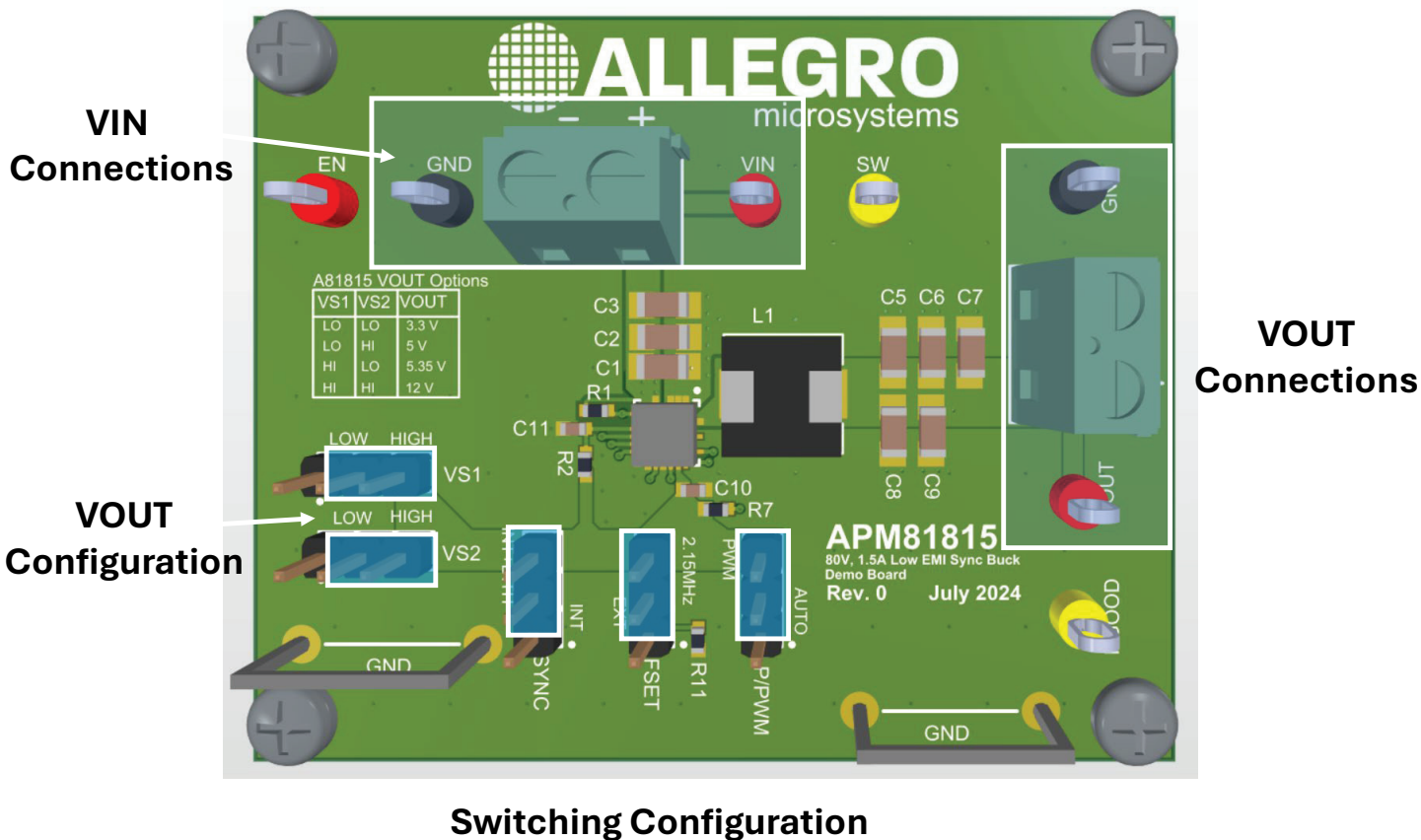

Figure 2: APM81815 Evaluation Board Input and Output (I/O) Connections and Default Jumper Positions

Power Input

Connect a power supply to the green terminal block using two wires and tighten down the screws to clamp the wires in place. Clip leads can be used on the test points located on either side of the green terminal block. Observe the polarity on the board, connect VIN to the positive supply terminal and GND to the negative supply terminal.

Power Output

Connect the load to the terminal block on the right side of the board and tighten down the screws to clamp the two wires in place, or use clip leads on either side of the terminal block. Observe the polarity for the load with VOUT as the positive terminal and GND as the negative terminal.

Output Voltage

The APM81815 evaluation board is configured for a 12 V output. However, it can be reconfigured for lower voltages using jumpers VS1 and VS2, per the table printed on the evaluation board next to the jumpers, which is repeated here, in Table 3.

Table 3: Output Voltage Configuration

APM81815 VOUT Options		
VS1	VS2	VOUT
LO	LO	3.3 V
LO	HI	5 V
HI	LO	5.35 V
HI	HI	12 V

Enable

The APM81815 evaluation board is configured with a 0 Ω resistor from VIN to the enable (EN) pin for continuous operation. If an external enable signal is required, the 0 Ω resistor R1 must be removed. An external enable signal can be applied to the enable test pin.

Sync

- To enable frequency dithering, place the SYNC jumper in the INT+DITH position.

- To disable frequency dithering, place the SYNC jumper in the INT position.

- To synchronize the APM81815 switching frequency with an external clock, remove the SYNC jumper and drive the center pin of the three-pin header with the external clock.

FSET

- To set the switching frequency to an internally generated 2.15 MHz, place the jumper in the 2.15MHz position.

- To set the frequency between 400 kHz and 2.4 MHz, use resistor R3 and move the jumper to the EXT position.

LP/PPM

- To configure the device for the always-on PWM mode, move the AUTO jumper to the PWM position.

- To configure the device for the low-power mode, move the jumper to the LP/PWM position; this allows the device to enter into low-power mode when the load condition is light.

Startup Procedure

To begin using the APM81815 evaluation board, follow the instructions below and refer to the diagram in Figure 2 or the test point descriptions outlined in Table 4.

1. Ensure the two jumpers for VS1 and VS2 are in the proper positions for the desired output voltage.

2. Connect a load to the regulated output connections of the APM81815 evaluation board.

3. Apply an input voltage across the power-input terminals that is higher than the expected output voltage. Do not exceed 72 V at the power-input connections. To ensure desirable startup behavior, the input power source should be able to supply twice the regulated output current level (1.5 A on the standard APM81815 evaluation board).

Table 4: APM81815 Test-Point Descriptions

Test Point	Description
VIN	Positive terminal for input-voltage connection or sensing.
GND	Negative terminal for input-voltage connection or sensing.
VOUT	Positive terminal for the output connection to the load.
GND	Negative terminal for the output connection to the load.
EN	Enable pin input. If an external signal is applied to the EN test point, remove R1.
PGOOD	Power good open-drain signal. If the output voltage is out of range, this pin asserts low.
SW	Regulator-switch node output pin. This pin is intended for oscilloscope probe analysis. Do not connect circuits to this pin.

EVALUATION BOARD PERFORMANCE DATA

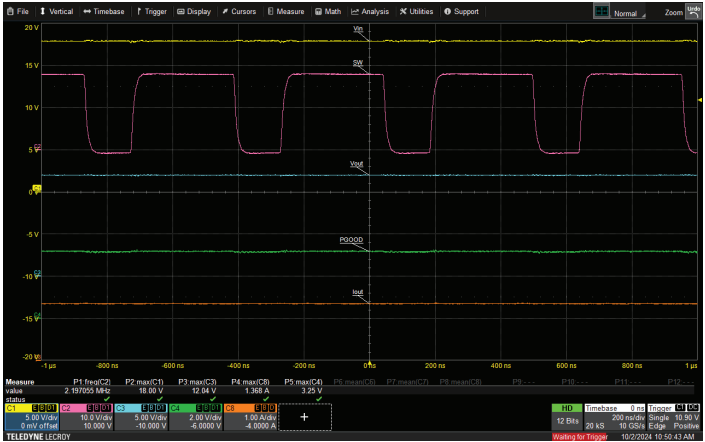**Figure 3: Startup, 8.6 Ω Load, Enable = VIN, VIN = 18 V**

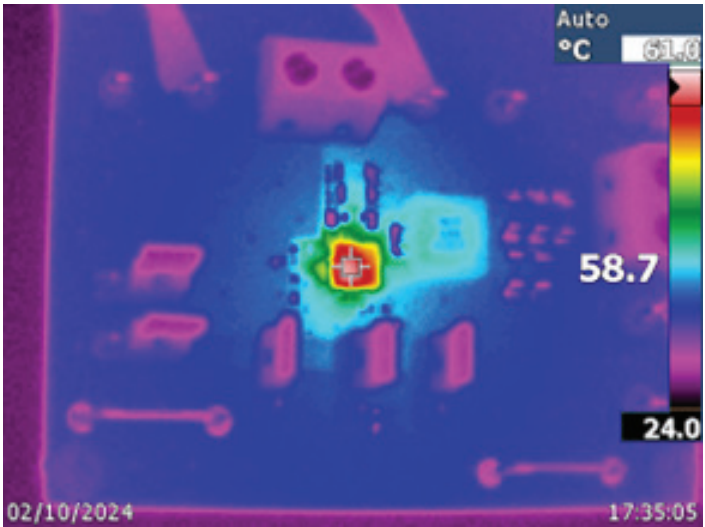**Figure 4: Typical Operation, PGOOD Pin Remains High**

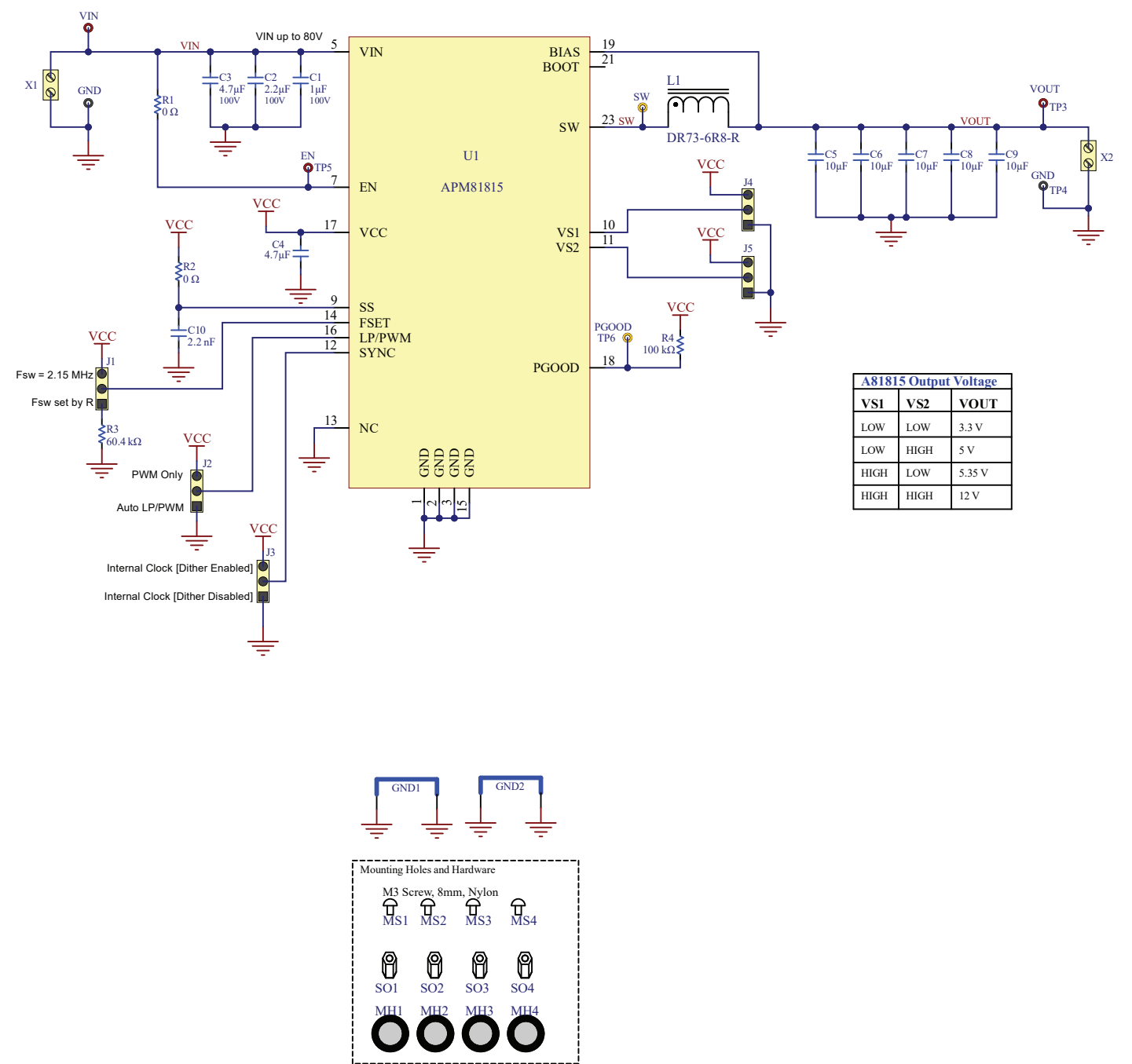**Figure 5: Thermal Performance, 8.6 Ω Load,
Enable = VIN, VIN = 18 V**

SCHEMATIC

A81815 Output Voltage		
VS1	**VS2**	**VOUT**
LOW	LOW	3.3 V
LOW	HIGH	5 V
HIGH	LOW	5.35 V
HIGH	HIGH	12 V

Figure 6: APM81815 Evaluation Board Schematic

BILL OF MATERIALS

Table 5: APM81815 Evaluation Board Bill of Materials

| Line #	Description	Designator	Qty	Manufacturer	Manufacturer Part Number	Supplier	Supplier Part Number
1	Capacitor, ceramic, 1 µF, 100 V, X7R, 1206	C1	1	Samsung	CL31B105KCHSNNE	Digikey	1276-2747-1-ND
2	Capacitor, ceramic, 2.2 µF, 100 V, X7S, 1206	C2	1	TDK	CGA5L3X7S2A225M160AB	Digikey	445-12947-1-ND
3	Capacitor, ceramic, 4.7 µF, 100 V, X7R, 1206	C3	1	Kyocera AVX	KGM31HS72A475KU	Digikey	478-KGM31HS72A475KUCT-ND
4	Capacitor, ceramic, 4.7 µF, 16 V, X5R, 0603	C4	1	TDK	C1608X5R1C475K080AC	Digikey	445-7478-6-ND
5	Capacitor, ceramic, 10 µF, 25 V, X7R, 1206	C5, C6, C7, C8, C9	5	Murata	GRM31CR71E106MA12L	Digikey	490-6519-1-ND
6	Capacitor, ceramic, 2.2 nF, 25 V, X7R, 0603	C10	1	KEMET	C0603C222J3RAC7867	Digikey	399-C0603C222J3RAC7867CT-ND
7	Ground bar, 18 AWG bus bar, 12 mm body	GND1, GND2	2	Jameco	8019000100-JVP		
8	Connection header, vertical, 3-position, 2.54 mm	J1	1	Wurth Electronics	61300311121	Digikey	732-5316-ND
9	Connection header, vertical, 3-position, 2.54 mm	J2	1	Wurth Electronics	61300311121	Digikey	732-5316-ND
10	Connection header, vertical, 3-position, 2.54 mm	J3	1	Wurth Electronics	61300311121	Digikey	732-5316-ND
11	Connection header, vertical, 3-position, 2.54 mm	J4	1	Wurth Electronics	61300311121	Digikey	732-5316-ND
12	Connection header, vertical, 3-position, 2.54 mm	J5	1	Wurth Electronics	61300311121	Digikey	732-5316-ND
13	Inductor, 6.8 µH, 2.55 A, 43.5 mΩ	L1	1	Eaton Cooper	DR73-6R8-R	Digikey	513-1134-1-ND
				Wurth Elektronik	784777068	Digikey	732-6757-1-ND
14	M3-sized mounting hole	MH1, MH2, MH3, MH4	4				
15	M3 × 8 mm pan-head screw	MS1, MS2, MS3, MS4	4	Wurth Electronics	97790803111	Digikey	732-13705-ND
16	Resistor, 0 Ω, 1/10 W, jumper, 0603	R1, R2	2	Bourns	CR0603-J/-000ELF	Digikey	CR0603-J/-000ELFCT-ND
17	Resistor, 60.4 kΩ, 1/10 W, 1%, 0603	R3	1	Panasonic	ERJ-3EKF6042V	Digikey	P60.4KHDKR-ND
18	Resistor, 100 kΩ, 1/10 W, 1%, 0603	R4	1	Panasonic	ERJ-3EKF1003V	Digikey	P100KHDKR-ND
19	Standoffs and spacers, 5.0 hex, 15.0 mm nylon	SO1, SO2, SO3, SO4	4	Keystone Electronics	25512	Digikey	36-25512-ND
20	Test point, red, through-hole mount, 1.6 mm	TP1	1	Keystone Electronics	5010	Digikey	36-5010-ND
21	Test point, black, through-hole mount, 1.6 mm	TP2, TP4	2	Keystone Electronics	5011	DigiKey	36-5011-ND
22	Test point, red, through-hole mount, 1.6 mm	TP3	1	Keystone Electronics	5010	Digikey	36-5010-ND
23	Test point, red, through-hole mount, 1.6 mm	TP5	1	Keystone Electronics	5010	Digikey	36-5010-ND
24	Test point, yellow, through-hole mount, 1.6 mm	TP6	1	Keystone Electronics	5014	Digikey	36-5014-ND
25	Test point, yellow, through-hole mount, 1.6 mm	TP7	1	Keystone Electronics	5014	Digikey	36-5014-ND
26	APM81815 in MIS package	U1	1				
27	Terminal block, 5.08 mm, vertical, 2-position	X1, X2	2	Phoenix Contact	1729128	Digikey	277-1247-ND

LAYOUT
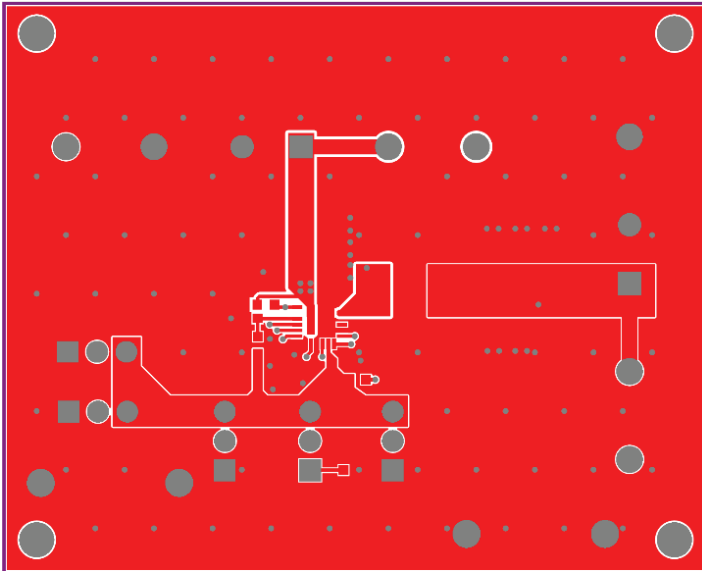
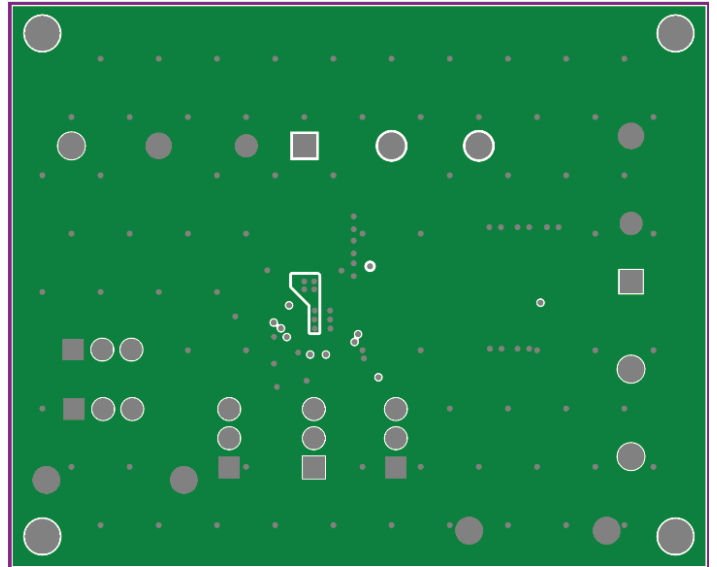**Figure 7: Top Layer 1 PCB**

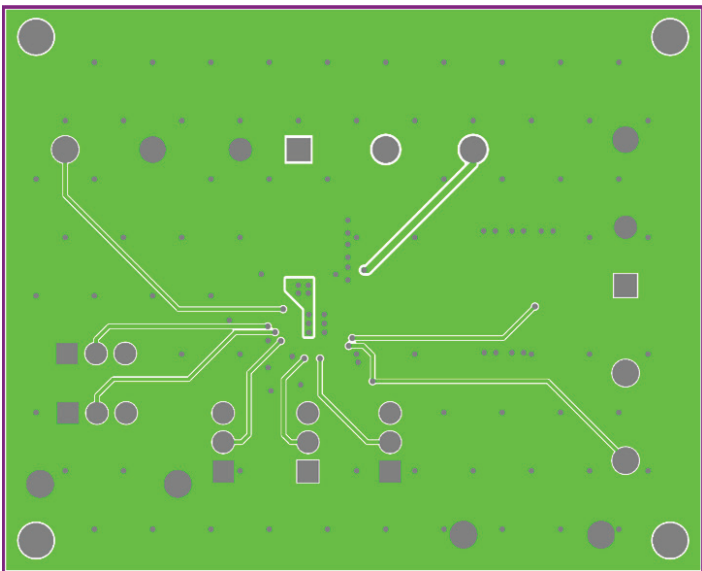**Figure 8: Inner Layer 2 PCB (PGND Plane)**

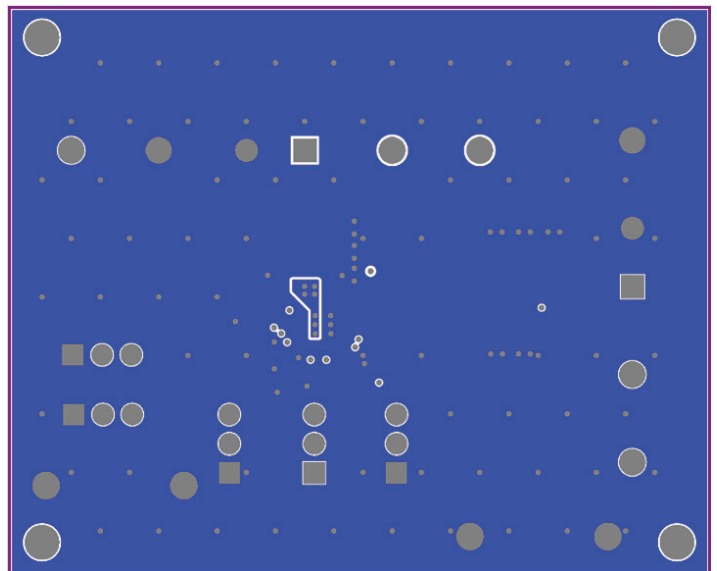**Figure 9: Inner Layer 3 PCB (PGND Plane)**

Figure 10: Bottom Layer 4 PCB

RELATED LINKS

- Product page https://www.allegromicro.com/en/products/regulate/clearpower-modules/regulator-modules/apm81815
- Datasheet: https://www.allegromicro.com/-/media/files/datasheets/apm81815-datasheet.pdf

APPLICATION SUPPORT

- Application support web page: https://www.allegromicro.com/en/about-allegro/contact-us/technical-assistance

Revision History

Number	Date	Description
–	October 16, 2024	Initial release
1	March 31, 2025	Added second source for TE L1 component to bill of materials (page 6)