APEK85003K15ES-02-MH

AHV85003/043 Evaluation Board User Guide

DESCRIPTION

The Allegro MicroSystems APEK85003K15ES-02-MH is an evaluation board for the AHV85003 and AHV85043 isolated SiC driver chipset. This driver provides a self-powered isolated gate drive solution for SiC FETs.

The APEK85003K15ES-02-MH evaluation board contains a AHV85003 and AHV85043 chipset coupled with external transformer to form a single channel driver.

The evaluation board can be used evaluate the AHV85003 and AHV85043 Isolated SiC driver chipset devices in isolation when driving a fixed capacitor load, and can be used to interface to to an external SiC FET when in an application board.

FEATURES

- Single channel isolated SiC FET driver.
- Positive gate drive voltage of 15 V
- Negative gate drive off voltage adjustable from –5 to 0 V
- No secondary side or bootstrap components required.
- Drives SiC FET Qg up to 130 nC

EVALUATION BOARD CONTENTS

- APEK85003K15ES-02-MH evaluation board

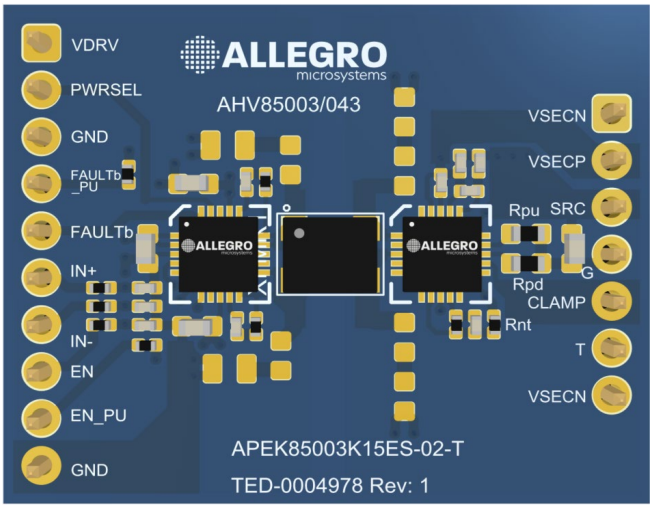

Figure 1: APEK85003K15ES-02-MH Evaluation Board

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DANGER

DO NOT TOUCH THE BOARD WHEN IT IS ENERGIZED AND ALLOW ALL COMPONENTS TO DISCHARGE COMPLETELY PRIOR HANDLING THE BOARD.

HIGH VOLTAGE CAN BE EXPOSED ON THE BOARD WHEN IT IS CONNECTED TO POWER SOURCE. EVEN BRIEF CONTACT DURING OPERATION MAY RESULT IN SEVERE INJURY OR DEATH.

Please ensure that appropriate safety procedures are followed. This evaluation kit is designed for **engineering evaluation in a controlled lab environment and should be handled by qualified personnel ONLY.** Never leave the board operating unattended.

WARNING

Some components can be hot during and after operation. There is NO built-in electrical or thermal protection on this evaluation kit. The operating voltage, current, and component temperature should be monitored closely during operation to prevent device damage.

CAUTION

This product contains parts that are susceptible to damage by electrostatic discharge (ESD). Always follow ESD prevention procedures when handling the product.

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USING THE EVALUATION BOARD

The following section includes the evaluation board pinout tables, quick start guide, and overview of features needed for setup.

Evaluation Board Pinout

The evaluation board pinouts are shown below in table 1 and table 2.

Table 1: APEK85003K15ES-02-MH primary connector pinout (CONN2)

Pin Number	Pin Name	Function
1	VDRV	Primary bias supply voltage
2	PWRSEL	Output power throughput adjustment
3	GND	Ground
4	FAULTb_PU	Fault pull-up resistor to VDRV
5	FAULTb	FAULT output. Open drain
6	IN+	Input PWM signal (positive logic)
7	IN–	Input PWM signal (negative logic)
8	EN	Driver enable
9	EN_PU	EN pull-up to VDRV
10	GND	Ground

Table 2: APEK85003K15ES-02-MH secondary connector pinout (CONN1)

Pin Number	Pin Name	Function
1	VSECN	Negative gate drive supply rail referenced to SOURCE
2	VSECP	Positive gate drive supply rail referenced to SOURCE
3	SOURCE	SOURCE connection of the driven SiC FET
4	VGATE	GATE connection of the driven SiC FET
5	CLAMP	Miller clamp pull-down to VSECN
6	TEST	Test pin. Must be connected to VSECN
7	VSECN	Negative gate drive supply rail referenced to SOURCE

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Quick Start Guide

The steps below are required to set up the APEK85003K15ES-02-MH for first-time use.

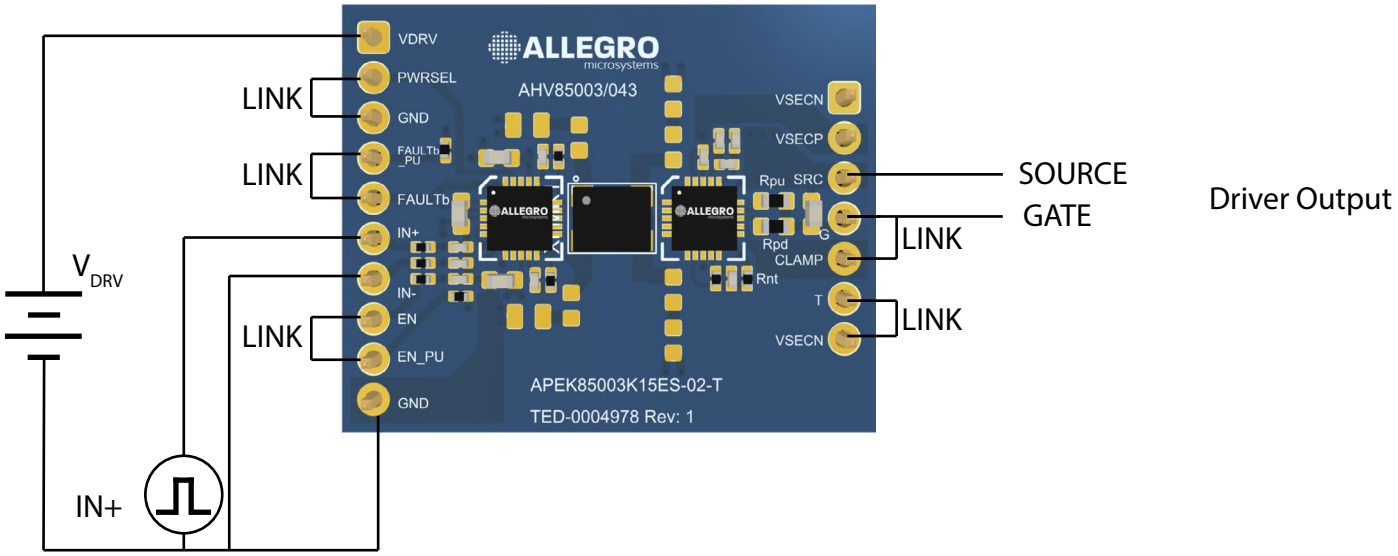

Figure 2: APEK85003K15ES-02-MH Quick Start Diagram

1. Link pins as shown above:
   A. EN_PU to EN (if not using external Enable control)
   B. PWRSEL to GND. See datasheet for PWRSEL options.
   C. FAULTb to FAULTb_PU to use internal pull up resistor for FAULT.
   D. CLAMP to GATE to use internal Miller clamp.
   E. T to VSECN.
2. Apply V_{DRV} = 12 V.
3. Apply input signal to IN+.
4. Observe the driver output from VGATE – SOURCE.

Gate Pull-up and Pull-down Resistors

The AHV85043 gate driver has independent output pins for the gate pull-up and gate pull-down allowing control of the turn-on and turn-off rise and fall times.

The default values for these resistors are:

OUTPU: R_{PU} = 10 Ω

OUTPD: R_{PD} = 1.0 Ω

The user can modify these values to suit their application.

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Start Sequence

When the primary supply voltage VDRV is applied, the primary side of the driver remains in low power mode until VDRV exceeds the UVLO threshold. Once the UVLO threshold is exceeded, the internal LDOs and regulators are enabled. If the EN input is held low, the primary side stays in a low power standby mode, with the FAULT output held low. Once EN goes high, or if EN is already high when VDRV UVLO is released, then the primary side of driver enables power transfer to the secondary, to charge the secondary-side isolated bias rails. When the secondary-side bias rails have settled to the target regulation levels, and if no faults are detected on either the primary side or the secondary side, then the open-drain FAULT pin is allowed to go high, via the required external pull-up resistor. This indicates to the system controller that the driver is ready to accept PWM input. Any PWM inputs at the IN+/IN– pins are ignored until the internal FAULT pull-down is released.

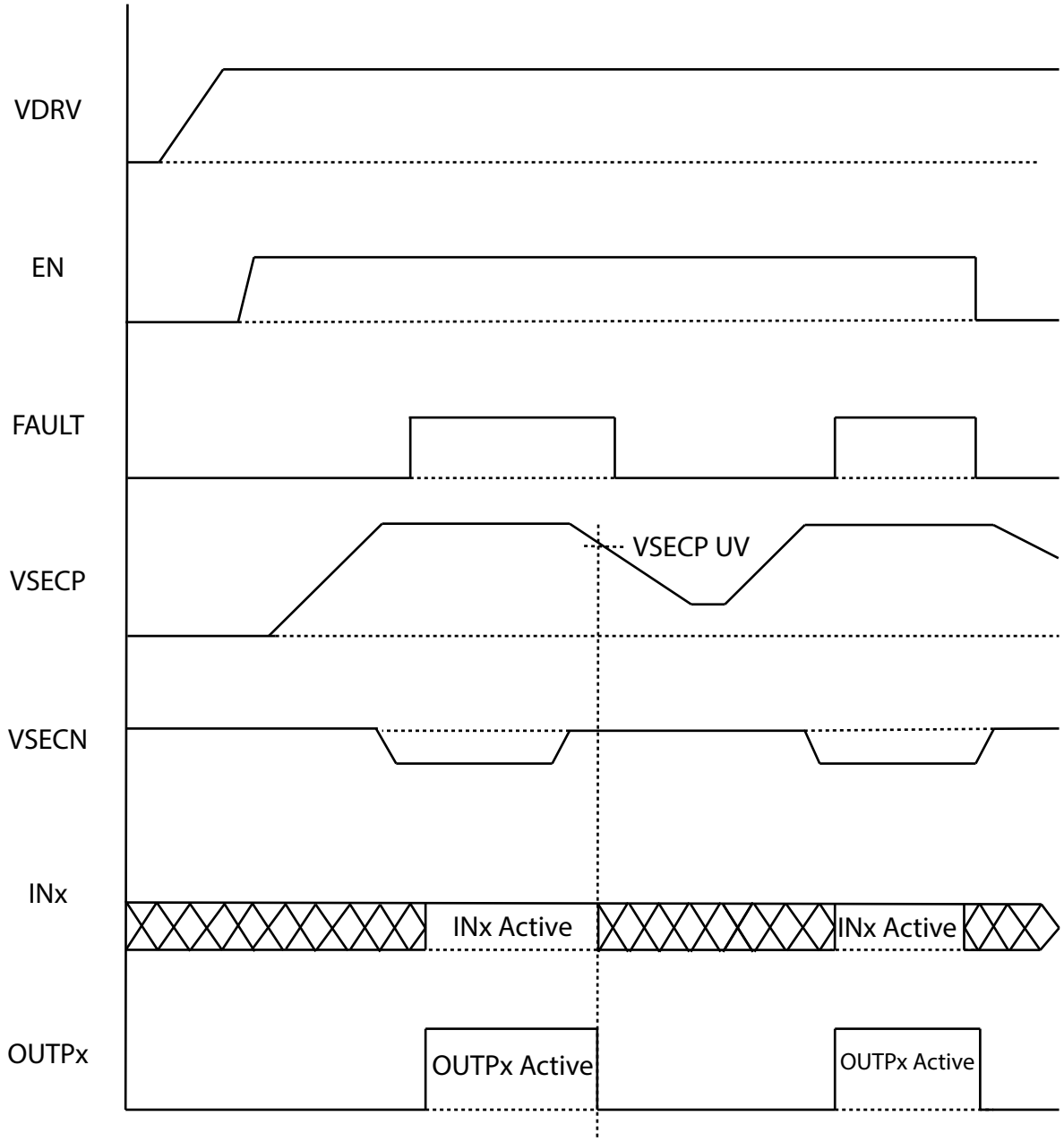

Figure 3: AHV85003/AHV85043 Start up sequence

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Negative Gate Drive Supply Rail

The APEK85003K15ES-02-MH has a default negative gate drive supply rail voltage of –4 V. This voltage can be set to between 0 V and –5 V. For full details, see datasheet.

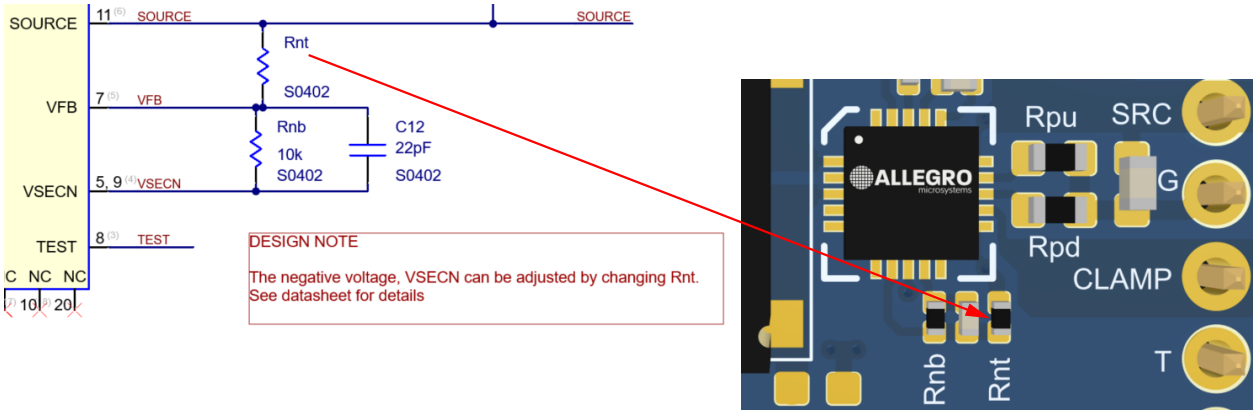

Figure 4: VSECN Adjustment

Power Selection Pin (PWRSEL)

The AHV85003 PWRSEL pin allows the user to adjust the rate of energy transfer to the secondary side, to suit load FETs with differing levels of gate charge. Three settings are selectable, by connecting the PWRSEL pin to GND or VDRV or leaving it open (floating). The PWRSEL pin setting is sampled only during startup and is in force until the VDRV pin is power cycled.

On the APEK85003K15ES-02-MH EVM board, PWRSEL can be selected at connector CONN2. The connector and explanatory table for selection is shown in figure 5.

PWRSEL Selection	Pulse-width Range	$QG_{(TOT)}$ Maximum (nC)
GND	Low	50
Open (floating)	Medium	85
VDRV	High	130

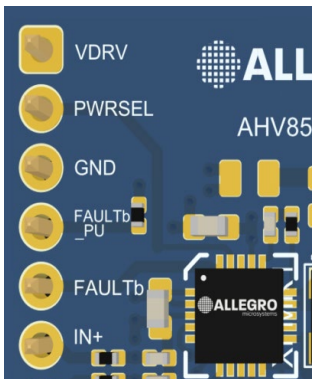

Figure 5: PWRSEL Selection

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EVALUATION BOARD PERFORMANCE DATA

Typical Measurements of Propagation Delay

The typical measurements of prpagation delay are as follows: V_{DRV} = 12 V, Input = 100 kHz, R_{PU} = 10 Ω, R_{PD} = 1.0 Ω and C_{LOAD} = 1 nF. Typical driver output at 100 kHz is shown in figure 6.

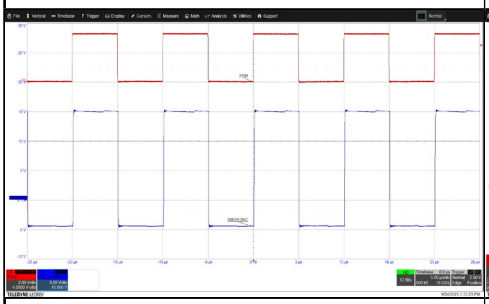
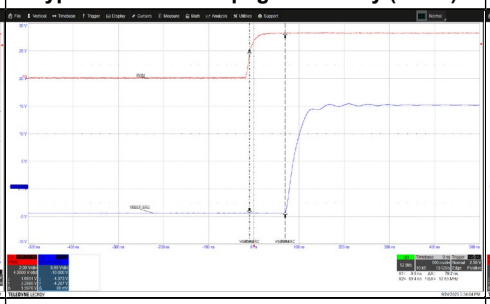
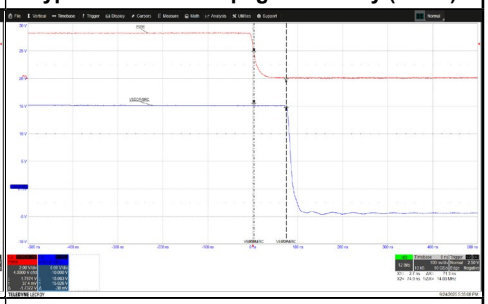
Overview	Typical Turn-on Propagation Delay (79 ns)	Typical Turn-off Propagation Delay (79 ns)
		
CH2 (Red): Driver Input **CH5 (Blue):** VGATE-SRC	**CH2 (Red):** Driver Input **CH5 (Blue):** VGATE-SRC	**CH2 (Red):** Driver Input **CH5 (Blue):** VGATE-SRC

Figure 6: Typical Driver Output at 100 kHz

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SCHEMATIC

The APEK85003K15ES-02-MH evaluation board schematic is shown in figure 7.

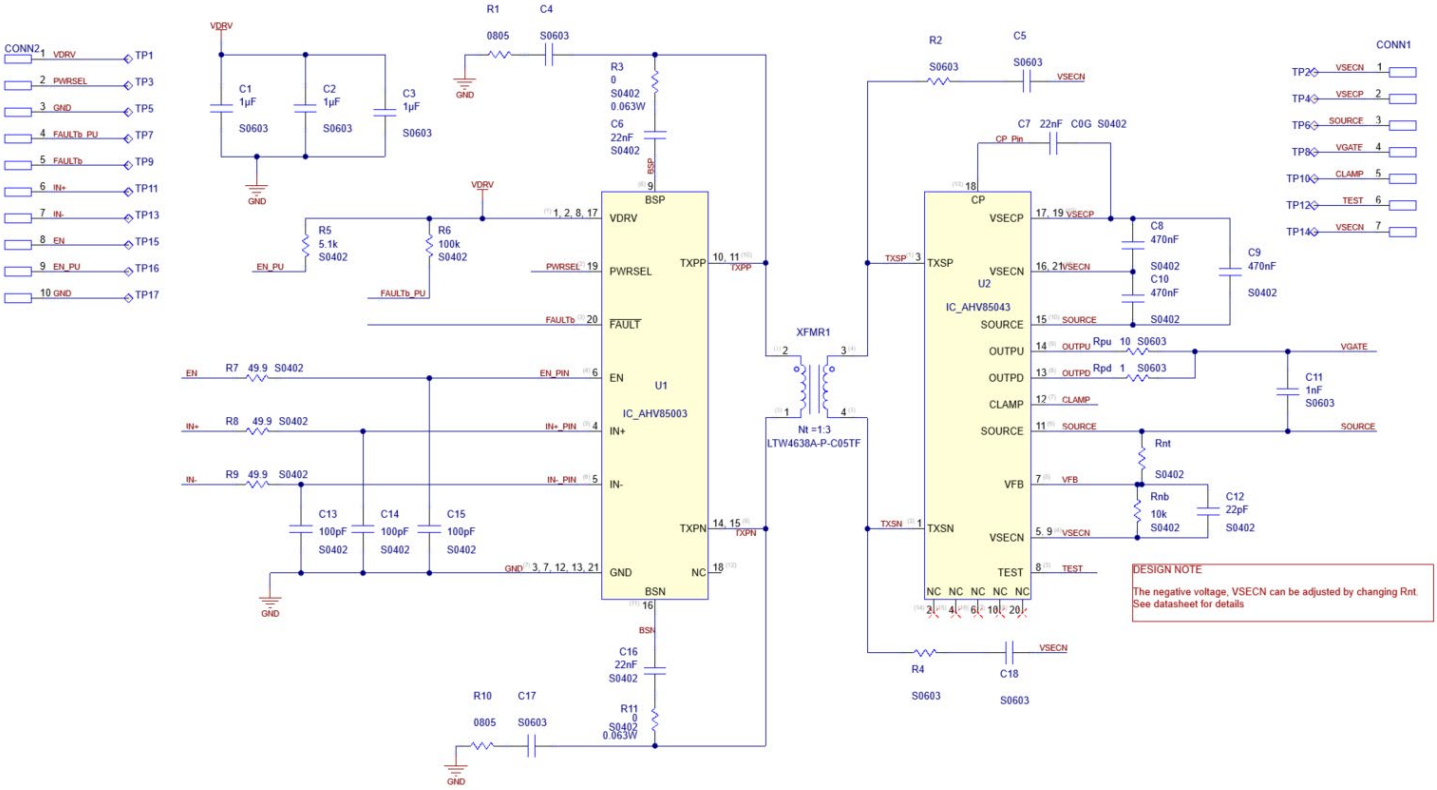

Figure 7: APEK85003K15ES-02-MH Schematic

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LAYOUT

The evaluation board layout is shown in figure 8 and figure 9.

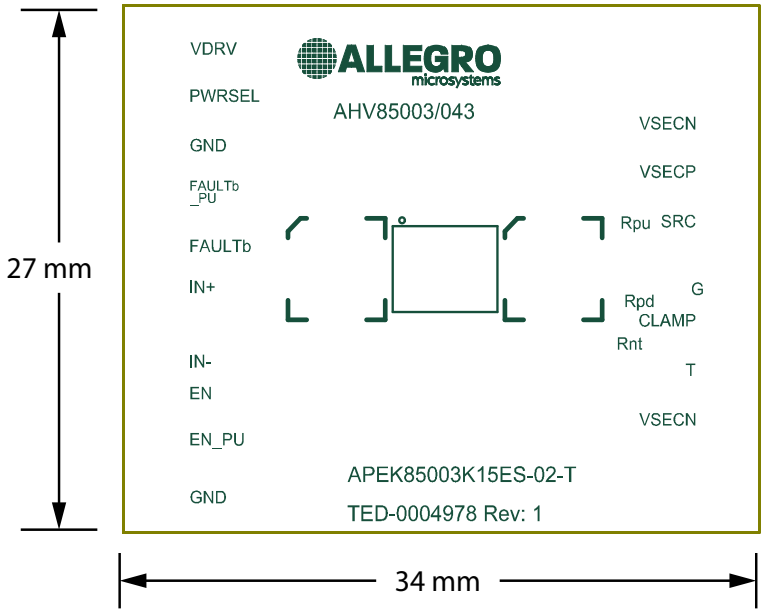

Figure 8: APEK85003K15ES-02-MH Top Overlay

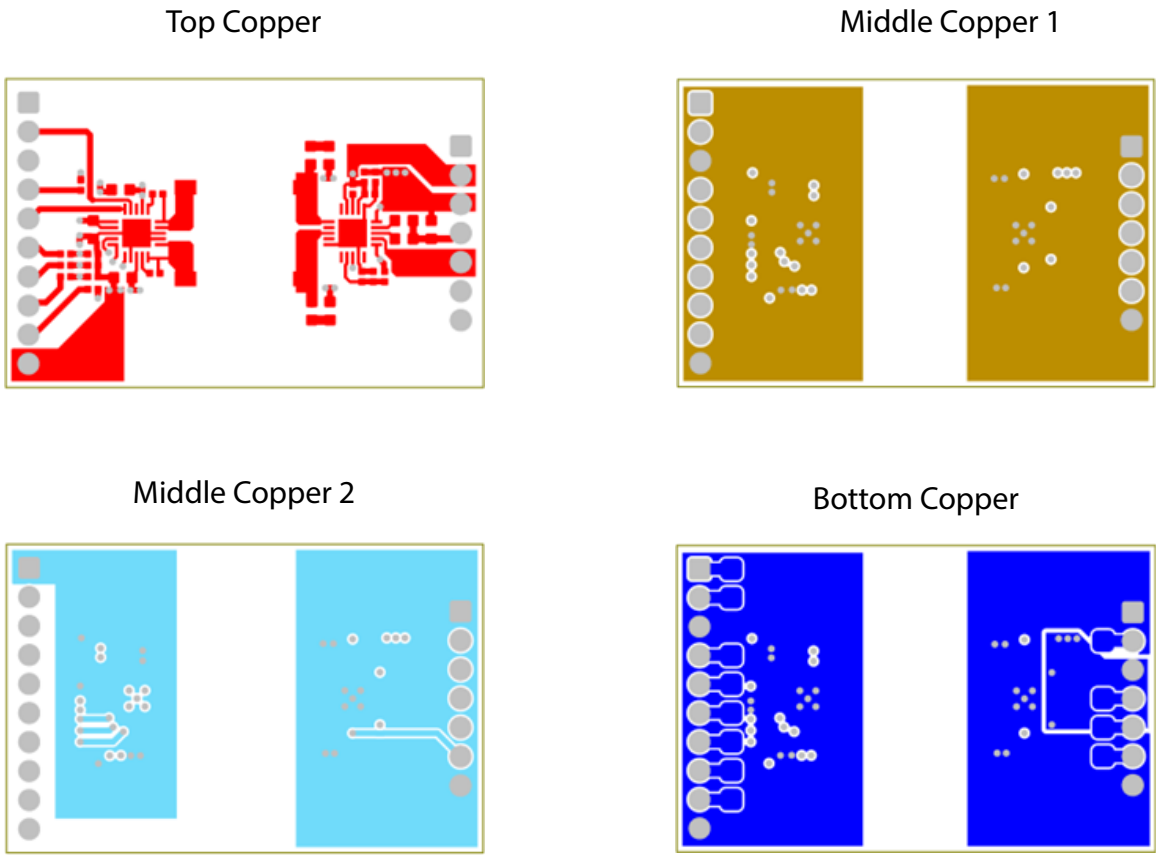

Figure 9: APEK85003K15ES-02-MH PCB Copper Layers

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BILL OF MATERIALS

The APEK85003K15ES-02-MH Evaluation Board Bill of Materials is shown in table 3.

Table 3: APEK85003K15ES-02-MH Evaluation Board Bill of Materials

ELECTRICAL COMPONENTS					
Designator	**Quantity**	**Description**	**Manufacturer**	**Manufacturer Part Number**	**Value**
C1, C2, C3	3	CAP, CER, 1 µF, 50 V, X5R, 0603	TDK	C1608X5R1H105K080AB	1 µF
C4, C5, C17, C18	0	Not Installed	–	–	–
C6, C7, C16	3	CAP, CER, 22 nF, 50 V, COG/NPO, 0402	Yageo Group	CC0402KRX7R9BB223	22 nF
C8, C9, C10	3	CAP, CER, 0.47 µF, 50 V, X5R, 0402	Yageo Group	CC0402KRX5R9BB474	470 nF
C11	1	CAP, CER, 1 nF, 50 V, C0G, 0603	Murata	GRM1885C1H102JA01D	1 nF
C12	1	CAP, CER, 22 pF, 50 V, C0G, 0402	TDK	CGA2B2C0G1H220J050BA	22 pF
C13, C14, C15	3	CAP, CER, 100 pF, 50 V, COG/NPO, 0402	Murata	GCM1555C1H101JA16D	100 pF
R1, R2, R4, R10	0	Not Installed	–	–	–
R3, R11	2	RES, 0R, 0.063 W, 1%, 0402	Walsin Technologies	WR04X000 PTL	0
R5	1	RES, 5.1k, 0.063 W, 1%, 0402	TE Connectivity	CRG0402F5K1	5.1k
R6	1	RES, 100k, 0.063 W, 1%, 0402	Yageo Group	RC0402FR-13100KL	100k
R7, R8, R9	3	RES, 49.9R, 0.063 W, 1%, 0402	Vishay	CRCW040249R9FKED	49.9
Rnb	1	RES, 10k, 0.10 W, 1%, 0402	Panasonic	ERJ-2RKF1002X	10k
Rnt	1	RES, 30.1k, 63 mW, 1%, 0402	Yageo Group	RC0402FR-0730K1L	30.1k
Rpd	1	RES, 1R, 0603, 0.25 W, 5%, Anti Surge	TE Connectivity	CRGS0603J1R0	1
Rpu	1	RES, 10R, 0603, 0.25 W,1%, Anti Surge	Bourns	CMP0603AFX-10R0ELF	10
U1	1	AHV85003 Primary IC, QFN-20 4×4×0.8, 15 V	Allegro MicroSystems	AHV85003K15ESTR	–
U2	1	AHV85043 Secondary IC, QFN-20 4×4×0.8, 15 V	Allegro MicroSystems	AHV85043K15ESTR	–
XMFR1	1	XFMR, AHV85003, 1:3, LTW4638A-P-C05TF. Func Isol	SUNLORD	LTW4638A-P-C05TF	–
OTHER COMPONENTS					
Designator	**Quantity**	**Description**	**Manufacturer**	**Manufacturer Part Number**	**Value**
CONN1	1	Pin Header, Board-to-Board, 2.54 mm, 1 Rows, 7 Contacts, Through Hole Straight	Multicomp	2211S-07G	Connector 7 Way
CONN2	1	Pin Header, Board-to-Board, 2.54 mm, 1 Rows, 10 Contacts, PTH	Wurth Electronik	61301011121	Connector 10 Way
PCB1	1	PCB from gerber files	Allegro MicroSystems	Gerbers TED-0004978 Rev: 1	–

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Revision History

Number	Date	Description
–	December 11, 2025	Initial release

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