APEK85003K18ES-04-MH

AHV85003/043 Evaluation Board User Guide

DESCRIPTION

The Allegro MicroSystems APEK85003K18ES-04-MH is an evaluation board for the AHV85003 and AHV85043 isolated SiC driver chipset. This driver provides a self-powered isolated gate drive solution for SiC FETs.

The APEK85003K18ES-04-MH evaluation board contains an AHV85003 and AHV85043 chipset coupled with external transformer to form a single channel driver.

The evaluation board can be used evaluate the AHV85003 and AHV85043 Isolated SiC driver chipset devices in isolation when driving a fixed capacitor load, and can be used to interface to to an external SiC FET when in an application board.

FEATURES

- Single channel isolated SiC FET driver.
- Positive gate drive voltage of 18 V
- Negative gate drive off voltage adjustable from –3 to 0 V
- No secondary side or bootstrap components required.
- Drives SiC FET Qg up to 130 nC

EVALUATION BOARD CONTENTS

- APEK85003K18ES-04-MH evaluation board

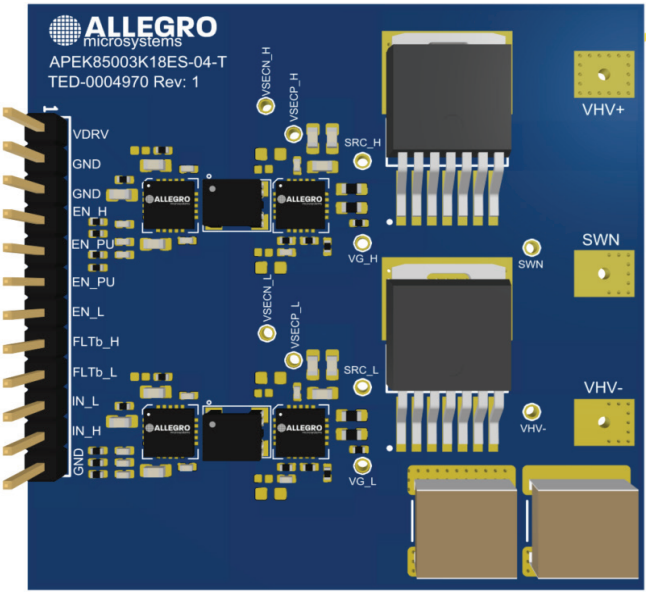

Figure 1: APEK85003K18ES-04-MH Evaluation Board

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DANGER

DO NOT TOUCH THE BOARD WHEN IT IS ENERGIZED AND ALLOW ALL COMPONENTS TO DISCHARGE COMPLETELY PRIOR HANDLING THE BOARD.

HIGH VOLTAGE CAN BE EXPOSED ON THE BOARD WHEN IT IS CONNECTED TO POWER SOURCE. EVEN BRIEF CONTACT DURING OPERATION MAY RESULT IN SEVERE INJURY OR DEATH.

Ensure that appropriate safety procedures are followed. This evaluation kit is designed for **engineering evaluation in a controlled lab environment and should be handled by qualified personnel ONLY.** Never leave the board operating unattended.

WARNING

Some components can be hot during and after operation. There is NO built-in electrical or thermal protection on this evaluation kit. The operating voltage, current, and component temperature should be monitored closely during operation to prevent device damage.

CAUTION

This product contains parts that are susceptible to damage by electrostatic discharge (ESD). Always follow ESD prevention procedures when handling the product.

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USING THE EVALUATION BOARD

The following section includes the evaluation board quick start guide, and overview of features needed for use.

Quick Start Guide

The steps below are required to set up the APEK85003K18ES-04-MH for first-time use.

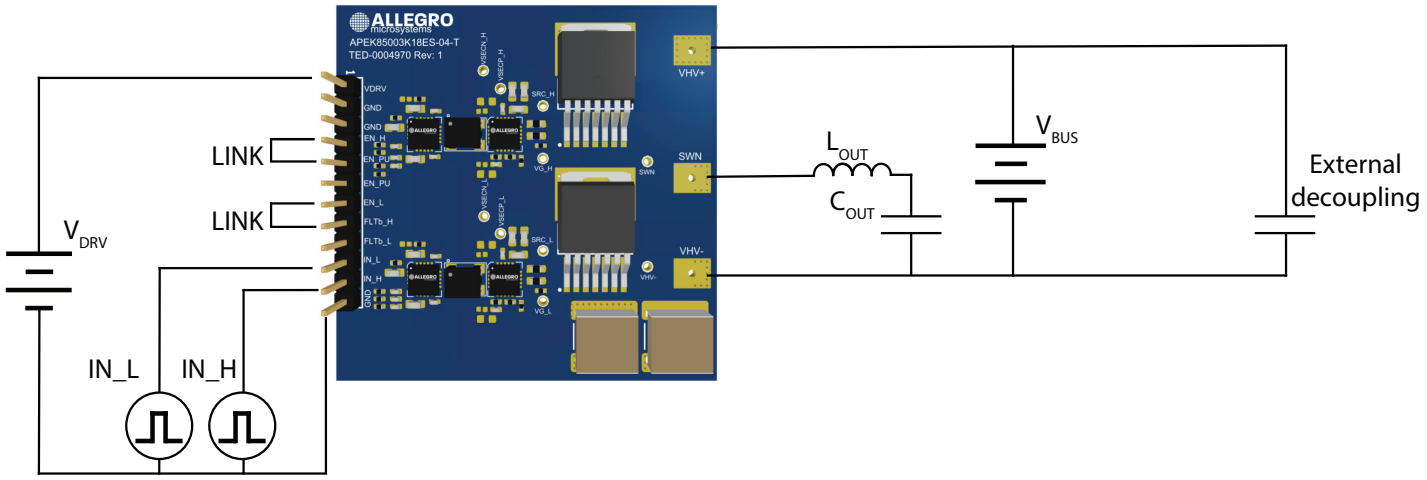

Figure 2: APEK85003K18ES-04-MH Quick Start Diagram

1. Apply V_{DRV} = 12 V.
2. Link pins EN_PU to EN_H, and EN_PU to EN_L (if not using external Enable control).
3. Apply input gate signals, with adequate dead time, to the IN_L and IN_H inputs.
4. Convenient test points are located on the test board as shown in Figure 4 below. A suitable differential oscilloscope should be used to monitor the high side gate signal from V_{G_H} to SRC_H.

Gate Pull-up and Pull-down Resistors

The AHV85043 secondary side gate driver has independent output pins for the gate pull up and gate pull down allowing control of the turn-on and turn-off rise and fall times.

The default values for these resistors are:

OUTPU: R15_H and R15_L = 10 Ω

OUTPD: R16_H and R16_L = 2.2 Ω

The user can modify these values to suit their application.

Thermal Management

The APEK85003K18ES-04-MH is supplied without a heatsink. As such, do not use the board at continuous operation at high power levels.

Add a heatsink to the underside of the PCB to operate the evaluation board in continuous mode or at elevated power levels. The operating temperature of the AHV85003/043 driver and the SiC FETs must be maintained below their maximum temperatures.

When adding a heatsink it must be noted that the heat sink may span the primary to secondary isolation boundary and also high voltage PCB traces on the secondary side. As such it is critical to use a suitable thermal interface material between the heatsink and the PCB.

Exercise caution when probing the test points to ensure the integrity of the thermal interface material is not compromised.

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Start Sequence

When the primary supply voltage VDRV is applied, the primary side of the driver remains in low power mode until VDRV exceeds theUVLO threshold. Once the UVLO threshold is exceeded, the internal LDOs and regulators are enabled. If the EN input is held low, the primary side stays in a low power standby mode, with the FAULT output held low. Once EN goes high, or if EN is already high when VDRV UVLO is released, then the primary side of driver enables power transfer to the secondary, to charge the secondary-side isolated bias rails. When the secondary-side bias rails have settled to the target regulation levels, and if no faults are detected on either the primary side or the secondary side, then the open-drain FAULT pin is allowed to go high, via the required external pull-up resistor. This indicates to the system controller that the driver is ready to accept PWM input. Any PWM inputs at the IN+/IN– pins are ignored until the internal FAULT pull-down is released.

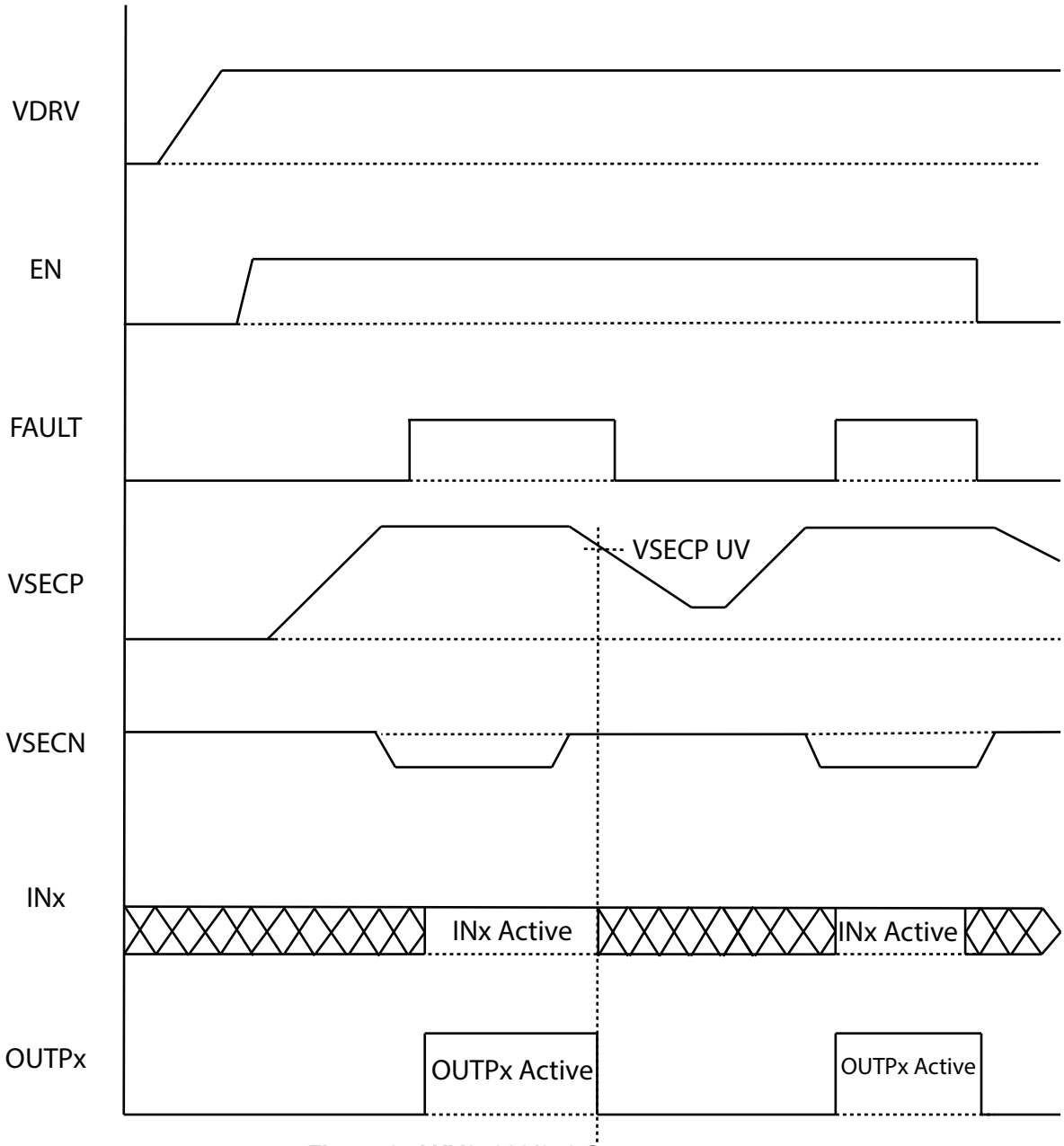

Figure 3: AHV85003/043 Start up sequence

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Measurement Points

The APEK85003K18ES-04-MH evaluation board contains convenient test points for monitoring the high and low side gate drives as well as the switch node as shown in Figure 4 below.

When measuring V_{GS_H} use a differential probe with suitable ratings for the applied bus voltage. The AHV85003/043 SiC FET drivers have a bipolar output. When measuring V_{GS}, both gate drives are measured relative to the source of their associated SiC FET. Therefore, the off-state voltage is negative.

It is important to use a low inductance scope probe ground lead as shown to avoid pickup of spurious switching noise.

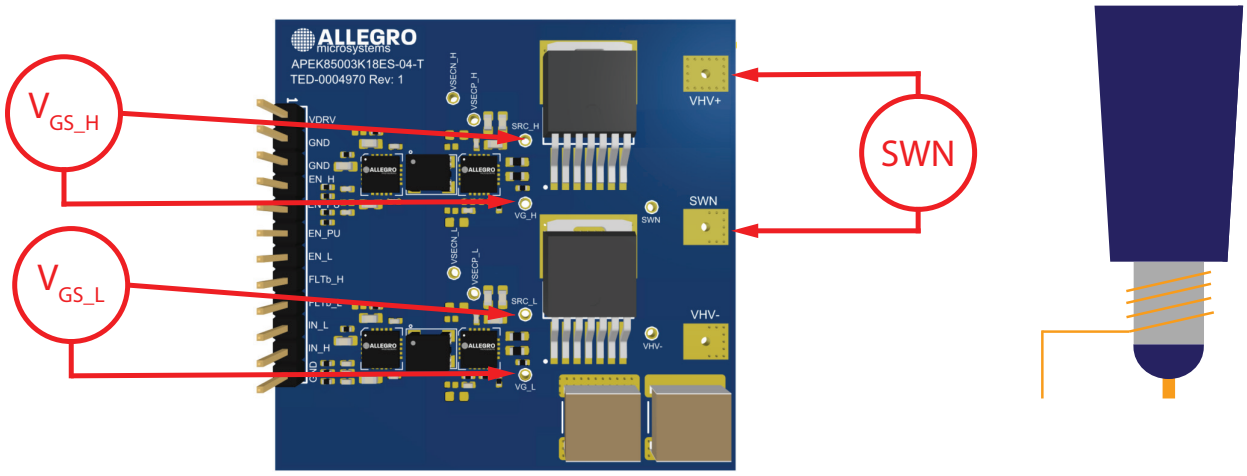

Figure 4: Measurement points

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EVALUATION BOARD PERFORMANCE DATA

Typical Driver Output

The typical measurements of propagation delay are as follows: V_{DRV} = 12 V, Input = 100 kHz, R_{PU} = 10 Ω, R_{PD} = 2.2 Ω and VHV+ = 0 V. That is, power train is unloaded. Typical driver output at 100 kHz is shown in figure 5.

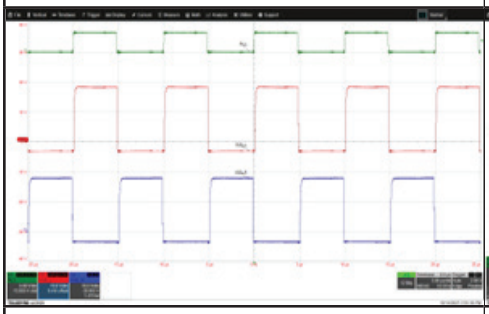
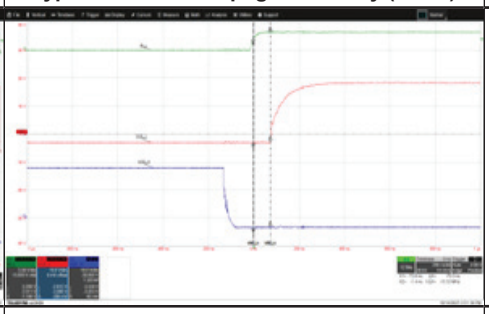
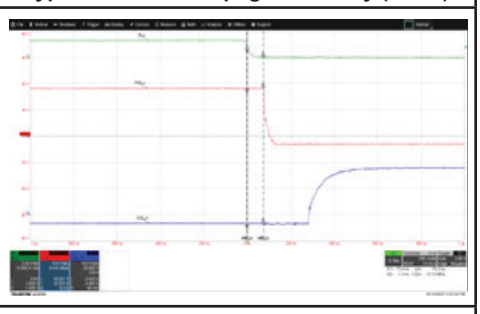
Overview	Typical Turn-on Propagation Delay (75 ns)	Typical Turn-off Propagation Delay (75 ns)
		
CH1 (Green): Driver Input **CH2 (Red):** Low side VGS **CH5 (Blue):** High side VGS	**CH1 (Green):** Driver Input **CH2 (Red):** Low side VGS **CH5 (Blue):** High side VGS	**CH1 (Green):** Driver Input **CH2 (Red):** Low side VGS **CH5 (Blue):** High side VGS

Figure 5: Typical Driver Output at 100 kHz

Double Pulse Test

The double pulse test is used to evaluate the switching characteristics of a power switch under hard switching but in a safe manner.

For a low side switch the setup is as shown below:

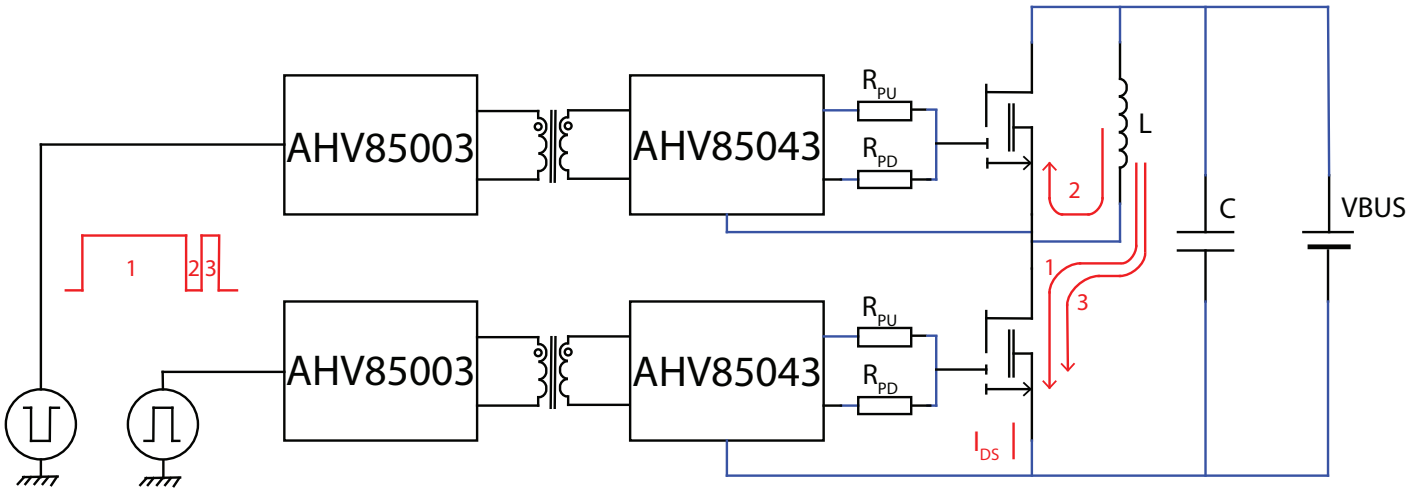


Figure 6: Double Pulse test

The low side switch is driven with two pulses as shown below. The high side switch can be held off or driven with the inverse of the low side gate switch (with adequate dead time).

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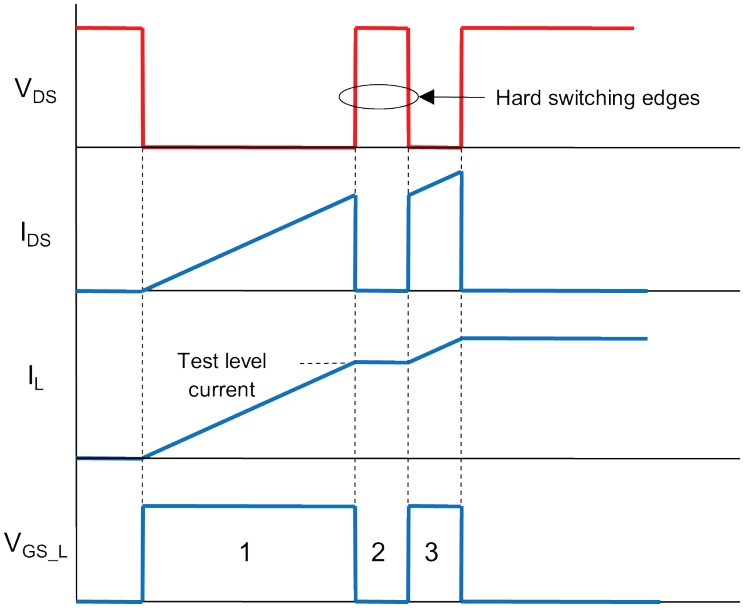

Figure 7: Double Pulse Test Waveforms

An inductor is placed in parallel with the high side switch. The goal of this inductor is to establish the test level current in the low side switch at the end of the first on pulse (1). The magnitude of the test level current at the end of period 1 is given by:

$$I_L = \frac{V_{BUS} T_{ON\_1}}{L}$$

During period 2, the inductor current naturally decays. Ensure the duration of period 2 is not too long such that inductor current deviates significantly from the desired test level.

During period 3, the inductor current rises again. Ensure the duration of period 3 is not so long that the inductor current rises to an excessive level.

The falling edge of pulse 1 is used to examine the hard turn off characteristics of the switch. The rising edge of pulse 3 is used to examine the hard turn on characteristics of the switch. By only applying these two pulses, the switches are only on for a very short time and should not overheat.

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Double Pulse Test Results

DPT Result 200 V–15 A (Rpu = 10 Ω, Rpd = 2.2 Ω)

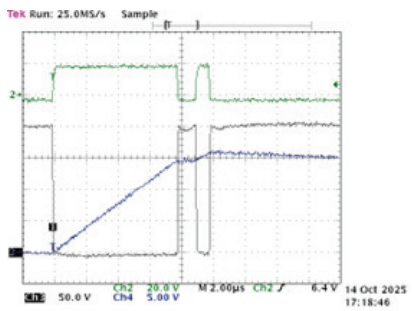
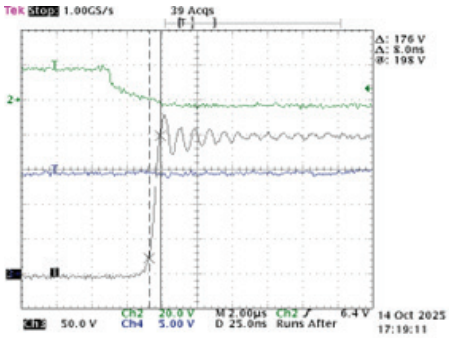
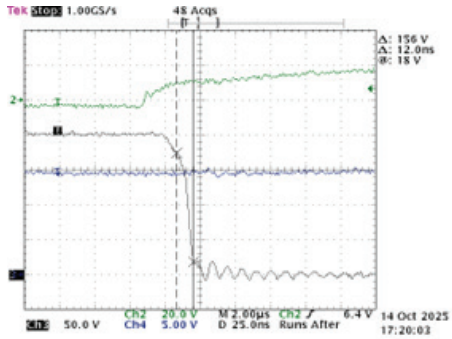
DPT Overview	DPT Hard switching turn-off	DPT Hard switching turn-on
		
CH1(Red): Low side V_{GS} CH3(Black): Switch Node CH4(Blue): Inductor Current (5 A/Div)	CH1(Red): Low side V_{GS} CH3(Black): Switch Node CH4(Blue): Inductor Current (5 A/Div)	CH1(Red): Low side V_{GS} CH3(Black): Switch Node CH4(Blue): Inductor Current (5 A/Div)

Figure 8: 200 V–15 A

DPT Result 400 V–30 A (Rpu = 10 Ω, Rpd = 2.2 Ω)

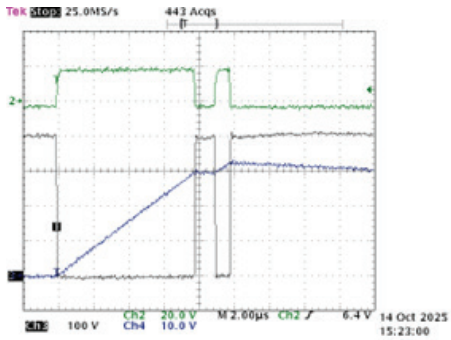
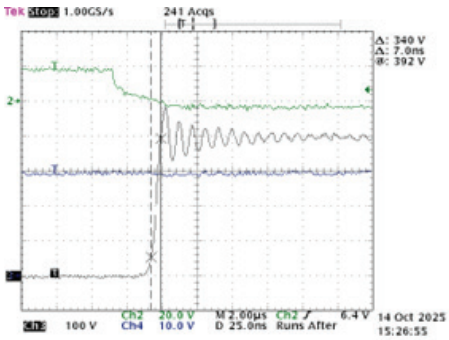
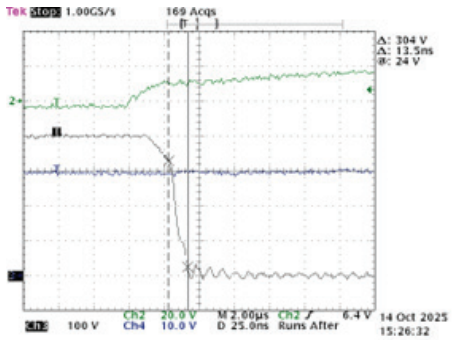
DPT Overview	DPT Hard switching turn off, T_{RISE} = 7 ns	DPT Hard switching turn on, T_{FALL} = 13.5 ns
		
CH1(Red): Low side V_{GS} **CH3(Black):** Switch Node **CH4(Blue):** Inductor Current (10 A/Div)	**CH1(Red):** Low side V_{GS} **CH3(Black):** Switch Node **CH4(Blue):** Inductor Current (10 A/Div)	**CH1(Red):** Low side V_{GS} **CH3(Black):** Switch Node **CH4(Blue):** Inductor Current (10 A/Div)

Figure 9: 400 V–30 A

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SCHEMATIC

The APEK85003K18ES-04-MH evaluation board schematic is shown in figure 10.

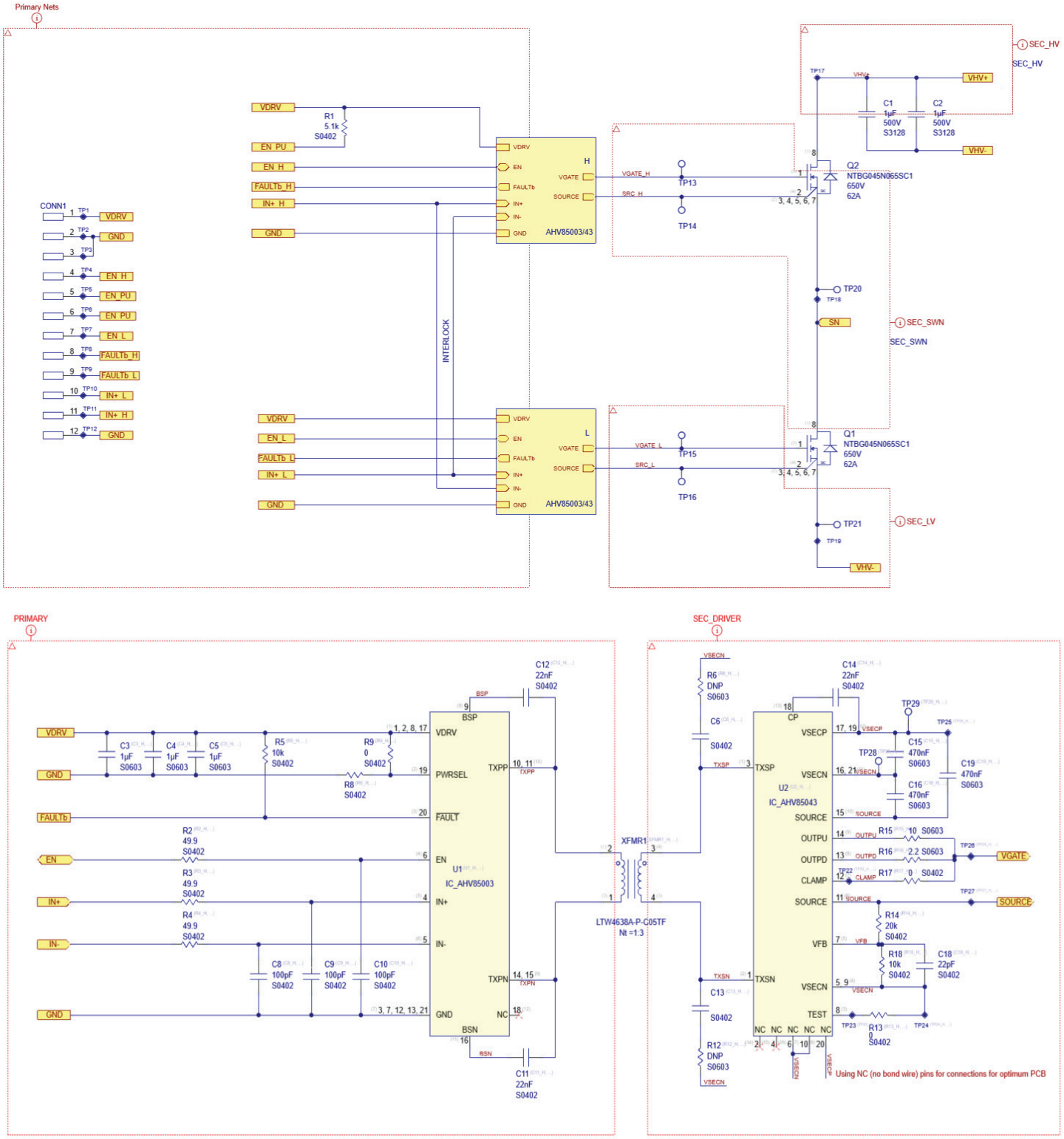

Figure 10: APEK85003K18ES-04-MH Schematic

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LAYOUT

The evaluation board layout is shown in figure 11 and figure 12.

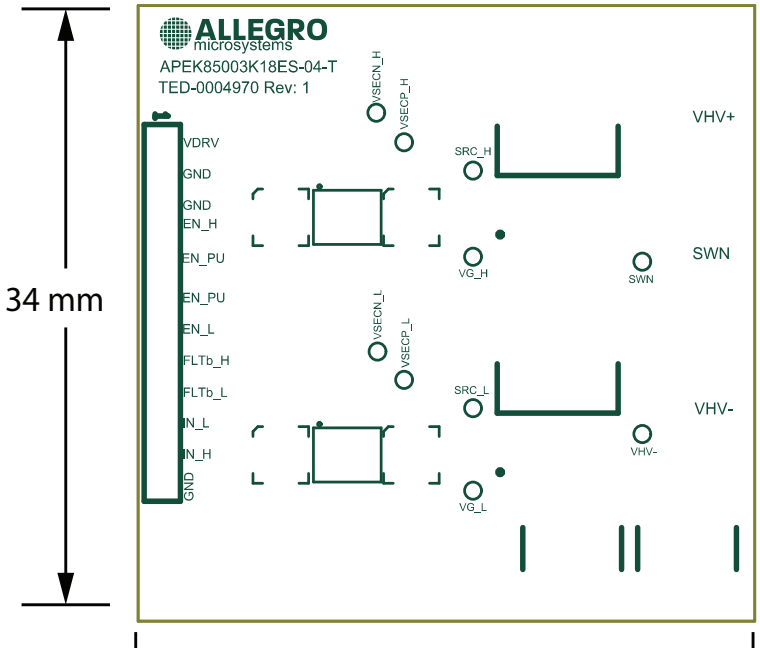

Figure 11: APEK85003K18ES-04-MH Top Overlay

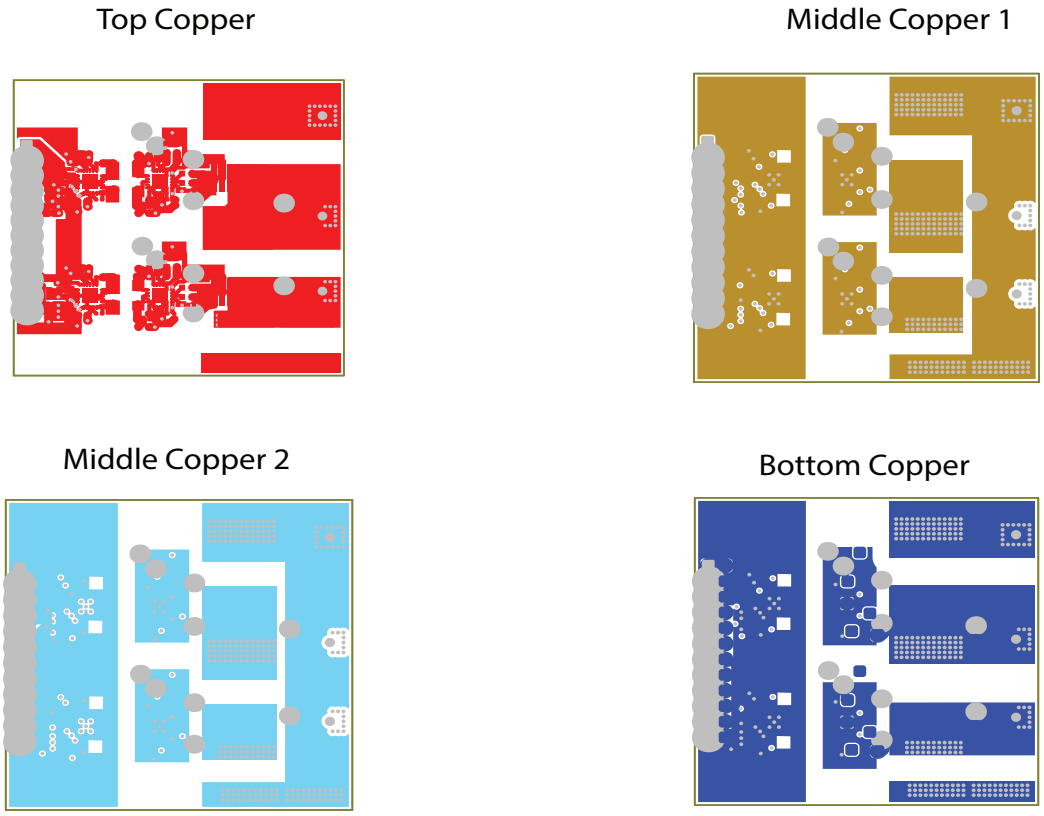

Figure 12: APEK85003K18ES-04-MH PCB Copper Layers

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BILL OF MATERIALS

The APEK85003K18ES-04-MH Evaluation Board Bill of Materials is shown in table 1.

Table 1: APEK85003K18ES-04-MH Evaluation Board Bill of Materials

ELECTRICAL COMPONENTS					
Designator	**Quantity**	**Description**	**Manufacturer**	**Manufacturer Part Number**	**Value**
C1, C2	2	CAP, CERALINK, 1 µF, 500 V	EPCOS	B58031U5105M062	1 µF
C3_H, C3_L, C4_H, C4_L, C5_H, C5_L	6	CAP, CER, 1 µF, 25 V, X7R, 0603	TDK	CGA3E1X7R1E105M080AC	1 µF
C6_H, C6_L, C13_H, C13_L	0	CAP, CER, 100 pF, 50 V, COG/NPO, 0402	Murata	GCM1555C1H101JA16D	100 pF
C8_H, C8_L, C9_H, C9_L, C10_H, C10_L	6	CAP, CER, 100 pF, 50 V, COG/NPO, 0402	Murata	GCM1555C1H101JA16D	100 pF
C11_H, C11_L, C12_H, C12_L, C14_H, C14_L	6	CAP, CER, 22 nF, 50 V, COG/NPO, 0402	Yageo	CC0402KRX7R9BB223	22 nF
C15_H, C15_L, C16_H, C16_L, C19_H, C19_L	6	CAP, CER. 470 nF, 50 V, X7R, 0603	TDK	C1608X7R1H474K080AC	470 nF
C18_H, C18_L	2	CAP, CER, 22 pF, 50 V, C0G, 0402	TDK	CGA2B2C0G1H220J050BA	22 pF
Q1, Q2	2	SiC FET, 650 V, 62 A, 31 mΩ, 105 nC, D2PAK-7L	OnSemi	NTBG045N065SC1	–
R1	1	RES, 5.1k, 0.063 W, 1%, 0402	TE Connectivity	CRG0402F5K1	5.1k
R2_H, R2_L, R3_H, R3_L, R4_H, R4_L	6	RES, 49.9 R, 0.063 W, 1%, 0402	Vishay	CRCW040249R9FKED	49.9
R5_H, R5_L, R18_H, R18_L	4	RES, 10k, 0.10 W, 1%, 0402	Panasonic	ERJ-2RKF1002X	10k
R6_H, R6_L, R8_H, R8_L, R12_H, R12_L	0	RES, 0603, Not Assembled, RES, 0402, Not Assembled	–	–	–
R9_H, R9_L, R13_H, R13_L, R17_H, R17_L	6	RES, 0 R, 0.063 W, 1%, 0402	Bourns	CR0402-J/-000GLF	0
R14_H, R14_L	2	RES, 20k, 63 mW, 1%, 0402	Panasonic	ERJ-2RKF2002X	20k
R15_H, R15_L	2	RES, 10 R, 0.63 W, 1%, Anti Surge	Bourns	CMP0603AFX-10R0ELF	10
R16_H, R16_L	2	RES, 2.2 R, 0603, 0.25 W,1%, Anti Surge	Rohm	ESR03EZPF2R20	2.2
U1_H, U1_L	1	AHV85003 Primary IC, QFN-20 4×4×0.8, 18 V	Allegro MicroSystems	AHV85003K18ESTR	AHV85003
U2_H, U2_L	1	AHV85043 Secondary IC, QFN-20 4×4×0.8, 18 V	Allegro MicroSystems	AHV85043K18ESTR	AHV85043
XMFR1_H, XMFR1_L	2	XFMR, AHV85003, 1:3, LTW4638A-P-C05TF. Func Isolation	SUNLORD	LTW4638A-P-C05TF	–
OTHER COMPONENTS					
Designator	**Quantity**	**Description**	**Manufacturer**	**Manufacturer Part Number**	**Value**
CONN1	1	Pin Header, Board-to-Board, 2.54 mm, 1 Rows, 12 Contacts, PTH	Multicomp	MC34733	Connector 12 Way
CONN2, CONN3	1	CONN, 2-WAY, SHUNT JUMPER, 2.54 mm	Multicomp	MC-2228DG	2-pin Shunt
PCB1	1	PCB from gerber files	Allegro MicroSystems	Gerbers TED-0004970 Rev: 1	–

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Revision History

Number	Date	Description
–	December 17, 2025	Initial release

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