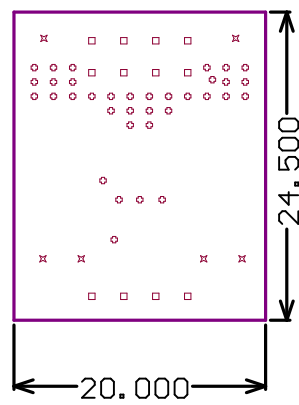


Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	TopOverlay				
2	TopSolder	Solder Resist	0.40mil	3.5	
3	TopLayer	Copper	2.80mil		
4	Dielectric1	FR-4	55.60mil	4	
5	BottomLayer	Copper	2.80mil		
6	BottomSolder	Solder Resist	0.40mil	3.5	
7	BottomOverlay				

Symbol	Count	Hole Size	Plated	Hole Type	Via/Pad
⊗	35	15.00mil (0.381mm)	PTH	Round	Via
⊗	6	36.00mil (0.914mm)	PTH	Round	Pad
□	12	40.00mil (1.016mm)	PTH	Round	Pad
	53 Total				



# FAB Drawing / FAB Notes and Requirements

Rev 1  
5/5/2017

- Finished PCB is RoHS
- Dimensions are in millimeters, unless otherwise noted.
- Applicable Standards:
  - Manufacture in accordance to IPC-6011, IPC-6012 for Class 2 applications.
  - PCB shall meet acceptance criteria as required for Class 2 PCB as defined in IPC-600
  - UL Approved to a minimum catagory of 94V0.
- Laminate:
  - Thickness: 0.062inch +/- 10%
  - Type: high temp FR4
  - this line left blank
  - Core/prepreg thickness:
    - See chart to left.
    - Core/prepreg thicknesses to be roughly uniform thickness or +/-5mil from indicated
    - No impedance controlled stackup required
- Copper:
  - Layer Count: 2
  - Exterior layers: 2oz min
  - Interior layers: N/A
  - Plated through holes: plate to 1mil min copper thickness
  - Trace separation: 5mil
  - Trace min width: 8mil
  - Line width reduction due to pinholes nicks or shrinking: 20% max.
  - No impedance controlled route used; no trace width adjustment required.
- this line left blank
- Total board flatness shall not exceed 0.002inch per inch.
- Artwork layer registration shall be within 0.003inch total.
- Surface Finish:
  - Immersion Gold
  - No hard gold required, no \*.gm8 nor \*.gm9 layer provided
- Soldermask:
  - Top/Bottom soldermask required
  - Soldermask color shall be green.
  - Soldermask finish may be matte or glossy.
- Silkscreen
  - Top/bottom silkscreen required.
  - Silkscreen color shall be white.
  - Min silkscreen line width: 4mil
  - Epoxy or acrylic ink allowed
  - Photoimaging or inkject printing shall be used
  - Allegro Logo shall be printed as accurately as possible.
  - 11f1. Silkscreen imperfections in other regions allowed. Do not hold job for minor blemishes elsewhere.
- Drill holes:
  - No blind or buried vias.
  - Hole sizes are specified after plating.
  - No via in pad used. No via filling required.
- Mill separate according to mech1 (\*.gm1) layer.
- Electrical testing required.
- Contact information:
  - Matt Siopes, msiopes@allegromicro.com, 603.626.2610
  - If fast turn board, 24hr contact info: N/A

