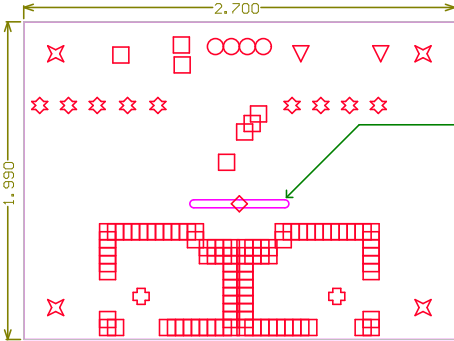


TED-0002170-FAB
Originator: S. Upton

| Layer | Name | Material | Thickness | Constant | Board Layer Stack |
|-------|---------------|---------------|-----------|----------|-------------------|
| 1 | TopPaste | | | | / / / / / |
| 2 | TopOverlay | | | | |
| 3 | TopSolder | Solder Resist | 0.40mil | 3.5 | / / / / / |
| 4 | TopLayer | Copper | 2.80mil | | |
| 5 | Dielectric1 | FR-4 | 56.00mil | 4 | / / / / / |
| 6 | BottomLayer | Copper | 2.80mil | | |
| 7 | BottomSolder | Solder Resist | 0.40mil | 3.5 | / / / / / |
| 8 | BottomOverlay | | | | |
| 9 | BottomPaste | | | | / / / / / |

| Symbol | Hit Count | Finished Hole Size | Plated | Hole Type |
|--------|-----------|---------------------|--------|-----------|
| ◇ | 1 | 50.00mil (1.270mm) | NPTH | Slot |
| ▽ | 2 | 56.00mil (1.422mm) | PTH | Round |
| ○ | 2 | 266.00mil (6.756mm) | PTH | Round |
| ◊ | 4 | 42.00mil (1.067mm) | PTH | Round |
| × | 4 | 125.00mil (3.175mm) | PTH | Round |
| ☆ | 9 | 62.00mil (1.575mm) | PTH | Round |
| □ | 99 | 15.00mil (0.381mm) | PTH | Round |
| | 121 Total | | | |

Mechanical Layer 1 *.gm1 is Board Outline, slots and circular cutouts
Mechanical Layer 2 *.gm2 is footprint notes (not for fab house)
Mechanical Layer 3 *.gm3 is hole location guide
Mechanical Layer 4 *.gm4 is board outline dimensions
Mechanical Layer 5 *.gm5 is topside labels (if no silk)
Mechanical Layer 6 *.gm6 is bottomside labels (if no silk)
Mechanical Layer 7 *.gm7 is FAB drawing notes
Mechanical Layer 8 *.gm8 is top selective hard gold
Mechanical Layer 9 *.gm9 is bottom selective hard gold
Mechanical Layer 10 and up are not for usage by PCB board house
*.gto and *.gbo are top and bottom layer silkscreen (aka overlay)
*.gts and *.gbs are top and bottom soldermask
*.drl is NC Drill
*.apr is aperture file
*.gpb and *.gpt are pad master layers, and are not used (ignore if in zip file)
Keepout layer *.gko is for internal usage only, and is not to be used by board house



FAB Drawing / FAB Notes and Requirements

Rev 3
5/29/2018

- Finished PCB is RoHS
- Dimensions are in inches, unless otherwise noted.
- Applicable Standards:
 - Manufacture in accordance to IPC-6011, IPC-6012 for Class 2 applications.
 - PCB shall meet acceptance criteria as required for Class 2 PCB as defined in IPC-600
 - UL Approved to a minimum catagory of 94V0.
- Laminate:
 - Thickness: 0.062inch +/- 10%
 - Type: high temp FR4
 - this line left blank
 - Core/prepreg thickness:
 - See chart to left.
 - Core/prepreg thicknesses to be roughly uniform thickness or +/-5mil from indicated
 - No impedance controlled stackup required
- Copper:
 - Layer Count: 2
 - Exterior layers: 2oz min
 - Interior layers: N/A
 - Plated through holes: plate to 1mil min copper thickness
 - Trace separation: 10mil
 - Trace min width: 10mil
 - Line width reduction due to pinholes nicks or shrinking: 20% max.
 - No impedance controlled route used; no trace width adjustment required.
- this line left blank
- Total board flatness shall not exceed 0.002inch per inch.
- Artwork layer registration shall be within 0.003inch total.
- Surface Finish:
 - Immersion Gold
 - No hard gold required, no *.gm8 nor *.gm9 layer provided
- Soldermask:
 - Top/Bottom soldermask required
 - Soldermask color shall be green.
 - Soldermask finish may be matte or glossy.
- Silkscreen:
 - Top/bottom silkscreen required.
 - Silkscreen color shall be white.
 - Min silkscreen line width: 4mil
 - Epoxy or acrylic ink allowed
 - Photoimaging or inkjet printing shall be used
 - Allegro Logo shall be printed as accurately as possible.
 - Silkscreen imperfections in other regions allowed. Do not hold job for minor blemishes elsewhere.
- Drill holes:
 - No blind or buried vias.
 - Hole sizes are specified after plating.
 - No via in pad used. No via filling required.
- Mill separate according to mech1 (*.gm1) layer.
- Electrical testing required.
- Contact information:
 - Shawn Upton supton@allegromicro.com, 603.626.2429
 - If fast turn board, 24hr contact info: N/A

