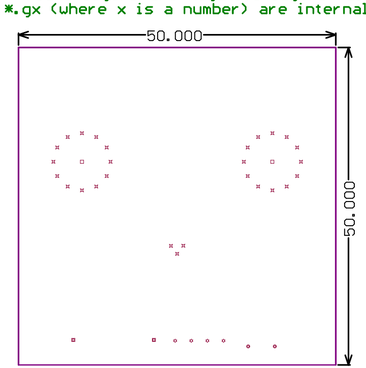
ASEK37612, EVB, 4.5mm
TED-0003004-FAB
Originator: S. Upton
Rev 2
10/25/2019

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	TopOverlay				
2	TopSolder	Solder Resist	0.40mil	3.5	
3	TopLayer	Copper	1.40mil		
4	Dielectric1	FR-4	10.00mil	4	
5	Signal Layer 1	Copper	2.80mil		
6	Dielectric 3		8.00mil	4.2	
7	Signal Layer 2	Copper	2.80mil		
8	Dielectric 4		10.00mil	4.2	
9	Signal Layer 3	Copper	2.80mil		
10	Dielectric 5		8.00mil	4.2	
11	Signal Layer 4	Copper	2.80mil		
12	Dielectric 2		10.00mil	4.2	
13	BottomLayer	Copper	2.80mil		
14	BottomSolder	Solder Resist	0.40mil	3.5	
15	BottomOverlay				

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad
⌘	27	15.00mil (0.381mm)	PTH	Round	TopLayer - BottomLayer	(Mixed)
✡	4	42.00mil (1.067mm)	PTH	Round	TopLayer - BottomLayer	Pad
▣	2	56.00mil (1.422mm)	PTH	Round	TopLayer - BottomLayer	Pad
◎	2	62.00mil (1.575mm)	PTH	Round	TopLayer - BottomLayer	Pad
□	2	266.00mil (6.756mm)	PTH	Round	TopLayer - BottomLayer	Pad
	37 Total					

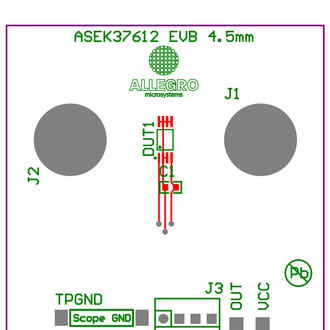
Layers not for PCB fabrication (ignore if present in zip file)
- Mechanical Layer 2 *.gm2 is footprint notes (not for fab house)
- Mechanical Layer 3 *.gm3 is hole location guide
- Mechanical Layer 5 *.gm5 is topside labels (if no silk)
- Mechanical Layer 6 *.gm6 is bottomside labels (if no silk)
- Mechanical Layer 13 *.gm13 is 3D Bodies
- Mechanical Layer 15 *.gm15 is Component Courtyard
- Mechanical Layer 16 *.gm16 is Topside height restrictions
- Mechanical Layer 17 *.gm17 is Bottomside height restrictions
- Keepout layer *.gko is for internal usage only, and is not to be used by board house
- *.gpb and *.gpt are pad master layers, and are not used (ignore if in zip file)

Layers for PCB fabrication:
- Mechanical Layer 1 *.gm1 is Board Outline, slots and circular cutouts
- Mechanical Layer 4 *.gm4 is board outline dimensions
- Mechanical Layer 7 *.gm7 is FAB drawing notes
- Mechanical Layer 8 *.gm8 is top selective hard gold
- Mechanical Layer 9 *.gm9 is bottom selective hard gold
- Mechanical Layer 20 *.gm20 is top layer shorting traces
- Mechanical Layer 21 *.gm21 is bottom layer shorting traces
  Mech layer 20 and 21 already combined with top and bottom, but provided to show where deliberate shorts exist between different nets.
- *.gtl and *.gbl are top and bottom layers
- *.gto and *.gbo are top and bottom layer silkscreen (aka overlay)
- *.gts and *.gbs are top and bottom soldermask
- *.drl is NC Drill
- *.apr is aperature file
- *.gpx (where x is a number) are plane layers. Refer to stackup table for location
  Plane layers are negative layers (all other layers positive)
- *.gx (where x is a number) are internal layers. Refer to stackup table for location



FAB Drawing / FAB Notes and Requirements

1. Finished PCB is RoHS
2. Dimensions are in millimeters, unless otherwise noted.
3. Applicable Standards:
   - 3a. Manufacture in accordance to IPC-6011, IPC-6012 for Class 2 applications.
   - 3b. PCB shall meet acceptance criteria as required for Class 2 PCB as defined in IPC-600
   - 3c. UL Approved to a minimum catagory of 94V0.
4. Laminate:
   - 4a. Thickness: 0.062inch +/- 10%
   - 4b. Type: high temp FR4
   - 4c. This line left blank
   - 4d. Core/prepreg thickness:
     - 4d.1. See chart to left.
     - 4d.2. Core/prepreg thicknesses to be roughly uniform thickness or +/-5mil from indicated
     - 4d.3. No impedance controlled stackup required
     - 4d.4. Top layer be any thickness from 0.5oz to 2oz as vendor thinks best
5. Copper:
   - 5a. Layer Count: 6
   - 5b. Finish copper to thickness indicated in stackup table.
   - 5c. Top layer may be 1oz or 2oz as vendor best sees fit
   - 5d. Plated through holes: plate to 1mil min copper thickness
   - 5e. Trace separation: 10mil
   - 5f. Trace min width: 10mil
   - 5g. Line width reduction due to pinholes nicks or shrinking: 20% max.
   - 5h. No impedance controlled route used; no trace width adjustment required.
6. If PCB has regions where more than 1 square inch of soldermask is removed:
   - 6a. All PCB lands in this region (square and round) are to be 100% pristine.
   - 6b. Lands outside this region may remain at 80% pristine as defined by IPC-6012.
   - 6c. Board flatness in this region shall not exceed 0.001inch total
7. Total board flatness shall not exceed 0.002inch per inch.
8. Artwork layer registration shall be within 0.003inch total.
9. Surface Finish:
   - 9a. Immersion Gold
   - 9b. No hard gold plating required.
10. Soldermask:
    - 10a. Top/Bottom soldermask required
    - 10b. Soldermask color shall be blue
    - 10c. Soldermask finish may be matte or glossy.
    - 10d. Soldermask openings may be modified to remove soldermask slivers. Other alterations require approval.
11. Silkscreen
    - 11a. Top/bottom silkscreen required.
    - 11b. Silkscreen color shall be white.
    - 11c. Min silkscreen line width: 4mil
    - 11d. Epoxy or acrylic ink allowed
    - 11e. Photoimaging or inkject printing shall be used
    - 11f. Allegro Logo shall be printed as accurately as possible.
      - 11f1. Silkscreen imperfections in other regions allowed. Do not hold job for minor blemishes elsewhere.
12. Drill holes:
    - 12a. No blind or buried vias.
    - 12b. Hole sizes are specified after plating.
    - 12c. No via in pad used. No via filling required.
    - 12d. If not stated elsewhere: drill diam tolerance is +/-5mil
    - 12e. If not stated elsewhere: drill registration is +/-3mil
13. Mill separate or v-score according to mech1 (*.gm1) layer.
14. Electrical testing required.
15. Contact information:
    - 15a. Shawn Upton supton@allegromicro.com, 603.626.2429
    - 15b. If fast turn board, 24hr contact info: N/A


ASEK37612 EVB 4.5mm
ALLEGRO
microsystems
J1
J2
DUT1
C1
J3
TPGND
Scope GND
OUT
VCC

TED-0003004 Rev 2
2019-10-25