# A89503 Evaluation Board User Guide

## INTRODUCTION

The A89503 evaluation board is designed to aid system designers with evaluating the operation and performance of the Allegro A89503 48 V safety automotive, half-bridge MOSFET driver. This application note describes the components of the A89503 evaluation board and explains how it can be used to achieve normal operation. To simplify understanding, components of the evaluation board are categorized into different topics.

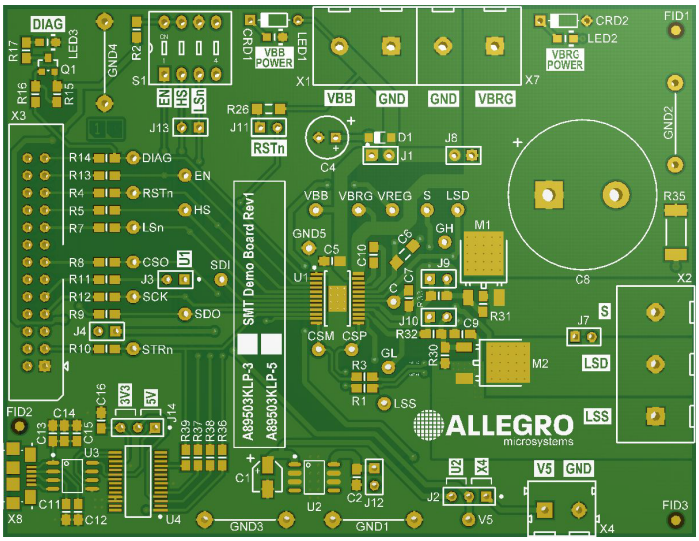


**Figure 1: A89503 Evaluation Board**

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## POWER SUPPLIES

Three power supplies must be available on the board for full operation. These are the VBB, VBRG, and VL power supplies. In each case, there is a ground terminal next to the supply terminal. This ground terminal is connected to the common ground plane.

### VBB Supply

This terminal provides the main power to the A89503. There are two connection options for energizing VBB and VBRG:

1. Common VBB, VBRG: Connect power to X7 and fit J8 (no external power connection to X1).
2. Independent VBB, VBRG: Remove J8 and connect separate power supplies to X1 and X7.

The diode D1 protects the VBB pin from negative transients by ensuring unidirectional current flow. This diode can be bypassed by engaging jumper J1.

### VBRG Supply

The voltage bias on the half bridge is supplied by this terminal. As discussed in the previous section, J8 interconnects VBRG to VBB.

### VL Supply

This supply provides power to the control logic (HS and LSn), the ENABLE pin, and the DIAG status LED (LED3). Because this is a logic supply, its maximum voltage is dependent on the product variant (3.3 V or 5 V).

VL may be generated from VREG via linear regulator U2 (J2 in position U2) or a suitable external supply may be connected via connector X4 (J2 in position X4).

The linear regulator U2 is fitted on both the 5 V and 3.3 V boards. Although this is a 5 V regulator, the A89503 logic inputs are tolerant to this voltage level, will operate correctly, and will not suffer any damage. However, care should be taken to ensure that any 3V3 devices connected to ENABLE, HS, or LS will not suffer damage; therefore, 1 kΩ buffer resistors are placed in series to provide a level of protection to devices connected to X3.

## COMMUNICATION PORTS

Communication to the microcontroller is accomplished via a USB micro-B header or an IDC 26-way ribbon header.

The default method of communication is the USB micro-B connection. This header is connected to an on-board FTDi FT232RL device (U4) that translates the USB signals to serial communication logic. The logic levels can be set to either 3.3 V or 5 V using jumper J14.

To switch from the default method of communication to SPI communication, the R36 through R39 resistors are removed, then the SPI-compatible signals are connected to the X3 header pins 1, 3, 5, 7, 9, and 11.

## SWITCHES

The DIL four-way switch actuator (S1) contains three active switches—S1, S2, and S3. The operation of these switches is described in Table 1.

**Table 1: A89503 Evaluation Board Switch Operation**

| Switch | Control Pin | On State | Off State |
|---|---|---|---|
| S1 | ENABLE | ENABLE connected to VS | ENABLE floating |
| S2 | HS | HS connected to VS | HS Floating |
| S3 | LSn | LSn connected to GND | LSn floating |

Both the ENABLE and HS pins contain an internal pull-down resistor so when they are left floating, they are pulled to logic low. The LSn pin contains an internal pull-up resistor that pulls it to logic high when it is left floating.



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## RESETn

The A89503 contains a RESETn input pin that allows the device to be put into standby mode when it is pulled low. This pin has a voltage rating up to the supply voltage, so it can be directly connected to VBB via R26. This 470 kΩ resistor limits the current flowing into RESETn. The jumper J11 is in series with RESETn. To put the device into sleep mode, jumper J11 is removed. When J11 is removed and left open, the internal pull-down resistor pulls the pin to a logic low level.

To clear latched faults, RESETn can also be pulsed low for the reset pulse width, $t_{RST}$. To achieve this function, J11 is removed and RESETn is connected directly to a logic controller.

## OUTPUT TERMINALS

The half-bridge contains three output terminals; S, LSD, and LSS. These terminals can be connected to various external devices to produce different series-connected and external load configurations. The jumper (J7), found between S and LSD, allows the user to switch between operational configurations.

When J7 is engaged, the A89503 can be used in a complementary half-bridge configuration allowing an external load to be connected. Removal of J7 allows the device to drive independent high-side and low-side MOSFETs for the series-connected load configuration.

Current-carrying loads must be connected to the S and LSD terminals instead of the J7 pins because they have a higher current-carrying capability.

## JUMPERS

The 10 different jumpers of the A89503 evaluation board are used as follows:

- J1 bypasses the VBB protection diode.
- J2 selects the source of the logic supply. This can be either from the on-board regulator (U2) or the external supply (X4).
- J7 connects the source (S) of the high-side MOSFET to the drain (LSD) of the low-side MOSFET. Removal of J7 allows independent control of both MOSFETs.
- J8 connects the VBB and VBRG supplies together.
- J9 short-circuits the gate resistor of the high-side MOSFET to allow it to operate in slew rate control mode. This jumper must be removed from the board when operating with gate drive control disabled.
- J10 short-circuits the gate resistor of the low-side MOSFET to allow it to operate in slew rate control mode. This jumper must be removed from the board when operating with gate drive control disabled.
- J11 pulls RESETn to a high logic level when it is engaged. RESETn is internally pulled to logic low if J11 is removed.
- J12 connects VREG to the supply of the on-board regulator. This jumper must be engaged if VS is being supplied from the regulator.
- J13 is left open in its default state. When this jumper is engaged, it allows complementary control of HS and LSn.
- J14 toggles between 3.3 V and 5 V logic when using the USB micro-B communication port.

## LEDS

The A89503 evaluation board contains three red LEDs. Each LED is used as a different indicator:

- LED1 is connected between VBB and ground through a current source and is used to indicate when the VBB terminal is energized.
- LED2 is connected to VBRG and is used to indicate when the bridge is energized. This LED may be considered as an additional safety feature of the evaluation board because it remains on until the DC link capacitor is discharged.
- LED3 is connected to DIAG, and it turns on when DIAG goes low. This LED, therefore, displays when the A89503 has a fault in the diagnostic register.



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## A89503 EVALUATION BOARD SCHEMATIC

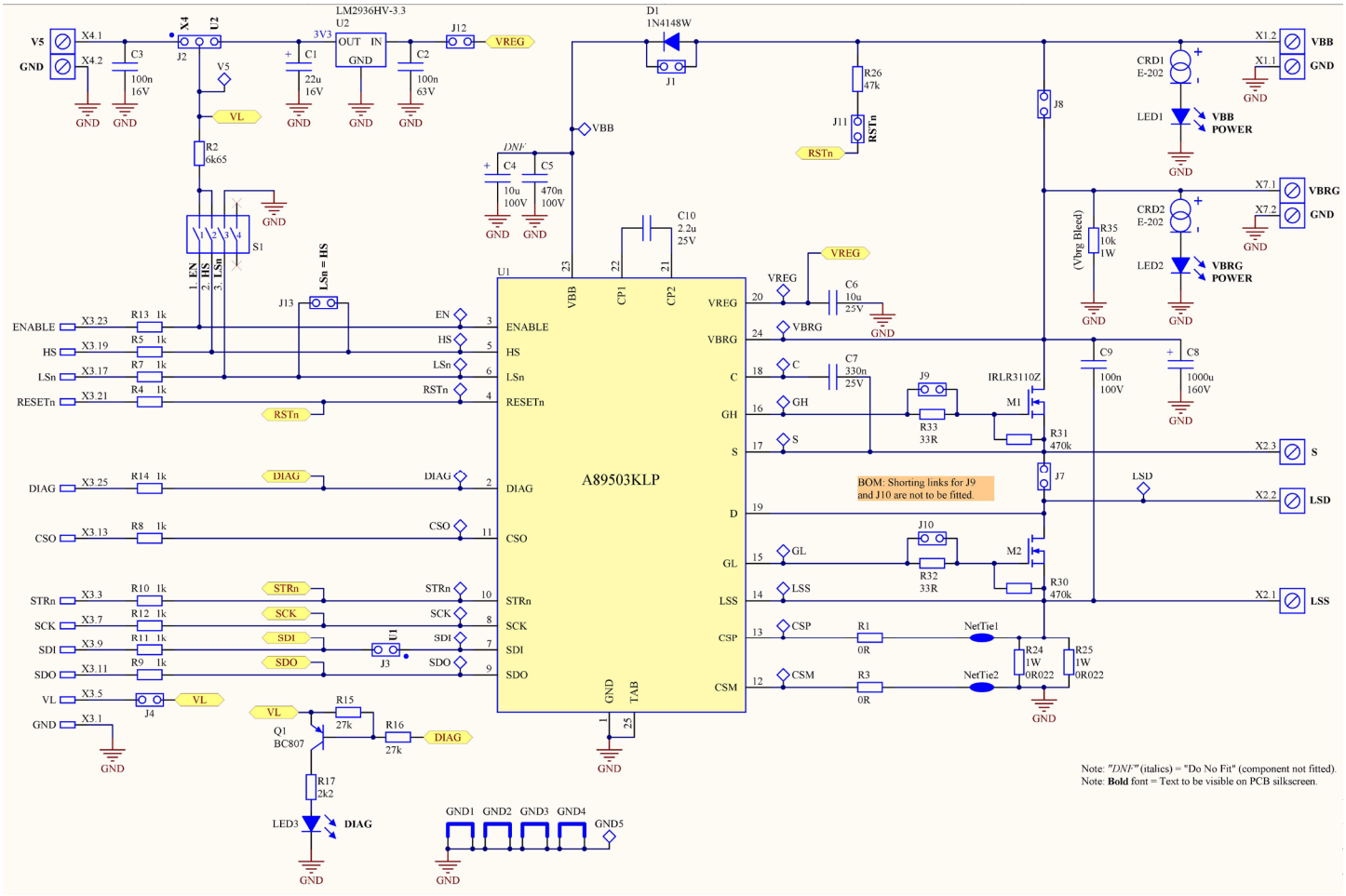


**Figure 2: A89503KLP SMT Evaluation Board Schematic (1 of 2)**



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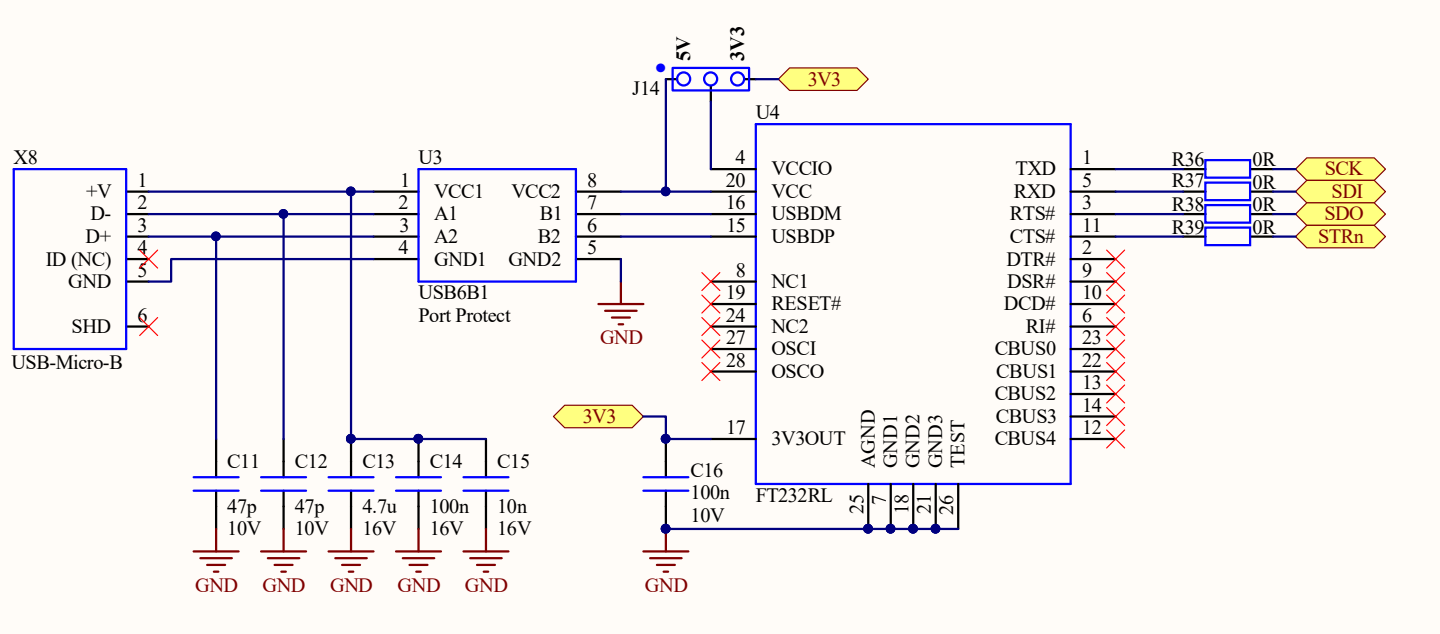


**X3 PINOUT**

| | | | |
|---|---|---|---|
| 26 | | DIAG | 25 |
| 24 | | EN | 23 |
| 22 | | RSTn | 21 |
| 20 | | HS | 19 |
| 18 | | LSn | 17 |
| 16 | | OOS | 15 |
| 14 | | CSO | 13 |
| 12 | | SDO | 11 |
| 10 | | SDI | 9 |
| 8 | | SCK | 7 |
| 5 | | VL | 5 |
| 4 | | STRn | 3 |
| 2 | | GND | 1 |

**Figure 3: A89503KLP SMT Evaluation Board Schematic (2 of 2)**



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## Revision History

| Number | Date | Description |
|---|---|---|
| – | December 9, 2021 | Initial Release |
| 1 | January 4, 2023 | Standardized product naming conventions per new guidelines and made minor editorial and updates (all pages) |





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