AMT49502 Evaluation Board User Guide

DESCRIPTION

The AMT49502 evaluation board is designed to aid system designers with evaluating the operation and performance of the Allegro AMT49502 48 V safety automotive, half-bridge MOSFET driver. This application note describes the components of the AMT49502 evaluation board and explains how it can be used to achieve typical operation. To simplify understanding, components of the evaluation board are categorized into different topics.

FEATURES

- Evaluation of the operation and performance of AMT49502

EVALUATION BOARD CONTENTS

- APEK49502 evaluation board

Table 1:AMT49502 Evaluation Board Configurations

Configuration Name	Part Number
AMT49402 Evaluation Board	APEK49502LP

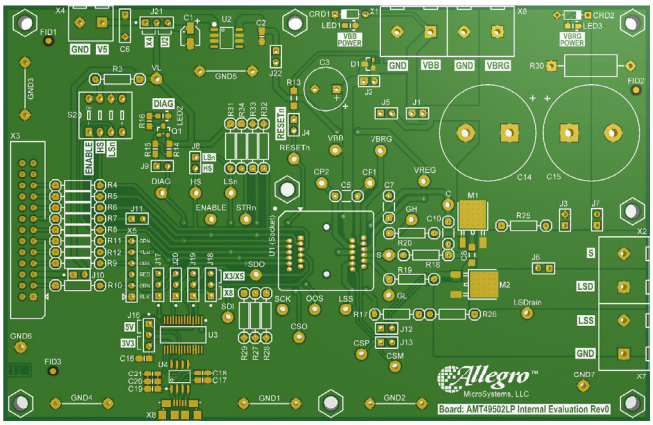

Figure 1: AMT49502LP Evaluation Board

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USING THE EVALUATION BOARD

Power Supplies

Three power supplies must be available on the board for full operation. These are the VBB, VBRG, and VL power supplies. In each case, there is a ground terminal next to the supply terminal. This ground terminal is connected to the common ground plane.

VBB SUPPLY

This terminal provides the main power to the AMT49502. There are two connection options for energizing VBB and VBRG:

1. Common VBB, VBRG: Connect power to X7 and fit J8 (no external power connection to X1).
2. Independent VBB, VBRG: Remove J8 and connect separate power supplies to X1 and X7.

The diode D1 protects the VBB pin from negative transients by ensuring unidirectional current flow. This diode can be bypassed by engaging jumper J1.

VBRG SUPPLY

The voltage bias on the half bridge is supplied by this terminal. As discussed in the previous section, J8 interconnects VBRG to VBB.

VL SUPPLY

This supply provides power to the control logic (HS and LSn), the ENABLE pin, and the DIAG status LED (LED3). Because this is a logic supply, its maximum voltage is dependent on the product variant (3.3 V or 5 V).

VL may be generated from VREG via linear regulator U2 (J2 in position U2) or a suitable external supply may be connected via connector X4 (J2 in position X4).

The linear regulator U2 is fitted on both the 5 V and 3.3 V boards. Although this is a 5 V regulator, the AMT49502 logic inputs are tolerant to this voltage level, will operate correctly, and will not suffer any damage. However, care should be taken to ensure that any 3V3 devices connected to ENABLE, HS, or LS will not suffer damage; therefore, 1 kΩ buffer resistors are placed in series to provide a level of protection to devices connected to X3.

Communication Ports

Communication to the microcontroller is accomplished via a USB micro-B header or an IDC 26-way ribbon header.

The default method of communication is the USB micro-B connection. This header is connected to an on-board FTDi FT232RL device (U4) that translates the USB signals to serial communication logic. The logic levels can be set to either 3.3 V or 5 V using jumper J14.

To switch from the default method of communication to SPI communication, the R36 through R39 resistors are removed, then the SPI-compatible signals are connected to the X3 header pins 1, 3, 5, 7, 9, and 11.

Switches

The DIL four-way switch actuator (S1) contains three active switches—S1, S2, and S3. The operation of these switches is described in Table 2.

Table 2: AMT49502 Evaluation Board Switch Operation

Switch	Control Pin	On State	Off State
S1	ENABLE	ENABLE connected to VS	ENABLE floating
S2	HS	HS connected to VS	HS Floating
S3	LSn	LSn connected to GND	LSn floating

Both the ENABLE and HS pins contain an internal pull-down resistor so when they are left floating, they are pulled to logic low. The LSn pin contains an internal pull-up resistor that pulls it to logic high when it is left floating.

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RESETn

The AMT49502 contains a RESETn input pin that allows the device to be put into standby mode when it is pulled low. This pin has a voltage rating up to the supply voltage, so it can be directly connected to VBB via R26. This 470 kΩ resistor limits the current flowing into RESETn. The jumper J11 is in series with RESETn. To put the device into sleep mode, jumper J11 is removed. When J11 is removed and left open, the internal pull-down resistor pulls the pin to a logic low level.

To clear latched faults, RESETn can also be pulsed low for the reset pulse width, t_{RST}. To achieve this function, J11 is removed and RESETn is connected directly to a logic controller.

Output Terminals

The half-bridge contains three output terminals; S, LSD, and LSS. These terminals can be connected to various external devices to produce different series-connected and external load configurations. The jumper (J7), found between S and LSD, allows the user to switch between operational configurations.

When J7 is engaged, the AMT49502 can be used in a complementary half-bridge configuration allowing an external load to be connected. Removal of J7 allows the device to drive independent high-side and low-side MOSFETs for the series-connected load configuration.

NOTE: In this configuration, the low-side VDS monitor should be disabled by setting the LO bit to 1 in the Mask 1 register. This is necessary as the reference voltage for the drain of the low-side MOSFET is the S terminal, which will be pulled to the supply when the high-side MOSFET is on and will cause a false low-side VDS fault if the low-side VDS monitor is active.

Current-carrying loads must be connected to the S and LSD terminals instead of the J7 pins because they have a higher current-carrying capability.

Jumpers

The 10 different jumpers of the AMT49502 evaluation board are used as follows:

- J1 bypasses the VBB protection diode.
- J2 selects the source of the logic supply. This can be either from the on-board regulator (U2) or the external supply (X4).
- J7 connects the source (S) of the high-side MOSFET to the drain (LSD) of the low-side MOSFET. Removal of J7 allows independent control of both MOSFETs.
- J8 connects the VBB and VBRG supplies together.
- J9 short-circuits the gate resistor of the high-side MOSFET to allow it to operate in slew rate control mode. This jumper must be removed from the board when operating with gate drive control disabled.
- J10 short-circuits the gate resistor of the low-side MOSFET to allow it to operate in slew rate control mode. This jumper must be removed from the board when operating with gate drive control disabled.
- J11 pulls RESETn to a high logic level when it is engaged. RESETn is internally pulled to logic low if J11 is removed.
- J12 connects VREG to the supply of the on-board regulator. This jumper must be engaged if VS is being supplied from the regulator.
- J13 is left open in its default state. When this jumper is engaged, it allows complementary control of HS and LSn.
- J14 toggles between 3.3 V and 5 V logic when using the USB micro-B communication port.

LEDs

The AMT49502 evaluation board contains three red LEDs. Each LED is used as a different indicator:

- LED1 is connected between VBB and ground through a current source and is used to indicate when the VBB terminal is energized.
- LED2 is connected to VBRG and is used to indicate when the bridge is energized. This LED may be considered as an additional safety feature of the evaluation board because it remains on until the DC link capacitor is discharged.
- LED3 is connected to DIAG, and it turns on when DIAG goes low. This LED, therefore, displays when the AMT49502 has a fault in the diagnostic register.

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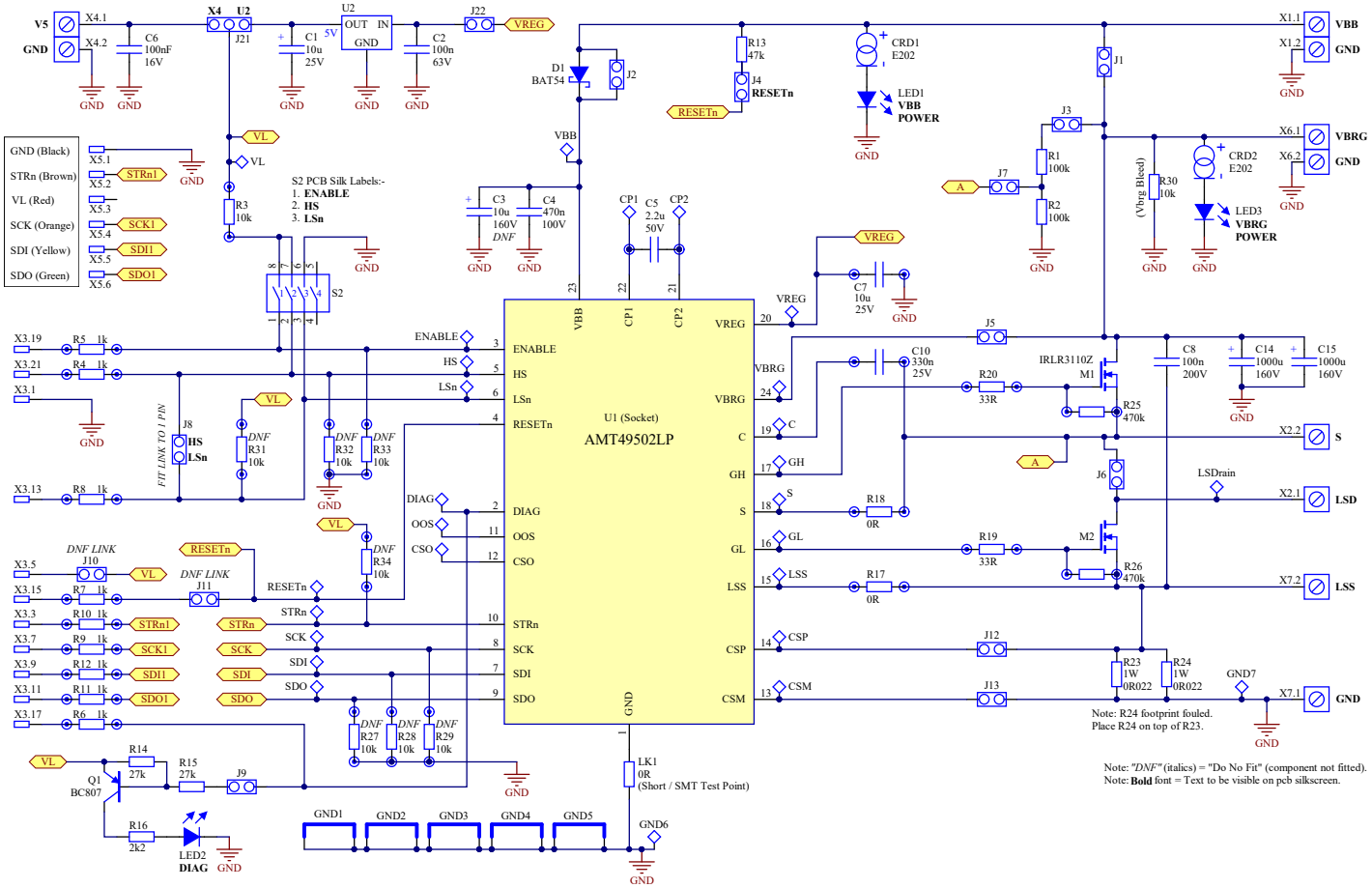
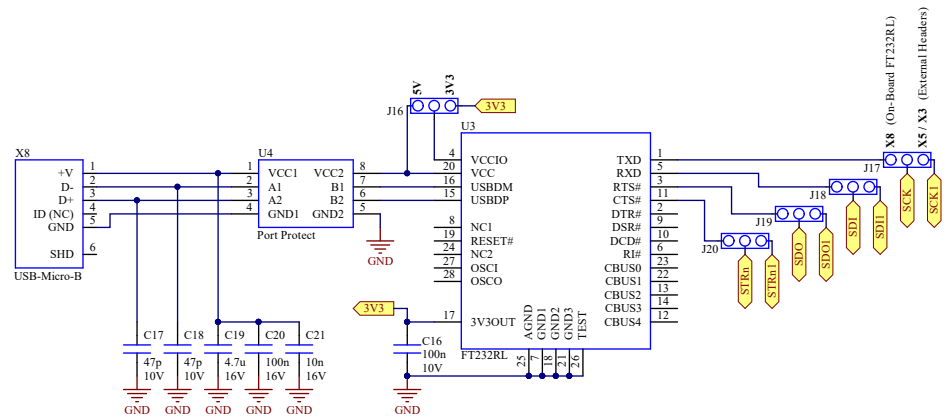
SCHEMATIC





SPI over USB:-

If desired, the FTDi TTL-232R-5V cable can be used instead of the Micro-B-USB connector X10 and on-board FTDi FT232RL device U4.

Move links on J17-J20, then connect the cable 6 pin socket to X5, or X3 header pins 1, 3, 5, 7, 9 & 11 as shown.

X3 pinout:-

26			25
24			23
22		HS	21
20		EN	19
18		DIAG	17
16		RSTn	15
14		LSn	13
12		SDO	11
10		SDI	9
8		SCK	7
6		VL	5
4		STRn	3
2		GND	1

FTDi

Green	
Yellow	
Orange	
Red	
Brown	
Black	

Figure 2: AMT49502LP Evaluation Board Schematic

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LAYOUT

The top and bottom layers of the APEK49502LP evaluation board are shown in Figure 3 and Figure 4.

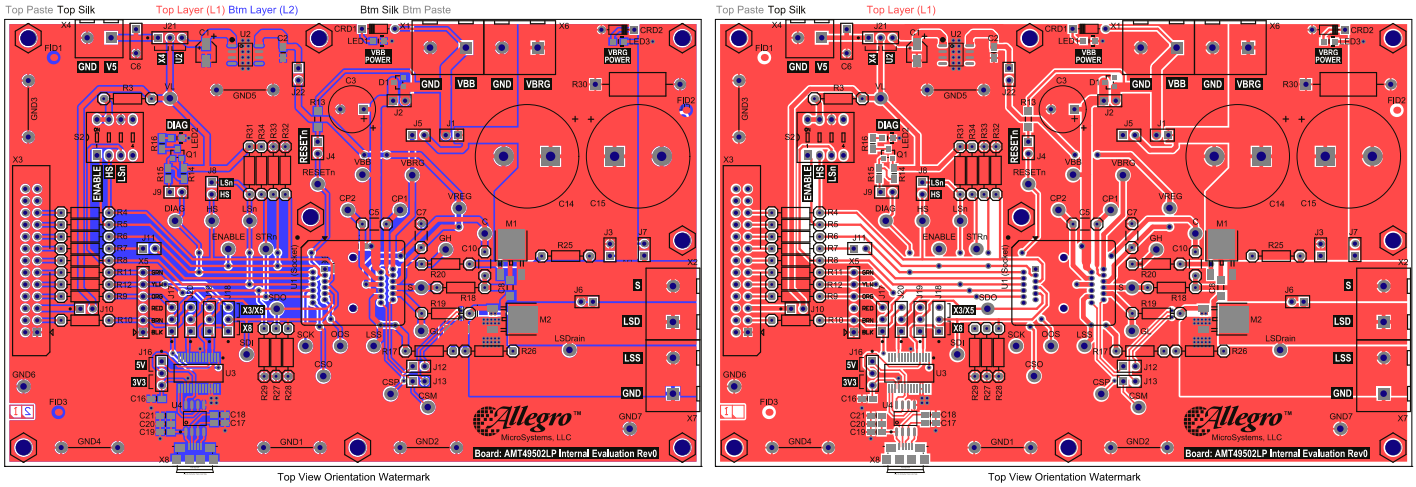

Figure 3: Top Layer

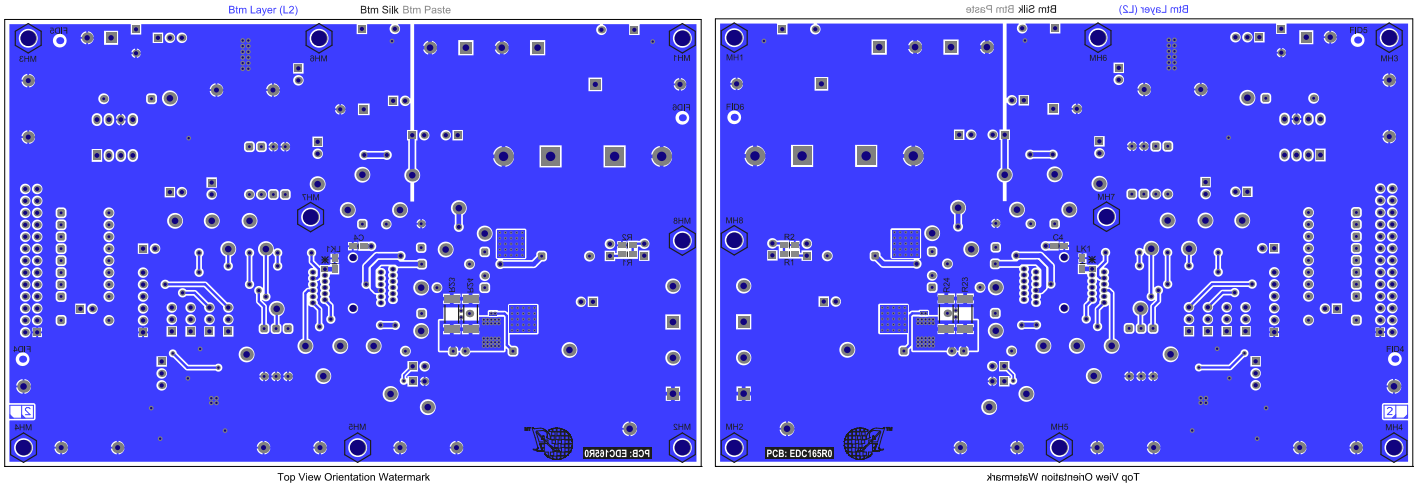

Figure 4: Bottom Layer

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BILL OF MATERIALS

Table 3: Component Function, Specification, and Selection Criteria [1][2][3]

Designator	SIL Skt	Value	Rating	Tol	Part Number	Footprint	Description	DNF	Qty	RS #1 [4]	Farnell #1 [5]
C1	–	10 µF	25 V	20%	EEEFP1E100AR	SM: Case B	Capacitor: Electrolytic SMT	–	1	568-711	1539481
C2	–	100 nF	63 V	X7R	–	SM: 0805	Capacitor: Ceramic chip	–	1	698-3361	1740681
C3	–	10 µF	160 V	20%	–	TH: 5 mm pitch, 10 mm diameter	Capacitor: Electrolytic radial; component not fitted	DNF	0	365-4565	9693181
C4	–	470 nF	100 V	X7R	–	SM: 0805	Capacitor: Ceramic chip	–	1	723-6124	2210999
C5	Skt	2.2 µF	50 V	X7R	–	TH: 5 mm pitch [SKT]	Capacitor: Dipped ceramic radial [SKT]	–	1	–	–
C6	–	100 nF	16 V	X7R	–	TH: 5 mm pitch	Capacitor: Dipped ceramic radial	–	1	653-0153	–
C7	Skt	10 µF	25 V	X7R	–	TH: 5 mm pitch [SKT]	Capacitor: Dipped ceramic radial [SKT]	–	1	379-135	811-8367
C8	–	100 nF	200 V	X7R	–	SM: 1206	Capacitor: Ceramic chip	–	1	885-1900	1855877
C10	Skt	330 nF	25 V	X7R	–	TH: 5 mm pitch [SKT]	Capacitor: Dipped ceramic radial [SKT]	–	1	721-5278	2309021
C14, C15	–	1000 µF	160 V	20%	EKMQ161VSN102MP40S	TH: 10 mm P, 22 mm D, 40 mm H	Capacitor: Electrolytic radial	–	2	841-4848	–
C16	–	100 nF	10 V	X7R	–	SM: 0805	Capacitor: Ceramic chip	–	1	264-4416	2070445
C17, C18	–	47 pF	10 V	COG	–	SM: 0805	Capacitor: Ceramic chip	–	2	264-4270	2497035
C19	–	4.7 µF	16 V	X7R	–	SM: 0805	Capacitor: Ceramic chip	–	1	820-2778	2497057
C20	–	100 nF	16 V	X7R	–	SM: 0805	Capacitor: Ceramic chip	–	1	264-4416	2070445
C21	–	10 nF	16 V	X7R	–	SM: 0805	Capacitor: Ceramic chip	–	1	264-4371	–
C, CP1, CP2, CSM, CSO, CSP, DIAG, ENABLE, GH, GL, HS, LSDrain, LSn, LSS, OOS, RESETn, S, SCK, SDI, SDO, STRn, VBB, VBRG, VL, VREG	–	–	–	–	–	TH: 1.33 mm-diameter hole	Test point: 2.1 mm round loop, red	–	25	262-2220	8731209
CRD1, CRD2	–	–	–	–	E202	TH: 1.8 × 3.9 mm body	Diode: Current regulation, 100 V, 2 mA	–	2	RapidOnline 47-2602	
D1	–	–	–	–	BAT54	SM: SOT23	Diode: Schottky, 30 V, 0.2 A	–	1	436-7818	1081190
GND1, GND2, GND3, GND4, GND5	–	–	–	–	–	TH: 12 mm pitch, 20 swg	Ground bar: Tinned copper wire	–	5	355-063	–
GND6, GND7	–	–	–	–	–	TH: 1.33 mm-diameter hole	Test point: 2.1 mm round loop, black	–	2	262-2214	8731195
J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J22	–	–	–	–	–	TH: SIL2, 2.54 mm pitch, 1 × 2	Jumper: Header male 2-pin	–	14	251-8086	–
J16, J17, J18, J19, J20, J21	–	–	–	–	–	TH: SIL3, 2.54 mm pitch, 1 × 3	Jumper: Header male 3-pin	–	6	251-8092	–
LED1, LED2, LED3	–	–	–	–	SML-211UT	SM: Proprietary 0805	LED: Chipled, 2-pin, red, 2 mA	–	3	700-7907	1685056
LK1	–	0 Ω	–	–	–	SM: 0805	Shorting link: Test point loop	–	1	389-811	1422593
M1, M2	–	–	–	–	IRLR3110ZPBF	SM: TO-252 (DPAK)	Mosfet: N-Channel, logic, 63 A, 100 V	–	2	650-4514	1436990
MH1, MH2, MH3, MH4, MH5, MH6, MH7, MH8	–	–	–	–	–	TH: M3 (130 mm) hole	Mount hole: Standoff M3 6 mm	–	8	382-967	–
PCB	–	–	–	–	EDC165R0	FR4, 2 oz Cu, 2-layer	PCB: AMT49502LP evaluation board	–	1	–	–
Q1	–	–	–	–	BC807	SM: SOT23	Transistor: PNP, 45 V, 0.5 A	–	1	436-7896	1081221
R1, R2	–	100 kΩ	0.125 W	1%	–	SM: 0805	Resistor: Ceramic chip	–	2	223-0691	2074335
R3	Skt	10 kΩ	0.125 W	1%	–	TH: 10 mm pitch, 6 mm body [SKT]	Resistor: Axial [SKT]	–	1	148-736	9341110
R4, R5, R6, R7, R8, R9, R10, R11, R12	Skt	1 kΩ	0.125 W	1%	–	TH: 10 mm pitch, 6 mm body [SKT]	Resistor: Axial [SKT]	–	9	148-506	–
R13	–	47 kΩ	0.25 W	1%	–	SM: 1206	Resistor: Ceramic chip	–	1	679-2156	2447521
R14, R15	–	27 kΩ	0.125 W	1%	–	SM: 0805	Resistor: Ceramic chip	–	2	223-0613	–

[1] DNF = Do not fit (component not fitted).
[2] SPI connection at X8 (and GUI file/drivers) requires a USB-A to USB-Micro-B cable.
[3] SPI connection at X5 or X3 (and driver file and GUI file) requires an FTDi TTL-232R-5V USB cable.
[4] http://uk.RS-online.com/
[5] http://uk.FARNELL.com/

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BILL OF MATERIALS (continued)

Table 3 (continued): Component Function, Specification, and Selection Criteria [1][2][3]

Designator	SIL Skt	Value	Rating	Tol	Part Number	Footprint	Description	DNF	Qty	RS #1 [4]	Farnell #1 [5]
R16	–	2.2 kΩ	0.125 W	1%	–	SM: 0805	Resistor: Ceramic chip	–	1	223-0477	–
R17, R18	Skt	0 Ω	–	–	–	TH: 10 mm pitch, 6 mm body [SKT]	Resistor: Axial [SKT]	–	2	188-374	1700196
R19, R20	Skt	33 Ω	0.125 W	1%	–	TH: 10 mm pitch, 6 mm body [SKT]	Resistor: Axial [SKT]	–	2	148-130	2330112
R23	–	0.022 Ω	1 W	1%	–	SM: 2512	Resistor: Ceramic chip	–	1	294-5602	1173980
R24 **Fit on top of R23 manually**	–	0.022 Ω	1 W	1%	–	SM: 2512	Resistor: Ceramic chip; R24 on R23	R24 on R23	1	294-5602	1173980
R25, R26	Skt	470 kΩ	0.125 W	1%	–	TH: 10 mm pitch, 6 mm body [SKT]	Resistor: Axial [SKT]	–	2	683-3730	9468455
R27, R28, R29, R31, R32, R33, R34	Skt	10 kΩ	0.125 W	1%	–	TH: 10 mm pitch, 6 mm body [SKT]	Resistor: Axial [SKT]; component not fitted	DNF	0	148-736	9341110
R30	–	10 kΩ	1 W	5%	–	TH: 18mm pitch, 12 × 5 mm body	Resistor: Axial	–	1	–	–
S2	–	–	–	–	–	TH: 2.54 mm (100 mm) pitch	Switch: DIL, 4-way, raised actuator	–	1	690-3567	9479040
U1 (Device)	–	–	–	–	AMT49502LP	SM: eTSSOP24	Device: Allegro motor driver; component not fitted	DFN	0	–	–
U1 (Socket)	–	–	–	–	OTS-24(28)-0.65-02	TH: TSSOP24 skt	Socket: Enplas (TSSOP24)	–	1	–	–
U2	–	–	–	–	LM2936HVMA-5.0/NOPB	SM: SOIC8	Device: Voltage regulator 5 V	–	1	651-3726	2400656
U3	–	–	–	–	FT232RL	SM: SSOP28	Device: FTDi USB UART	–	1	406-580	1146032
U4	–	–	–	–	USB6B1	SM: SO8	Device: USB port protection	–	1	687-1075	9804358
X1, X2, X6, X7	–	–	–	–	–	TH: 7.62 mm (300 mm) pitch	Connector: Screw terminal, 2-way	–	4	189-5966	1793006
X3	–	–	–	–	–	TH: 2.54 mm pitch, 2 × 13	Connector: IDC 26-way ribbon header	–	1	542-8835	9838287
X4	–	–	–	–	–	TH: 5.08 mm (200 mm) pitch	Connector: Screw terminal, 2-way	–	1	425-8720	1131855
X5	–	–	–	–	–	TH: 2.54 mm pitch, 6 × 1, SIL6	Connector: 6-way header unshrouded	–	1	360-6308	9733337
X8	–	–	–	–	–	SM: Horizontal, top mount	Connector: USB micro-B female	–	1	702-5475	1568026
[ESDBAG_6x10]	–	–	–	–	–	–	ESD bag: 152 × 254 mm (6" × 10")	–	1	182-8821	168488
[JMP_SHORT_R]	–	–	–	–	–	–	Jumper short/shunt link: Red	–	17	251-8531	150411
[SIL_SKT]	–	–	–	–	–	TH: SIL1	Socket: SIL1 (Parts = x19, Skts = x38)	–	38	267-7416	–
[STANDOFF_NUT]	–	–	–	–	–	–	Mount: Standoff nut, plastic, M3	–	8	292-546	–

[1] DNF = Do not fit (component not fitted).
[2] SPI connection at X8 (and GUI file/drivers) requires a USB-A to USB-Micro-B cable.
[3] SPI connection at X5 or X3 (and driver file and GUI file) requires an FTDi TTL-232R-5V USB cable.
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RELATED LINKS

AMT49502 product page: https://www.allegromicro.com/en/products/motor-drivers/brush-dc-motor-drivers/amt49502.

Both GUI software and programming guide can be downloaded from the Allegro Customer Portal, which requires registration and login at: http://registration.allegromicro.com/login.

APPLICATION SUPPORT

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Revision History

Number	Date	Description
–	December 9, 2021	Initial Release
1	January 4, 2023	Standardized product naming conventions per new guidelines and made minor editorial and updates (all pages)
2	April 19, 2024	Changed Introduction section to Description section, added Features and Evaluation Board Contents sections, changed example evaluation board from -KLP version to -LP version, and changed the term “normal” to “typical” (page 1), added parent heading Using the Evaluation Board (page 2); updated schematic (page 4); and added Layout, Bill of Materials, Related Links, and Application Support sections (pages 5–8).

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