# APEK85000-GEJ-01-T

## AHV85000 + AHV85040 Evaluation Board User Guide

## DESCRIPTION

The Allegro MicroSystems Half-Bridge Driver-Switch APEK85000-GEJ-01-T is a demonstration board containing two AHV85000 + AHV85040 GaN FET driver chip sets and two GaN FETs configured in a half-bridge configuration.

## FEATURES

The APEK85000-GEJ-01-T can be used to perform double-pulse tests, or to interface the half bridge to an existing LC power section, both as shown in this guide.

The isolated AHV85000 + AHV85040 driver chip set does not require secondary-side power or bootstrap components. Gate drive power is supplied to the secondary side from the primary-side supply voltage, $V_{DRV}$. The amplitude of the gate drive can be varied by varying $V_{DRV}$ between 10.8 V and 13.2 V.

## EVALUATION BOARD CONTENTS

- APEK85000-GEJ-01-T evaluation board.

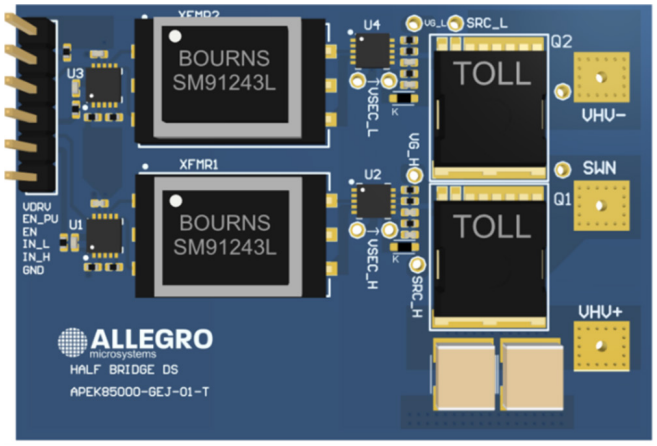


**Figure 1: AHV85000 + AHV85040 Evaluation Board (APEK8500-GEJ-01-T)**

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# DANGER

**DO NOT TOUCH THE BOARD WHEN IT IS ENERGIZED AND ALLOW ALL COMPONENTS TO DISCHARGE COMPLETELY PRIOR HANDLING THE BOARD.**

**HIGH VOLTAGE CAN BE EXPOSED ON THE BOARD WHEN IT IS CONNECTED TO POWER SOURCE. EVEN BRIEF CONTACT DURING OPERATION MAY RESULT IN SEVERE INJURY OR DEATH.**

Ensure that appropriate safety procedures are followed. This evaluation kit is designed for **engineering evaluation in a controlled lab environment and should be handled by qualified personnel ONLY.** Never leave the board operating unattended.

**WARNING**

Some components can be hot during and after operation. **There is NO built-in electrical or thermal protection on this evaluation kit.** The operating voltage, current, and component temperature should be monitored closely during operation to prevent device damage.

**CAUTION**

This product contains parts that are susceptible to damage by electrostatic discharge (ESD). Always follow ESD prevention procedures when handling the product.



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## USING THE EVALUATION BOARD

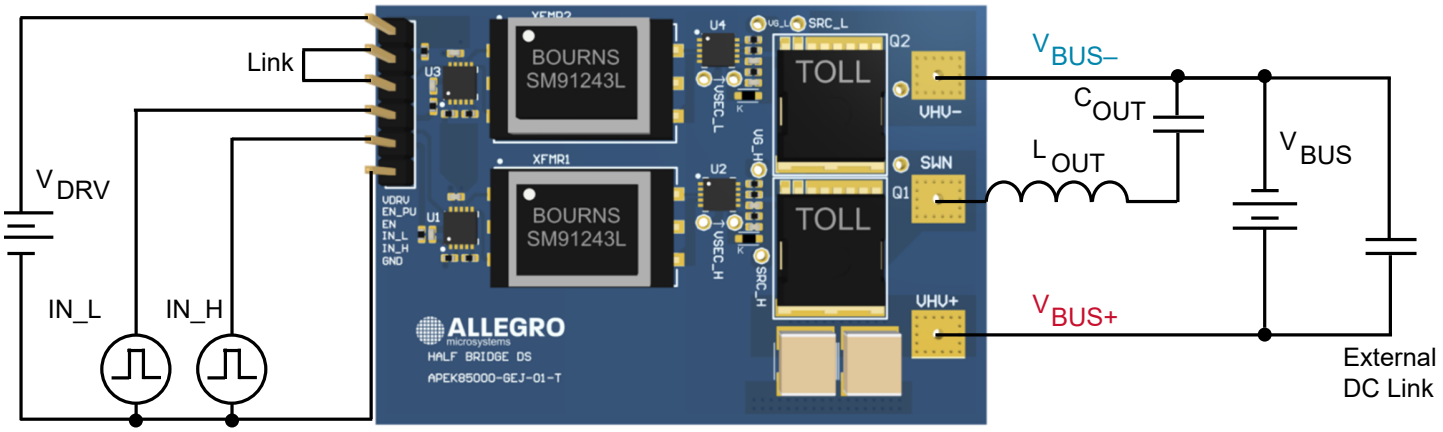


**Figure 2: APEK85000-GEJ-01-T Quick Start**

1. Apply $V_{DRV}$ = 12 V.
2. Link pins EN_PU and EN (if not using external enable control).
3. Apply input gate signals, with adequate dead time, to the IN_L and IN_H inputs.
4. Convenient test points are located on the test board as shown in the Measurement Points section. A suitable differential oscilloscope should be used to monitor the high-side gate signal from $V_{GH}$ to $V_{SW}$.

## GATE PULL-UP AND PULL-DOWN RESISTORS

The AHV85040 gate driver has independent output pins for the gate pull-up and gate pull-down, allowing control of the turn-on and turn-off rise and fall times.

The default values for these resistors are:

OUTPU: R7 and R13 = 10 Ω

OUTPD: R1 and R15 = 1 Ω

These values can be modified to suit the application.



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## ENABLE SEQUENCE

The AHV85000 has an open-drain enable pin (EN) to facilitate a system-level wired-AND startup.

When the enable pin is externally pulled low, the driver is forced into a low-power mode. The driver output is pulled low in this mode. In the event of an internal fault condition, such as UVLO or typical startup delay, the EN pin is actively pulled low internally by the driver.

During typical operation, the pin is released by the driver and must be pulled high with an external pull-high resistor. This functionality can be used by the PWM controller as an indication that it can start sending IN pulses to the driver. It is typically wired-AND with the controller enable pin as shown in Figure 3.

The APEK85000-GEJ-01-T evaluation board provides direct access to the EN pin on connector CONN1. Internally, the board contains a 100 kΩ pull-up resistor connected from $V_{DRV}$ to the EN_PU pin on connector CONN1 (see the Schematic section). If external control of the enable function is not required, pins EN and EN_PU must be linked together on CONN1 to make use of the internal 100 kΩ pull-up resistor to enable the driver. If the EN pin is left floating, the drivers do not respond to IN_L or IN_H input signals.

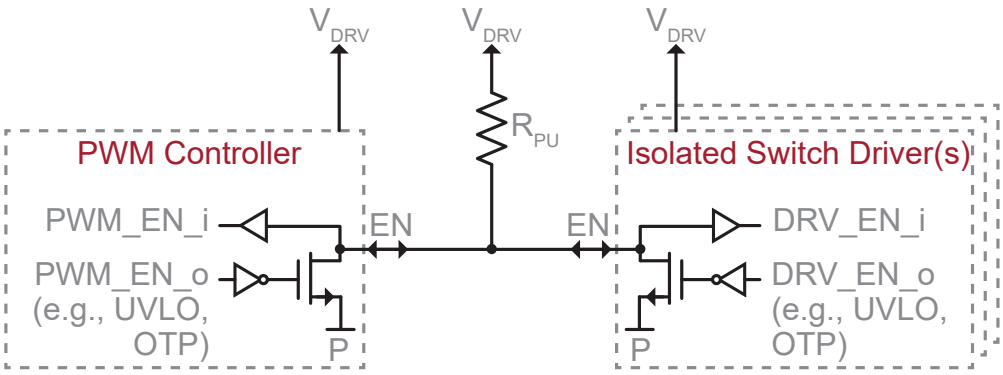


**Figure 3: AHV85000 Wired-AND Enable**

When the EN pin is pulled low, the driver output is disabled and pulls down the OUTPD pin, regardless of the IN pin level (high or low). The driver goes to a low-power standby mode, and the isolated $V_{SEC}$ bias rail is allowed to discharge. The rate of decay of $V_{SEC}$ depends on the value of the $C_{SEC}$ capacitor.

When the EN pin is subsequently pulled high, the driver reenables, and the isolated $V_{SEC}$ bias rail starts to recharge.



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## START SEQUENCE

The startup sequence of the AHV85000 chip set is shown in Figure 4. Time $t_{START}$ is defined as the time after which $V_{DRV}$ reaches the UVLO rising level to the AHV85000, releasing the EN internal pull-down.

Any PWM signal applied to IN must remain low until $V_{DRV}$ > UV threshold to avoid parasitic charging of the $V_{DRV}$ rail through the IN pin internal ESD structures.

After $V_{DRV}$ exceeds the UV enable threshold, a startup time delay, $t_{START}$, is required to charge $V_{SEC}$ and allow all internal circuits to initialize and stabilize. During $t_{START}$, any IN signal inputs are ignored. EN internal pull-down remains active during $t_{START}$ and becomes disabled (i.e., go open-drain) only when $V_{DRV}$ has reached its UVLO voltage level, all on-chip voltages have stabilized, and the internal $t_{START}$ timer has elapsed. Thus, the EN pin can be used via a shared EN line to flag when $t_{START}$ has elapsed and the driver is ready to respond to PWM signals at the IN pin, as outlined previously in this guide.

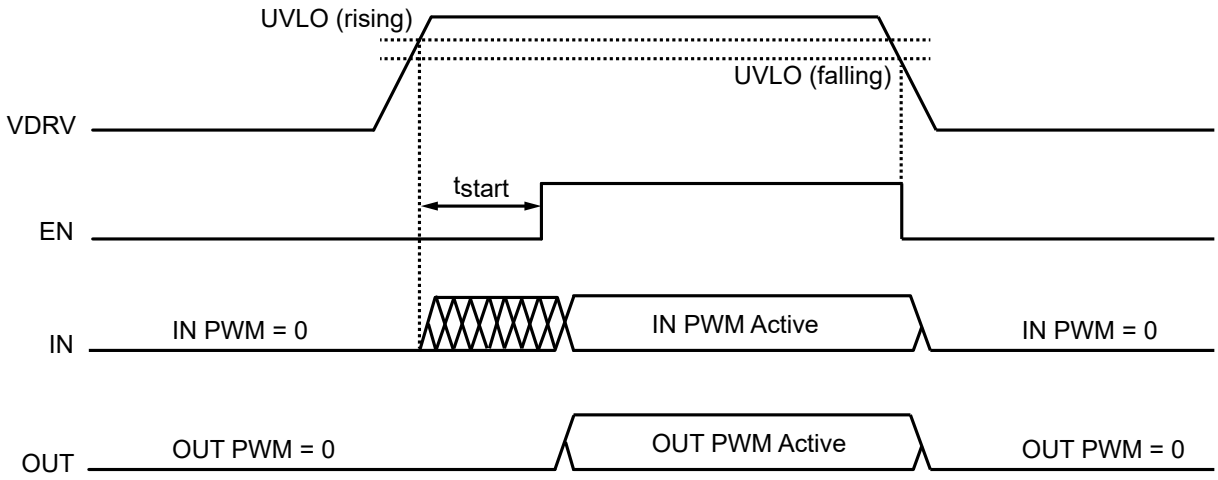


**Figure 4: AHV85000 Chip-Set Startup Sequence**



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## MEASUREMENT POINTS

The APEK85000-GEJ-01-T evaluation board contains convenient test points for monitoring the high- and low-side gate drives as well as the switch node, as shown in Figure 5.

When measuring $V_{GS\_H}$, use a differential probe with suitable ratings for the applied bus voltage. The APEK85000-GEJ-01-T EVM uses a bipolar gate drive arrangement, as shown in Figure 5. When measuring $V_{GS}$, both gate drives are measured relative to the source of their associated GaN FET. Therefore, the off-state voltage is negative.

To avoid pickup of spurious switching noise, it is important to use a low-inductance scope probe ground lead, as shown.

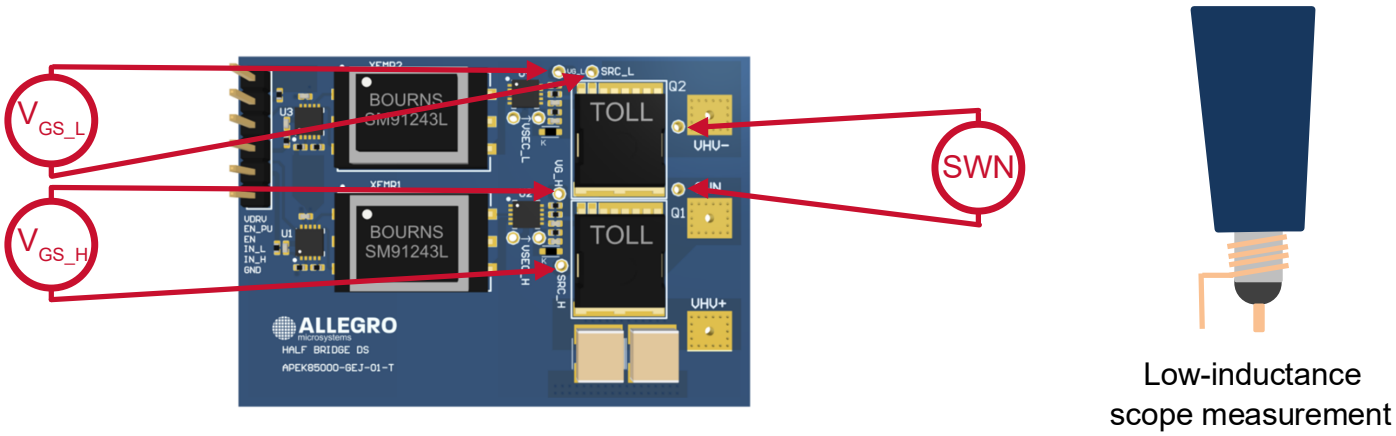


**Figure 5: Measurements Points**



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## BIPOLAR GATE DRIVE

The high rate of change of voltages and currents in power-switching circuits can create unwanted inductor currents and capacitor voltage drops.

One example is the false turn-on of a FET due to a dV/dt event. In a half-bridge circuit, after the low-side FET has turned-off and a suitable dead time has elapsed, the high-side FET turns on. This produces a rapidly changing switch-node voltage at the drain of the low-side FET. This voltage produces a capacitor current:

$$i_{C_{GD}} = C_{GD} \frac{dV_{DS\_L}}{dt},$$

flowing in the gate-drain capacitance, $C_{GD}$, and driver output; this causes the voltage on the gate of the low-side FET to rise. If this voltage spike peaks beyond the threshold voltage, $V_{TH}$, the FET conducts. Because the high-side FET also conducts, a potentially destructive shoot-through event can result.

The APEK85000-GEJ-01-T evaluation board uses a bipolar gate drive arrangement that helps mitigate the effects of gate-drain capacitor currents. The secondary supply voltage, $V_{SEC}$, is a function of the primary supply voltage, $V_{DRV}$. The Zener diode, CR1, regulates the positive turn-on voltage of the GaN FET. During the turn-off period, the gate voltage is negative with a value of:

$$V_{GS\_OFF} = V_{SEC} - V_{ZENER}.$$

$V_{SEC}$ is typically 8 V.

This negative $V_{GS\_OFF}$ voltage allows more margin before the threshold voltage is reached.

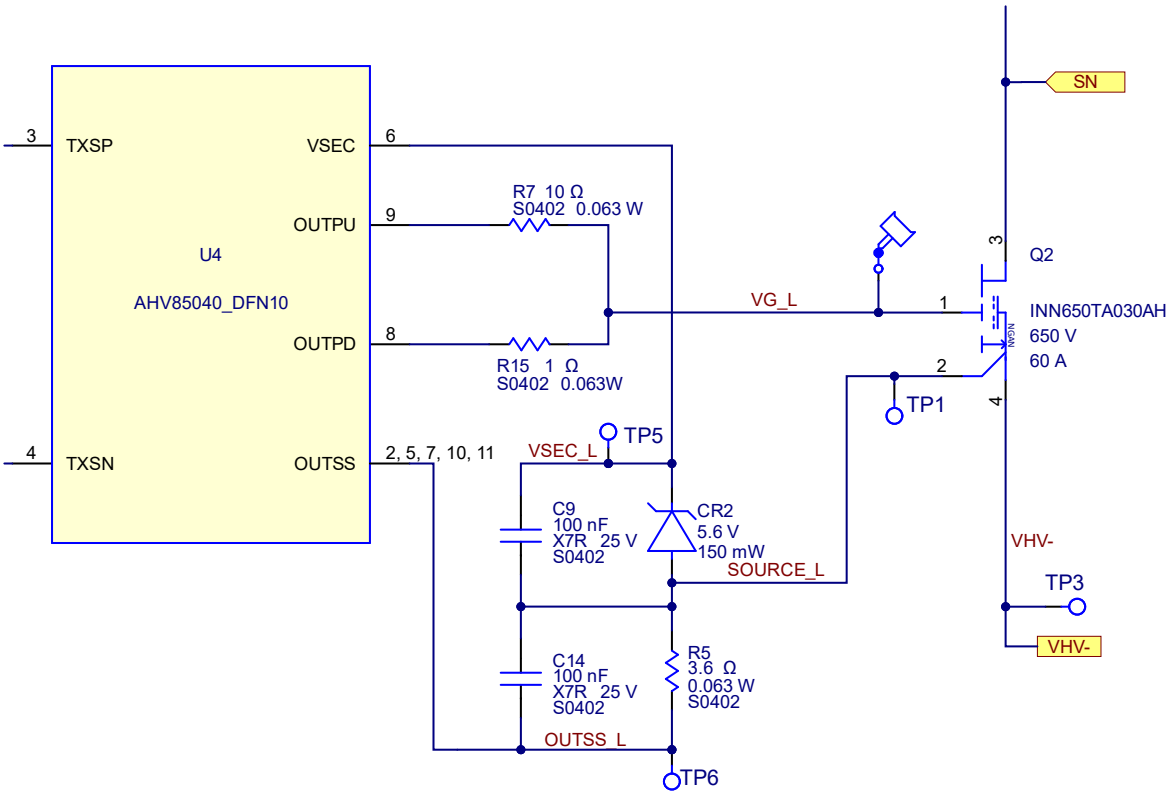


**Figure 6: Bipolar Gate Drive Schematic**



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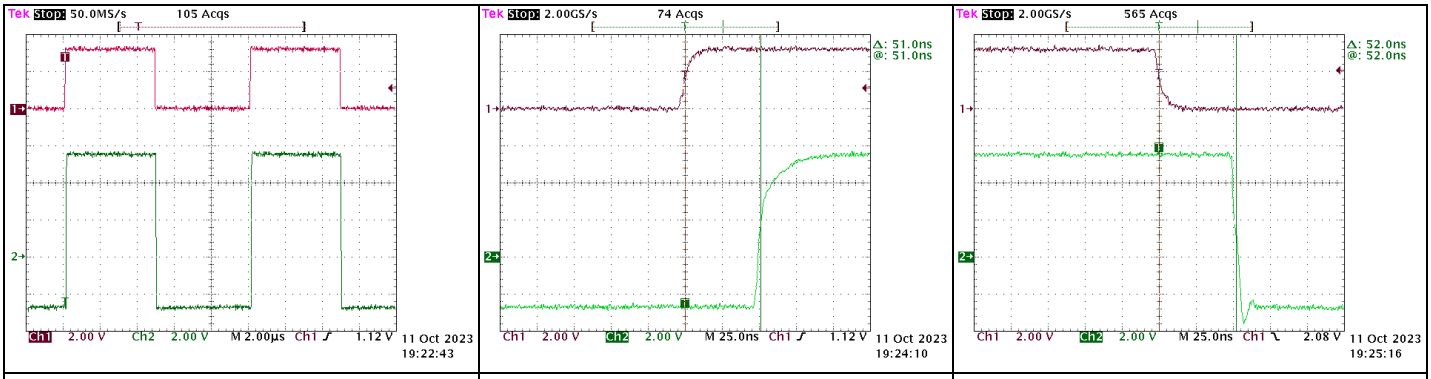
## PROPAGATION DELAY

- $V_{DRV}$ = 12 V
- Input = 100 kHz
- $R_{PU}$ = 10 Ω, $R_{PD}$ = 1 Ω
- Power train unloaded. That is, VHV+ = 0 V.




| CH1 (Top): Driver Input<br>CH2 (Bottom): Driver Output wrt VHV– | CH1 (Top): Driver Input<br>CH2 (Bottom): Driver Output wrt VHV– | CH1 (Top): Driver Input<br>CH2 (Bottom): Driver Output wrt VHV– |
|---|---|---|
| **Low-Side Driver Output** | **Typical Turn-on Propagation Delay** | **Typical Turn-Off Propagation Delay** |

**Figure 7: Typical Driver Output at 100 kHz**



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## DOUBLE-PULSE TEST

The double-pulse test is used to evaluate the switching characteristics of a power switch under hard switching but in a safe manner.

For a low-side switch, the setup is as shown in Figure 8. The low-side switch is driven with two pulses as shown in Figure 9. The high-side switch can be held off or driven with the inverse of the low-side gate switch (with adequate dead time).

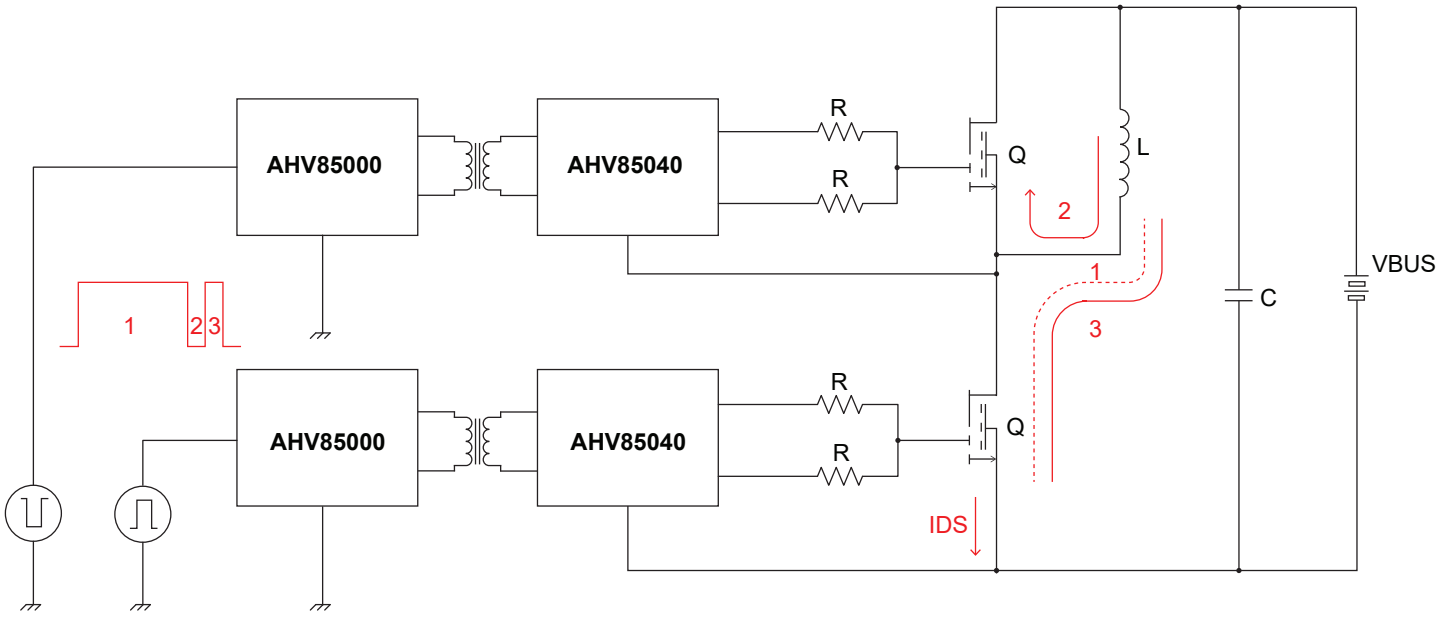


**Figure 8: Double-Pulse Test**

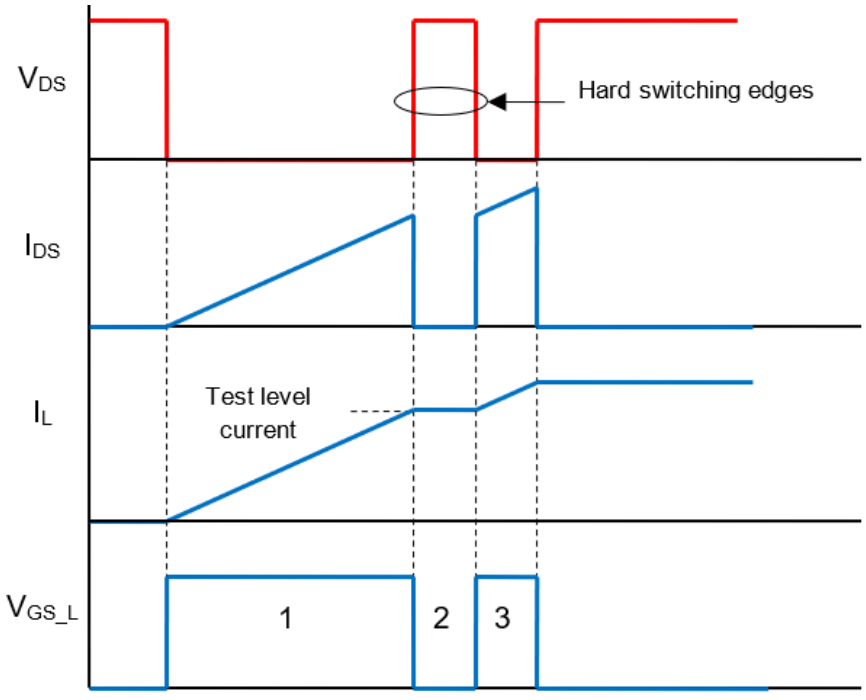


**Figure 9: Double-Pulse Test Waveforms**



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An inductor is placed in parallel with the high-side switch. The goal of this inductor is to establish the test level current in the low-side switch at the end of the first on pulse (1). The magnitude of the test level current at the end of period 1 is given by:

$$I_L = V_{BUS} \frac{t_{ON\_1}}{L}$$

During period 2, the inductor current naturally decays. The duration of period 2 should not be so long that inductor current deviates significantly from the desired test level.

During period 3, the inductor current again rises. Period 3 should not be so long that the inductor current rises to an excessive level.

The falling edge of pulse 1 is used to examine the hard turn-off characteristics of the switch. The rising edge of pulse 3 is used to examine the hard turn-on characteristics of the switch. By only applying these two pulses, the switches are only on for a very short time and should not overheat.

## DOUBLE-PULSE TEST RESULTS

### DPT Result 200 V, 8 A

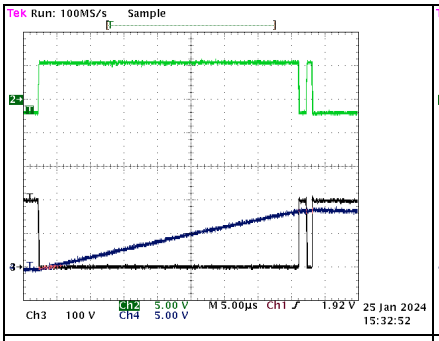
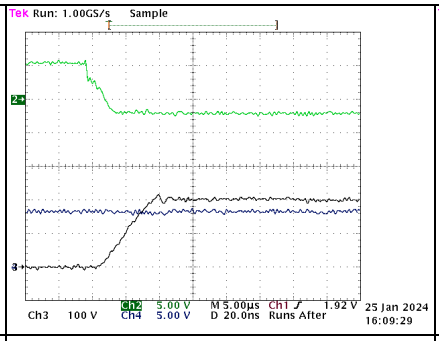
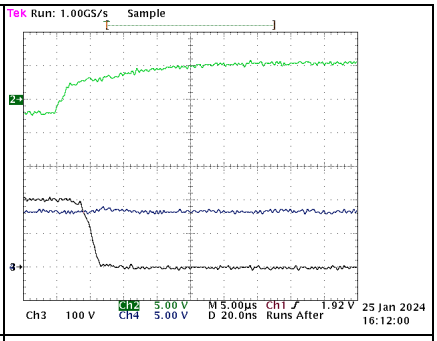
|  |  |  |
|---|---|---|
| **CH2 (Green): Low-Side $V_{GS}$**<br>**CH3 (Black): Switch Node**<br>**CH4 (Blue): Inductor Current (1 A/V)** | **CH2 (Green): Low-Side $V_{GS}$**<br>**CH3 (Black): Switch Node**<br>**CH4 (Blue): Inductor Current (1 A/V)** | **CH2 (Green): Low-Side $V_{GS}$**<br>**CH3 (Black): Switch Node**<br>**CH4 (Blue): Inductor Current (1 A/V)** |
| **DPT Overview** | **DPT Hard-Switching Turn-Off Time Base (20 ns/div)** | **DPT Hard-Switching Turn-On Time Base (20 ns/div)** |

**Figure 10: DPT 200 V, 8 A**

### DPT Result 400 V, 17 A

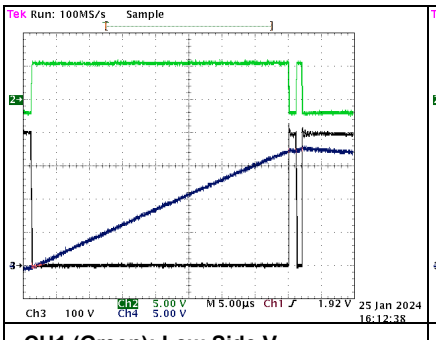
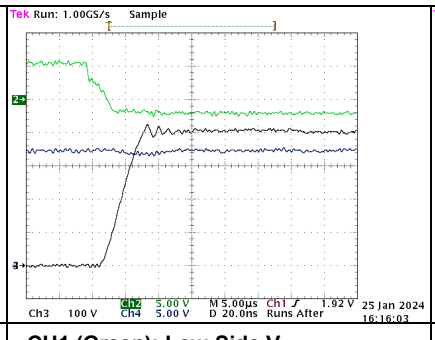
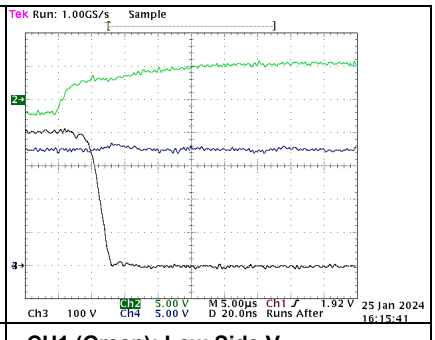
|  |  |  |
|---|---|---|
| **CH1 (Green): Low-Side $V_{GS}$**<br>**CH3 (Black): Switch Node**<br>**CH4 (Blue): Inductor Current (1 A/V)** | **CH1 (Green): Low-Side $V_{GS}$**<br>**CH3 (Black): Switch Node**<br>**CH4 (Blue): Inductor Current (1 A/V)** | **CH1 (Green): Low-Side $V_{GS}$**<br>**CH3 (Black): Switch Node**<br>**CH4 (Blue): Inductor Current (1 A/V)** |
| **DPT Overview** | **DPT Hard-Switching Turn-Off Time Base (20 ns/div)** | **DPT Hard-Switching Turn-On Time Base (20 ns/div)** |

**Figure 11: DPT 400 V, 17 A**



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## SCHEMATIC

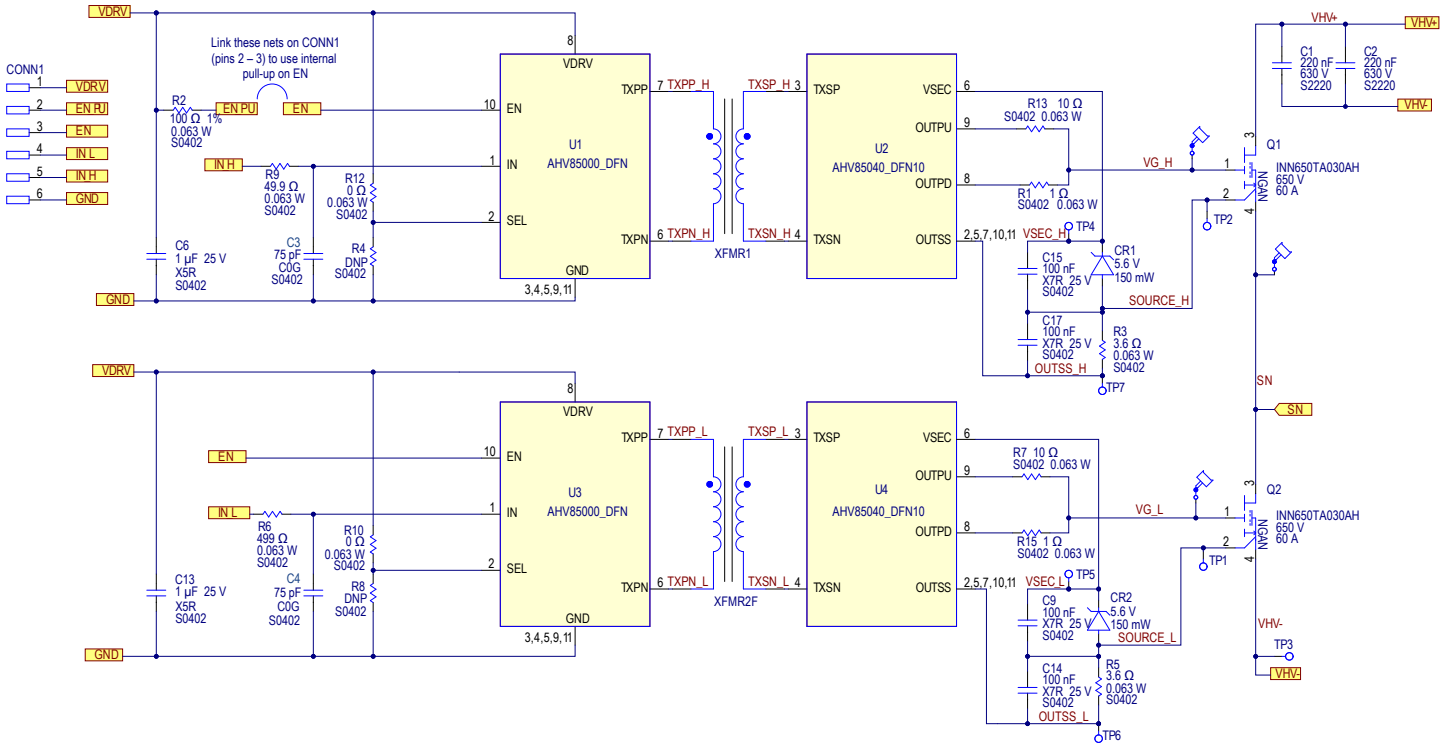


**Figure 12: APEK85000-GEJ-01-T Schematic**



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## PCB LAYOUT

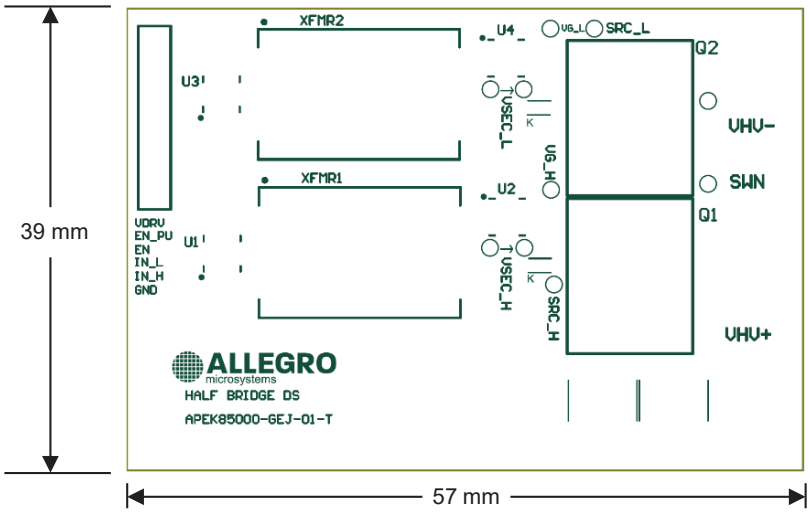


**Figure 13: APEK85000-GEJ-01-T Top Overlay**

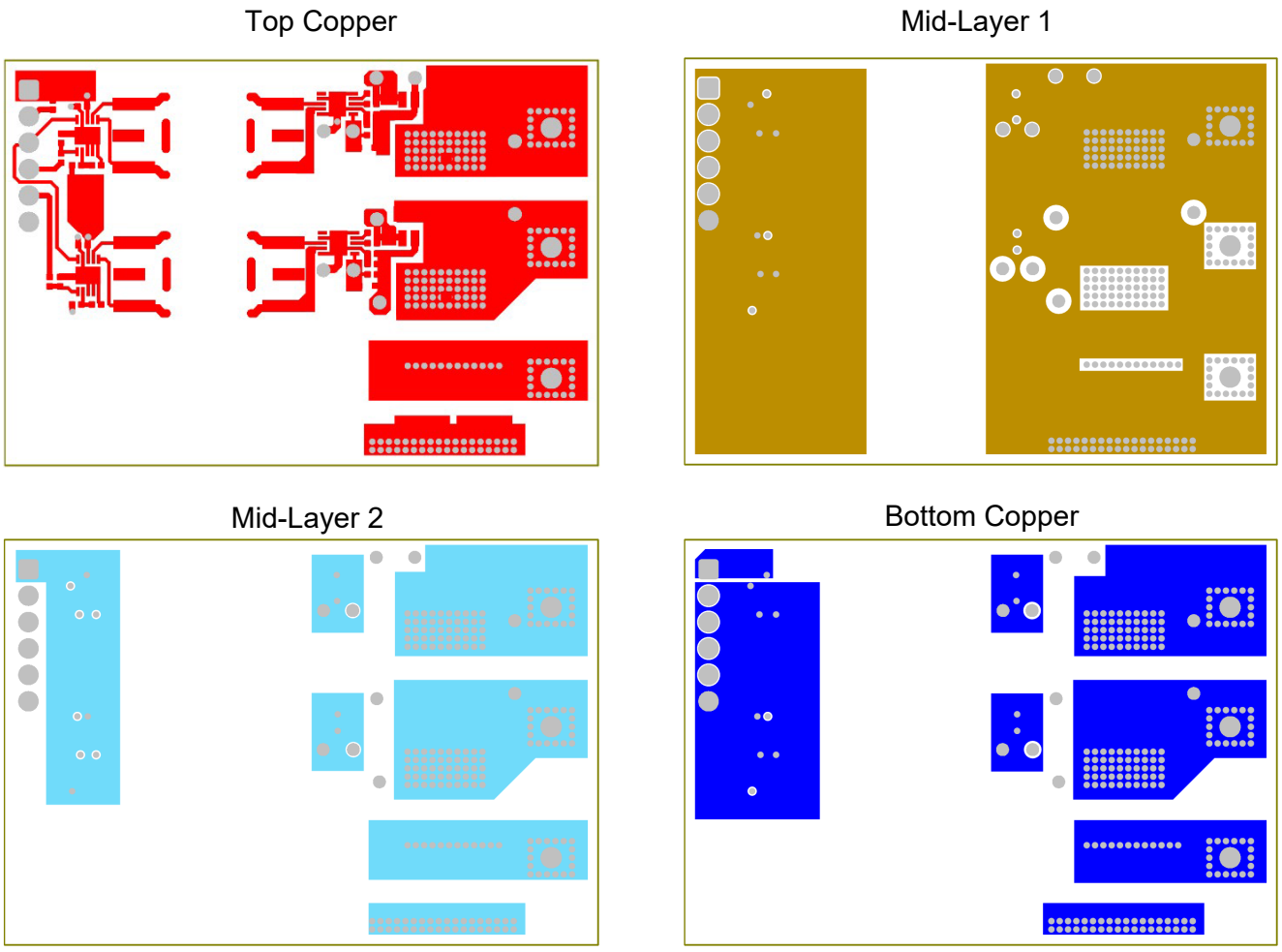


**Figure 14: APEK85000-GEJ-01-T PCB Copper Layers**



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## BILL OF MATERIALS

**Table 1: APEK85000-GEJ-01-T Evaluation Board Bill of Materials**

| Ref Name | Description | Value | Qty | Manufacturer | Manufacturer PN |
|---|---|---|---|---|---|
| CONN1 | Pin Header, Board-to-Board, 2.54 mm, 1 Row, 6 Contacts | Connector 6 Way | 1 | Molex | 22284065 |
| R2 | RES, 100 Ω, 0.063 W, 1%, 0402 | 100 Ω | 1 | Walsin Technologies | SR04X1003FTL |
| XFMR1, XFMR2 | AHV85000 TRANSFORMER | SM91234L | 2 | Bourns | SM91234L |
| U1, U3 | AHV85000 PRIMARY DFN10_EJ | AHV85000 | 2 | Allegro MicroSystems | AHV85000 |
| U2, U4 | AHV85040 SECONDARY DFN10_EJ | AHV85040 | 2 | Allegro MicroSystems | AHV85040 |
| C6, C13 | CAP, CER, 1uF, 25V, X5R, 0402 | 1 µF | 2 | Murata | GRT155R61E105KE01D |
| C3, C4 | CAP, CER, 75 pF, 50 V, COG/NPO, 0402 | 75 pF | 2 | Multicomp | MC0402N750J500CT |
| C1, C2 | Ceramic Capacitor, 0.22 µF, 630 V, 2220, X7R, GRM Series | 220 nF | 2 | Murata | GRM55DR72J224KW01L |
| Q1, Q2 | Innoscience eGaN FET 650V, 60 A, 34 mΩ, 16 nC | INN650TA030AH | 2 | Innoscience | INN650TA030AH |
| R10, R12 | RES, 0 Ω, 0.063 W, 1%, 0402 | 0 | 2 | Walsin Technologies | WR04X000PTL |
| R1, R15 | RES, 1 Ω, 0.20 W, 5%, 0402 | 1 | 2 | KOA Speer | SG73P1EWTTP1R00F |
| R3, R5 | RES, 3.6 Ω, 0.063 W, 1%, 0402 | 3.6 Ω | 2 | TE Connectivity | CRG0402F3K6 |
| R7, R13 | RES, 10 Ω, 0.20 W, 1%, 0402 | 10 Ω | 2 | KOA Speer | SG73P1EWTTP10R0F |
| R6, R9 | RES, 49.9 Ω, 0.063 W, 1%, 0402 | 49.9 Ω | 2 | Vishay | CRCW040249R9FKED |
| R4, R8 | RES, 0402, Not Assembled | | 2 | | |
| CR1, CR2 | Zener Diode, 5.6 V, 150 mW, SOD-523 | 5V6 | 2 | Rohm | EDZVFHT2R5.6B |
| C9, C14, C15, C17 | CAP, CER, 100 nF, 25 V, X7R, 0402 | 100nF | 4 | Murata | GRM155R71E104KE14D |



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## Revision History

| Number | Date | Description |
|---|---|---|
| – | February 20, 2024 | Initial release |





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