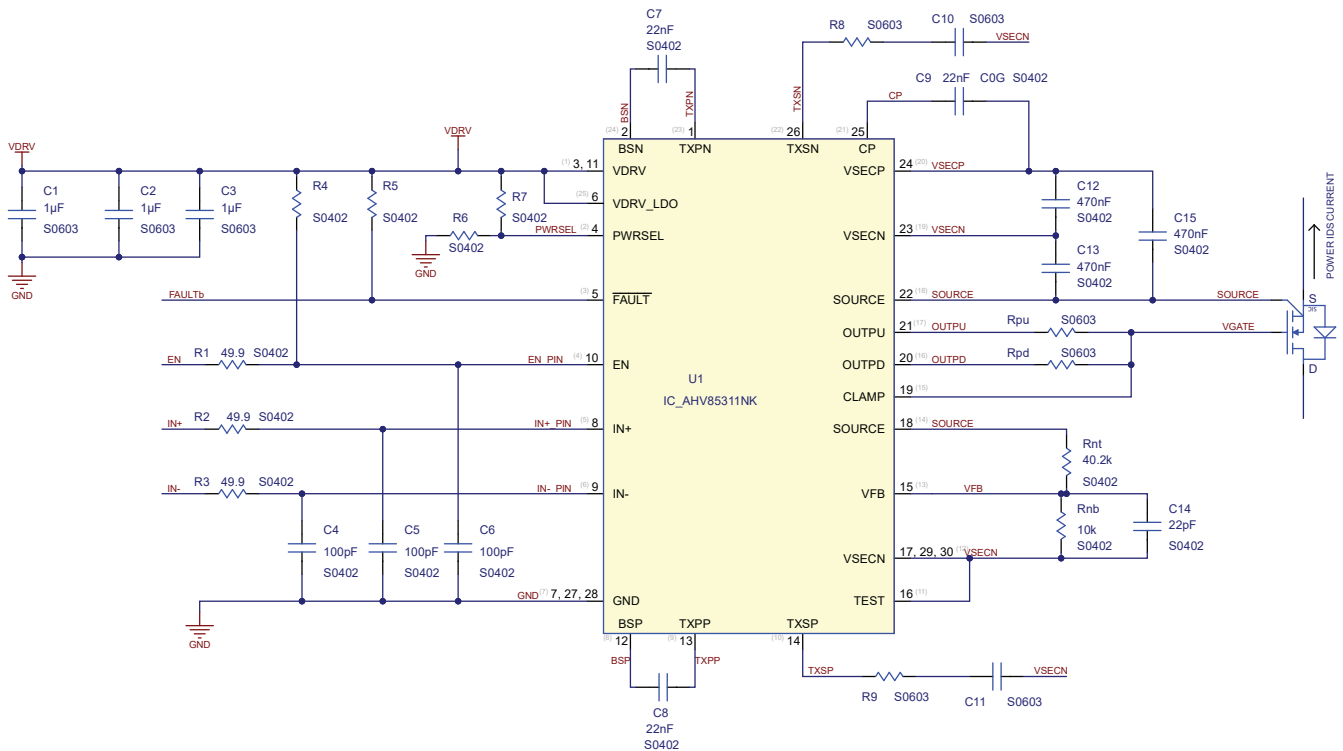


PCB Layout Guide

OVERVIEW

The purpose of this document is to provide printed-circuit-board (PCB) layout guidelines for the correct operation of the AHV85311NK module gate driver.

The guidelines in this document are presented in order of priority for both the primary side and the secondary side. Failure to adhere to these guidelines may result in incorrect operation or suboptimal operation of the AHV85311NK module.



Typical Schematic

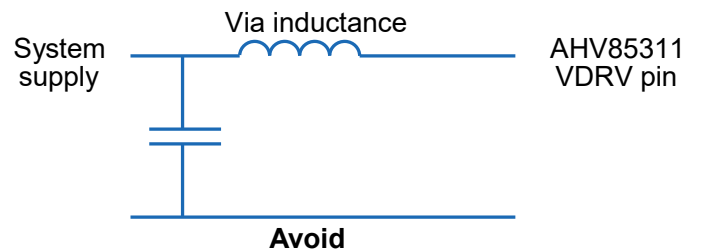
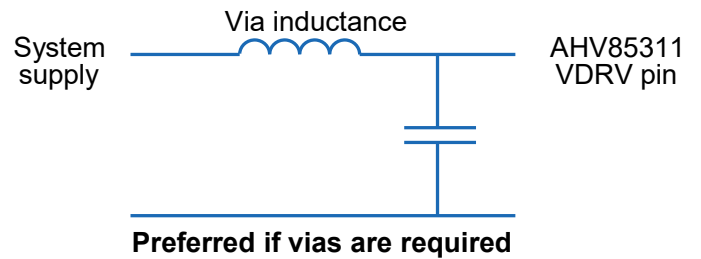
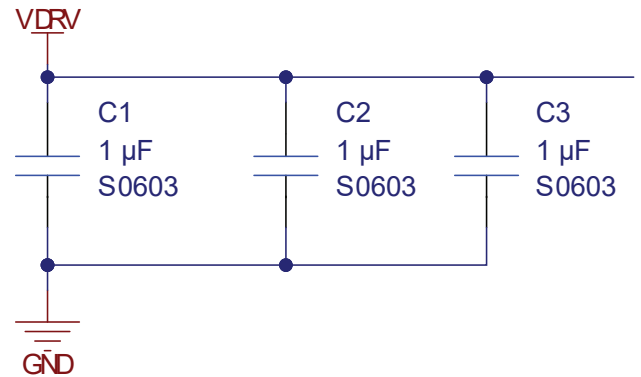
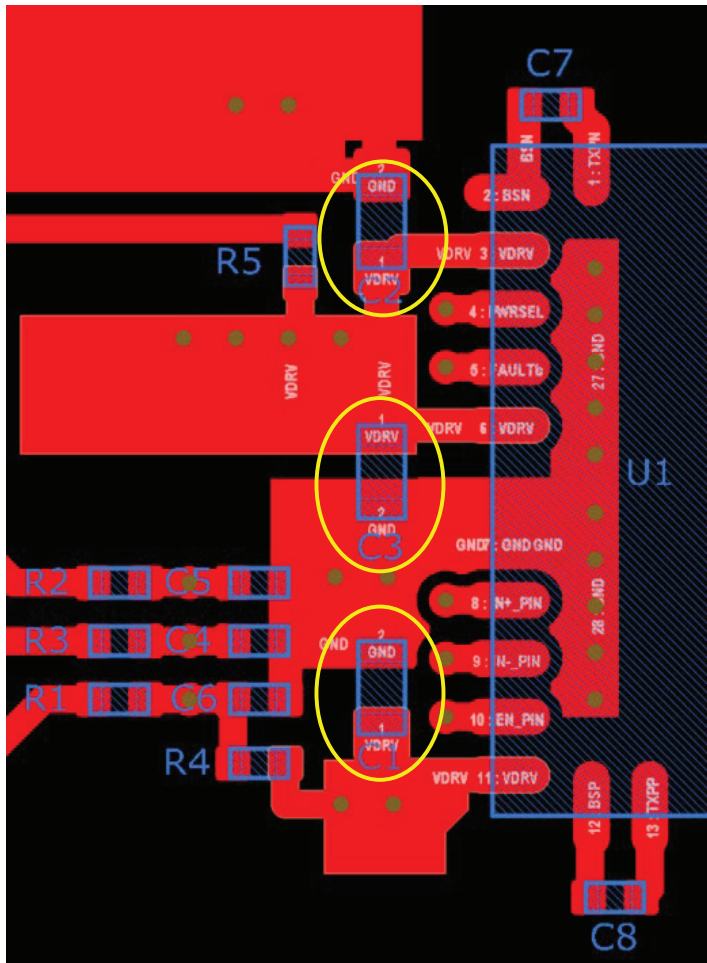
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PRIMARY SIDE

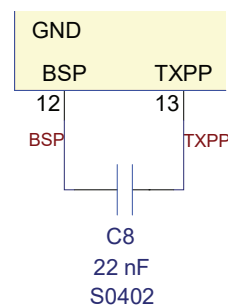
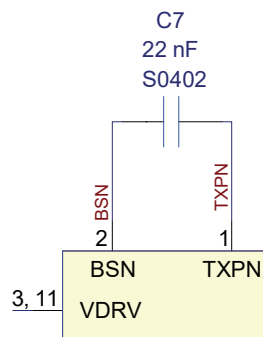
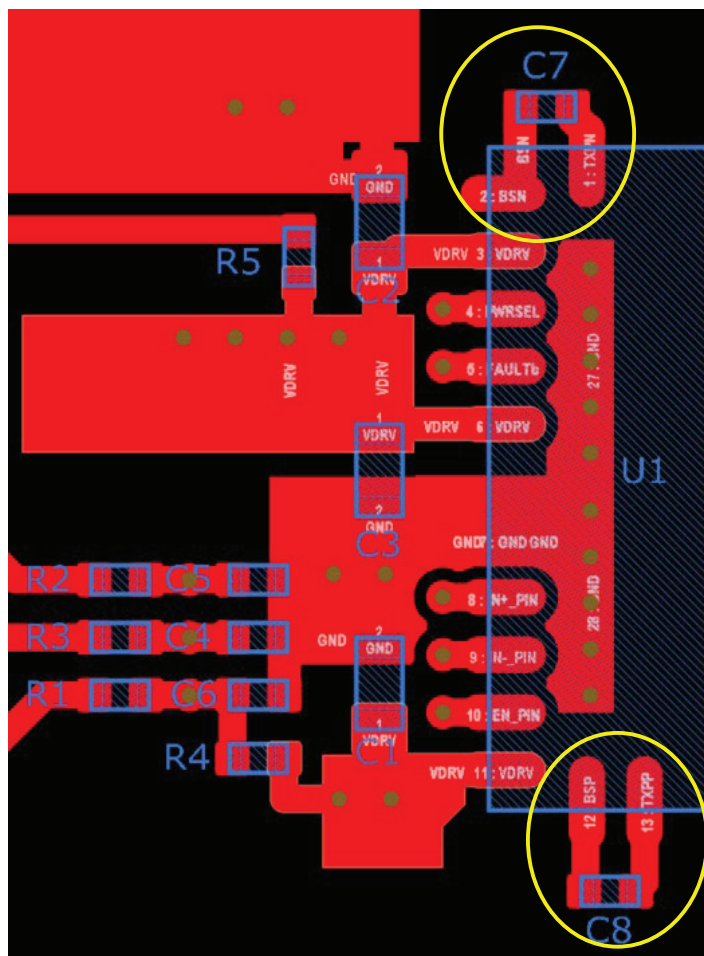
VDRV Decoupling

Correct VDRV decoupling is critical for correct device operation. The minimum requirement is one $1\ \mu\text{F}$ capacitor per VDRV pin. The preferred decoupling is $1\ \mu\text{F}$ in parallel with $100\ \text{nF}$ on each VDRV pin. A decoupling capacitor should be a good-quality (i.e., X7R or better) ceramic capacitor with an adequate voltage rating (i.e., at least 25 V). GND and VDRV should be routed with coplanar planes on internal layers. Between any decoupling capacitor and pin, via use should be avoided.



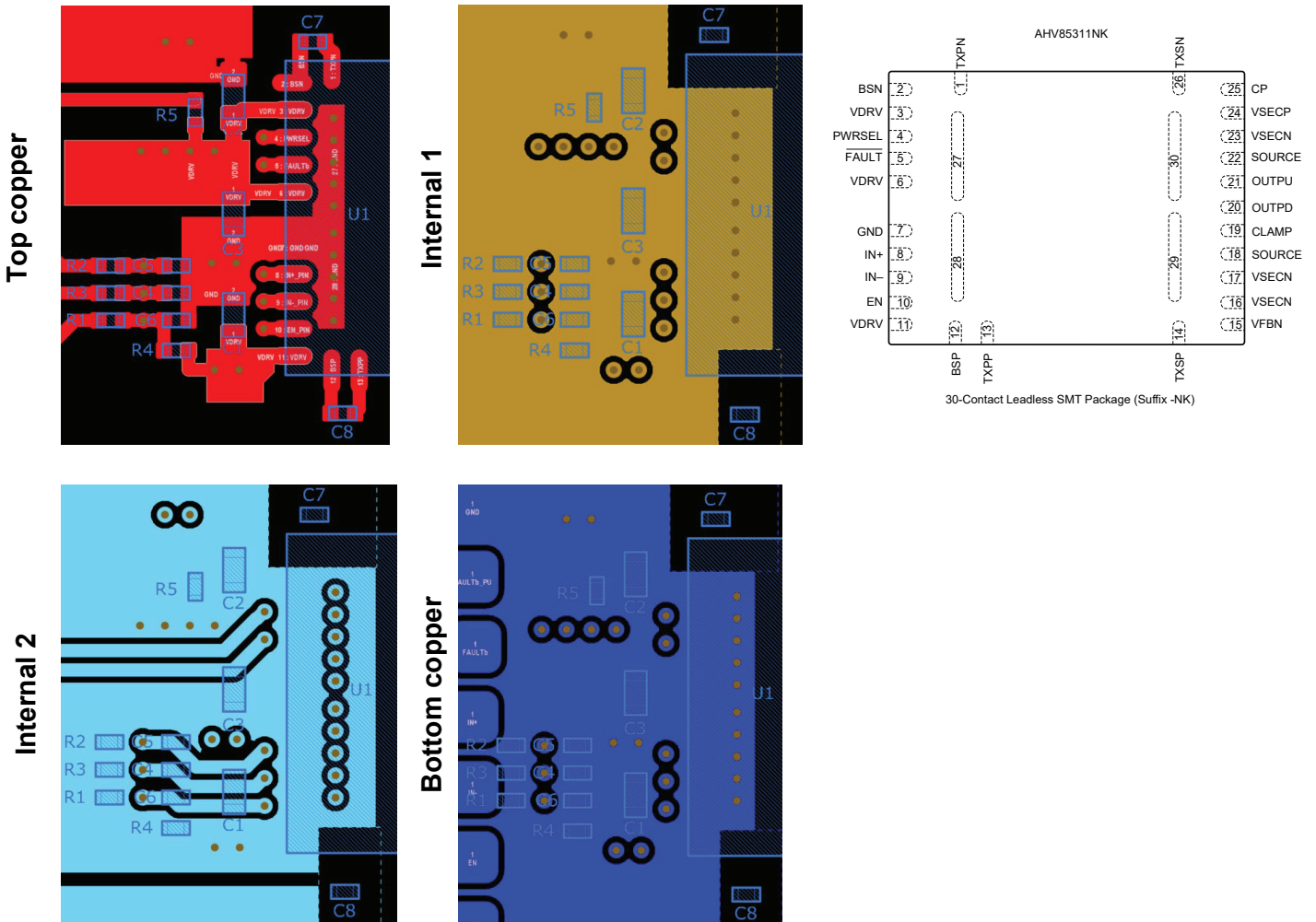
Bootstrap Capacitors

A bootstrap capacitor should be placed as close as practicable to each of the BSN-to-TXPN and BSP-to-TXPP pins.



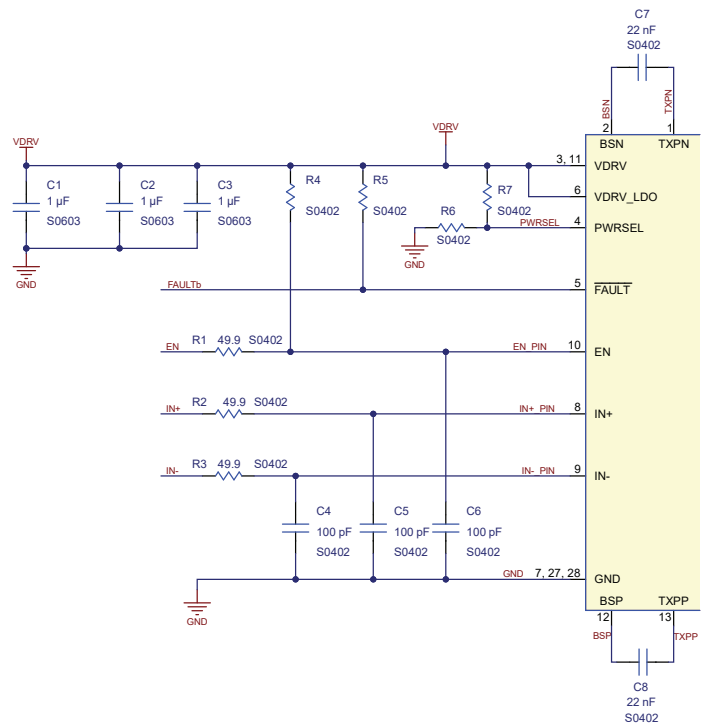
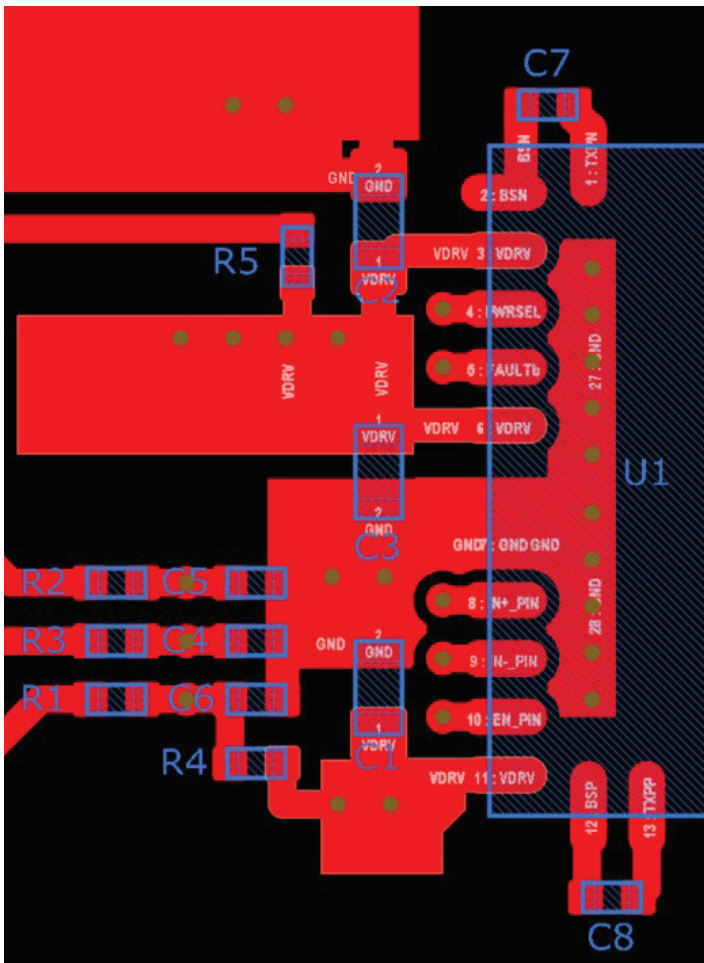
GND Plane and Thermal Management

The AHV85311 is manufactured in a quad-flat no-lead (QFN) package. The primary method of thermal management is conduction through the GND plane, primarily through the exposed pads (pins 27 and 28). Internal layers should be used for GND planes with vias connected directly to the exposed pads (pins 27 and 28). To avoid parasitic capacitance to the BSP and BSN pads, copper plane cutouts should be employed under these pads. VDRV should also be connected from the system supply to the VDRV decoupling paths. Low-impedance copper planes should be used for these connections.



Signal Connections

The remaining primary-side connections are signal-interface connections to the system controller. While these connections are of lower priority than the previously discussed connections, it is important that these signals are not corrupted with noise. High-frequency, resistor-capacitor (RC) filters should be employed as shown. Good signal-layout practices should be observed.



SECONDARY SIDE

Decoupling

As with the primary side, good decoupling of the secondary-side bias voltages is critical for correct device operation.

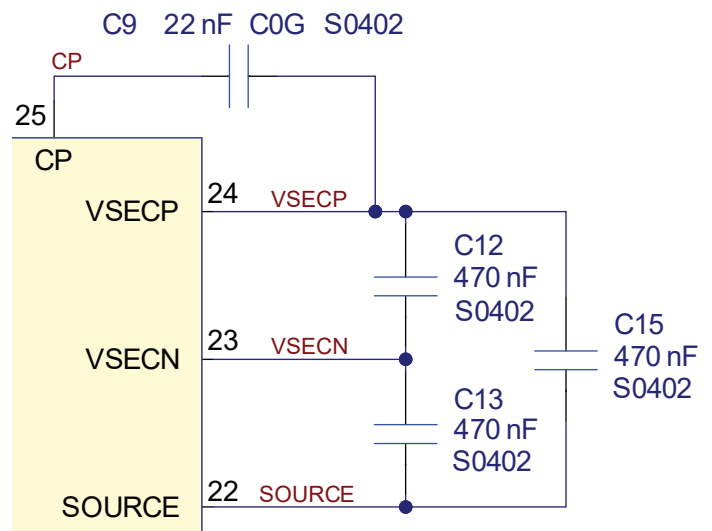
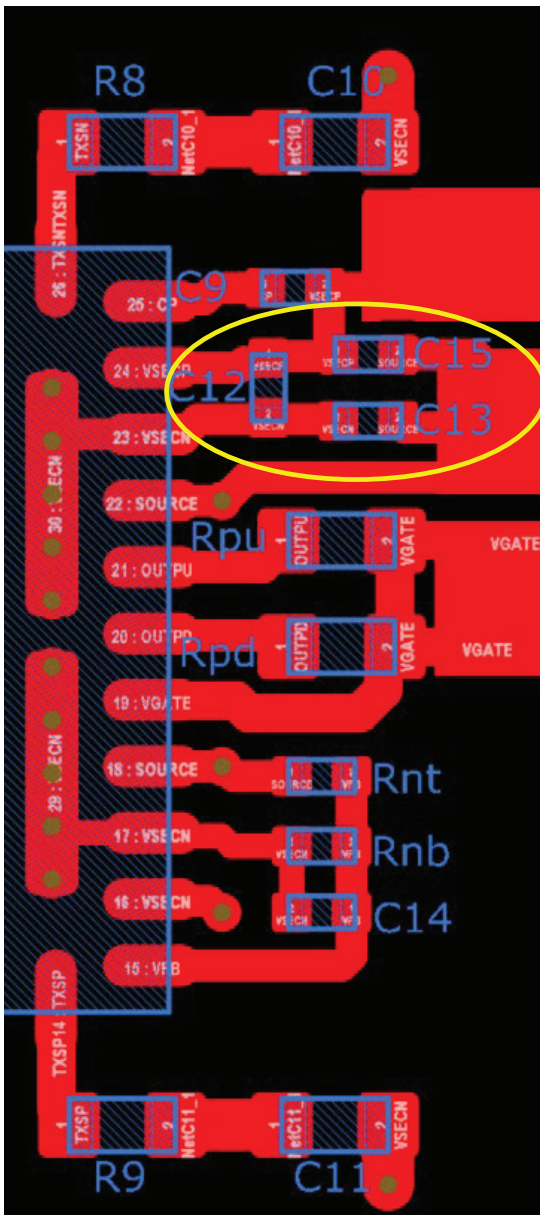
- For designs that use a negative VSECN voltage, three decoupling capacitors are used:
 - VSECP to VSECN: C12
 - VSECP to SOURCE: C15
 - VSECN to SOURCE: C13
- For designs that use VSECN = 0 V, only C12 is required.

For details, see the datasheet.

Decoupling capacitor placement should be as follows:

- The VSECP-to-VSECN capacitor (C12) should be placed as close as practicable to pins 23 and 24, as shown.
- The VSECP-to-SOURCE capacitor (C15) and the VSECN-to-SOURCE capacitor (C13) should be placed close to C12.

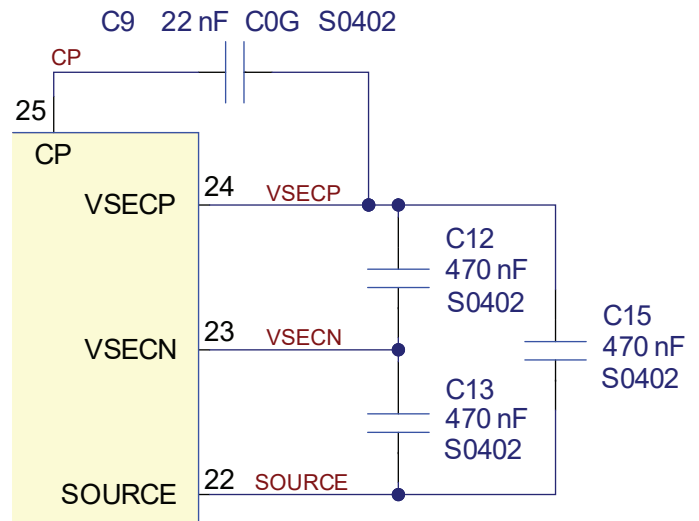
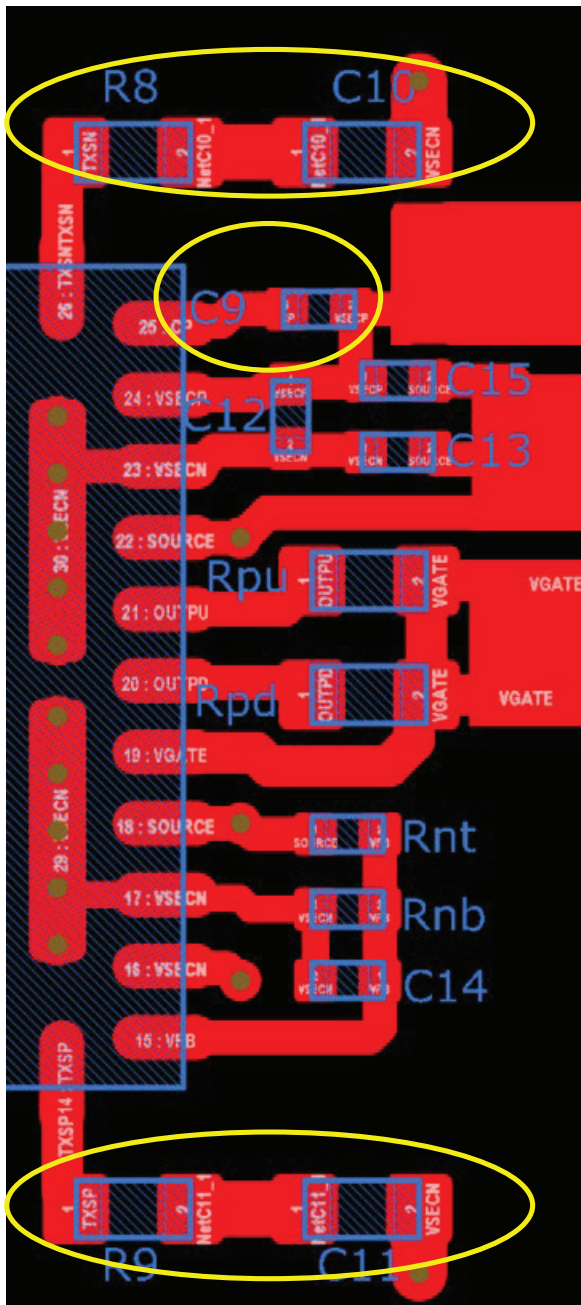
Any decoupling capacitor used should be a good-quality (i.e., X7R or better) ceramic capacitor with a voltage rating that is adequate for the VSECP-to-VSECN voltage used. The recommended value is 470 nF.



Charge-Pump Capacitor

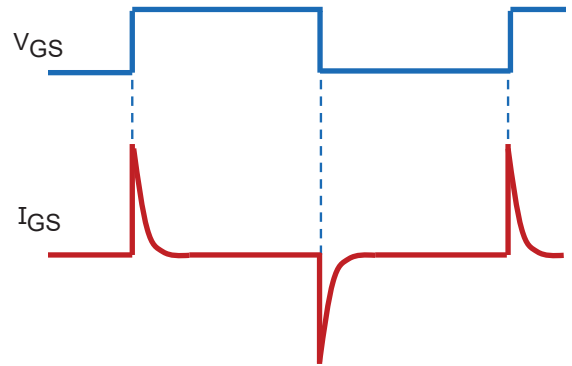
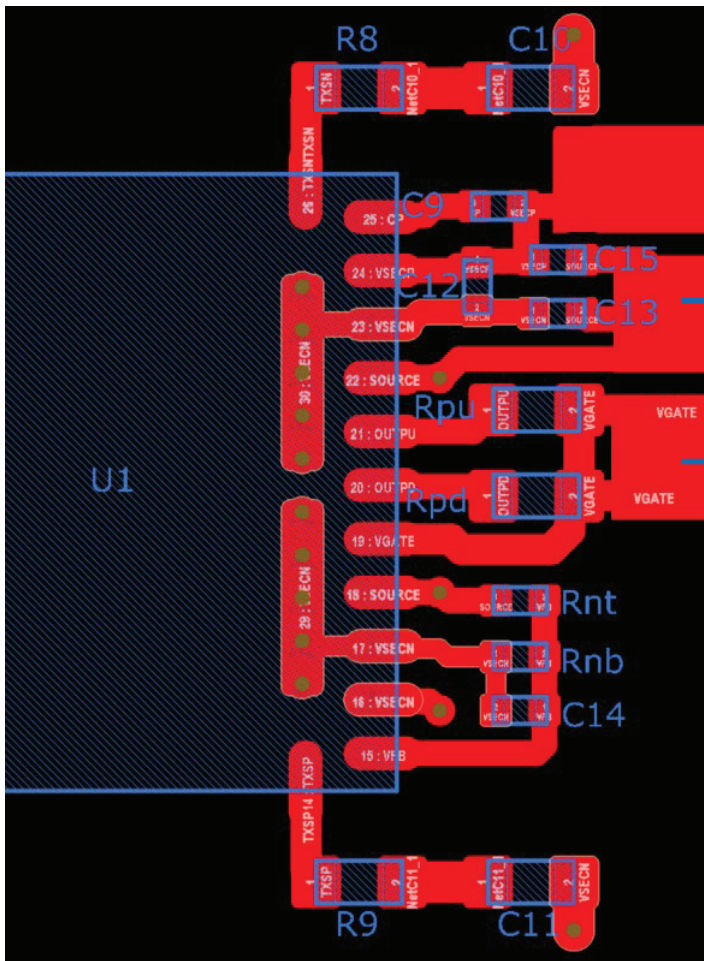
The charge-pump capacitor (C9) should be placed as close as practicable to pins 24 and 25, such that a low-impedance loop area is created.

For designs that require an RC snubber from TXSP to VSECN (C11/R9), and from TXSN to VSECN (C10/R8), these snubbers should be placed close to the TXSP or TXSN pins with a low-impedance return to VSECN.



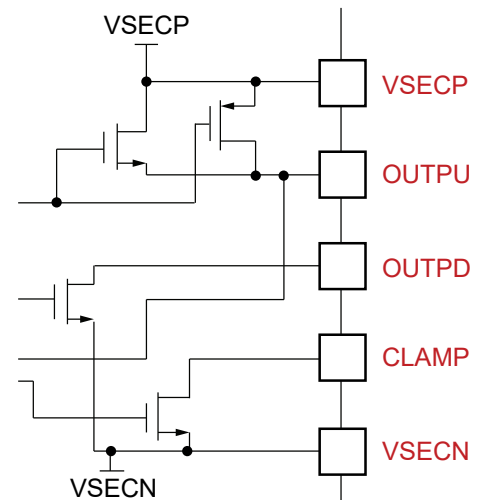
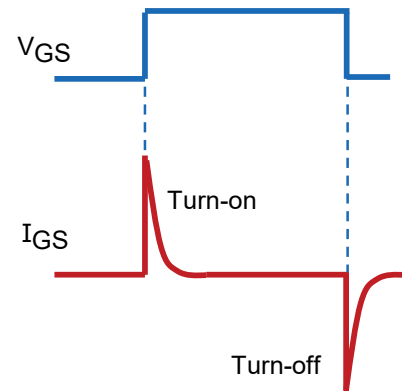
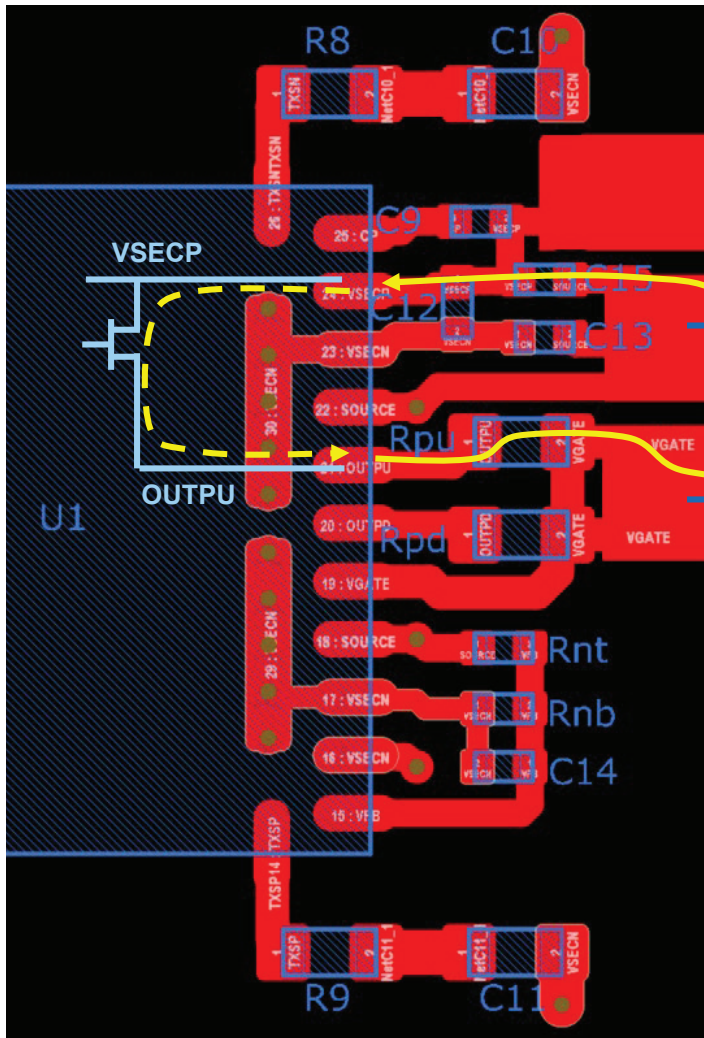
Gate-Drive Loop

FET turn-on and turn-off results in very-short-duration (~10 ns) surges of gate current, as shown. These current peaks can be several amperes, and they flow through the decoupling capacitors. PCB layout of the gate-drive loop is critical and should be implemented with low-impedance, low-inductance traces between the gate driver and the driven FET to avoid any $L \times di/dt$ voltage drops. Furthermore, the gate-drive resistors should be suitably rated for surge currents.



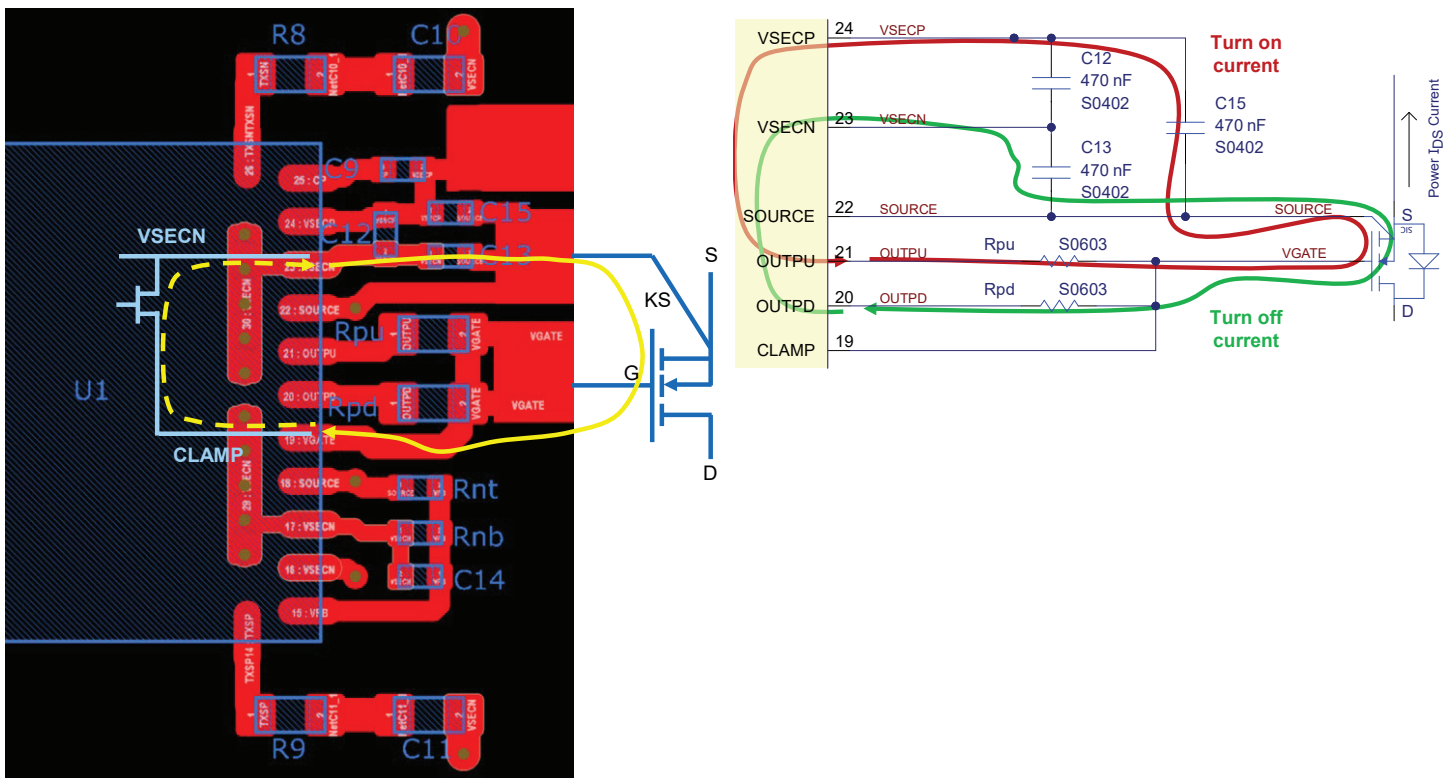
Gate-Drive Loop—Turn On

During the turn-on period, the FET gate is charged through OUTPUT. The gate-surge current flows in the VSECP-to-SOURCE decoupling capacitor (C15), as shown. Therefore, a low-impedance path from the FET kelvin source to C15 is critical.



Gate-Drive Loop—Miller Clamp

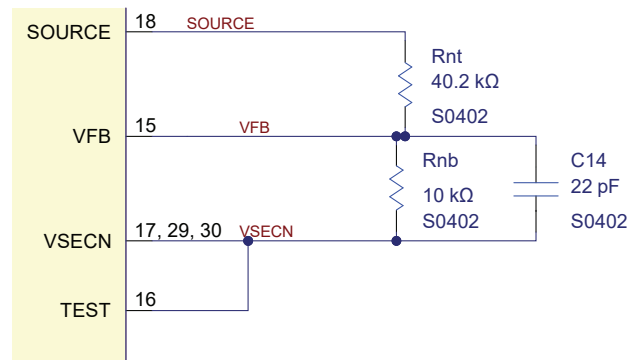
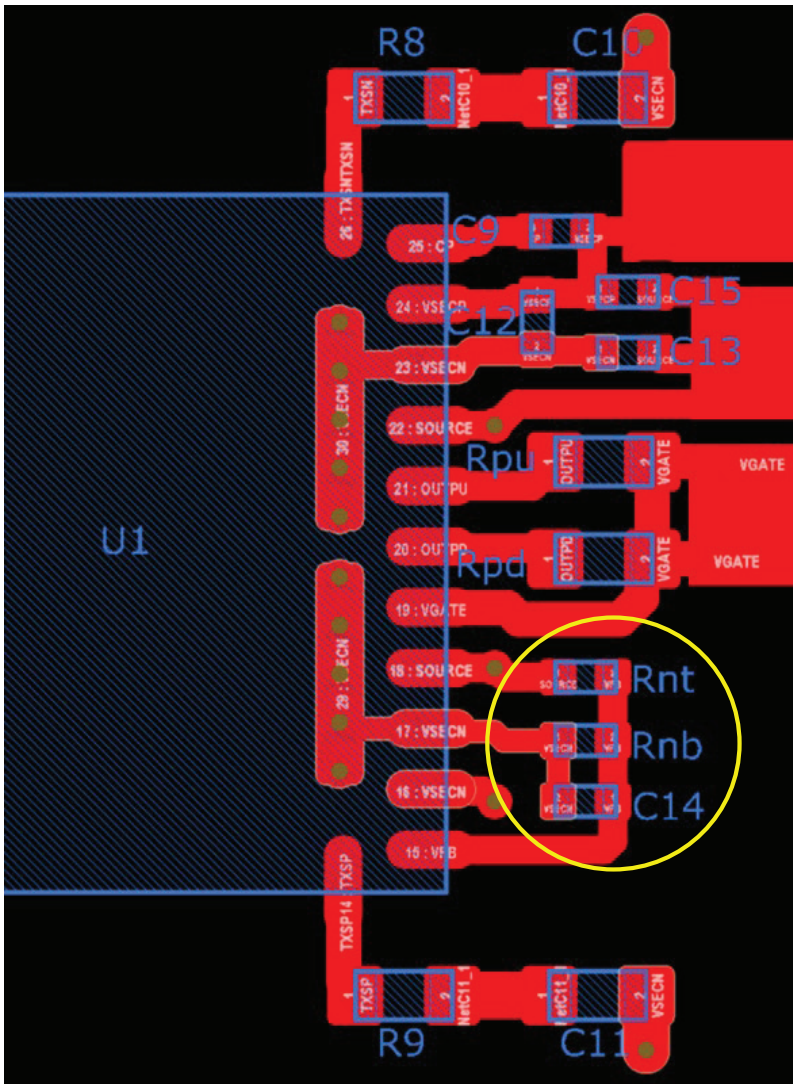
The Miller clamp pin operates similarly to the typical turn-off operation. The connection from the CLAMP pin to the FET gate should be of the lowest-impedance practicable.



VSECN Setting Network

The AHV85311 driver allows for programming of the negative off-voltage VSECN with two resistors. For details, see the product datasheet. These resistors should be placed close to the driver. To avoid noise coupling into the feedback network, these resistors should be isolated from traces that carry large driver-switching current. A high-frequency compensation capacitor (C14) with a recommended value of 22 pF should be placed close to Rnb.

For designs where $VSECN = 0$ V, these components are omitted and VSECN, VFB, and SOURCE are connected together. The test pin, 16, must be connected to VSECN and should not be left floating.



Revision History

Number	Date	Description
–	November 17, 2025	Initial release

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