

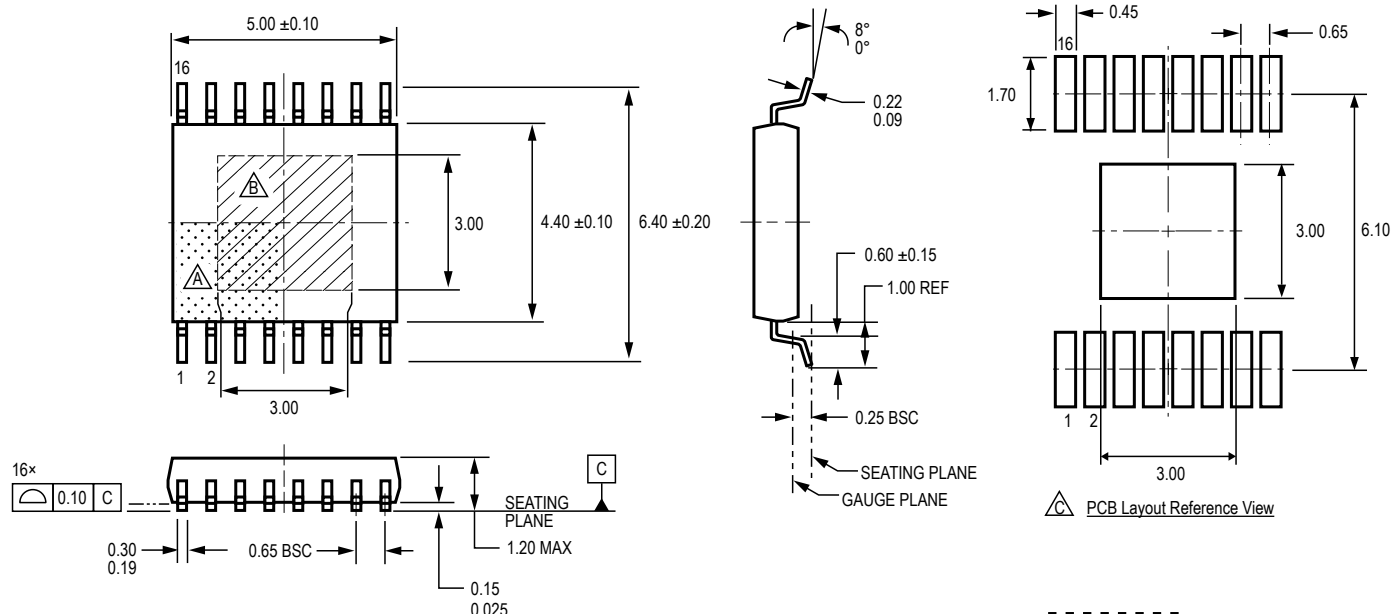
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


(Reference JEDEC MO-153 ABT; Allegro DWG-0000379, Rev. 3)


Dimensions in millimeters – NOT TO SCALE

Dimensions exclusive of mold flash, gate burrs, and dambar protrusions

Exact case and lead configuration at supplier discretion within limits shown



-  Terminal #1 mark area
-  Exposed thermal pad (bottom surface)
-  Reference land pattern layout (reference IPC7351 SOP65P640X110-17M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)
-  Branding scale and appearance at supplier discretion

-  **Standard Branding Reference View**
- Line 1, 2 = 7 characters
- Line 3 = 5 characters
- Line 1: Part Number
- Line 2: Logo A, 4 digit Date Code
- Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

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