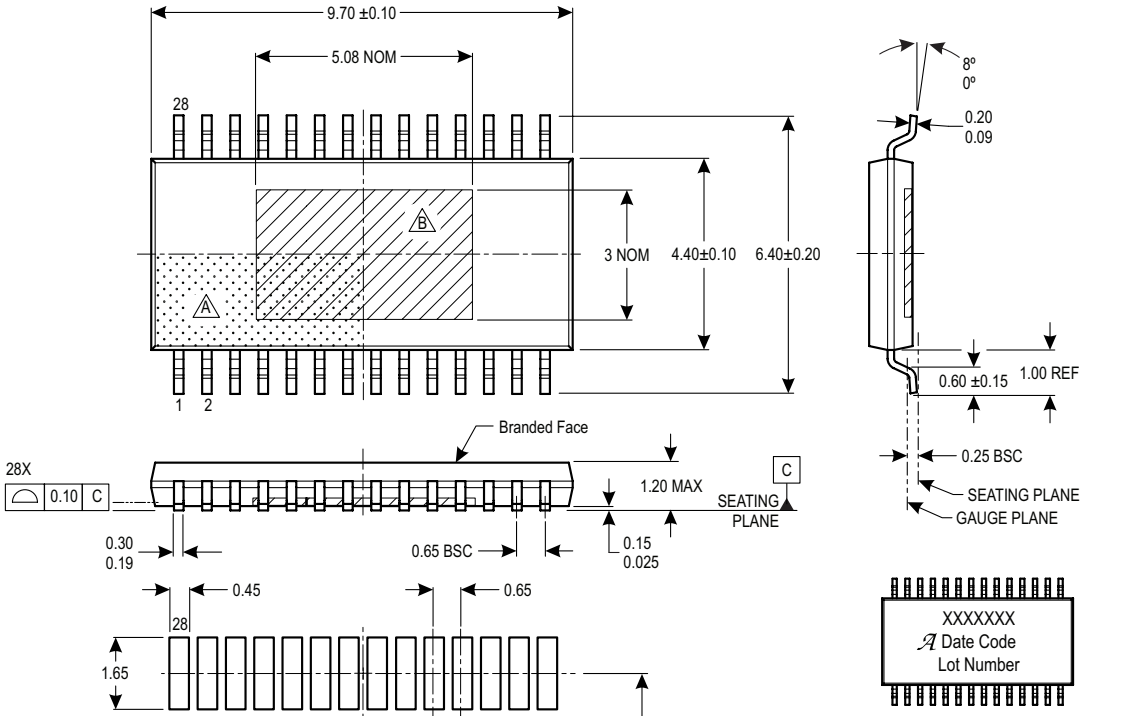
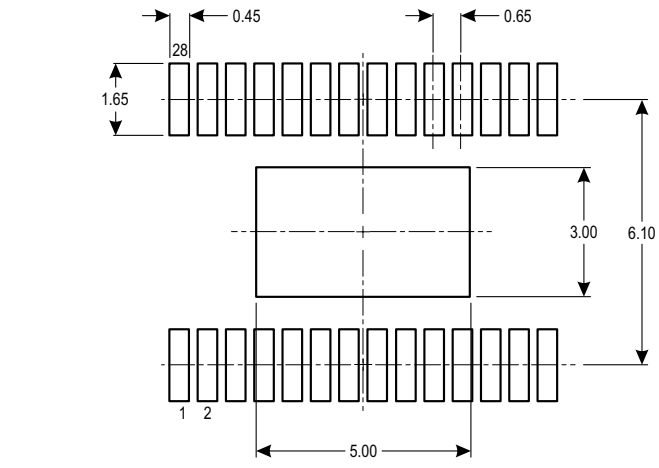
Package Drawing

Designator: LP
Type: 28-pin eTSSOP

For Reference Only – Not for Tooling Use
(Reference Allegro DWG-0000379, Rev. 3 and JEDEC MO-153AET)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown





C Reference PCB Layout Reference View

E Standard Branding Reference View

Lines 1, 2, 3 = 10 characters

Line 1: Part Number
Line 2: Logo A, 4-digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOP65P640X120-29CM); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Branding scale and appearance at supplier discretion.

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