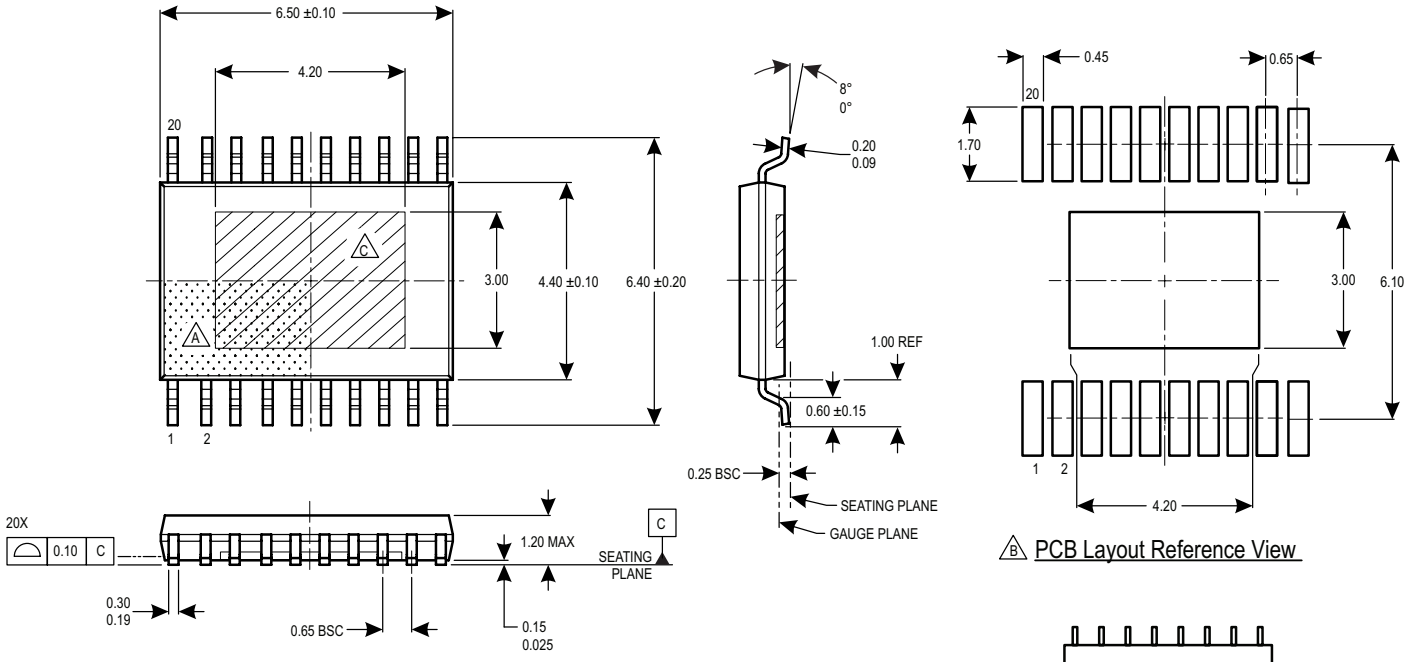
Package Drawing

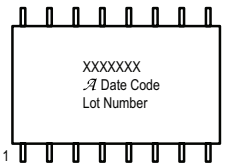
Designator: LP
Type: 20-pin eTSSOP

For Reference Only – Not for Tooling Use

(Reference JEDEC MO-153ACT; Allegro DWG-0000379, Rev. 3)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



B PCB Layout Reference View



D Standard Branding Reference View

Line 1, 2, 3 = 8 characters

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 SOP65P640X110-21M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Exposed thermal pad (bottom surface)

D Branding scale and appearance at supplier discretion

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