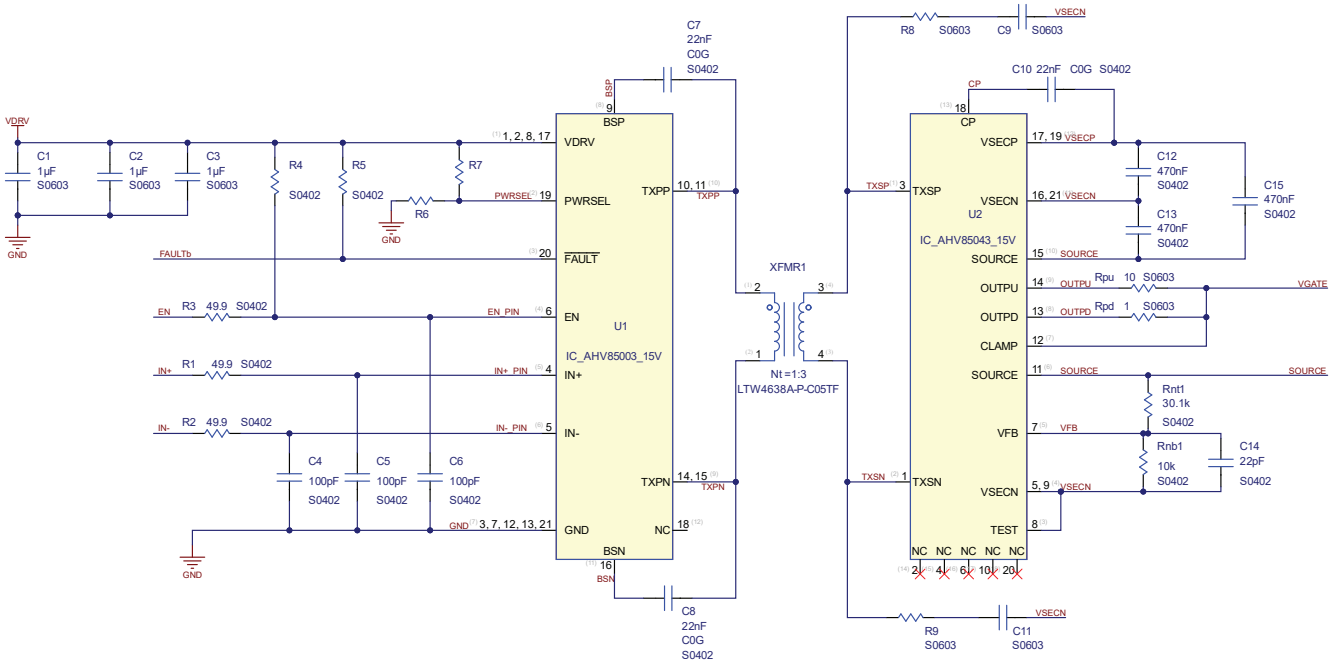
OVERVIEW

The purpose of this document is to provide printed-circuit-board (PCB) layout guidelines for the correct operation of the AHV85003 and AHV85043 external-transformer gate-driver chipset.

The guidelines in this document are presented in order of priority for both the primary side and the secondary side. Failure to adhere to these guidelines may result in incorrect operation or suboptimal performance of the AHV85003 and AHV85043 driver chipset.



Typical Schematic

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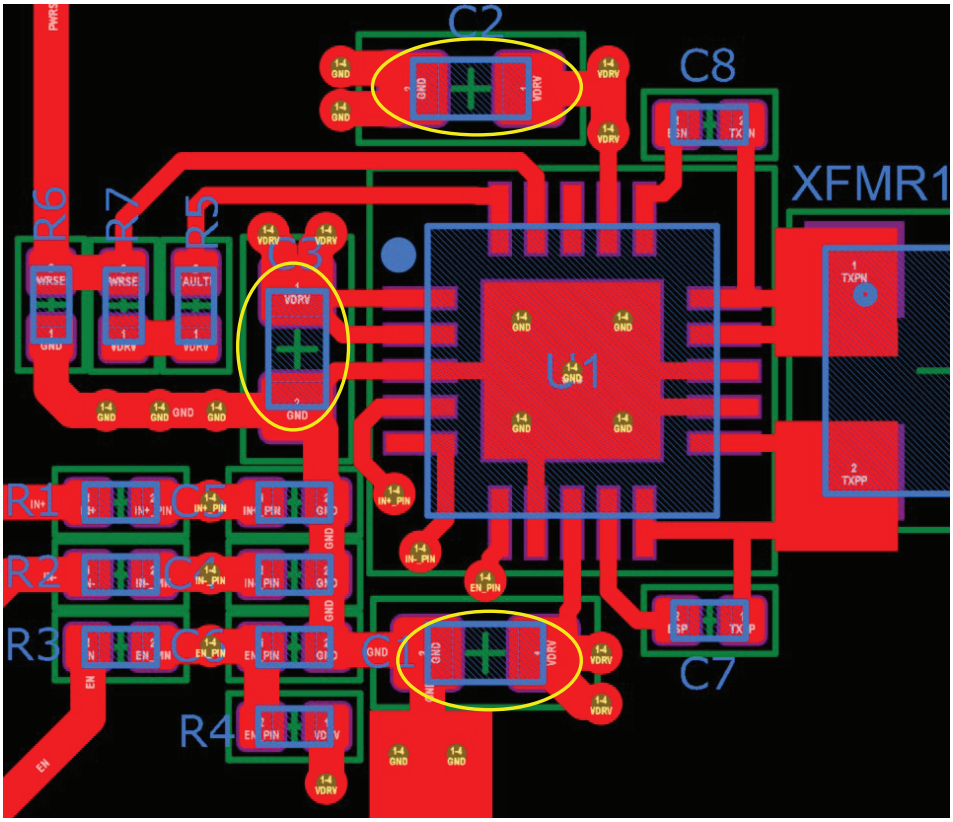
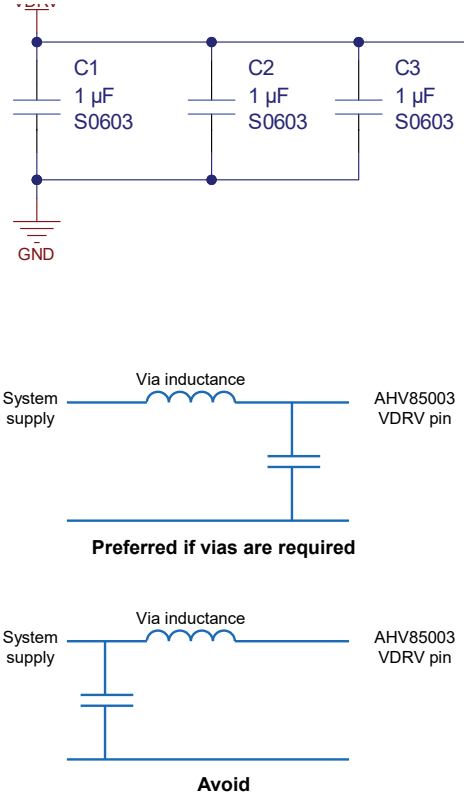
PRIMARY SIDE

VDRV Decoupling

Correct VDRV decoupling is critical for correct device operation. The minimum requirement is one 1 µF capacitor per VDRV pin. The preferred decoupling is 1 µF in parallel with 100 nF on each VDRV pin. A decoupling capacitor should be a good-quality (i.e., X7R or better) ceramic capacitor with an adequate voltage rating (i.e., at least 25 V). GND and VDRV should be routed with copper planes on internal layers. Between any decoupling capacitor and pin, via use should be avoided.





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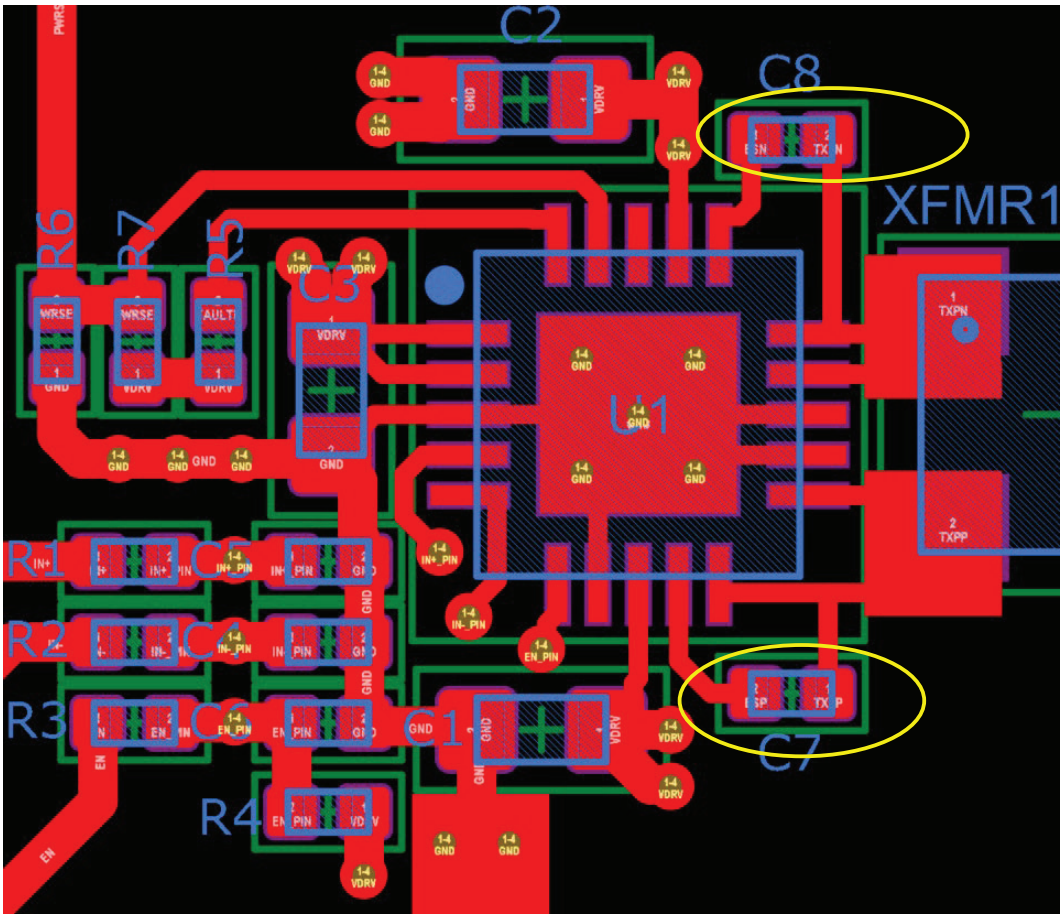
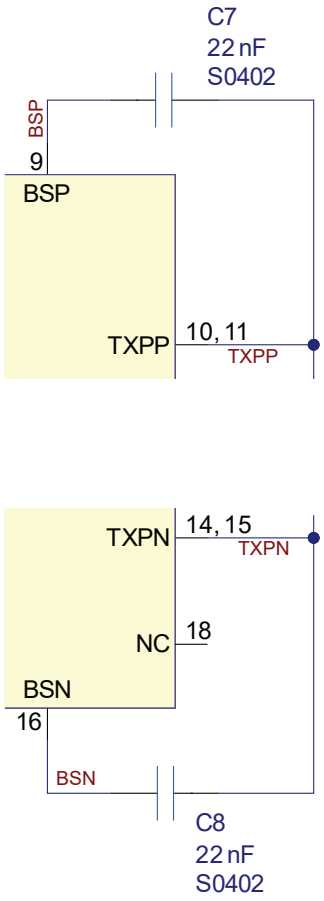
Bootstrap Capacitors

A bootstrap capacitor should be placed as close as practicable to each of the BSN-to-TXPN and BSP-to-TXPP pins.





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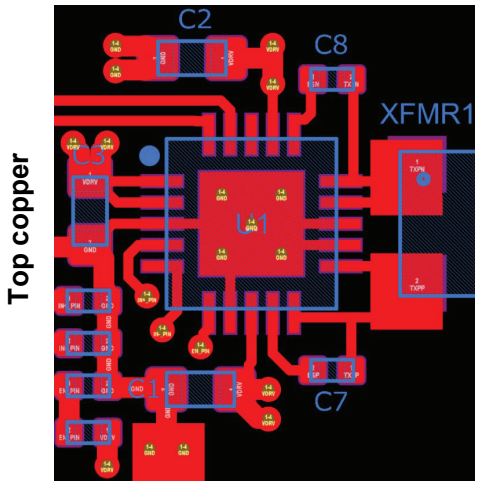
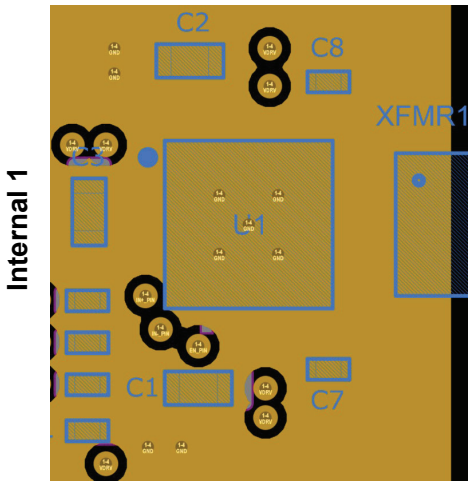
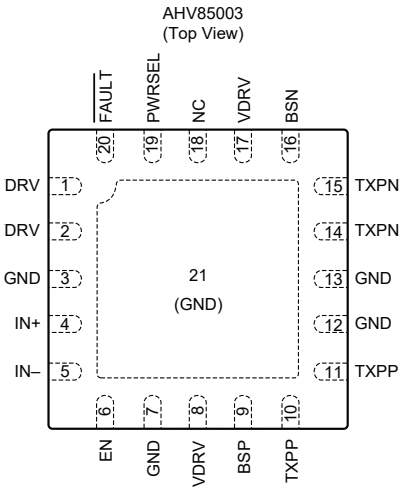
GND Plane and Thermal Management

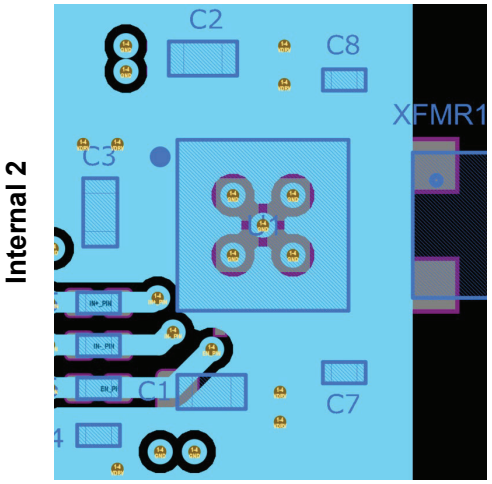
The AHV85003 is manufactured in a quad-flat no-lead (QFN) package. The primary method of thermal management is conduction through the GND plane, primarily through the exposed pad (pin 21). Internal layers should be used for GND planes with vias connected directly to the exposed pad (pin 21). VDRV should also be connected from the system supply to the VDRV decoupling paths. Low-impedance copper planes should be used for these connections.



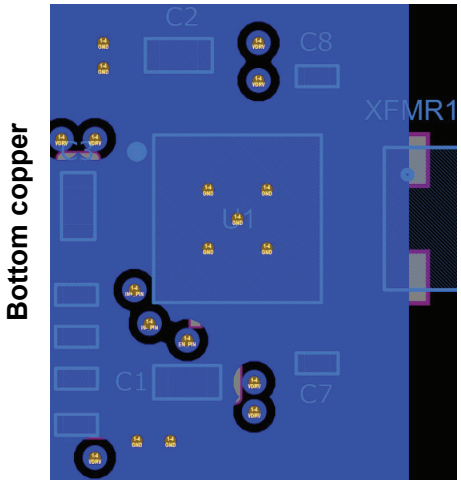


GND PLANE

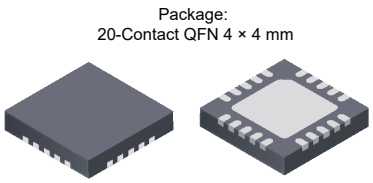




VDRV PLANE



GND PLANE



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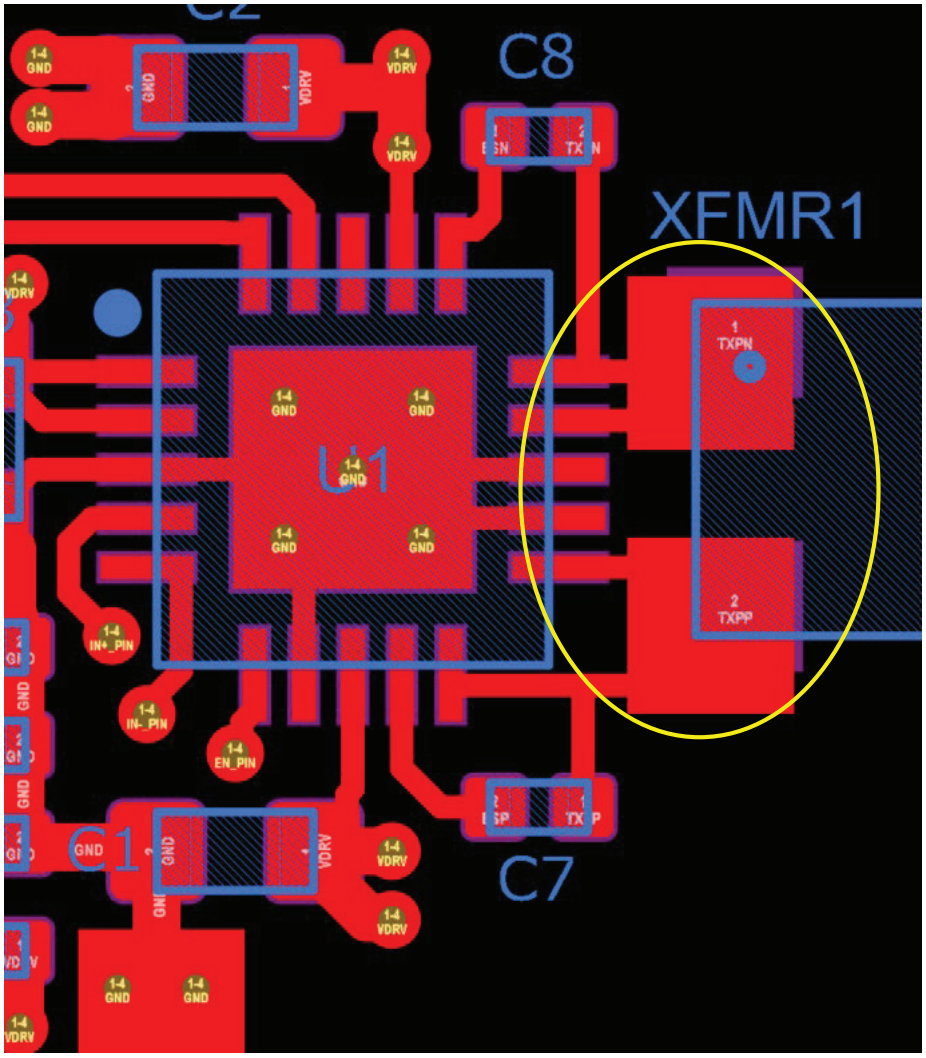
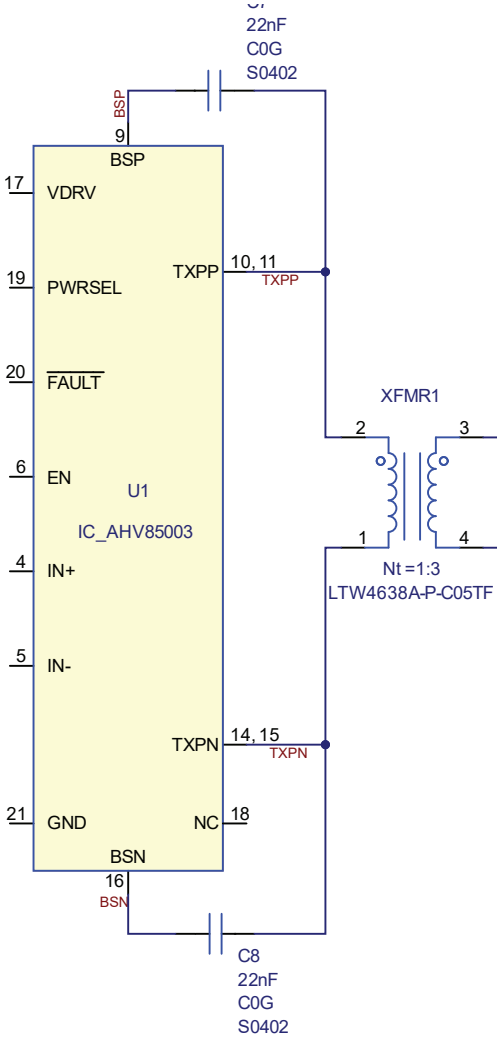
Transformer Primary

The transformer should be placed close to the IC, and low-impedance tracks should be used.





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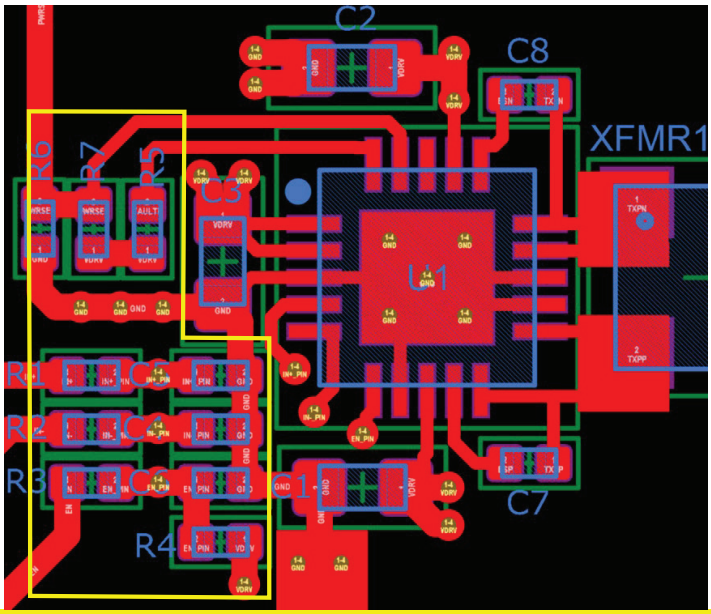
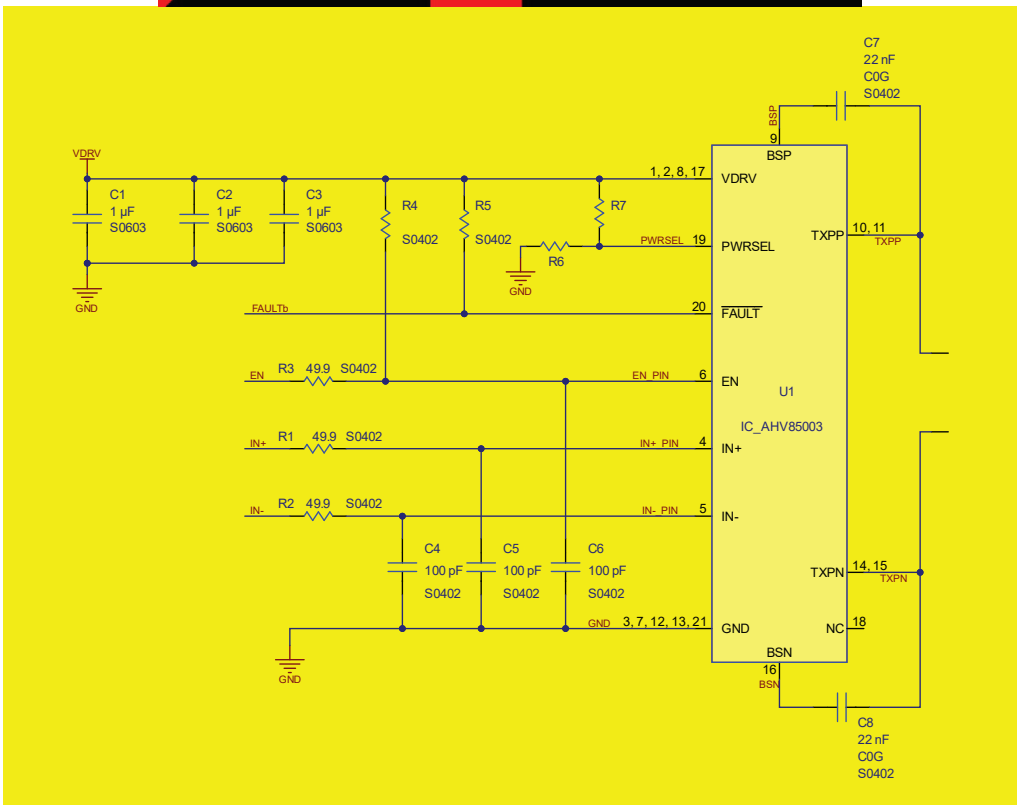
Signal Connections

The remaining primary-side connections are signal-interface connections to the system controller. While these connections are of lower priority than the previously discussed connections, it is important that these signals are not corrupted with noise. High-frequency, resistor-capacitor (RC) filters should be employed as shown. Good signal-layout practices should be observed.





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SECONDARY SIDE

Decoupling

As with the primary side, good decoupling of the secondary-side bias voltages is critical for correct device operation.

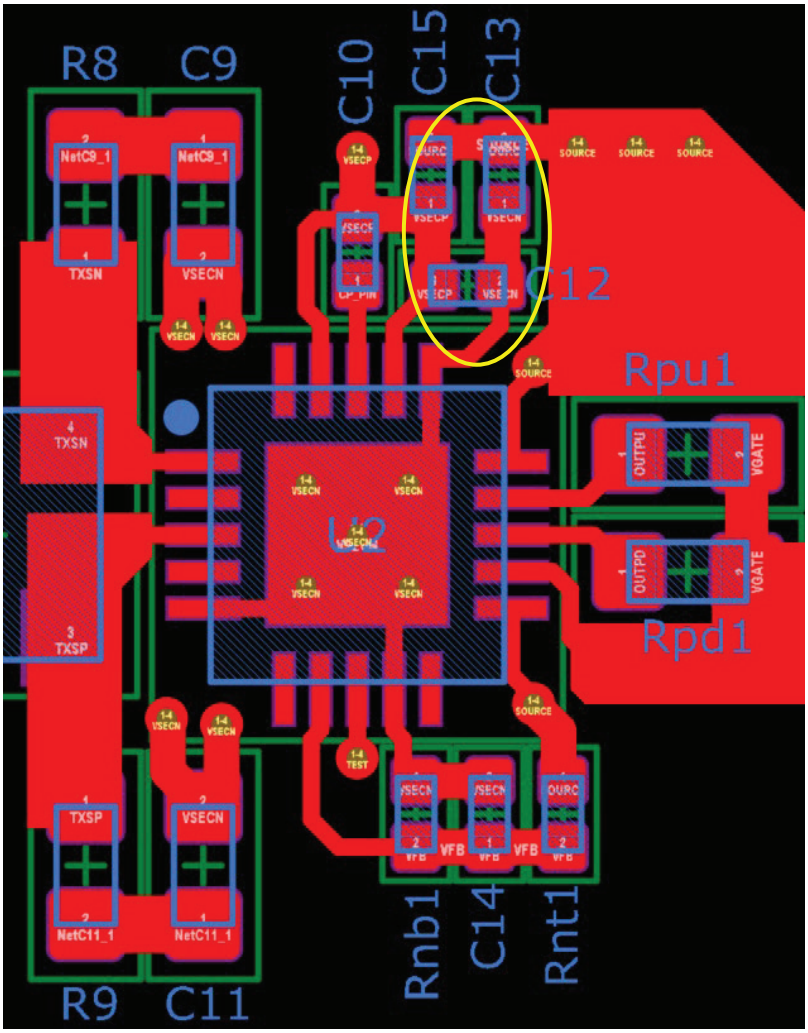
- For designs that use a negative VSECN voltage, three decoupling capacitors are used:
  - □ VSECP to VSECN: C12
  - □ VSECP to SOURCE: C15
  - □ VSECN to SOURCE: C13
- For designs that use VSECN = 0 V, only C12 is required.

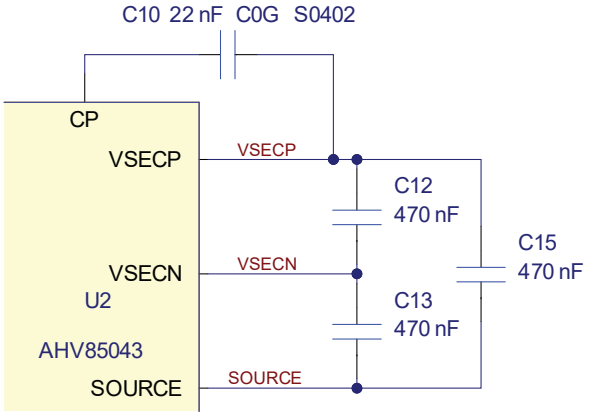
For details, see the datasheet.

Decoupling capacitor placement should be as follows:

- The VSECP-to-VSECN capactior (C12) should be placed as close as practicable to pins 16 and 17, as shown.
- The VSECP-to-SOURCE capacitor (C15) and the VSECN-to-SOURCE capacitor (C13) should be placed close to C12.

Any decoupling capacitor used should be a good-quality (i.e., X7R or better) ceramic capacitor with a voltage rating that is adequate for the VSECP voltage used. The recommended value is 470 nF.





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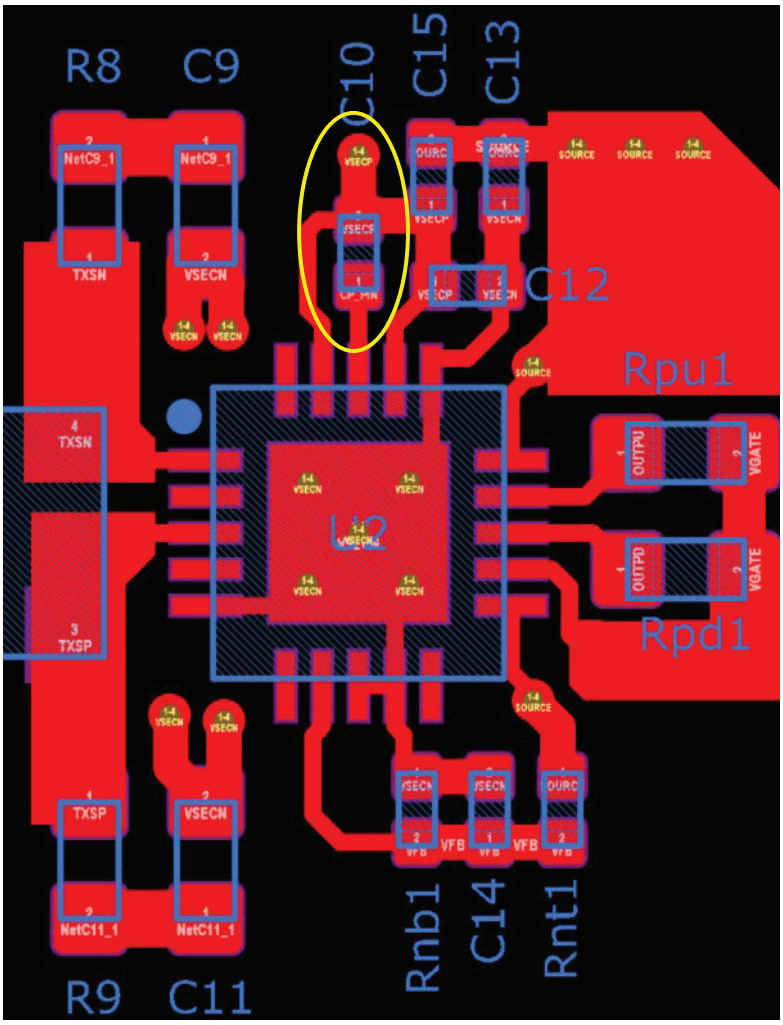
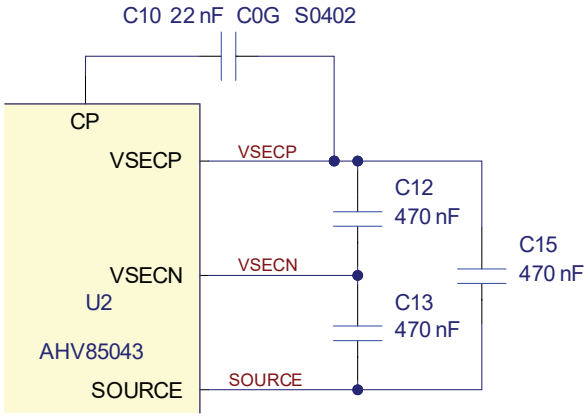
Charge-Pump Capacitor

The charge-pump capacitor should be placed as close as practicable to pins 18 and 19, such that a low-impedance loop area is created.





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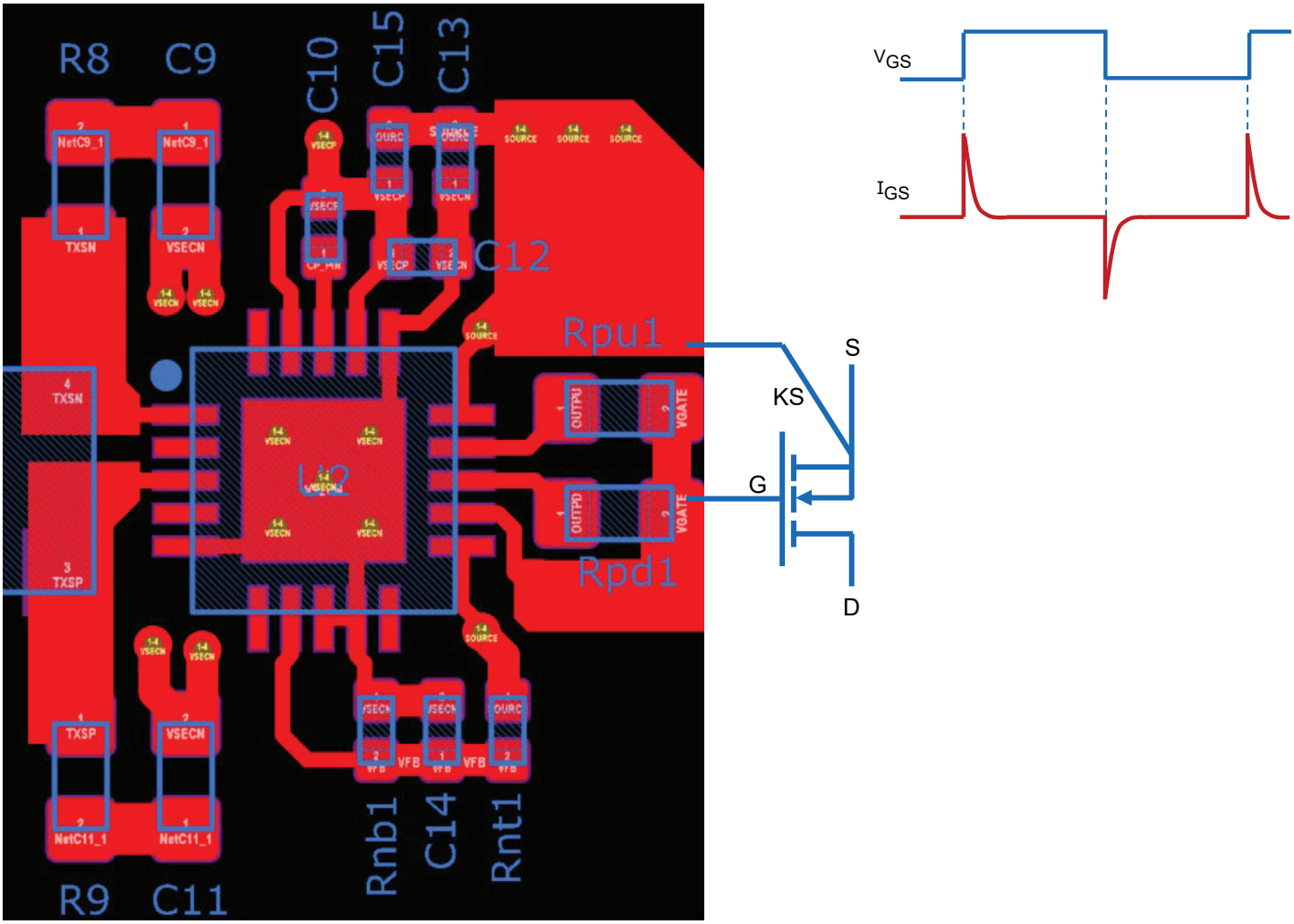
Gate-Drive Loop

FET turn-on and turn-off results in very-short-duration (~10 ns) surges of gate current, as shown. These current peaks can be several amperes, and they flow through the decoupling capacitors. PCB layout of the gate-drive loop is critical and should be implemented with low-impedance, low-inductance traces between the gate driver and the driven FET to avoid any L × dI/dt voltage drops. Furthermore, the gate-drive resistors, Rpu1 and Rpd1, should be suitably rated for surge currents.



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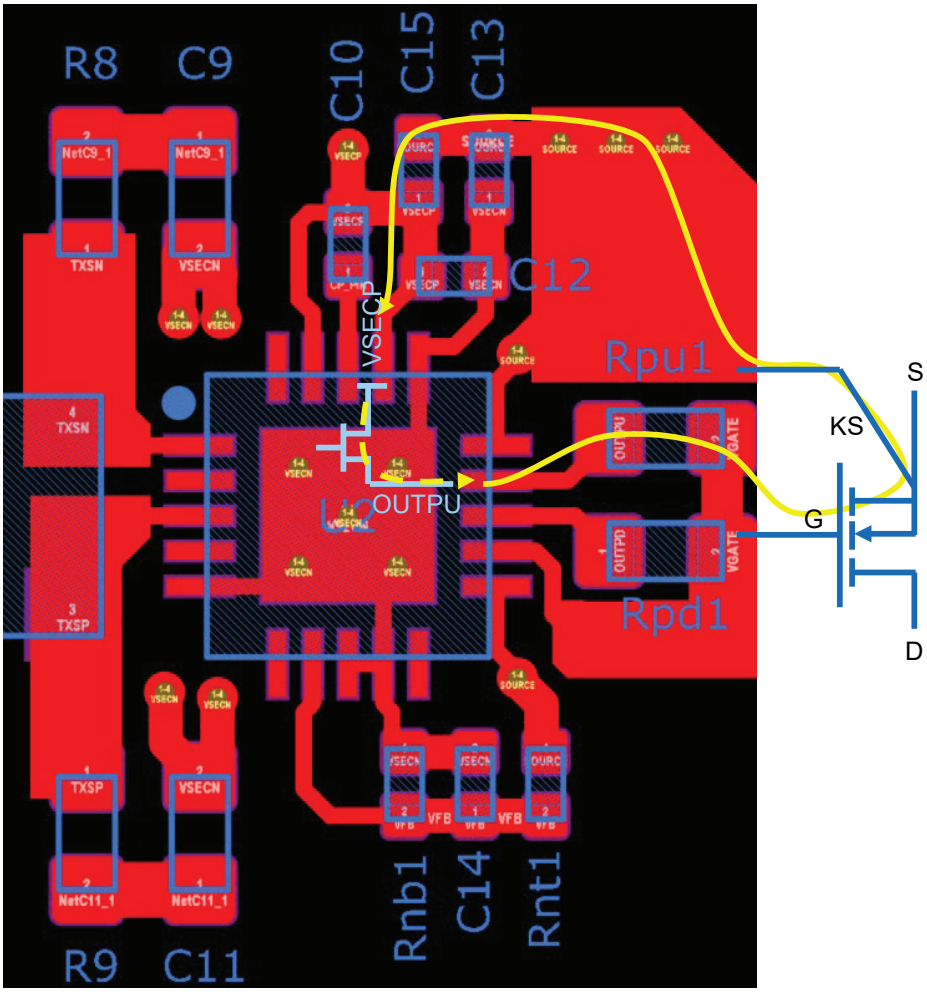
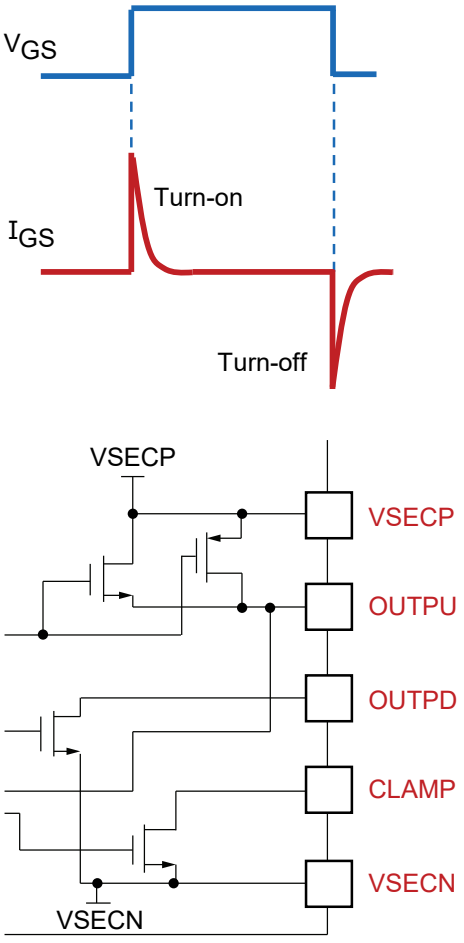
Gate-Drive Loop—Turn On

During the turn-on period, the FET gate is charged through OUTPU. The gate-surge current flows in the VSECP-to-SOURCE decoupling capacitor (C15), as shown. Therefore, a low-impedance path from the FET kelvin source to C15 is critical.





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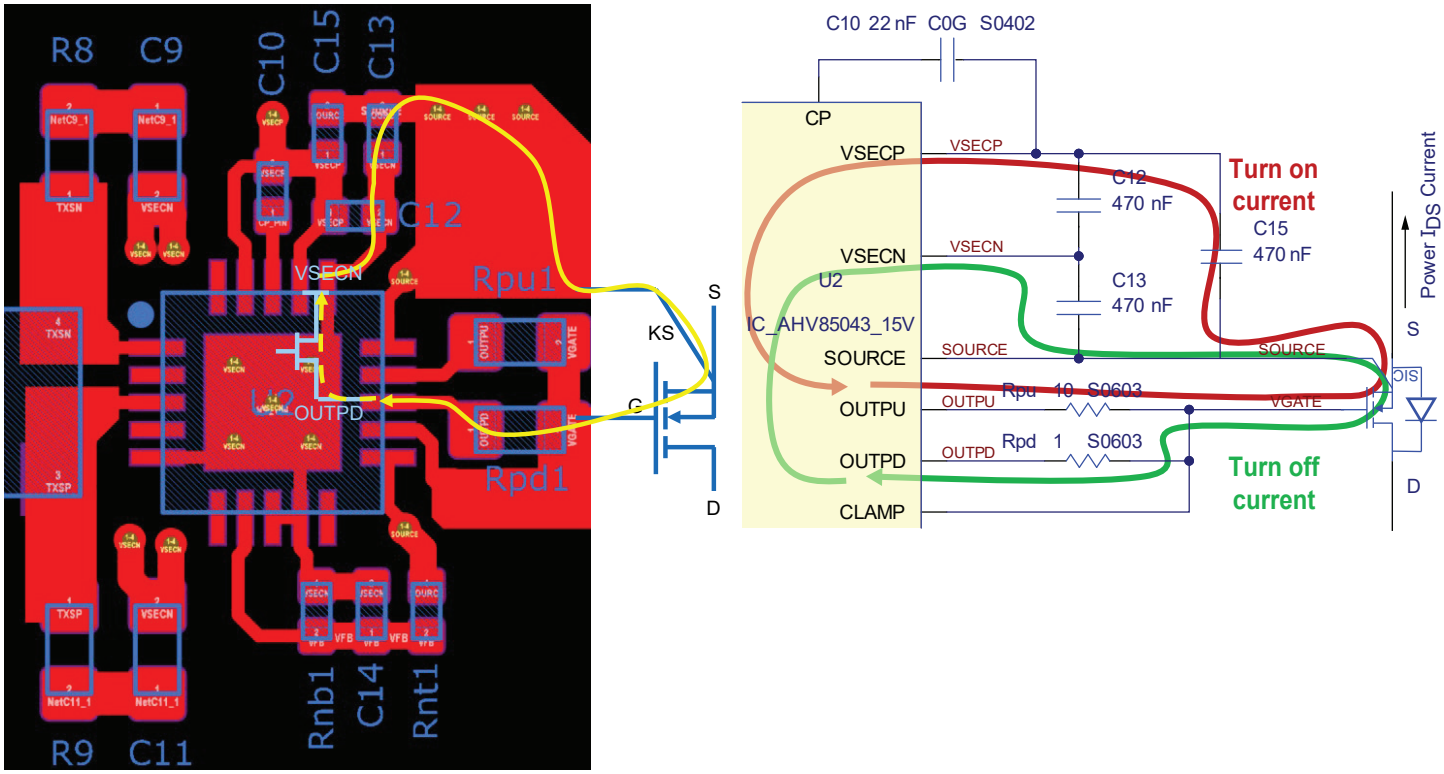
Gate-Drive Loop—Turn Off

Similar to the turn-on period, during the turn-off period, the FET gate must be discharged through the VSECN-to-SOURCE decoupling capacitor (C13). For power FETs that do not have a dedicated kelvin source (KS) pin, the source return from the power FET should be Kelvin-connected to the FET source pin such that the gate-to-source (GS) current does not interact with the FET drain-to-source (DS) current.

To optimize the source return loop, it is often best to place the source path on an internal copper plane layer, on the layer below the layer with the driver. In such cases, to reduce the series inductance, the source connection to the decoupling capacitors should use as many vias as practicable.



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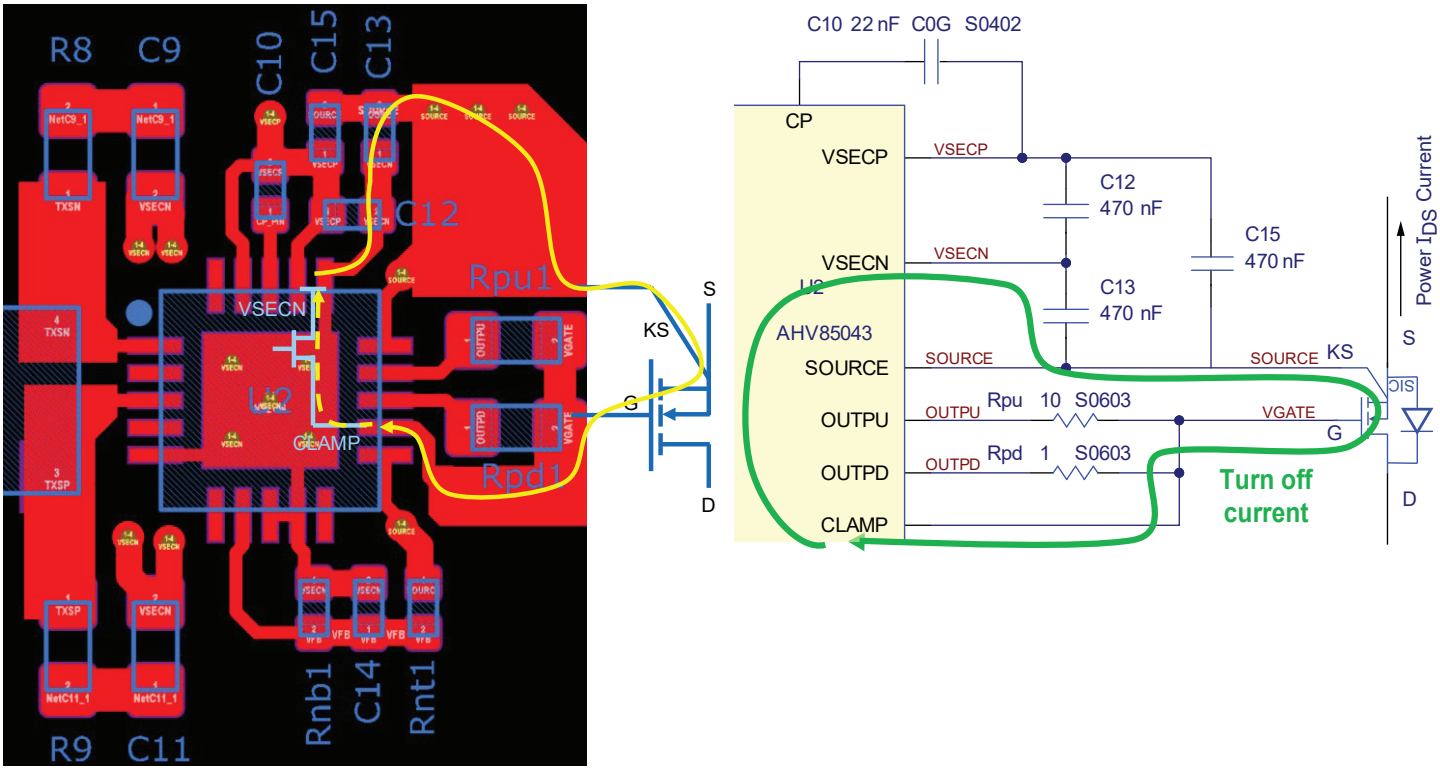
Gate-Drive Loop—Miller Clamp

The Miller clamp pin operates similarly to the typical turn-off operation. The connection from the CLAMP pin to the FET gate should be of the lowest-impedance practicable.



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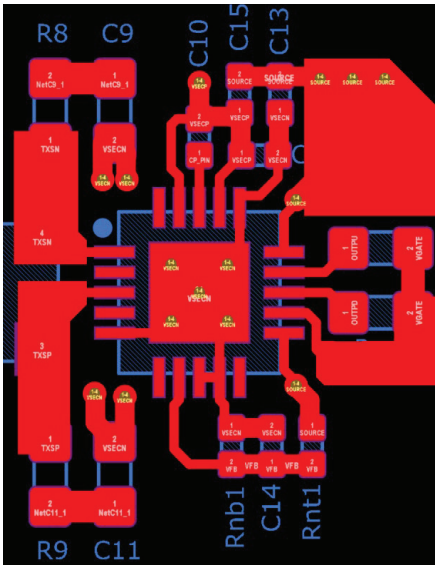
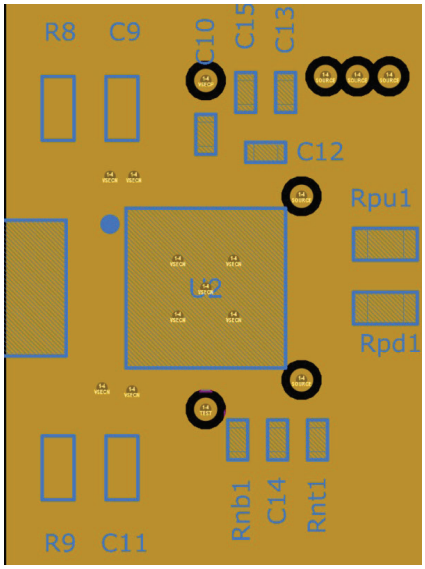
Thermal Management

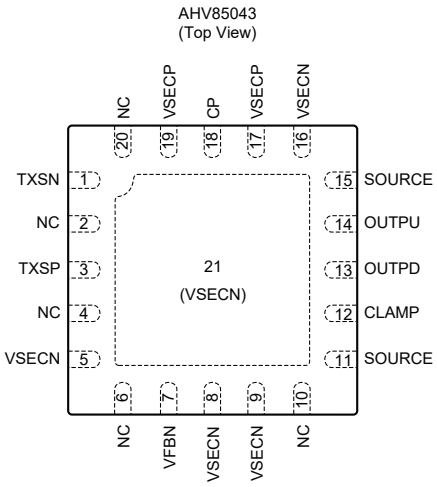
As with the primary side, the main method of thermal management in the secondary-side AHV85043 QFN is through thermal conduction from the VSECN pads—in particular, exposed pad 21. VSECN should be connected to a large copper area. Multiple vias should be used to connect pad 21 to this copper plane.

Top copper

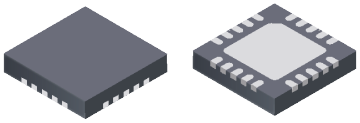


Internal 1

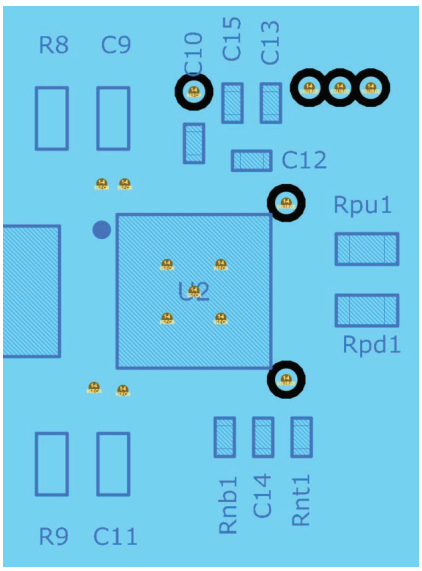




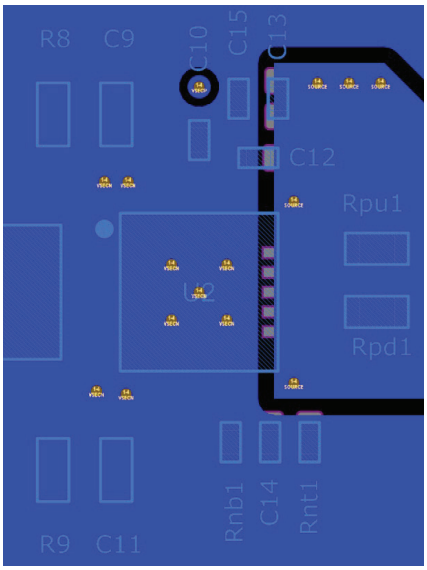
Package:
20-Contact QFN 4 × 4 mm



Internal 2



Bottom copper



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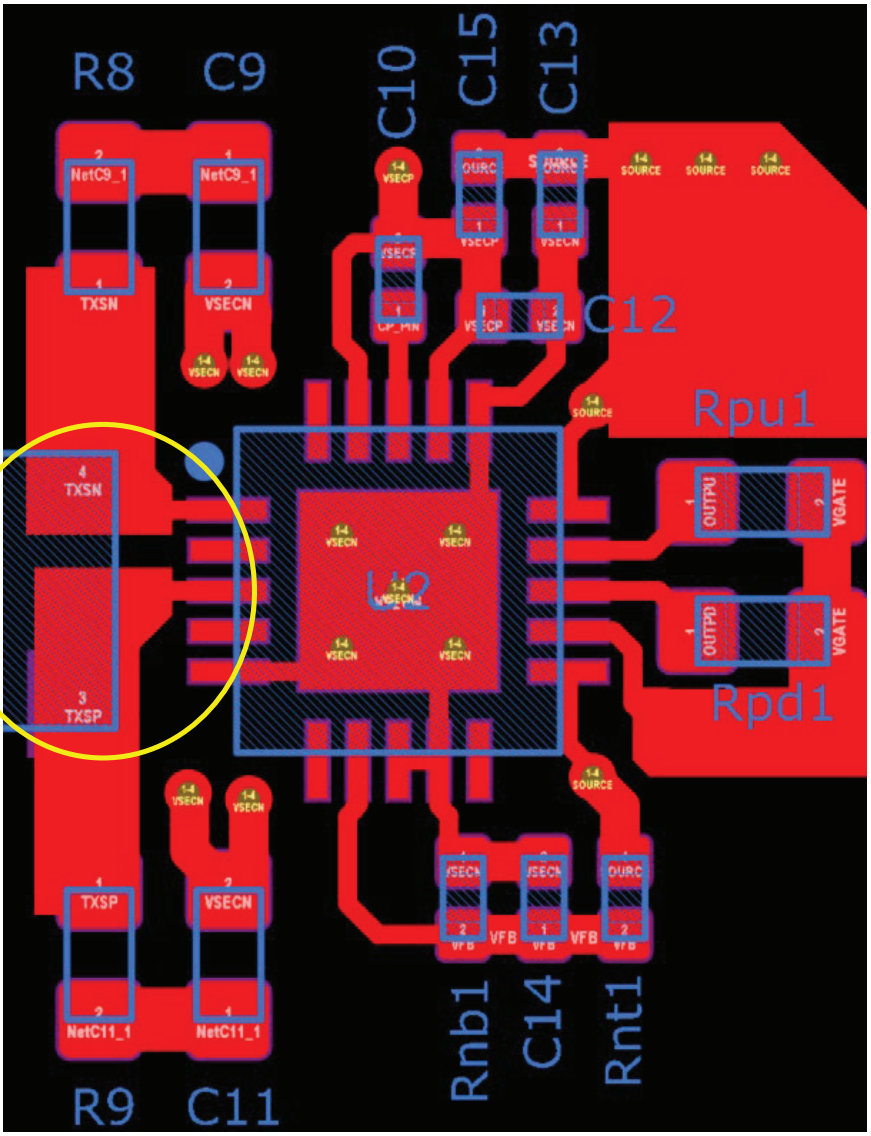
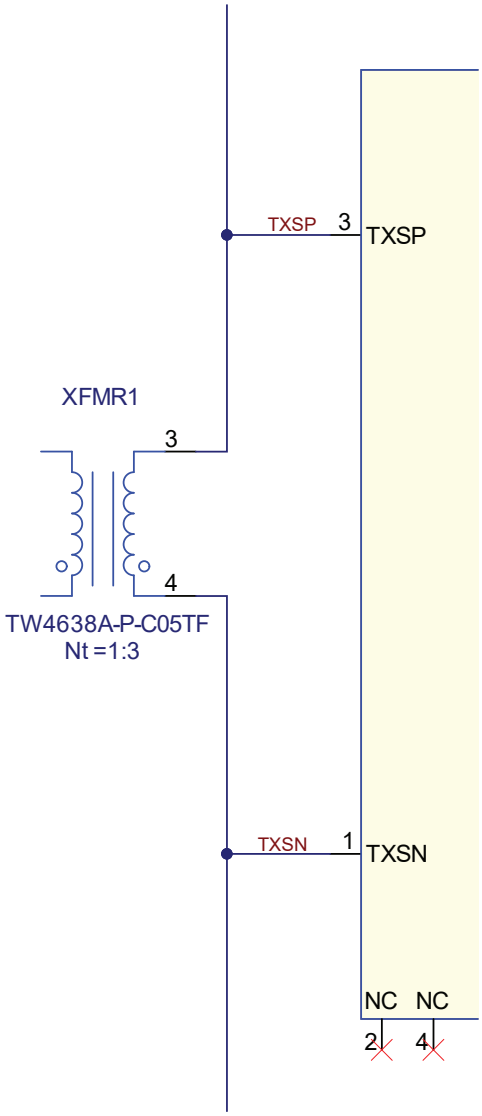
Transformer Secondary

The transformer should be placed close to the IC with low-impedance tracks.





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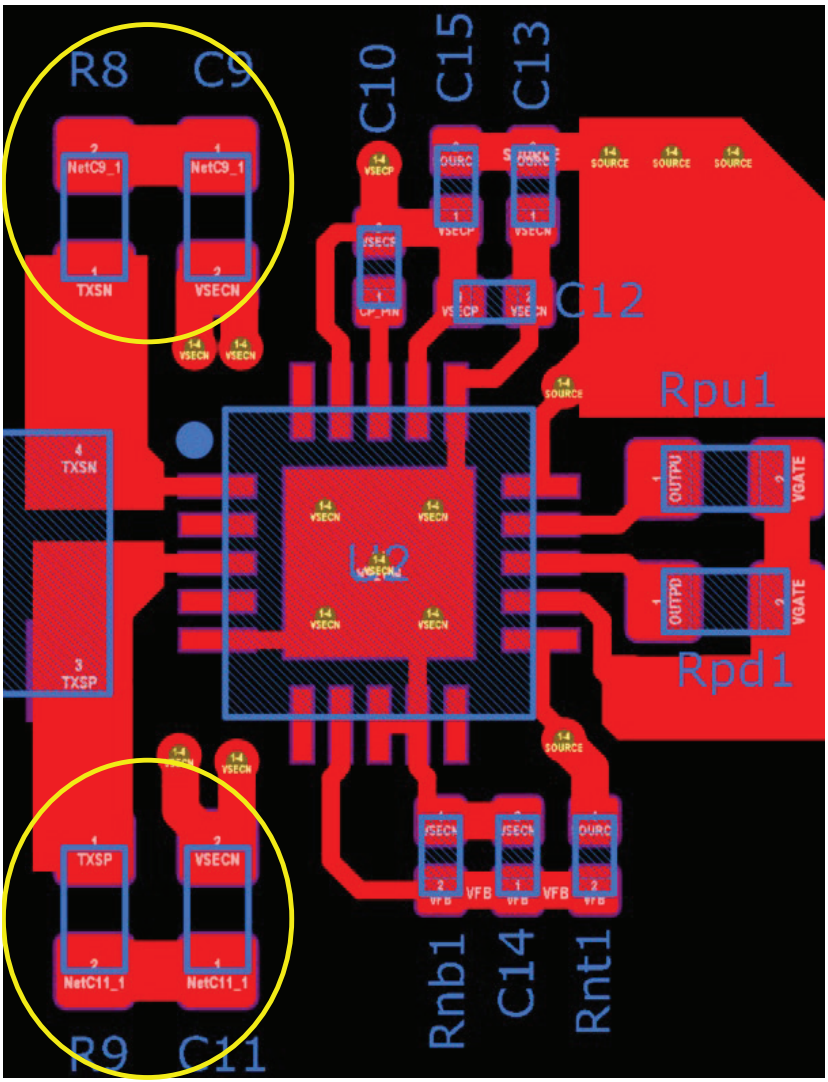
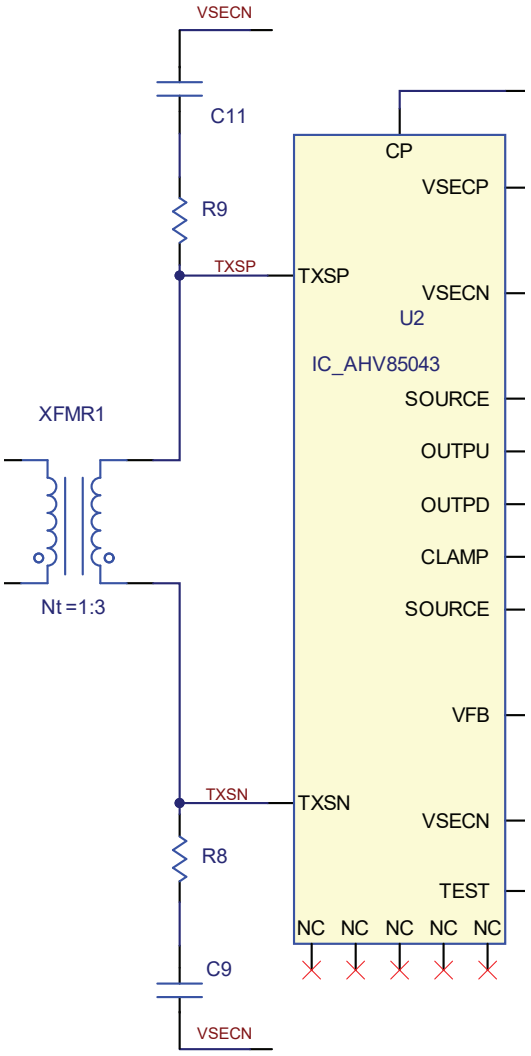
CMTI Snubbers

For designs that require additional snubbers for improved common-mode transient immunity (CMTI) performance, these components should be placed close to the transformer, and the connection to VSECN should be low-impedance. For full details see the application note AHV85003 and AHV85043 Chipset Secondary-Side Snubber for Improved CMTI Performance (AN296372). [1]





[1] https://www.allegromicro.com/-/media/files/application-notes/an296377-ahv85003-and-ahv85043-secondary-side-snubbers-for-improved-cmti-performance

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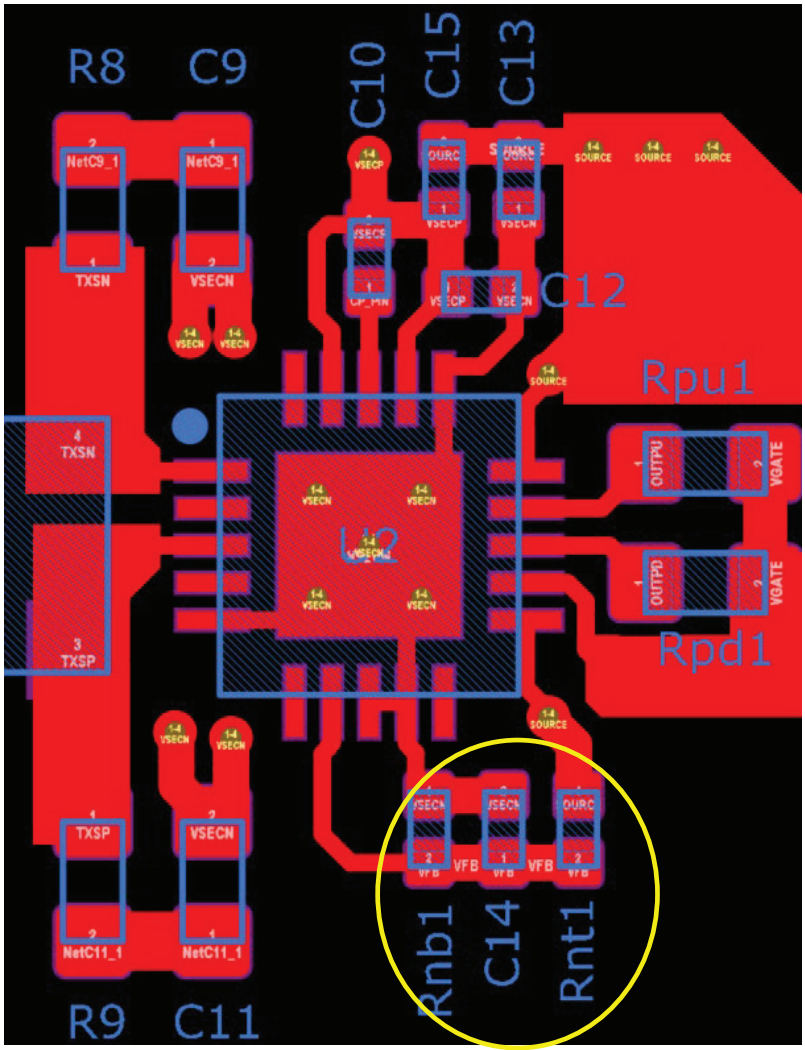
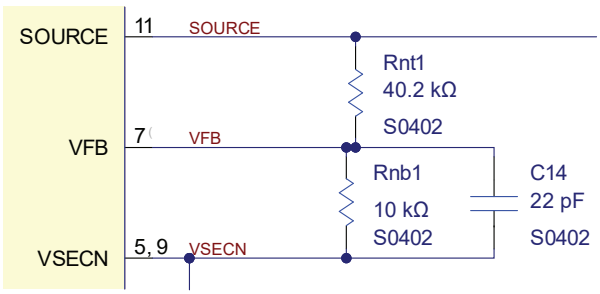
VSECN Setting Network

The AHV85043 driver allows for programming of the negative off-voltage VSECN with two resistors. For details, see the product datasheet. These resistors should be placed close to the driver. To avoid noise coupling into the feedback network, these resistors should be isolated from traces that carry large driver-switching current. A high-frequency compensation capacitor (C14) with a recommended value of 22 pF should be placed close to Rnb1.

For designs where VSECN = 0 V, these components are omitted and VSECN, VFB, and SOURCE are connected together. The test pin, 8, must be connected to VSECN and should not be left floating.





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Revision History

Number	Date	Description
–	November 12, 2025	Initial release

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