EXTERNAL TRANSFORMER DESIGN GUIDELINES FOR AHV85003 AND AHV85043 SELF-POWERED ISOLATED SIC DRIVER CHIPSET WITH BIPOLAR OUTPUT

By Dermot Dobbyn, Principal Application Engineer
Allegro MicroSystems

ABSTRACT

The AHV85003 and AHV85043 gate-driver chipset is optimized to drive discrete silicon carbide (SiC) field-effect transistors (FETs) in applications such as automotive on-board chargers (OBCs), solar inverters, industrial robotics, data-center power shelves, and general power-supply applications. When combined with an external transformer, the chipset provides a self-powered isolated gate-drive solution that is ideal for multiple applications and topologies.

INTRODUCTION

The AHV85003 and AHV85043 isolated SiC FET driver uses the Allegro MicroSystems patented Power-Thru technology. The transformer used with the chipset is a critical component in its operation.

Transformers that have already been tested and validated by Allegro MicroSystems for use with the AHV85003 and AHV85043 chipset are discussed in the section AHV85003 and AHV85043 Chipset, Validated External Transformers. The required transformer can be selected to suit different system-design requirements, e.g., the required system creepage distance, isolation rating, and target FET drive voltage and gate charge.

The AHV85003 and AHV85043 chipset, however, is not limited to these transformers that have been tested and validated. System designers may have design constraints or requirements for which these transformers are not suitable. In such cases, the designer can design a customer transformer to optimize the overall system.

This application note details the key specifications that must be achieved for correct operation in the target application.

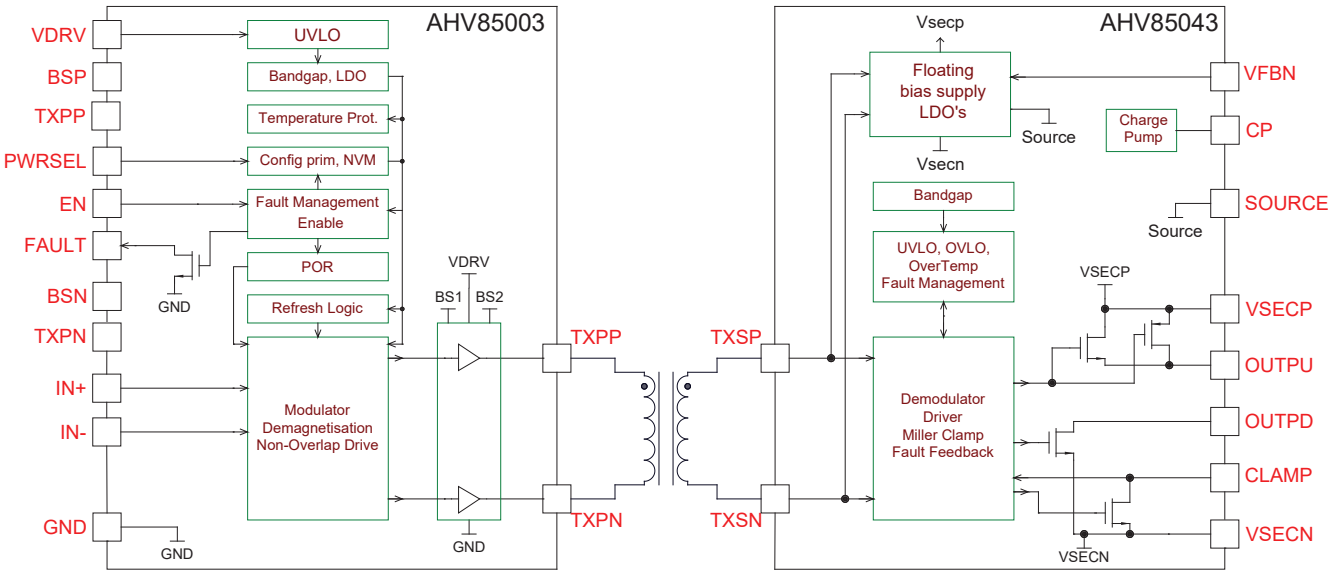


Figure 1: AHV85003 and AHV85043 Chipset, System Block Diagram

System Block Diagram

The system block diagram of the AHV85003 and AHV85043 chipset solution, including the external transformer, is shown in Figure 1.

The AHV85003 and AHV85043 are the primary-side (transmitter) and secondary-side (receiver) integrated circuits (ICs), respectively, of the isolated SiC FET gate-driver chipset. The chipset interfaces to an external transformer, connected between the transmitter (TX) and receiver (RX) ICs, which transmits both the pulse-width modulated (PWM) signal and the gate-driver bias power for the isolated side. The required transformer consists of a simple two-winding, four-pin structure.

When the supply voltage, V_{DRV}, is applied to the primary-side AHV85003 IC, the IC remains in low-power mode until V_{DRV} exceeds the undervoltage lockout (UVLO) threshold. Once the UVLO threshold is exceeded, the internal low-dropout (LDO) regulators become enabled.

If the EN input is held low, the primary side remains in a low-power standby mode, with the FAULT output held low. Once EN becomes high, or if EN is already high when V_{DRV} UVLO is released, the primary side of the driver enables power transfer to the secondary side of the driver, to charge the secondary-side isolated bias rails. This is achieved by sending pulses to the TXPP and TXPN pins to energize the external transformer. On the secondary-side AHV85043 IC, when the secondary-side bias rails have settled to the target regulation levels, and if a fault is not detected on either the primary side or the secondary side, the open-drain FAULT pin is allowed to transition to the high state via the required external pull-up resistor. This indicates to the system controller that the driver is ready to accept PWM signal input. Any PWM signal input at the IN+ or IN– pin is ignored until the internal FAULT pull-down is released.

Refresh Pulse Mechanism

In cases where the PWM signal frequency at the AHV85003 INx pins is too low, or where an INx pin is set to a continuous high (1) or low (0) state, the AHV85003 transmits a refresh pulse to the external transformer through the TXPP and TXPN pins. On the isolated side of the external transformer, the TXSP and TXSN pins of the AHV85043 rectify these pulses, to transfer the energy to the V_{SECP} and V_{SECN} rails. This mechanism ensures that the V_{SECP} and V_{SECN} rails do not sag due to the internal bias consumption of the AHV85043, and it ensures that regulation is maintained when, due to frequency and/or duty cycle, PWM signal transitions are not present or are infrequent at the AHV85003 INx pins.

EXTERNAL TRANSFORMER SPECIFICATIONS

The specifications required for an external transformer to be used with the AHV85003 and AHV85043 chipset are shown in Table 1. The generalized transformer model related to these specifications is shown in Figure 2.

Table 1: External Transformer Specifications

Parameter	Description	Min	Typ	Max	Units
L_{LK}	Primary leakage inductance	135	–	225	nH
L_{MAG}	Primary magnetizing inductance	3	5	–	µH
Np:Ns	Primary-to-secondary turns ratio	–	1:3	–	–
DCR_{PRI}	Primary DC resistance	–	–	250	mΩ
DCR_{SEC}	Secondary DC resistance	–	–	900	mΩ
C_{PS}	Primary-to-secondary capacitance	–	–	5	pF
Volt-sec	Primary volt-seconds product	4	–	–	V-µs
f_{MAX}	Maximum operating frequency	–	500	–	kHz
Temp	Operating temperature range	–40	–	125	°C

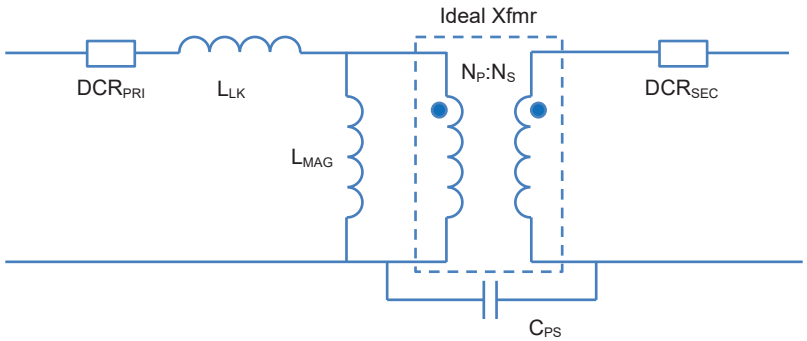


Figure 2: Generalized Transformer Model

For correct operation of the AHV85003 and AHV85043 chipset, it is critical that the parameters of the designed transformer remain within these specifications. Furthermore, these specifications must be met over the entire operating temperature range of the device.

Primary Referenced Leakage Inductance (L_{LK})

In designs with the AHV85003 and AHV85043 chipset, the most important magnetic parameter of the transformer is the primary referenced leakage inductance (L_{LK}). This parameter dominates the primary-side transformer current and, as such, dictates the amount of energy available to transfer to the secondary side and sets the overcurrent threshold for the fault management.

If L_{LK} is too high, insufficient voltage is impressed across the transformer primary, resulting in a secondary-side voltage that is insufficient to maintain regulation and charge delivery.

If L_{LK} is too low, the primary-side current becomes too high, causing the overcurrent protection to activate and generate a fault in the system.

Leakage inductance is largely a result of the physical structure of the transformer that is the coupling between the primary and secondary windings. Leakage inductance is generally stable over the operating temperature range. However, verification that leakage is stable on a number of transformer samples remains important.

Furthermore, given the importance of the leakage inductance parameter for correct operation of the AHV85003 and AHV85043 chipset, measurement of the primary referenced leakage inductance is recommended on all transformers in production.

Primary Magnetizing Inductance (L_{MAG})

The transformer current observed by the AHV85003 primary-side device is the sum of the leakage inductance current and the magnetizing inductance current.

Because operation of the primary-side is dictated by the leakage inductance as previously described, the contribution from the magnetizing inductance should be minimized. The recommended magnetizing inductance is 15 to 20 times the leakage inductance.

Magnetizing inductance is a result of the core material used, and it has a dependence on temperature. For this reason, it is important to verify the magnetizing inductance over the entire operating temperature range of the device.

Transformer Turns Ratio

The transformer turns ratio is fundamental to the correct operation of the AHV85003 and AHV85043 chipset. It must be set to the value indicated in Table 1.

Primary and Secondary DC Resistance

Primary and secondary DC resistances are largely due to conductors used to form the primary and secondary windings. These impedances appear in series with the ideal transformer model, causing voltage drops on both the primary and secondary sides. These voltage drops reduce the available power transferred and increase power losses in the transformer. For those reasons, minimization of both DCR_{PRI} and DCR_{SEC} is recommended. These values should not exceed the maximum values in Table 1.

These parameters also have a strong dependence on temperature and must be verified over the entire operating range.

Primary-to-Secondary Capacitance (C_{PS})

Primary-to-secondary capacitance (C_{PS}) is a parasitic parameter largely dictated by the physical construction of the transformer.

C_{PS} affects the common-mode transient immunity (CMTI) and electromagnetic compatibility (EMC) performance of the overall system. The transformer design and the overall system application should be designed to minimize this parameter. The transformer itself must have a C_{PS} value less than the maximum listed in Table 1.

For the AHV85003 and AHV85043 chipset driver solution, the effects of C_{PS} can be mitigated with the use of snubbers on the secondary side. For full details, see the Allegro MicroSystems application note AHV85003 and AHV85043 Chipset Secondary-Side Snubbers for Improved CMTI Performance. [1]

Primary Volt-Second Product

The transformer used with the AHV85003 and AHV85043 chipset is driven with fixed-duration pulses. It is important that the transformer does not saturate in typical operation.

The volt-second product is a measure of flux density in the core and must exceed the value shown in Table 1 over the entire operating temperature range.

[1] https://www.allegromicro.com/-/media/files/application-notes/an296377-ahv85003-and-ahv85043-secondary-side-snubbers-for-improved-cmti-performance

Maximum Operating Frequency (f_{MAX})

The maximum operating frequency (f_{MAX}) of the AHV85003 and AHV85043 chipset is 450 kHz. The transformer should be designed with some margin on this parameter with a recommended maximum value of 500 kHz.

The operating frequency is a key contributor to power dissipation within the entire system, and the final application design must be evaluated to ensure that the transformer and AHV85003 and AHV85043 chipset do not exceed their maximum temperatures.

Isolation Requirements

The isolation requirements of the transformer are defined by the end application and system design. Isolation is achieved with the physical design of the transformer, materials used, and separation distances. As such, isolation requirements are beyond the scope of this application note.

VERIFYING TRANSFORMER DESIGN

Most parameters can be measured with a good-quality inductance-capacitance-resistance (LCR) meter. Many published technical papers detail how to accurately measure component parameters, and such detail is beyond the scope of this application note.

It is important that all parameters are verified over the entire operating temperature range of the system.

Primary Referenced Leakage Inductance (L_{LK})

Leakage inductance is largely a result of the physical structure of the transformer itself. It can be measured on a transformer sample by applying a short circuit across the secondary winding and measuring inductance observed from the primary terminals.

The purpose of the short circuit across the secondary winding is to create a true-zero-volts state across the primary of the ideal transformer in the model shown in Figure 2. This feature short-circuits the magnetizing inductance, and the inductance measured at the primary terminals is the leakage inductance. Therefore, it is important for the short circuit that is applied to be low impedance and as close as practicable to the secondary terminals.

Primary Magnetizing Inductance (L_{MAG})

The primary magnetizing inductance should be measured with the secondary side in the open-circuit state. It should be noted that, for the transformer model in Figure 2, the resulting measurement is the leakage inductance plus the magnetizing inductance. However, given that the magnetizing inductance should be 15 to 20 times the leakage inductance, the error should be low.

Furthermore, the absolute value of the magnetizing inductance is of lower priority for system operation, so the error introduced by the leakage inductance is negligible.

Primary-to-Secondary Capacitance (C_{PS})

The primary-to-secondary capacitance, C_{PS}, is measured by connecting all primary pins together, connecting all secondary pins together, and measuring the capacitance from primary to secondary, as shown in Figure 3.

It is important to remember that, while this application note refers only to the design of the transformer itself, the capacitance from primary to secondary is a parameter related to the final application system design. It represents the total capacitance from primary to secondary across the isolation boundary and is affected by the printed circuit board (PCB) layout, component position, and all components that span the boundary. Minimization of the total capacitance requires careful PCB layout.

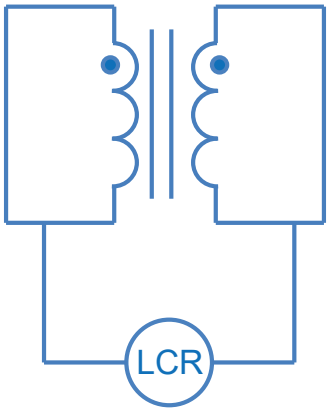


Figure 3: Primary-to-Secondary Capacitance Measurement

Primary Volt-Second Product

The transformer used with the AHV85003 and AHV85043 chipset must be capable of sustaining a minimum volt-second product applied to the primary winding. This can be measured with a simple test circuit, as shown in Figure 4.

For this test circuit, a low RDS_{ON} FET with a voltage rating of 2 to 3 times the test voltage, V_{TEST}, should be used.

The voltage across the transformer primary and the current, as shown in Figure 4, should be monitored.

Connect the transformer primary to the test circuit as shown, leaving the secondary winding in the open-circuit state.

With V_{TEST} set to zero volts, apply gate pulses to the FET. The width of the gate pulse, t_{ON}, should be set to 333 ns with a period of greater than 20 µs. The period should be long enough that, when V_{TEST} is applied, the core has enough time to reset between pulses.

While monitoring the primary current, slowly increase V_{TEST} so that V_{PRI} increases from zero to 12 V. The current in the primary should remain mostly linear (there might be a slight curve) for the entire on time.

To achieve the specification requirement for the AHV85003 and AHV85043 chipset, the transformer should exceed the volt-second specification in Table 1, as follows:

Equation 1:

$$V_{PRI} \times t_{ON} \geq 4\ V\mu s$$
$$12\ V \times 333\ ns = 4\ V\mu s$$

With V_{TEST} at a suitable level, increase the pulse width, t_{ON}. Eventually, for the transformer design, the saturation of the core becomes evident as the primary current starts to tail upward, as shown in Figure 4. Alternatively, with the pulse width fixed, the test voltage can be increased. This test should be repeated over the entire operating temperature range of the transformer.

As a verification test for the magnetizing and leakage inductance, the same test fixture can be used. In the case of the leakage inductance, short circuit the secondary winding and apply a suitable test voltage and pulse width. The inductance then can be calculated from:

Equation 2:

$$L = \frac{V_{PRI} \times t_{ON}}{I_{PRI}}$$

where I_{PRI} is the primary current at the end of the pulse.

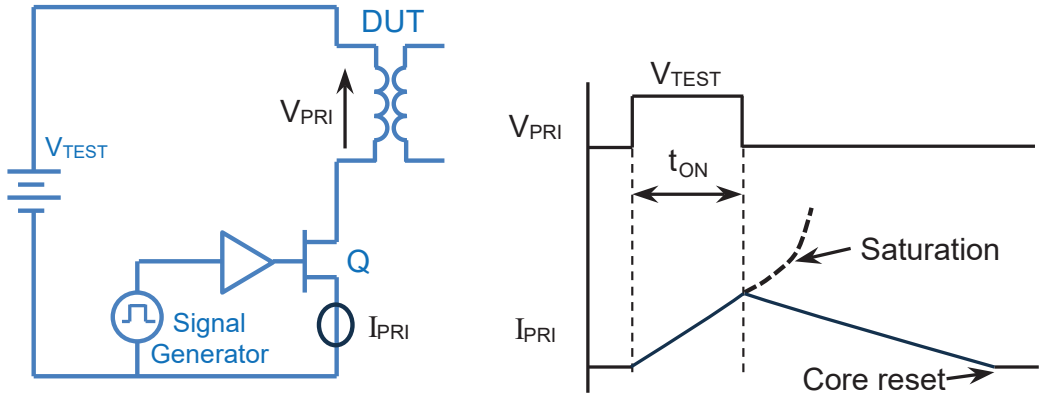


Figure 4: Primary Volt-Second Test Circuit

Typical Test Results

A typical volt-second product measurement using this technique is shown in Figure 5, where:

Left plot shows a 12 V, 335 ns pulse applied to the transformer primary, resulting in a 4.02 V-µs product. The reference (Ref) waveforms in the plot represent the measured performance at –40°C and 125°C. These measurements meet the requirements for the AHV85003 and AHV85043 chipset.

Right plot shows the effect of increasing the test voltage further: As the primary current begins to sharply increase, the onset of saturation is visible. This occurs at a test voltage of 20 V with a pulse width of 250 ns, resulting in a volt-second product of 5 V-µs. This provides adequate margin to the design.

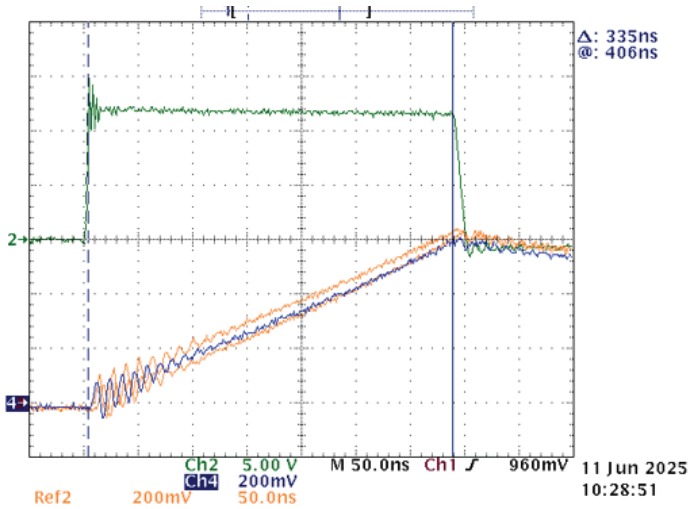
As noted previously, the magnetizing inductance can be calculated from this plot. The current scale here is 0.2 A/div, resulting in a peak current of 0.6 A. The magnetizing inductance then is:

Equation 3:

$$L = \frac{V_{PRI} \times t_{ON}}{I_{PRI}} = \frac{12\,V \times 335\,ns}{0.6\,A} = 6.7\,\mu H$$

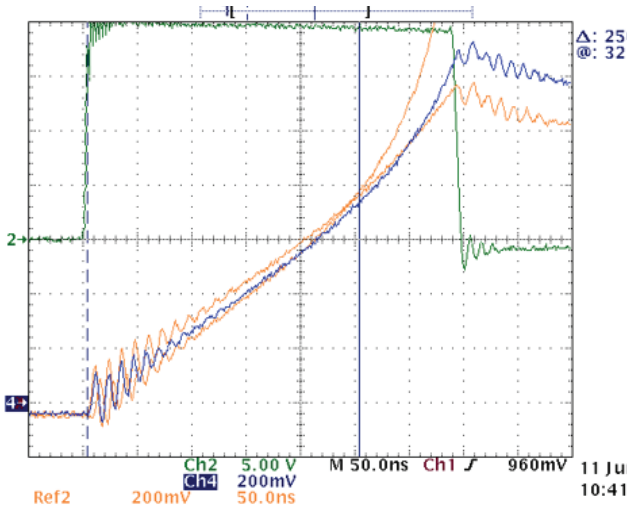
It should be noted that the calculated value might differ from that measured using an LCR meter. An LCR meter typically measures inductance with a low-voltage (e.g., 0.5 V) sine wave, which does not exercise the full magnetic hysteresis (BH) loop of the transformer core.

Given that the leakage inductance does not magnetize the core material, the measurements from an LCR meter and this test circuit broadly align.



CH2 (Green): V_{TEST}
CH4 (Blue): Device under test current (1 A/V)
Ref (Orange): Current at –40˚C and 125˚C

Required Specification
V_{TEST} = 12 V
t_{ON} = 335 ns
V-s = 4 V-µs



CH2 (Green): V_{TEST}
CH4 (Blue): Device under test current (1 A/V)
Ref (Orange): Current at –40˚C and 125˚C

Saturation Limit
V_{TEST} = 20 V
t_{sat} = 250 ns
V-s = 5 V-µs

Figure 5: Typical Volt-Second Measurement

PINOUT AND PCB LAYOUT

The required transformer is a simple four-terminal device. The primary interfaces with the TXPP and TXPN pins of the AHV85003 primary-side device while the secondary interfaces with the TXSP and TXSN pins of the AHV85043 secondary-side device. With this in mind, where possible, the pinout of the transformer should be designed to interface directly to the quad-flat no-lead (QFN) devices in the final application, as shown in Figure 6.

The PCB tracks to both devices should be low impedance with minimal loop area. For full details about PCB layout, see the application note AHV85003 and AHV85043 Chipset QFN PCB Layout Guidelines (AN296376). [2]

AHV85003 AND AHV85043 CHIPSET, VALIDATED EXTERNAL TRANSFORMERS

Transformers already been validated for use with the AHV85003 and AHV85043 chipset are shown in Table 2. Additional validated parts are available upon request.

Table 2: AHV85003/AHV85043 Validated External Transformers

Part Number	Manu-facturer	Isolation Rating	Foot-print (mm)	Max Height (mm)
LTW4638A-P-C05TF	Sunlord	Functional	5 × 3.8	3.2

CONCLUSION

Allegro MicroSystems has already validated a number of transformers that are suitable for use with the AHV85003 and AHV85043 chipset. These transformers are available directly from manufacturers or from distributors and are listed in Table 2.

For applications where these transformers do not meet system requirements, this application note describes the key design parameters to ensure compatibility with the AHV85003 and AHV85043 chipset.

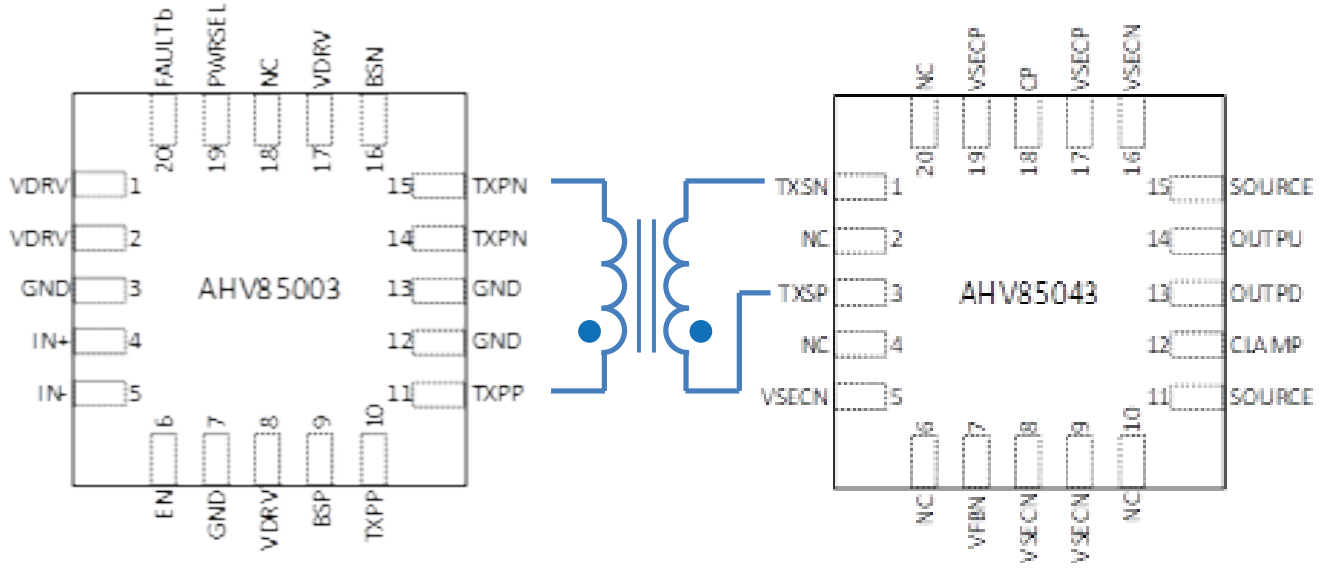


Figure 6: Transformer Interface to AHV85003 and AHV85043

[2] https://www.allegromicro.com/-/media/files/application-notes/an296376-ahv85003-and-ahv85043-chipset-qfn-pcb-layout-guidelines

Revision History

Number	Date	Description	Responsibility
–	November 7, 2025	Initial release	D. Dobbyn

955 PERIMETER ROAD • MANCHESTER, NH 03103 • USA
+1-603-626-2300 • FAX: +1-603-641-5336 • ALLEGROMICRO.COM