AHV85003 AND AHV85043 CHIPSET SECONDARY-SIDE SNUBBERS FOR IMPROVED CMTI PERFORMANCE

By Dermot Dobbyn, Principal Application Engineer
Allegro MicroSystems

ABSTRACT

The AHV85003 and AHV85043 gate-driver chipset is optimized to drive discrete SiC FETs in applications that include automotive on-board-chargers (OBC), solar inverters, industrial robotics, data center power shelves, and general power supply applications. In combination with an external transformer, it provides a self-powered isolated gate drive solution that is ideal for multiple applications and topologies.

All components with an isolation barrier contain an inherent capacitance from primary to secondary, C_{PS}. This parasitic capacitance is a crucial factor in the CMTI and EMC performance of the final application system.

INTRODUCTION

The AHV85003 and AHV85043 isolated SiC FET driver uses the patented Power Thru technology from Allegro MicroSystems in combination with an external transformer.

In a typical SiC-FET-based converter, very-high-voltage fast-transitions (dV/dt) are generated. These transitions result in a common-mode current that flows through C_{PS}. This current creates noise and power losses that are not wanted and that require management within the system design. Furthermore, these common-mode transients can disrupt the operation of a gate driver or its signal integrity.

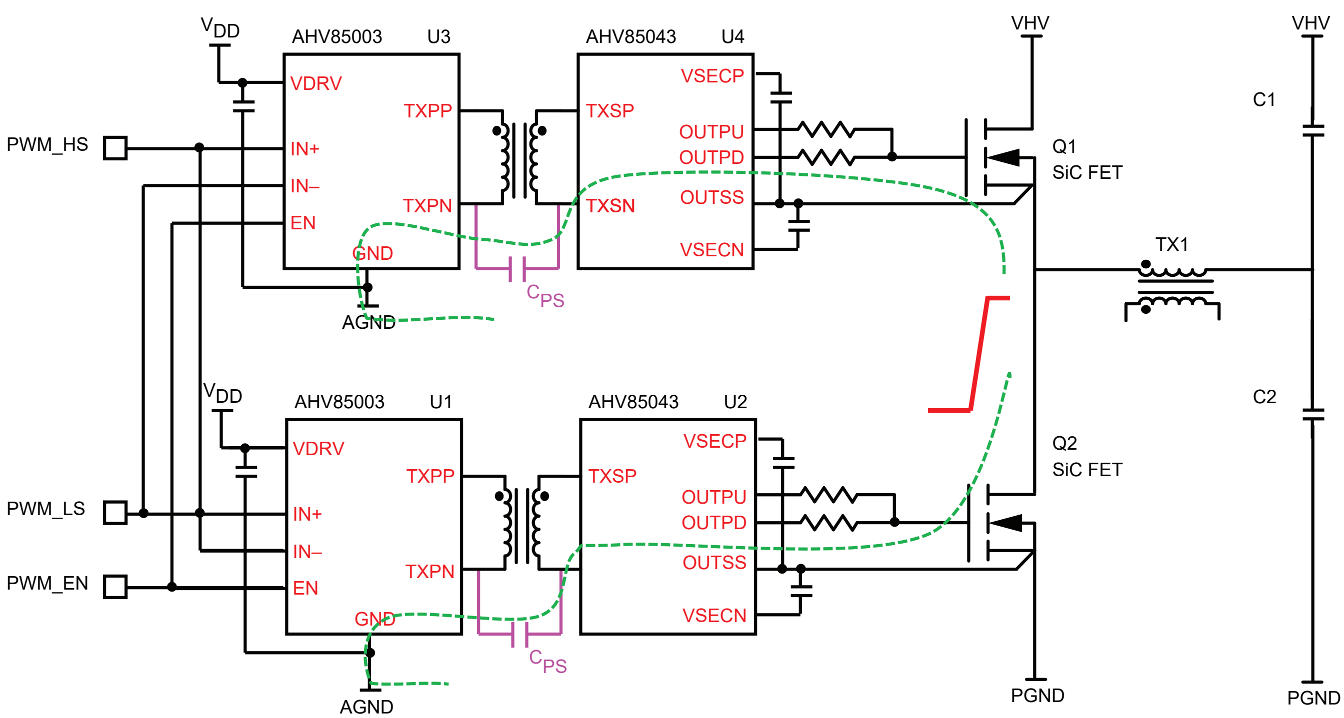

Figure 1: AHV85003 and AHV85043 Chipset, Typical Application Block Diagram

C_{PS} is a parasitic component that is generally related to the physical construction of the component or components that span the isolation boundary. This includes not only the isolated gate driver, but also the printed circuit board (PCB) and any other components that span the boundary.

Elimination of C_{PS} is not possible. However, minimization of this capacitance results in minimization of the effects of common-mode transients. The external transformer used with the AHV85003 and AHV85043 chipset forms the isolation barrier. With a suitable design, the primary-to-secondary capacitance, C_{PS}, is 10 to 20 times less than the capacitance of a typical external DC-DC converter module used with some gate-driver solutions.

A feature of the AHV85003 and AHV85043 chipset is the capacity for improvement of the common-mode transient immunity (CMTI) performance through the inclusion of a snubber pair on the secondary side.

This application note provides details about the selection of the snubber components and the impact these components have on the overall system.

TYPICAL APPLICATION BLOCK DIAGRAM

A typical application block diagram that uses the AHV85003 and AHV85043 chipset solution and includes the external transformer is shown in Figure 1. The parasitic common-mode capacitance, C_{PS}, of each transformer is shown. It is important to note that this is not the only common-mode capacitance that spans the isolation boundary.

In operation, the voltage at the switch node transitions from PGND to VHV or VHV to PGND as the power FETs are switched. This transition can occur very quickly, on the order of nanoseconds.

The resultant dV/dt results in a current in C_{PS} of:

Equation 1:

$$i(t) = C_{PS}\frac{dV}{dt}$$

It is important to note that the same dV/dt event can be generated in a number of ways. A 100 V/ns dV/dt event generated from three different voltage levels (100 V, 500 V, and 1000 V) is shown in Figure 2. It is important to note that, while the resultant capacitor current has the same amplitude in all cases because the dV/dt is constant, the duration of the current pulse is different in each case.

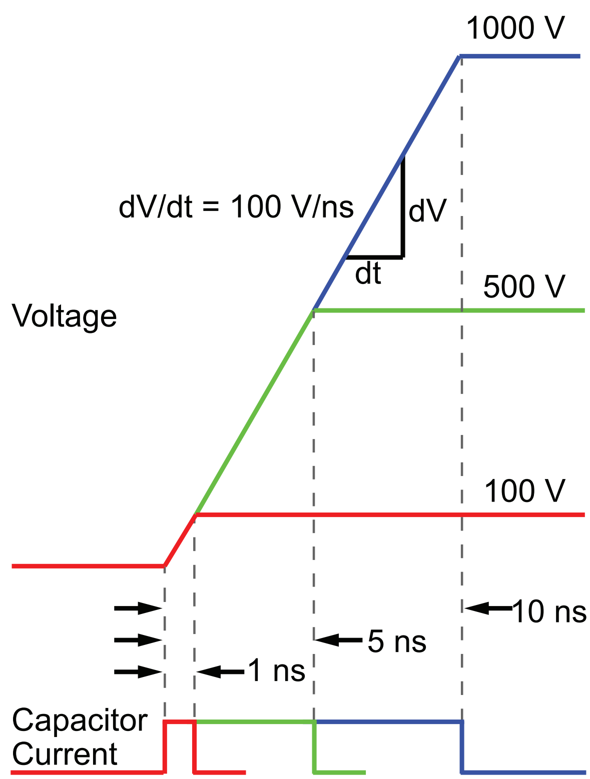

Figure 2: dV/dt Events

COMMON-MODE TRANSIENT IMMUNITY TEST

A full explanation of CMTI testing is beyond the scope of this application note. A single standard for CMTI does not exist. For magnetic isolated couplers, IEC 60747-17 section 6.7 defines the methods for the measurement of the CMTI of a coupler in both static and dynamic operation, under a specified common-mode pulse magnitude (V_{CM}) and a specified slew rate of the common-mode pulse (dV_{CM}/dt).

IEC 60747-17 section 6.7.3 also specifies precautions to be observed to obtain accurate CMTI test results.

A typical CMTI test circuit applied to a typical AHV85003 and AHV85043 chipset application is shown in Figure 3.

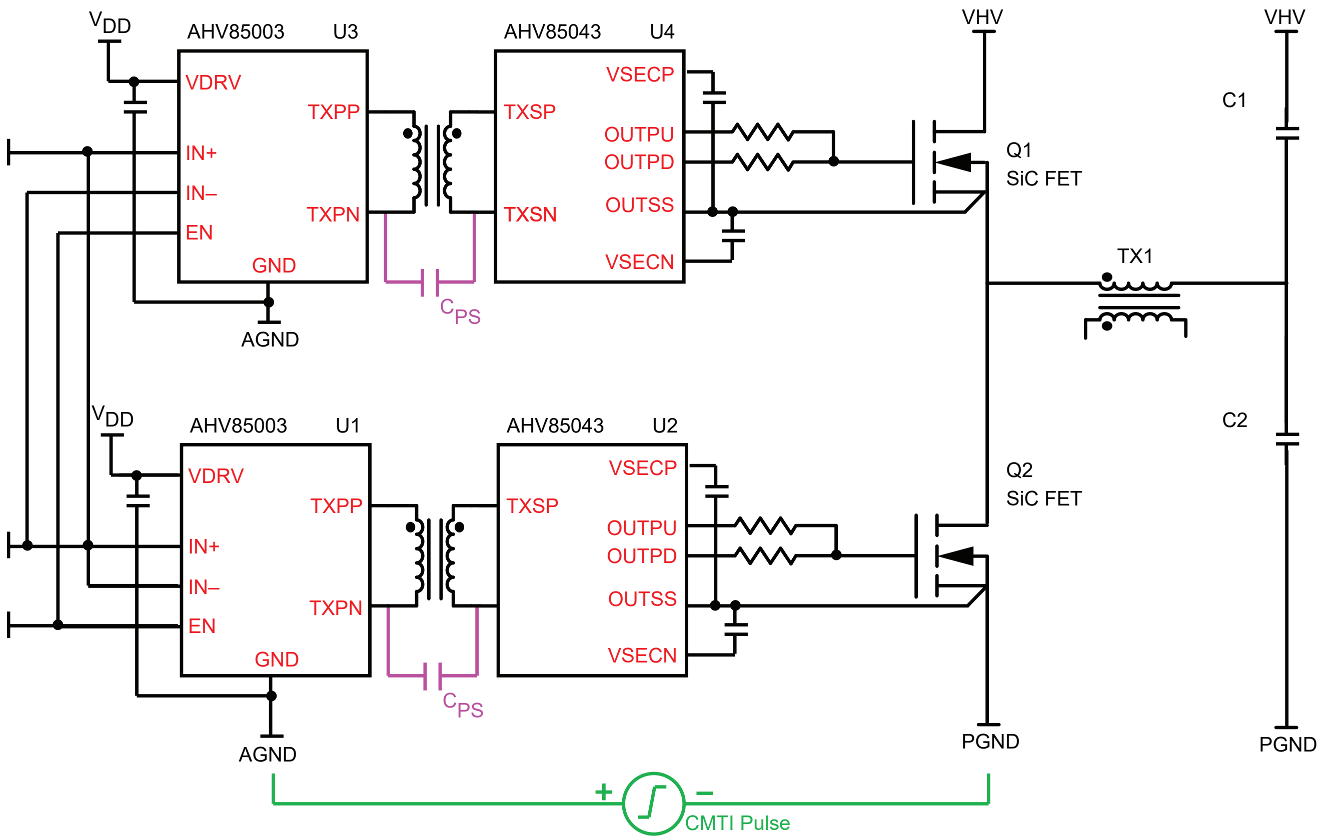

Figure 3: Typical CMTI Test Setup

IMPROVEMENT OF CHIPSET CMTI PERFORMANCE

In most cases, the AHV85003 and AHV85043 chipset, when used with a suitable external transformer, achieves CMTI > 100 V/ns.

However, if the system does not achieve the desired CMTI performance because of increased primary to secondary isolation capacitance, this performance can be improved with the inclusion of two simple snubbers on the secondary side, as shown in Figure 4.

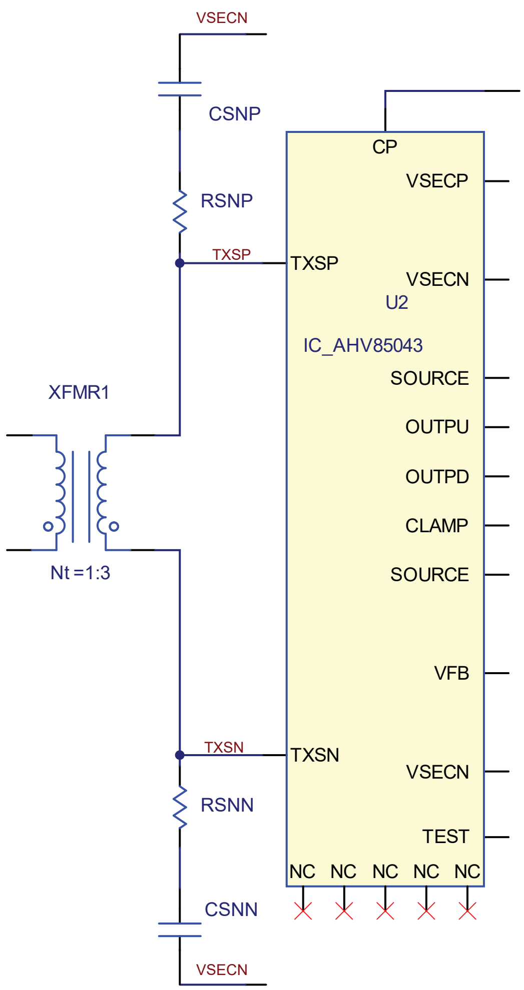

Figure 4: Secondary-Side Snubbers

The calculation of the required snubber component values requires a measurement of the total primary-to-secondary isolation capacitance, C_{IO}, of the system. The measurement method for the determination of this capacitance is described in IEC 60747-17 section 6.2.

This capacitance is distributed over the number of isolated drivers used in the system. The primary-to-secondary capacitance of each driver, C_{PS}, is determined as:

Equation 2:

$$C_{PS} = \frac{C_{IO}}{Number\ of\ isolated\ drivers}$$

With knowledge of the values:

- C_{PS}, primary to secondary capacitance
- V_{CM}, magnitude of common mode voltage
- dV_{CM}/dt, the slew rate of the common mode pulse

the required snubber values are determined from:

Equation 3:

$$R_{SN} = Min\ of \left[\frac{12}{\frac{1}{2}\ C_{PS} \frac{dV_{CM}}{dt} - \ 12e^{-3}} \right] or\ 1\ k\Omega$$

$$C_{SN} = Max\ of \left[\frac{2\ V_{CM}}{R_{SN}\ \frac{dV_{CM}}{dt}} \right] or\ 50\ pF$$

The selected capacitor should be a good quality ceramic capacitor with a dielectric of X7R or better and a minimum voltage rating of (VSECP – VSECN) plus a recommended margin of at least 30%.

The selected resistor should have a minimum power rating that can be determined from:

Equation 4:

$$P_R = max\ of\ ((VSECP - VSECN)^2\ \ C_{SN}\ \ Fsw)$$
or
$$((VSECP - VSECN)^2\ \ C_{SN}\ \ 150k)$$

In the system application, the snubbers should be located close to the transformer with a low impedance path to the AHV85043 exposed pad, VSECN. For full details of PCB layout considerations for the AHV85003 and AHV85043 chipset, refer to the AHV85003 and AHV85043 Chipset PCB Layout Guide. [1]

[1] https://www.allegromicro.com/-/media/files/AHV85003-AHV85043-Chipset-PCB-Layout-Guide

EFFECT OF SNUBBER ADDITION FOR CMTI

The addition of these snubbers introduces increased power dissipation in the circuit. Because these snubbers are on the secondary side that receives energy from the Power-Thru mechanism, this uses energy that otherwise is available to drive the FET Qg. For this reason, the snubber size should be designed to be the minimum value (minimum $C_{SN,}$ maximum R_{SN},) to achieve the required CMTI performance.

To determine the reduction in energy available to drive the load FET, refer to the AHV85003/043 datasheet.

It is important to note that the AHV85003 and AHV85043 chipset gate-driver solution is specified to deliver up to 130 nC of gate charge. Through use of the PWRSEL function, three power-level configurations exist: low, medium, and high. For full details, refer to the datasheet for the chipset.

CONCLUSION

Common-mode transient immunity (CMTI) is an important test for isolated gate drivers to ensure reliable and safe operation in high-frequency power switching environments.

The overall CMTI performance of a system is largely dependent on the total parasitic capacitance across the isolation boundary.

The AHV85003 and AHV85043 chipset, in combination with a well-designed external transformer, can achieve CMTI performance in excess of 100 V/ns.

This performance can be further refined with the inclusion of two resistor-capacitor (RC) snubbers on the secondary side.

Revision History

Number	Date	Description	Responsibility
–	November 24, 2025	Initial release	D. Dobbyn