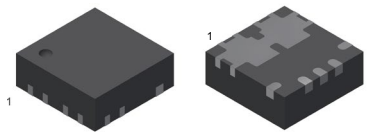
Low-Resistance Current Sensor in QFN Package

FEATURES AND BENEFITS

- Ultra-low primary conductor resistance, <100 μΩ, for high efficiency and high-inrush current capability
- Differential Hall sensing rejects common-mode fields
- Small footprint, 4 mm × 4 mm QFN package with wettable flank, suitable for space-constrained automotive applications
- 150 kHz analog output for fast response time in control applications
- Patented integrated digital temperature compensation
- Overcurrent fault output with configurable threshold
- Non-ratiometric output
- 3.3 V and 5 V supply options
- 100 V_{RMS} functional isolation
- AEC-Q100 Grade 0, automotive qualified

PACKAGE: 7-pin QFN with Wettable Flank (suffix EZ)



Not to scale

DESCRIPTION

The ACS37220 is an integrated current sensor that senses current flowing through the primary conductor of a compact 7-pin QFN package.

The small 4 mm × 4 mm sensor has very low internal conductor resistance, <100 μΩ, and is designed to measure currents up to 200 A. The current is sensed differentially via two Hall plates that provide common-mode field rejection and optimized performance in the presence of external magnetic fields.

The ACS37220 is factory-calibrated for high accuracy over the entire operating temperature range. It is an automotive Grade 0 device capable of operating between –40°C and 150°C ambient temperatures. Variants are available for 5 V and 3.3 V supply voltage, with current sensing ranges from ±100 A to ±200 A. An overcurrent fault output, with user-configurable threshold, provides fast short-circuit detection for enhanced system protection.

The ACS37220 is a lead (Pb) free device plated with 100% matte tin, compatible with standard lead-free printed circuit board (PCB) assembly processes.

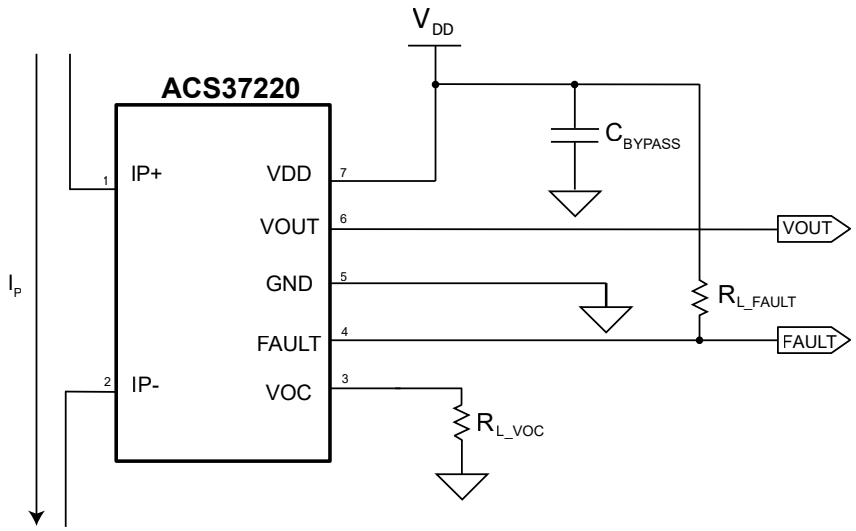
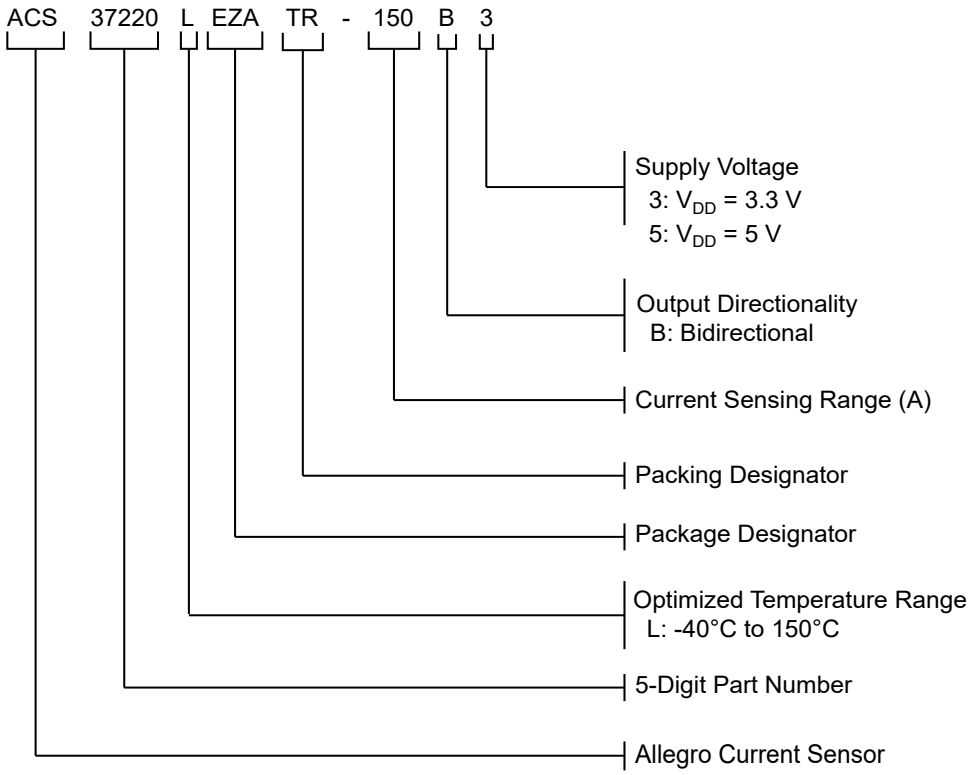


Figure 1: Typical Application Circuit

The ACS37220 outputs an analog signal at VOUT that varies linearly with the primary current, I_P.

SELECTION GUIDE

Part Number	Current Sensing Range (A)	Sensitivity (mV/A)	Supply Voltage V_{DD} (V)	Quiescent Voltage Output V_{QVO} (V)	Optimized Temperature Range T_A (°C)	Packing
ACS37220LEZATR-100B3	±100	13.2	3.3	1.65	–40 to 150	Tape and Reel, 3000 pieces per reel
ACS37220LEZATR-150B3	±150	8.8				
ACS37220LEZATR-100B5	±100	20	5	2.5		
ACS37220LEZATR-150B5	±150	13.3				
ACS37220LEZATR-200B5	±200	10				



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Min.	Max.	Unit
Supply Voltage	V_{DD}		–0.5	6.5	V
Forward Output Voltage	V_O	Applies to VOUT, VOC, and FAULT	–0.5	$(V_{DD} + 0.7) < 6.5$	V
Operating Ambient Temperature	T_A		–40	150	°C
Storage Temperature	T_{stg}		–65	165	°C
Maximum Junction Temperature	$T_{J(MAX)}$		–	165	°C

[1] Stresses that exceed those listed in the Absolute Maximum Ratings table might cause permanent damage to the device. This is a stress rating only; functional operation of the device at these conditions or any other condition that exceeds those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum ratings for extended periods might affect device reliability.

ISOLATION CHARACTERISTICS

Characteristic	Symbol	Notes	Value	Units
Working Voltage for Functional Isolation	V_{WVBI}	Approved working voltage for functional isolation	100	V_{RMS}
Creepage	D_{CR}	Distance along package body between the IP pins and signal pins	1	mm

PACKAGE CHARACTERISTICS

Characteristic	Symbol	Notes	Min.	Typ.	Max.	Unit
Internal Conductor Resistance	R_{IC}	T_A = 25°C	–	100	–	µΩ
Internal Conductor Inductance	L_{IC}	T_A = 25°C	–	0.5	–	nH
Moisture Sensitivity Level	MSL	Per IPC/JEDEC J-STD-020	–	2	–	–

THERMAL CHARACTERISTICS

Characteristic	Symbol	Notes	Value	Unit
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	Mounted on the Allegro EZ current sensor evaluation board (ACSEVB-EZ7)	55	°C/W
Package Thermal Metric (Junction to Top)	Ψ_{JT}		7.5	°C/W

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

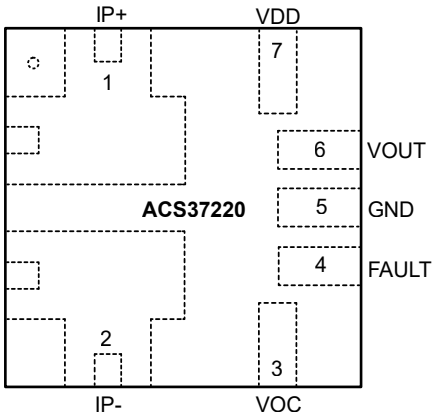


Figure 2: EZ Package Pinout Diagram (Top View)

Terminal List Table

Number	Name	Description
1	IP+	Positive terminal for current being sensed
2	IP–	Negative terminal for current being sensed
3	VOC	User-configurable overcurrent fault threshold
4	FAULT	Overcurrent fault output, active low
5	GND	Device ground terminal
6	VOUT	Analog output signal
7	VDD	Device power supply terminal

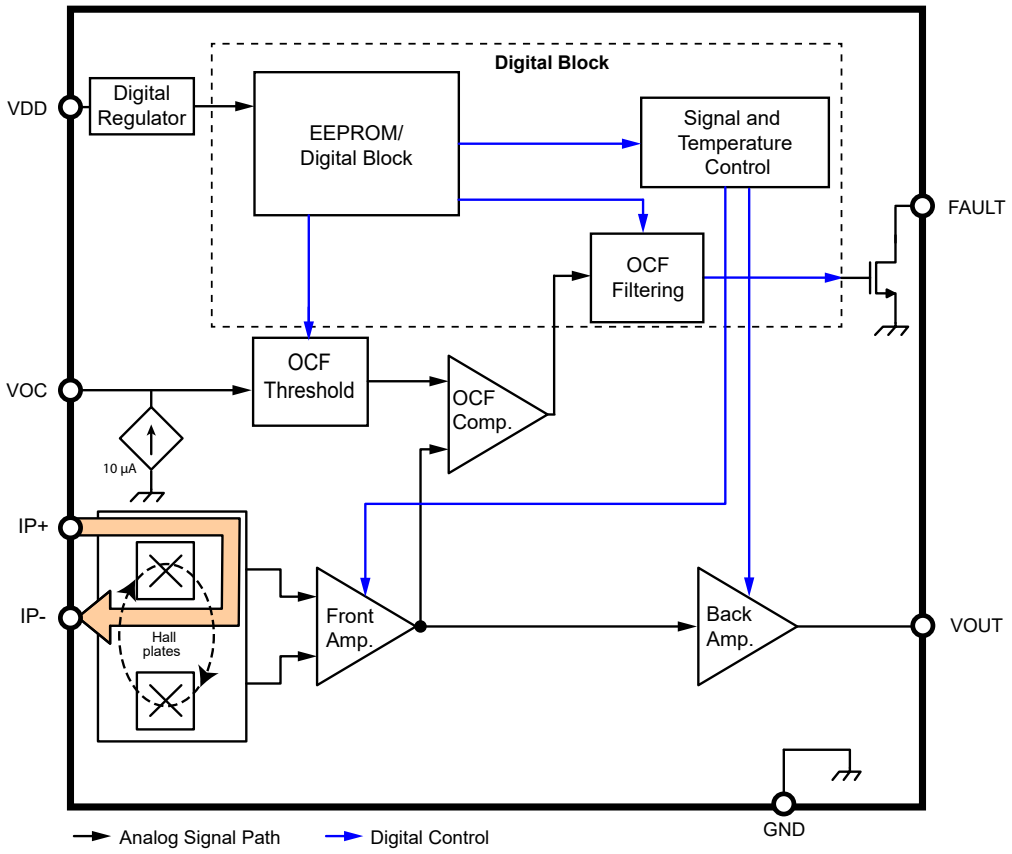


Figure 3: Functional Block Diagram

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

COMMON ELECTRICAL CHARACTERISTICS: Valid through the full operating temperature range, T_A = –40°C to 150°C, C_{BYPASS} = 0.1µF, and V_{DD} = $V_{DD(Typ)}$, unless specified otherwise. Minimum and maximum values are tested in production or validated by design and characterization.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{DD}	5 V variant	4.5	5	5.5	V
		3.3 V variant	3.15	3.3	3.45	V
Supply Current	I_{DD}	No load on VOUT, FAULT, and VOC; T_A = –40°C	–	–	15.5	mA
Supply Bypass Capacitor	C_{BYPASS}		–	0.1	–	µF
Power-On Voltage	V_{POR}	T_A = 25°C, V_{DD} rising 1 V/ms	2.65	–	3	V
Power-On Reset Hysteresis	V_{POR_HYS}	T_A = 25°C	250	–	350	mV
Power-On Time	t_{PO}		–	80	–	µs
OUTPUT SIGNAL CHARACTERISTICS (VOUT)						
Saturation Voltage [1]	V_{SAT_H}	T_A = 25°C, V_{DD} = $V_{DD(Typ)}$	V_{DD} – 0.3	–	–	V
	V_{SAT_L}	T_A = 25°C, V_{DD} = $V_{DD(Typ)}$	–	–	0.3	V
Output Resistive Load [2]	R_{L_VOUT}		10	–	–	kΩ
Output Capacitive Load [2]	C_{L_VOUT}		–	–	4.7	nF
VOUT Short Circuit Current to GND	I_{SC_VOUT}		–	30	–	mA
Bandwidth	BW	Small signal –3 dB, C_L = 100 pF	–	150	–	kHz
Rise Time	t_R	C_L = 100 pF	–	2.3	–	µs
Response Time [2]	t_{RESP}	C_L = 100 pF	–	–	4	µs
Propagation Delay	t_{PD}	C_L = 100 pF	–	1.6	–	µs
Noise Density	N_D	5 V variant, C_L = 1 nF	–	550	–	µA/√Hz
		3.3 V variant, C_L = 1 nF	–	660	–	µA/√Hz
Common-Mode Field Rejection	CMFR	Input-referred error due to common-mode field	–	2	–	mA/G
OVERCURRENT FAULT OUTPUT CHARACTERISTICS (FAULT)						
Overcurrent Fault Threshold	I_{OC}	T_A = 25°C	50	–	200	$\%I_{P(Max)}$
VOC Input Linear Operating Range	V_{OR_VOC}	5 V variant, T_A = 25°C	0.5	1	2	V
		3.3 V variant, T_A = 25°C	0.33	0.66	1.32	V
VOC Input Low Voltage	V_{VOC_L}		–	0.1	–	V
VOC Current	I_{VOC}		–	10	–	µA
Overcurrent Fault Pull-Up Resistor	R_{L_FAULT}		–	10	–	kΩ
Overcurrent Fault Output Error	E_{OC}	T_A = 25°C	–12	–	12	$\%I_{P(Max)}$
Overcurrent Fault Output Low Voltage	V_{FAULT_L}	R_{L_FAULT} = 10 kΩ, fault condition present	–	–	0.3	V
Overcurrent Fault Leakage Current	I_{FAULT_OFF}	R_{L_FAULT} = 10 kΩ, no fault condition present	–	100	–	nA
Overcurrent Fault Hysteresis	I_{OC_HYST}	T_A = 25°C	3.5	–	–	$\%I_{P(Max)}$
Overcurrent Fault Response Time	t_{OC_RESP}		–	3	–	µs

[1] The sensor may continue to respond to current beyond the specified current sensing range, $I_{P(Max)}$, until the output saturates at the high or low saturation voltage; however, the linearity and performance beyond the specified current sensing range are not validated.
[2] Validated by design and characterization.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ACS37220LEZATR-100B3 PERFORMANCE CHARACTERISTICS: Valid through the full operating temperature range, T_A = –40°C to 150°C, C_{BYPASS} = 0.1 µF, and V_{DD} = 3.3 V, unless specified otherwise. Minimum and maximum values are tested in production.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
NOMINAL PERFORMANCE						
Current Sensing Range [1]	I_P	Limited by $T_{J(MAX)}$ = 165°C	–100	–	100	A
Sensitivity [2]	Sens	$I_{P(Min)} < I_P < I_{P(Max)}$	–	13.2	–	mV/A
Quiescent Voltage Output	V_{QVO}	I_P = 0 A	–	1.65	–	V
Overcurrent FAULT Threshold	I_{OC}	V_{VOC} = 0.661 V or $V_{VOC} < V_{VOC_L}$	–	100	–	A
OVERCURRENT FAULT OUTPUT						
Overcurrent FAULT Error	I_{OC_E}	V_{VOC} = 0.661 V, T_A = 25°C	–12	–	12	A
ERROR COMPONENTS						
Sensitivity Error [2]	E_{SENS}	On Allegro evaluation board, T_A = 25°C, T_A = –40°C, T_A = 150°C	–2	–	2	%
Quiescent Voltage Output Error	V_{QVO_E}	I_P = 0 A; T_A = 25°C, T_A = –40°C, T_A = 150°C	–10	–	10	mV
Sensitivity Temperature Drift	E_{SENS_T}		–	±1.4	–	%
Quiescent Voltage Output Temperature Drift	V_{QVO_T}		–	±6	–	mV
Noise	N	T_A = 25°C, C_{L_VOUT} = 1 nF, BW = 150 kHz	–	4.2	–	mV_{RMS}
Power Supply Offset Error	V_{OE_PS}	V_{DD} = 3.15 V, V_{DD} = 3.45 V, T_A = 25°C	–15	–	15	mV
Power Supply Sensitivity Error	E_{SENS_PS}	V_{DD} = 3.15 V, V_{DD} = 3.45 V, T_A = 25°C	–1.5	–	1.5	%
LIFETIME DRIFT						
Sensitivity Lifetime Drift [1]	E_{SENS_LT}	Based on six-sigma drift of worst-case distribution observed after AEC-Q100 qualification stresses	–2.3	±1.2	2.3	%
Quiescent Voltage Output Lifetime Drift [1]	V_{QVO_LT}	Based on six-sigma drift of worst-case distribution observed after AEC-Q100 qualification stresses	–18	±10	18	mV

[1] Validated by design and characterization.
[2] See the Layout Guidelines section of this datasheet and the technical support documentation on the ACS37220 product page of the Allegro website.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ACS37220LEZATR-150B3 PERFORMANCE CHARACTERISTICS: Valid through the full operating temperature range, T_A = –40°C to 150°C, C_{BYPASS} = 0.1 µF, and V_{DD} = 3.3 V, unless specified otherwise. Minimum and maximum values are tested in production.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
NOMINAL PERFORMANCE						
Current Sensing Range [1]	I_P	Limited by $T_{J(MAX)}$ = 165°C	–150	–	150	A
Sensitivity [2]	Sens	$I_{P(Min)} < I_P < I_{P(Max)}$	–	8.8	–	mV/A
Quiescent Voltage Output	V_{QVO}	I_P = 0 A	–	1.65	–	V
Overcurrent FAULT Threshold	I_{OC}	V_{VOC} = 0.661 V or $V_{VOC} < V_{VOC_L}$	–	150	–	A
OVERCURRENT FAULT OUTPUT						
Overcurrent FAULT Error	I_{OC_E}	V_{VOC} = 0.661 V, T_A = 25°C	–18	–	18	A
ERROR COMPONENTS						
Sensitivity Error [2]	E_{SENS}	On Allegro evaluation board, T_A = 25°C, T_A = –40°C, T_A = 150°C	–2	–	2	%
Quiescent Voltage Output Error	V_{QVO_E}	I_P = 0 A, T_A = 25°C, T_A = –40°C, T_A = 150°C	–10	–	10	mV
Sensitivity Temperature Drift	E_{SENS_T}		–	±1.4	–	%
Quiescent Voltage Output Temperature Drift	V_{QVO_T}		–	±6	–	mV
Noise	N	T_A = 25°C, C_{L_VOUT} = 1 nF, BW = 150 kHz	–	2.8	–	mV_{RMS}
Power Supply Offset Error	V_{OE_PS}	V_{DD} = 3.15 V, V_{DD} = 3.45 V, T_A = 25°C	–15	–	15	mV
Power Supply Sensitivity Error	E_{SENS_PS}	V_{DD} =3.15 V, V_{DD} = 3.45 V, T_A = 25°C	–1.5	–	1.5	%
LIFETIME DRIFT						
Sensitivity Lifetime Drift [1]	E_{SENS_LT}	Based on six-sigma drift of worst-case distribution observed after AEC-Q100 qualification stresses	–2.3	±1.2	2.3	%
Quiescent Voltage Output Lifetime Drift [1]	V_{QVO_LT}	Based on six-sigma drift of worst-case distribution observed after AEC-Q100 qualification stresses	–18	±10	18	mV

[1] Validated by design and characterization.
[2] See the Layout Guidelines section of this datasheet and the technical support documentation on the ACS37220 product page of the Allegro website.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ACS37220LEZATR-100B5 PERFORMANCE CHARACTERISTICS: Valid through the full operating temperature range, T_A = –40°C to 150°C, C_{BYPASS} = 0.1 µF, and V_{DD} = 5 V, unless specified otherwise. Minimum and maximum values are tested in production.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
NOMINAL PERFORMANCE						
Current Sensing Range [1]	I_P	Limited by $T_{J(MAX)}$ = 165°C	–100	–	100	A
Sensitivity [2]	Sens	$I_{P(Min)} < I_P < I_{P(Max)}$	–	20	–	mV/A
Quiescent Voltage Output	V_{QVO}	I_P = 0 A	–	2.5	–	V
Overcurrent FAULT Threshold	I_{OC}	V_{VOC} = 1 V or $V_{VOC} < V_{VOC_L}$	–	100	–	A
OVERCURRENT FAULT OUTPUT						
Overcurrent FAULT Error	I_{OC_E}	V_{VOC} = 1 V, T_A = 25°C	–12	–	12	A
ERROR COMPONENTS						
Sensitivity Error [2]	E_{SENS}	On Allegro evaluation board, T_A = 25°C, T_A = –40°C, T_A = 150°C	–1.8	–	1.8	%
Quiescent Voltage Output Error	V_{QVO_E}	I_P = 0 A, T_A = 25°C, T_A = –40°C, T_A = 150°C	–10	–	10	mV
Sensitivity Temperature Drift	E_{SENS_T}		–	±1.4	–	%
Quiescent Voltage Output Temperature Drift	V_{QVO_T}		–	±6	–	mV
Noise	N	T_A = 25°C, C_{L_VOUT} = 1 nF, BW = 150 kHz	–	6.4	–	mV_{RMS}
Power Supply Offset Error	V_{OE_PS}	V_{DD} = 4.5 V, V_{DD} = 5.5 V, T_A = 25°C	–15	–	15	mV
Power Supply Sensitivity Error	E_{SENS_PS}	V_{DD} = 4.5 V, V_{DD} = 5.5 V, T_A = 25°C	–1.5	–	1.5	%
LIFETIME DRIFT						
Sensitivity Lifetime Drift [1]	E_{SENS_LT}	Based on six-sigma drift of worst-case distribution observed after AEC-Q100 qualification stresses	–2.3	±1.2	2.3	%
Quiescent Voltage Output Lifetime Drift [1]	V_{QVO_LT}	Based on six-sigma drift of worst-case distribution observed after AEC-Q100 qualification stresses	–18	±10	18	mV

[1] Validated by design and characterization.
[2] See the Layout Guidelines section of this datasheet and the technical support documentation on the ACS37220 product page of the Allegro website.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ACS37220LEZATR-150B5 PERFORMANCE CHARACTERISTICS: Valid through the full operating temperature range, T_A = –40°C to 150°C, C_{BYPASS} = 0.1 µF, and V_{DD} = 5 V, unless specified otherwise. Minimum and maximum values are tested in production.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
NOMINAL PERFORMANCE						
Current Sensing Range [1]	I_P	Limited by $T_{J(MAX)}$ = 165°C	–150	–	150	A
Sensitivity [2]	Sens	$I_{P(Min)} < I_P < I_{P(Max)}$	–	13.3	–	mV/A
Quiescent Voltage Output	V_{QVO}	I_P = 0 A	–	2.5	–	V
Overcurrent FAULT Threshold	I_{OC}	V_{VOC} = 1 V or $V_{VOC} < V_{VOC_L}$	–	150	–	A
OVERCURRENT FAULT OUTPUT						
Overcurrent FAULT Error	I_{OC_E}	V_{VOC} = 1 V, T_A = 25°C	–18	–	18	A
ERROR COMPONENTS						
Sensitivity Error [2]	E_{SENS}	On Allegro evaluation board, T_A = 25°C, T_A = –40°C, T_A = 150°C	–1.8	–	1.8	%
Quiescent Voltage Output Error	V_{QVO_E}	I_P = 0 A, T_A = 25°C, T_A = –40°C, T_A = 150°C	–10	–	10	mV
Sensitivity Temperature Drift	E_{SENS_T}		–	±1.4	–	%
Quiescent Voltage Output Temperature Drift	V_{QVO_T}		–	±6	–	mV
Noise	N	T_A = 25°C, C_{L_VOUT} = 1 nF, BW = 150 kHz	–	4.2	–	mV_{RMS}
Power Supply Offset Error	V_{OE_PS}	V_{DD} = 4.5 V, V_{DD} = 5.5 V, T_A = 25°C	–15	–	15	mV
Power Supply Sensitivity Error	E_{SENS_PS}	V_{DD} = 4.5 V, V_{DD} = 5.5 V, T_A = 25°C	–1.5	–	1.5	%
LIFETIME DRIFT						
Sensitivity Lifetime Drift [1]	E_{SENS_LT}	Based on six-sigma drift of worst-case distribution observed after AEC-Q100 qualification stresses	–2.3	±1.2	2.3	%
Quiescent Voltage Output Lifetime Drift [1]	V_{QVO_LT}	Based on six-sigma drift of worst-case distribution observed after AEC-Q100 qualification stresses	–18	±10	18	mV

[1] Validated by design and characterization.
[2] See the Layout Guidelines section of this datasheet and the technical support documentation on the ACS37220 product page of the Allegro website.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

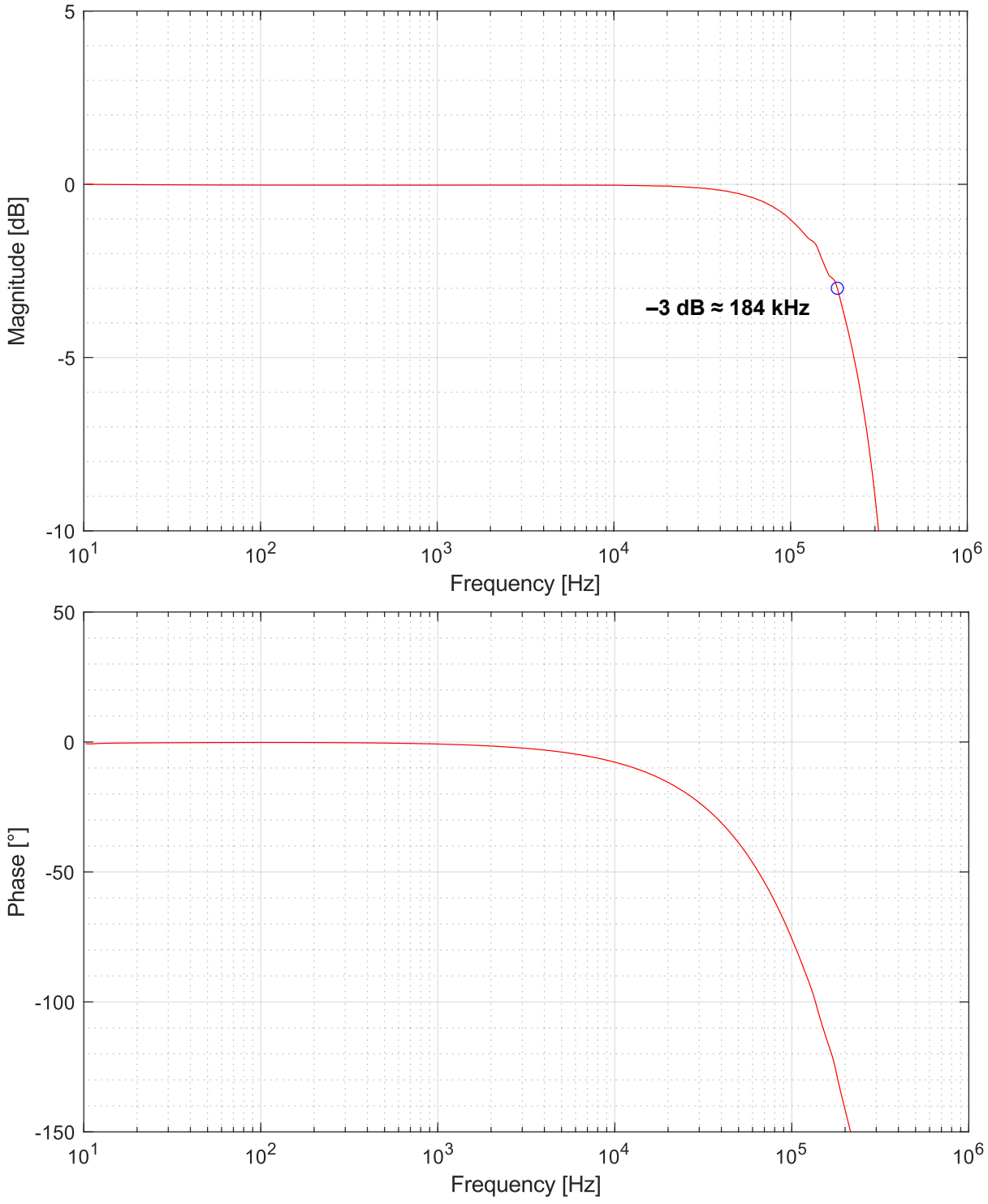
ACS37220LEZATR-200B5 PERFORMANCE CHARACTERISTICS: Valid through the full operating temperature range, T_A = –40°C to 150°C, C_{BYPASS} = 0.1µF, and V_{DD} = 5 V, unless specified otherwise. Minimum and maximum values are tested in production.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
NOMINAL PERFORMANCE						
Current Sensing Range [1]	I_P	Limited by $T_{J(MAX)}$ = 165°C	–200	–	200	A
Sensitivity [2]	Sens	$I_{P(Min)} < I_P < I_{P(Max)}$	–	10	–	mV/A
Quiescent Voltage Output	V_{QVO}	I_P = 0 A	–	2.5	–	V
Overcurrent FAULT Threshold	I_{OC}	V_{VOC} = 1 V or $V_{VOC} < V_{VOC_L}$	–	200	–	A
OVERCURRENT FAULT OUTPUT						
Overcurrent FAULT Error	I_{OC_E}	V_{VOC} = 1 V, T_A = 25°C	–24	–	24	A
ERROR COMPONENTS						
Sensitivity Error [2]	E_{SENS}	On Allegro evaluation board, T_A = 25°C, T_A = –40°C, T_A = 150°C	–1.8	–	1.8	%
Quiescent Voltage Output Error	V_{QVO_E}	I_P = 0 A, T_A = 25°C, T_A = –40°C, T_A = 150°C	–10	–	10	mV
Sensitivity Temperature Drift	E_{SENS_T}		–	±1.4	–	%
Quiescent Voltage Output Temperature Drift	V_{QVO_T}		–	±6	–	mV
Noise	N	T_A = 25°C, C_{L_VOUT} = 1 nF, BW = 150 kHz	–	3.2	–	mV_{RMS}
Power Supply Offset Error	V_{OE_PS}	V_{DD} = 4.5 V, V_{DD} = 5.5 V, T_A = 25°C	–15	–	15	mV
Power Supply Sensitivity Error	E_{SENS_PS}	V_{DD} = 4.5 V, V_{DD} = 5.5 V, T_A = 25°C	–1.5	–	1.5	%
LIFETIME DRIFT						
Sensitivity Lifetime Drift [1]	$E_{SENS_H_LT}$	Based on six-sigma drift of worst-case distribution observed after AEC-Q100 qualification stresses	–2.3	±1.2	2.3	%
Quiescent Voltage Output Lifetime Drift [1]	V_{QVO_LT}	Based on six-sigma drift of worst-case distribution observed after AEC-Q100 qualification stresses	–18	±10	18	mV

[1] Validated by design and characterization.
[2] See the Layout Guidelines section of this datasheet and the technical support documentation on the ACS37220 product page of the Allegro website.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

ACS37220 TYPICAL FREQUENCY RESPONSE



Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

RESPONSE CHARACTERISTICS DEFINITIONS

Response Time (t_{RESP})

The time interval between a) when the sensed input current reaches 90% of its full-scale value, and b) when the sensor output, V_{OUT}, reaches 90% of its full-scale output value.

Propagation Delay (t_{PD})

The time interval between a) when the sensed input current reaches 20% of its full-scale value, and b) when the sensor output, V_{OUT}, reaches 20% of its full-scale output value.

Rise Time (t_R)

The time interval between a) when the sensor output, V_{OUT}, reaches 10% of its full-scale value, and b) when the sensor output, V_{OUT}, reaches 90% of its full-scale value.

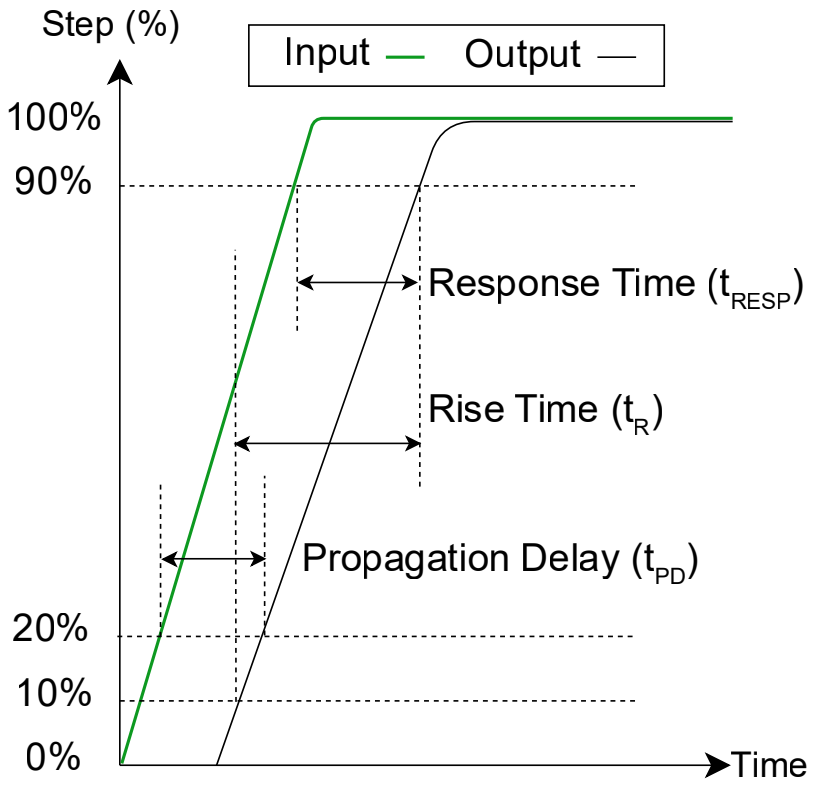


Figure 4: Step Response Characteristics

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

FUNCTIONAL DESCRIPTION OF POWER ON/OFF OPERATION

Introduction

The graphs in this section show the behavior of V_{OUT} as V_{DD} increases to greater than or reduces to less than the required power-on voltage. The same labeling convention for different voltage thresholds is used in Figure 5 and Figure 6. References in brackets "[ ]" are valid for each of these graphs.

Power-On Operation

As the supply voltage, V_{DD}, ramps up, the VOUT pin is in a high-impedance state (high-Z) until V_{DD} reaches and passes V_{POR} [1]. Once V_{DD} has passed V_{POR} [1], VOUT enters typical operation and starts responding to applied current, I_P.

Power-Off Operation

As V_{DD} reduces to less than $V_{POR} - V_{POR_HYS}$, the outputs enter a high-Z state. The hysteresis on the power-on voltage prevents noise on the supply line from causing V_{OUT} to repeatedly enter and exit the high-Z state at approximately the V_{POR} level.

NOTE: Because the device enters a high-Z state and does not drive the output in that state, the time it takes the output to reach a steady state depends on the external circuitry.

Voltage Thresholds

POWER-ON VOLTAGE (V_{POR})

The power-on voltage, V_{POR}, is the supply voltage at which the current sensor enters typical operation and the analog output pin VOUT starts to respond to the applied current, I_P.

POWER-ON RESET HYSTERESIS (V_{POR_HYS})

When the supply voltage reduces to less than $V_{POR} - V_{POR_HYS}$ [2] while the sensor is in operation, the digital circuitry turns off and the analog output enters a high-Z state. After V_{DD} recovers and exceeds V_{POR} [1], the output enters typical operation after a delay of t_{PO}.

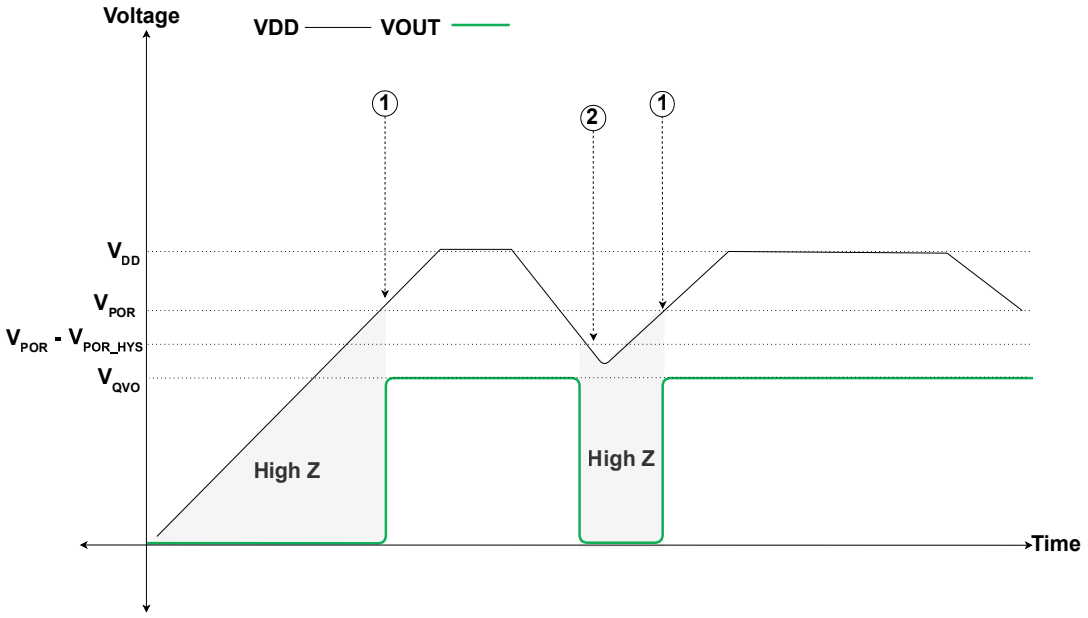


Figure 5: Power-On and Power-Off Operation

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Timing Thresholds

POWER-ON DELAY (t_{PO})

When the supply voltage reaches V_{POR} [1], the device requires a finite time to power its internal components before the outputs are released from the high-impedance state and start to respond to the measured current, I_P. Power-on time, t_{PO}, is defined as the time it takes for the output voltage to settle within ±10% of its steady-state value in the presence of an applied current, I_P, which can be observed as the time from [1] to [A] in Figure 6.

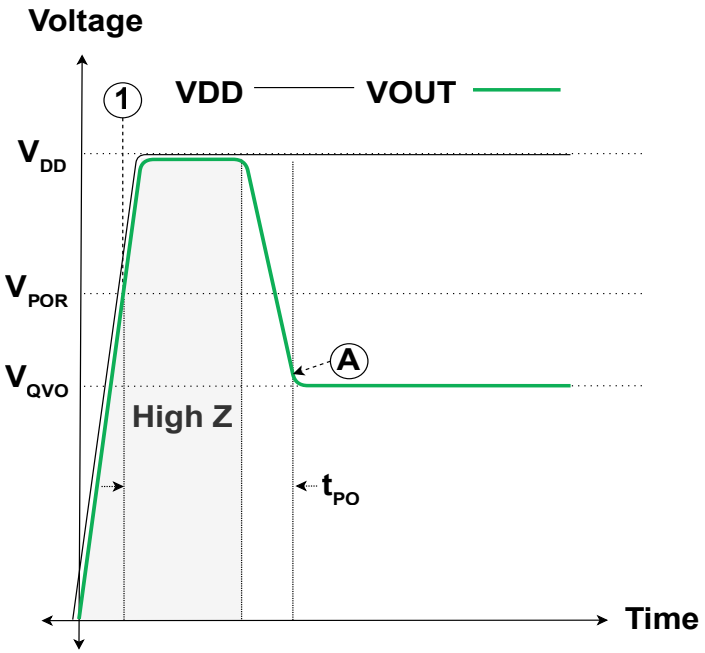


Figure 6: Power-On Delay, t_{PO}

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

DEFINITIONS OF OPERATING AND PERFORMANCE CHARACTERISTICS

Quiescent Voltage Output (V_{QVO})

Quiescent voltage output, V_{QVO}, is defined as the voltage on the analog output pin, VOUT, when current is not applied, $I_P = 0$.

Quiescent Voltage Output Error (V_{QVO_E})

Quiescent voltage output error, V_{QVO_E}, is defined as the deviation of V_{QVO} from the nominal target value.

Quiescent Voltage Output Temperature Drift (V_{QVO_T})

Quiescent voltage output temperature drift, V_{QVO_T}, is defined as the maximum deviation of V_{QVO} in the temperature range T_A= –40°C to 150°C, from its value at T_A= 25°C, based on population mean ±3-sigma temperature drifts.

OUTPUT SATURATION VOLTAGE (V_{SAT_H} and V_{SAT_L})

Output saturation voltage, V_{SAT}, is defined as the low or high voltage that V_{OUT} does not exceed. V_{SAT_H} is the highest voltage the output can reach, and V_{SAT_L} is the lowest.

NOTE: A change in sensitivity does not change the V_{SAT} points.

Sensitivity (Sens)

Sensitivity (Sens) is defined as the ratio of the V_{OUT} swing to the current through the primary conductor, I_P. The current causes a voltage change on V_{OUT} away from V_{QVO} until V_{SAT}. The magnitude and direction of the output voltage is proportional to the magnitude and direction of the current, I_P. The proportional relationship between output voltage and current is sensitivity, defined as:

$$Sens = [\, V_{OUT}(I_{P1}) - V_{OUT}(I_{P2}) \,] / [\, I_{P1} - I_{P2} \,]$$

where I_{P1} and I_{P2} are two different currents, and $V_{OUT}(I_{P1})$ and $V_{OUT}(I_{P2})$ are the respective output voltages, VOUT, at those currents.

Sensitivity Error (E_{SENS})

Sensitivity error, E_{SENS}, is the deviation of sensitivity from the nominal sensitivity target value in production testing.

Sensitivity Temperature Drift (E_{SENS_T})

Sensitivity temperature drift, E_{SENS_T}, is defined as the maximum deviation of Sens in the temperature range T_A= –40°C to 150°C, from its value at T_A= 25°C, based on population mean ±3-sigma temperature drifts.

Lifetime Drift (E_{SENS_LT} and V_{QVO_LT})

Sensitivity lifetime drift, E_{SENS_LT}, and quiescent voltage output lifetime drift, V_{QVO_LT}, derive from the worst-case distribution observed during population testing under AEC-Q100 qualification stresses at T_A= 25°C, T_A= –40°C, and T_A= 150°C. Lifetime drift is the change of Sens or V_{QVO} from its prestress value. The minimum and maximum limits are population mean ±6 sigma, and the typical specification is mean ±3 sigma.

Power Supply Sensitivity Error (E_{SENS_PS})

Power supply sensitivity error, E_{SENS_PS}, is defined as the percent change in Sens when V_{DD} varies within the specified test voltages.

Power Supply Offset Error (V_{OE_PS})

Power supply offset error, V_{OE_PS}, is defined as the change in V_{QVO} when V_{DD} varies within the specified test voltages.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

OVERCURRENT FAULT FUNCTION

The overcurrent fault function pulls the open-drain FAULT pin low when the applied current, I_P, exceeds a set threshold, I_{OC}. The threshold I_{OC} is adjustable via the VOC pin. Overcurrent fault activates symmetrically for positive and negative applied currents.

Voltage Overcurrent Pin (VOC)

The VOC pin is a voltage input that is used to set the overcurrent fault threshold, I_{OC}. There are two ways to set the threshold: 1) via a resistor, R_{L_VOC}, between VOC and GND, or 2) via an external low-impedance voltage source connected to the VOC pin.

The ACS37220 has an internal factory-calibrated 10 µA current source at VOC. To set the voltage at VOC via V_{VOC} [V] = R_{L_VOC} [Ω] × 10^{-5} [A], connect a resistor between VOC and GND. R_{L_VOC} must be chosen such that V_{VOC} is between 0.5 V and 2 V for 5 V supply variants, or between 0.33 V and 1.321 V for 3.3 V supply variants. The relationship between V_{VOC} and I_{OC} is shown in Table 1. I_{OC} is set as a percentage of the full-scale sensing range of the device, $I_{P(Max)}$, and can be between 50% $I_{P(Max)}$ and 200% $I_{P(Max)}$.

Additionally, the VOC pin has an internal voltage comparator and, when $V_{VOC} < V_{VOC_L}$, the device internally sets I_{OC} = 100% $I_{P(Max)}$.

Table 1: Overcurrent Fault Threshold, I_{OC}, As Set By V_{VOC}

V_{VOC} (V)		I_{OC} (%$I_{P(Max)}$)
5 V variants	3.3 V variants	
< V_{VOC_L}		100
0.5	0.33	50
0.75	0.466	75
1	0.661	100
1.25	0.86	125
1.5	0.991	150
1.75	1.156	175
2	1.321	200

The voltage at VOC can also be set using an external low-impedance voltage source that overdrives the internal 10 µA current source of the pin. If the application does not require the threshold to be adjusted once the sensor is in operation, it is recommended to use a low-tolerance resistor to set I_{OC}.

VOC INPUT LINEAR OPERATING RANGE (V_{OR_VOC})

VOC input linear operating range, V_{OR_VOC}, is the voltage range for V_{VOC} in which the overcurrent fault threshold, I_{OC}, varies linearly with V_{VOC}. I_{OC} can be set between 50% $I_{P(Max)}$ and 200% $I_{P(Max)}$ within the VOC input linear operating range.

VOC INPUT LOW VOLTAGE (V_{VOC_L})

VOC input low voltage, V_{VOC_L}, is defined as the voltage at the VOC pin, less than which the overcurrent fault threshold is internally set to I_{OC} = 100% $I_{P(Max)}$.

OVERCURRENT FAULT OUTPUT ERROR (E_{OC})

Overcurrent fault error, E_{OC}, is defined as the difference between the set threshold, I_{OC}, and the measured current, I_P, at which the overcurrent fault activates.

OVERCURRENT FAULT HYSTERESIS (I_{OC_HYST})

Overcurrent fault hysteresis, I_{OC_HYST}, is defined as the required decrease of I_P less than I_{OC} before assertion at the FAULT pin clears. This can be observed as the difference between levels [9] and [10] in Figure 7.

OVERCURRENT FAULT RESPONSE TIME (t_{OC_RESP})

Overcurrent fault response time, t_{OC_RESP}, is defined as the time between when the current reaches the set threshold I_{OC} and when the FAULT pin reduces to less than V_{FAULT_L}.

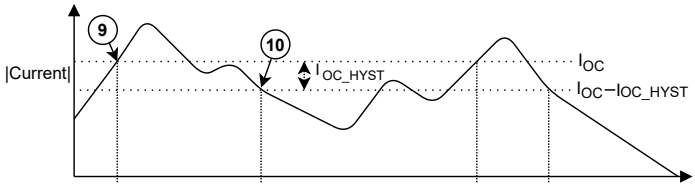


Figure 7: Overcurrent Fault Hysteresis

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

LAYOUT GUIDELINES

Introduction

The ACS37220 is factory-calibrated to achieve the specified typical sensitivity when placed on the ACS37220 evaluation board (ACSEVB-EZ7). Use of the sensor on a PCB with substantially different layout or layer stack-up than the ACSEVB-EZ7 can lead to systemic shifts of the typical value for sensitivity, Sens, specified in this datasheet. Design support files for the ACSEVB-EZ7 are available for download from the Allegro website.

When the sensor is mounted on a PCB, four important factors might cause a shift in the typical value for Sens:

- PCB layer stack-up
- Trace layout for measured current
- Thickness of the solder layer
- Voids in the solder layer at pins 1 and 2 (IP+ and IP–).

Design support files to minimize sensitivity shifts due to PCB layout and solder variability are available for download from the Allegro website. For more information, see the technical documents section of the ACS37220 website.

Solder Stencil Grid and Voids

Voids in the solder on pins 1 and 2 (IP+ and IP–) increase the resistance of the solder joints, reduce heat conduction to the PCB, and cause a shift in sensitivity. Voids can develop from solder flux outgassing. Trapped gas requires an escape route to under the package during reflow soldering. To help create a path for outgassing, a grid can be added in the solder stencil. For an example solder stencil, see Figure 8.

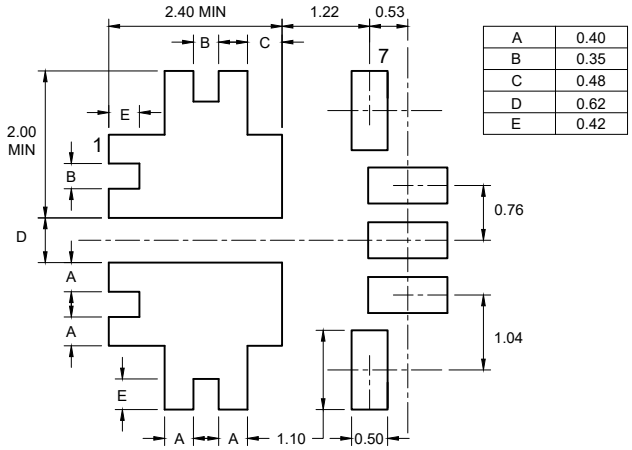


Figure 8: Example Solder Stencil for ACS37220

PCB Layout and Stack-Up

To minimize PCB layout-induced sensitivity shifts, it is recommended to use the general trace layout for the measured current as in the ACSEVB-EZ7. The measured current should enter the package from the sides, not at an angle; and the ACS37220 should be placed in the middle of traces that extend symmetrically on all sides. See Figure 9 and the design support document about how to minimize sensitivity shifts due to PCB layout in the technical documents section of the ACS37220 website.

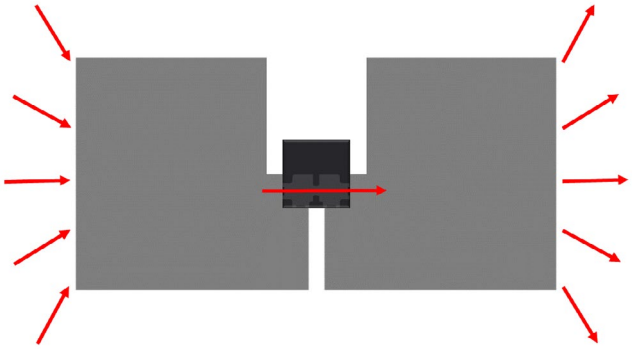


Figure 9: Recommended Trace Layout and Current Flow for IP+ and IP– Pins

To minimize the heat sink on the signal-side of the sensor, the GND and VDD pins should not be connected by a direct via to a ground or power layer. Instead, pins 3 to 7 should have a narrow trace with a length of at least 4 mm, as shown in Figure 10. This ensures low heat conduction on the signal side of the IC package and prevents thermal gradients on the die.

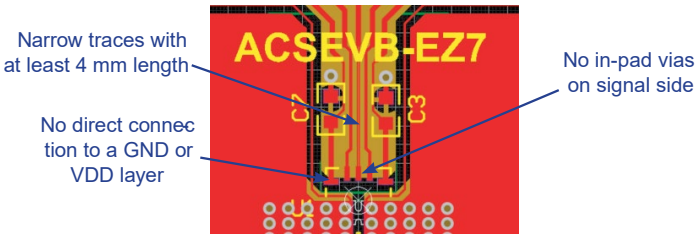


Figure 10: Top Layer of EZ Package Evaluation Board

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

THERMAL PERFORMANCE

In-Pad Vias and Thermal Management

Resistive heating due to the flow of electrical current in the package should be considered during the thermal design of the application. The sensor, PCB, and PCB terminals can generate heat and act as a heat sink.

The thermal response is highly dependent on the PCB layout, copper thickness, cooling method, and profile of the injected current (including peak current, current on-time, and duty cycle).

In-pad vias help improve thermal performance. To reduce electrical resistance and improve heat conduction to the PCB, vias can be placed under the copper pads for pins 1 and 2 (IP+ and IP–). See Figure 11 and Figure 12. The ACSEVB-EZ7 is designed with in-pad vias.

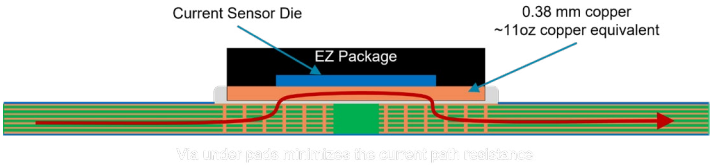


Figure 11: With In-Pad Vias

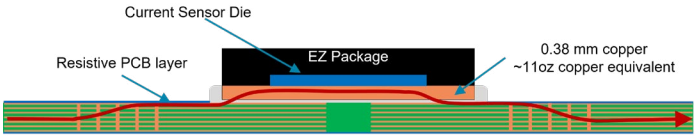


Figure 12: Without In-Pad Vias

Figure 13 shows the measured rise in steady-state die temperature of ACS37220 versus DC continuous current at an ambient temperature of 25°C for two board designs: with filled in-pad vias and without in-pad vias.

Figure 14 shows the measured rise in steady-state die temperature of ACS37220 versus DC continuous current at ambient temperatures of 25°C and 125°C.

The thermal performance of ACS37220 must always be verified in the specific conditions of the application. The maximum junction temperature of the sensor, $T_{J(MAX)}$ = 165°C, must not be exceeded.

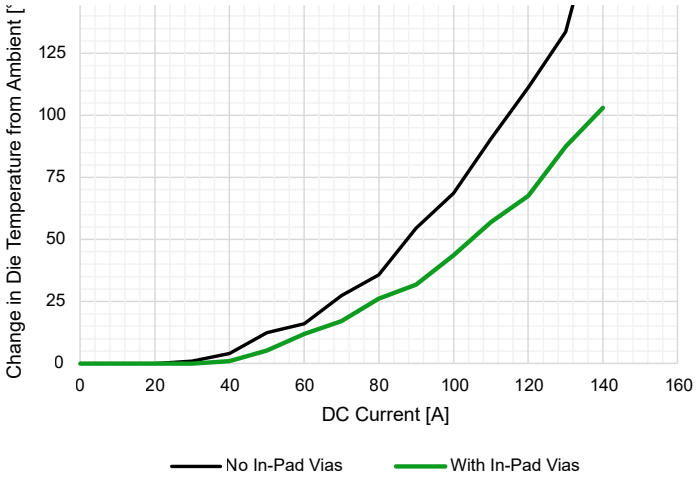


Figure 13: Comparison of Die-Temperature Increase with and without In-Pad Vias at T_A = 25°C

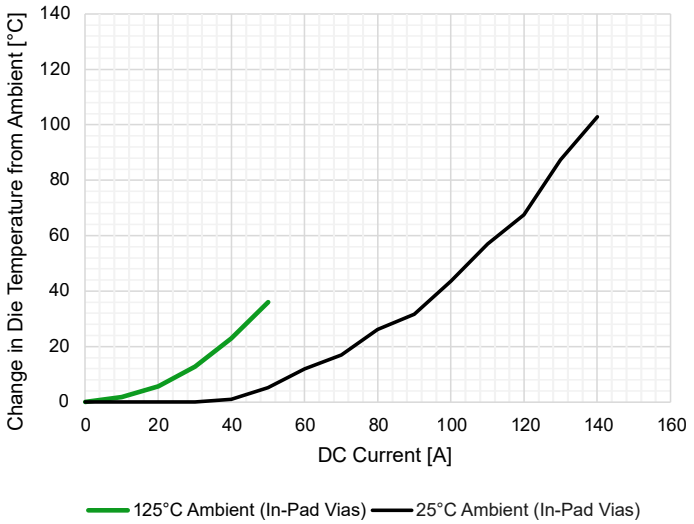


Figure 14: Comparison of Die-Temperature Increase at T_A = 25°C and T_A = 125°C, with In-Pad Vias

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Evaluation Board Layout

The reported thermal performance and nominal sensitivity are based on data collected using the EZ current sensor evaluation board (ACSEVB-EZ7, TED-0004114) shown in Figure 15.

Design support files for the ACSEVB-EZ7 are available for download from the Allegro website. For more information, see the technical documents section of the ACS37220 website.

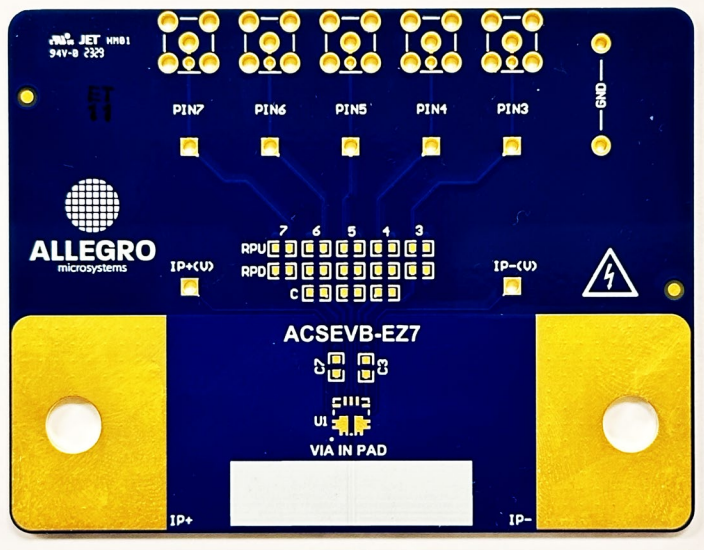
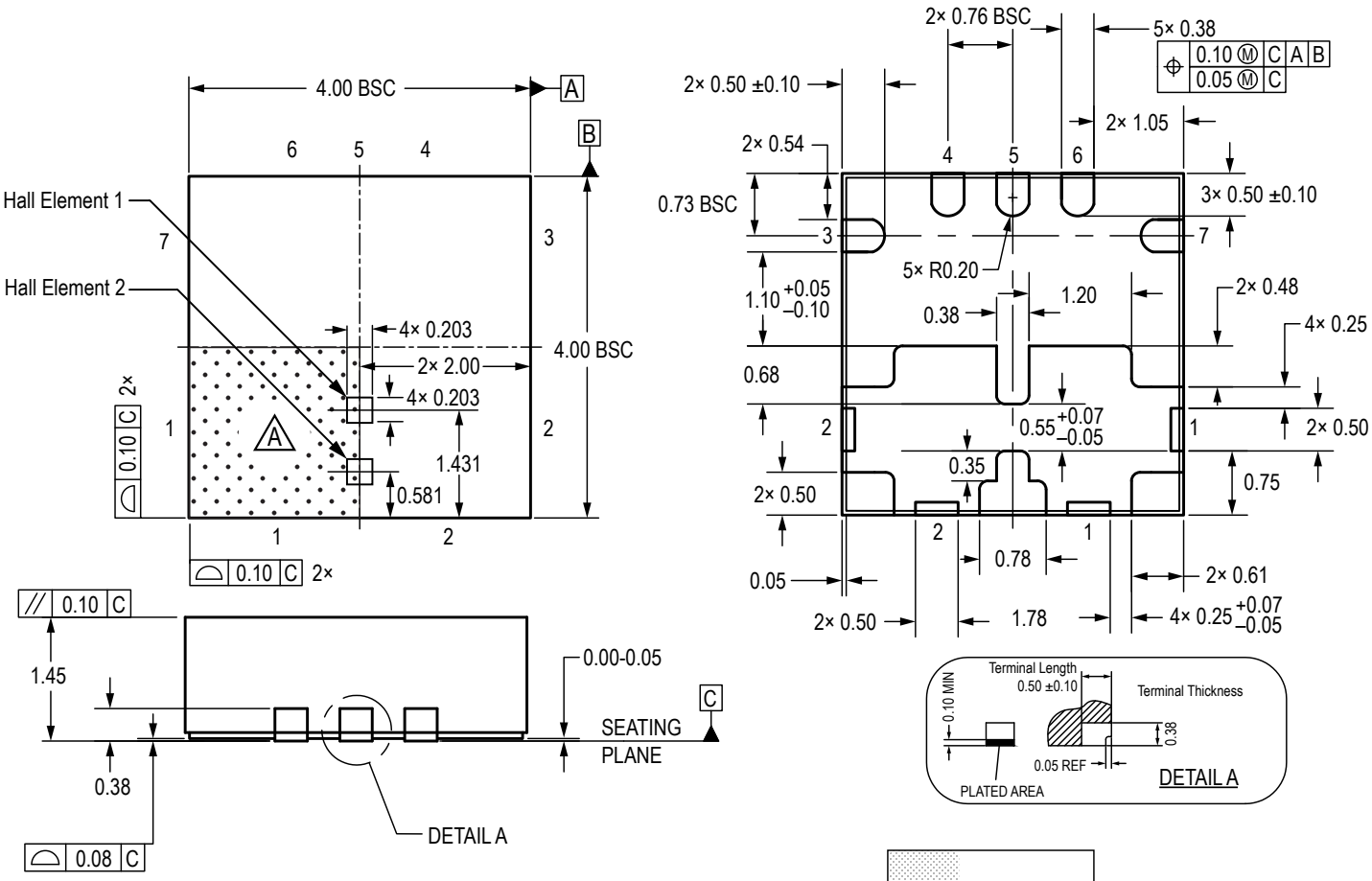


Figure 15: EZ Package Allegro Evaluation Board

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PACKAGE OUTLINE DRAWING



For Reference Only; not for tooling use
(Reference Allegro DWG-0000853, Rev. 2, PRELIMINARY)
Dimensions in millimeters; unspecified tolerances are ±0.05 mm
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Branding scale and appearance at supplier discretion

B Standard Branding Reference View

Line 1: Part Number
Line 2: 4-Digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Pin 1 Dot top left
Center align

Figure 16: 7-pin QFN with Wettable Flank (Suffix EZ)

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

REVISION HISTORY

Number	Date	Description
–	February 16, 2024	Initial release
1	February 29, 2024	Updated Features & Benefits (page 1)
2	September 3, 2024	Updated sensitivity error and sensitivity error including lifetime drift in Performance Characteristics tables (pages 6 – 10)
	November 18, 2024	Changed sensitivity error including lifetime drift to sensitivity lifetime drift, changed and quiescent voltage output error including lifetime drift to quiescent voltage output lifetime drift, and updated minimum and maximum specifications and added typical values (pages 6 – 10); and made minor editorial changes throughout (all pages).
3	March 13, 2025	Updated selection guide and part numbering schema (page 2) and minor editorial updates
4	June 5, 2025	Updated selection guide and part numbering schema (page 2), updated performance characteristics table titles (pages 6–9)

Copyright 2025, Allegro MicroSystems.
Allegro MicroSystems reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.
Allegro's products are not to be used in any devices or systems, including but not limited to life support devices or systems, in which a failure of Allegro's product can reasonably be expected to cause bodily harm.
The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.
Copies of this document are considered uncontrolled documents.

For the latest version of this document, visit our website:
www.allegromicro.com

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com