ASEK720, Board, Demo, SOIC16

85-0804-002-FAB
Originator: S. Upton

FAB Drawing / FAB Notes and Requirements

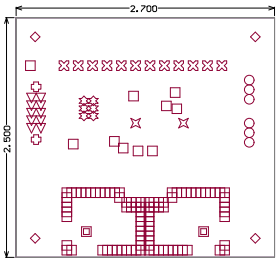
Rev 1
7/28/2015

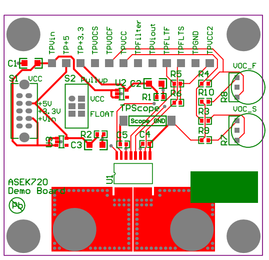
Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	TopPaste				
2	TopOverlay				
3	TopSolder	Solder Resist	0.40mil	3.5	
4	TopLayer	Copper	2.80mil		
5	Dielectricl	FR-4	17.87mil	4	
6	Signal Layer 1	Copper	1.42mil		
7	Dielectric 3		17.87mil	4.2	
8	Signal Layer 2	Copper	1.42mil		
9	Dielectric 2		17.87mil	4.2	
10	BottomLayer	Copper	2.80mil		
11	BottomSolder	Solder Resist	0.40mil	3.5	
12	BottomOverlay				
13	BottomPaste				

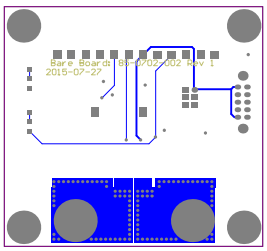
Symbol	Hit Count	Finished Hole Size	Plated	Hole Type
✖	2	56.00mil (1.422mm)	PTH	Round
✪	2	61.02mil (1.550mm)	PTH	Round
⊠	2	266.00mil (6.756mm)	PTH	Round
◇	4	125.00mil (3.175mm)	PTH	Round
○	6	28.00mil (0.711mm)	PTH	Round
⊕	6	42.00mil (1.067mm)	PTH	Round
▽	10	31.50mil (0.800mm)	PTH	Round
⊠	12	62.00mil (1.575mm)	PTH	Round
□	102	15.00mil (0.381mm)	PTH	Round
	146 Total			

1. Finished PCB is RoHS
2. Dimensions are in inches, unless otherwise noted.
3. Applicable Standards:
   - 3a. Manufacture in accordance to IPC-6011, IPC-6012 for Class 2 applications.
   - 3b. PCB shall meet acceptance criteria as required for Class 2 PCB as defined in IPC-600
   - 3c. UL Approved to a minimum catagory of 94V0.
4. Laminate:
   - 4a. Thickness: 0.062inch +/- 10%
   - 4b. Type: high temp FR4
   - 4c. this line left blank
   - 4d. Core/prepreg thickness:
     - 4d.1. See chart to left.
     - 4d.2. Core/prepreg thicknesses to be roughly uniform thickness or +/-5mil from indicated
     - 4d.3. No impedance controlled stackup required
5. Copper:
   - 5a. Layer Count: 4
   - 5b. Exterior layers: 2oz min
   - 5c. Interior layers: 1oz min
   - 5d. Plated through holes: plate to 1mil min copper thickness
   - 5e. Trace separation: 10mil
   - 5f. Trace min width: 10mil
   - 5g. Line width reduction due to pinholes nicks or shrinking: 20% max.
   - 5h. No impedance controlled route used; no trace width adjustment required.
6. this line left blank
7. Total board flatness shall not exceed 0.002inch per inch.
8. Artwork layer registration shall be within 0.003inch total.
9. Surface Finish:
   - 9a. Immersion Gold
   - 9b. No hard gold required, no *.gm8 nor *.gm9 layer provided
10. Soldermask:
    - 10a. Top/Bottom soldermask required
    - 10b. Soldermask color shall be green.
    - 10c. Soldermask finish may be matte or glossy.
11. Silkscreen
    - 11a. Top/bottom silkscreen required.
    - 11b. Silkscreen color shall be white.
    - 11c. Min silkscreen line width: 8mil
    - 11d. Epoxy or acrylic ink allowed
12. Drill holes:
    - 12a. No blind or buried vias.
    - 12b. Hole sizes are specified after plating.
    - 12c. No via in pad used. No via filling required.
13. Mill separate or V-score according to mech1 (*.gm1) layer.
14. Electrical testing required.
15. Contact information:
    - 15a. Shawn Upton supton@allegromicro.com, 603.626.2429
    - 15b. If fast turn board, 24hr contact info: N/A

Mechanical Layer 1 *.gml is Board Outline, slots and circular cutouts
Mechanical Layer 2 *.gm2 is footprint notes (not for fab house)
Mechanical Layer 3 *.gm3 is hole location guide
Mechanical Layer 4 *.gm4 is board outline dimensions
Mechanical Layer 5 *.gm5 is topside labels (if no silk)
Mechanical Layer 6 *.gm6 is bottomside labels (if no silk)
Mechanical Layer 7 *.gm7 is FAB drawing notes
Mechanical Layer 8 *.gm8 is top selective hard gold
Mechanical Layer 9 *.gm9 is bottom selective hard gold
Mechanical Layer 10 and up are not for usage by PCB board house
*.gto and *.gbo are top and bottom layer silkscreen (aka overlay)
*.gts and *.gbs are top and bottom soldermask
*.drl is NC Drill
*.apr is aperature file
*.gpb and *.gpt are pad master layers, and are not used (ignore if in zip file)
Keepout layer *.gko is for internal usage only, and is not to be used by board house




TPVin
TP+5
TP+3.3
TPVOCS
TPVOCF
TPVCC
TPFilter
TPViout
TPFLTF
TPFLTS
TPGND
TPVCC2
C1
S1
VCC
+5V
+3.3V
+Vin
S2
Pullup
VCC
FLOAT
U2
C2
R1
R5
R6
R4
R10
R3
R9
R8
R7
VOC_F
VOC_S
TPScope
Scope GND
R2
C3
C5
C4
U1
ASEK720
Demo Board
Pb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