

POWER IC PACKAGE PORTFOLIO

POWER INTEGRATED CIRCUITS

Allegro's power IC packages offer industry-leading thermal performance with limited board space.

TSSOP: Industry-standard TSSOP with optional exposed pad for enhanced thermal performance

QFP: Universal quad flat pack with exposed pad for enhanced thermal performance

**QFN/
TDFN:** Quad and dual, low-profile, surface-mount packages with exposed pad for enhanced thermal performance (wettable flank options available)

MSOP: Industry-standard miniature small outline package with optional exposed pad for enhanced thermal performance

SOIC: Small outline integrated circuit with optional exposed pad for enhanced thermal performance

CSP: Wafer level chip scale

Additional industry-standard packaging options are available to meet individual design requirements.

With Leads

JP (QFP with exposed pad)
Terminals: 32, 48
Size: 7 x 7 mm body width



LV, LP (TSSOP with exposed pad)
Terminals: 16-38
Size: 4.4 mm body width



LB (SOIC)
Terminals: 16-28
Size: 7.5 mm body width



LJ (SOIC with exposed pad)
Terminals: 8-10
Size: 3.9 mm body width

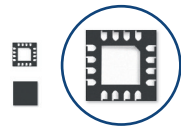


LY/LZ (MSOP with exposed pad)
Terminals: 10
Size: 3 mm body width

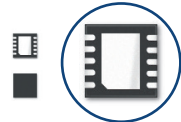


Without Leads

ES, EC, ET, EU, EV (QFN with exposed pad)
Terminals: 16-48
Size: 3 x 3 mm body width to 7 x 7 mm body width

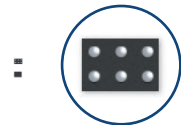


EJ (TDFN with exposed pad)
Terminals: 3-16
Size: 2 x 2 mm body to 3 x 3 mm body width



Chip Scale

CG (Chip Scale)
Terminals: 4-12



Please Note: Package sizes are photographed to show relative scale.