Fully Integrated PMIC for Safety-Related Systems with Buck-Boost PreRegulator, 5× Linear Regulators, and SPI

FEATURES AND BENEFITS

- A²-SIL™ product: Developed as a hardware safety element out of context with ASIL D capability for use in automotive safety-related systems
- Automotive AEC-Q100 Grade 0 qualified
- Wide input range: 3.2 to 36 V V_{IN} operating, 40 V V_{IN} maximum
- 2.2 MHz synchronous buck-boost preregulator (VREG: 5.35 V) with internal compensation
- Five internal linear regulators with fold-back short-circuit protection
  - □ VUC: 3.3 V or 5 V (selectable by a pin) regulator for microcontroller
  - □ VLDOA: 5 V (or 3.3 V factory option) general-purpose low-dropout (LDO) regulator
  - □ VLDOB: 5 V or 3.3 V (selectable by a pin) always-on LDO regulator
  - □ VLDOP1 and VLDOP2: Two programmed (5 V or 3.3 V) and enabled via serial-port-interface (SPI) LDO regulators with short-to-battery protection for remote sensors
- Pulse-width watchdog (PWWD), window watchdog

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DESCRIPTION

The A81411 is a power-management integrated circuit (IC) that integrates a buck-boost preregulator, five LDOs, and many safety features. The preregulator uses a buck-boost topology to efficiently convert automotive battery voltages into a tightly regulated intermediate voltage complete with control, diagnostics, and protections.

The output of the preregulator supplies a 600 mA linear regulator that can output 5 V or 3.3 V (VUC), a 5 V (or 3.3 V factory option) 200 mA linear regulator (VLDOA), and two 5 V or 3.3 V/150 mA linear regulators (VLDOP1 and VLDOP2) that are protected when shorted to battery. Designed to supply power for microprocessors, sensors, and CAN transceivers, the A81411 is ideal for under-the-hood applications. A fifth always-on LDO (VLDOB) can supply 50 mA at either 5 V or 3.3 V.

Two automotive-battery-rated enable inputs are available on the A81411. An additional logic-level enable is also available for control via a microcontroller unit (MCU).

Diagnostic outputs from the A81411 include watchdog fault (WD_Fn), power-on reset (NPOR), fault flag (FFn) to alert the microprocessor that a fault has occurred, and gate-driver enable (POE)

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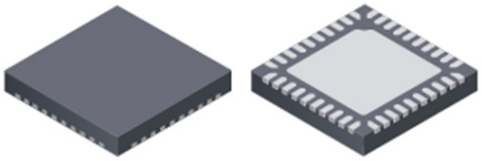
APPLICATIONS

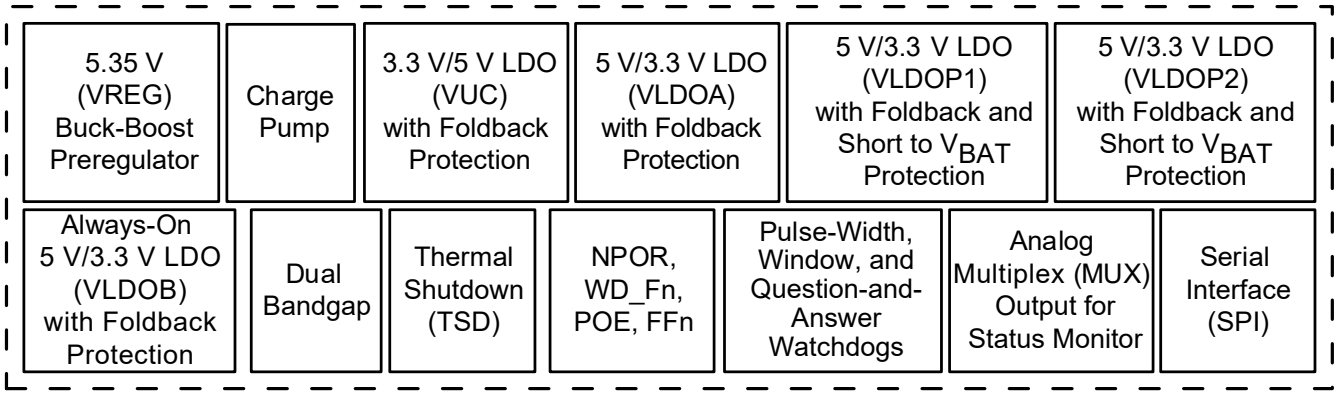
Provides system power for microcontroller/DSP, CAN, sensors, etc. in automotive-control modules, such as:

- Power steering
- Braking
- Transmission
- Onboard charger (OBC)/ DC-to-DC/inverter
- Other automotive applications

PACKAGE



40-pin QFN (suffix EV) 6 mm × 6 mm
Not to scale



Simplified Functional Block Diagram

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FEATURES AND BENEFITS

(WWD), and question-and-answer watchdog (QAWD)
- Control and diagnostic reporting through secure SPI
  - □ 16-bit data transfers
  - □ 5-bit cyclic redundancy check (CRC)
  - □ 3-bit frame counter
  - □ 5-bit request register identification (ID)
  - □ Read-back register
  - □ Chip ID
- Two high-voltage enable inputs (ENBAT and ENCAN)
- Frequency dithering and controlled slew rate help reduce electromagnetic interference (EMI) and improve electromagnetic compatibility (EMC)
- Undervoltage protection for all output rails
- Thermal shutdown protection

Continued from previous page

DESCRIPTION

The microprocessor can read fault registers through SPI.

Dual bandgaps, one for regulation and one for fault checking, improve safety coverage and fault detection of the A81411.

The A81411 contains three types of watchdog timers: pulse-width watchdog (PWWD), window watchdog (WWD), and question-and-answer watchdog (QAWD). The watchdog timers can be put into various operating states via secure SPI commands.

The A81411 is supplied in a low-profile 40-pin quad-flat no-lead (QFN) package (suffix EV) with exposed power pad and wettable flanks.

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SPECIFICATIONS

SELECTION GUIDE

Part Number	VLDOA Output Voltage	Package	Packing [1]	Lead Frame
A81411KEVGTR	5 V	40-pin QFN with thermal pad	1500 pieces per reel	100% matte tin
A81411KEVGTR-1	3.3 V			

[1] For additional packing options, contact Allegro.

ABSOLUTE MAXIMUM RATINGS [2][3]

Characteristic	Symbol	Notes	Rating	Unit
VIN, VINP	AMR_VIN, AMR_VINP		−0.3 to 40	V
VREG, VREGLDO, VUCIN	AMR_VREG, AMR_VREGLDO, AMR_VUCIN		−0.3 to 40	V
ENBAT, ENCAN	AMR_ENBAT, AMR_ENCAN		−0.3 to 40	V
	AMR_I_ENBAT, AMR_I_ENCAN		±75	mA
VUCSEL, VLDOBSEL	AMR_VUCSEL, AMR_VLDOBSEL		−0.3 to 40	V
LX1	AMR_LX1		−0.3 to V_{VIN} + 0.3	V
		t < 250 ns	−1.5	V
LX2	AMR_LX2		−0.3 to V_{VREG} + 0.3	V
		t < 250 ns	−1.5	V
CP1	AMR_CP1		– 0.3 to V_{VREG} + 0.3	V
CP2	AMR_CP2		V_{VREG} – 0.3 to 40	V
VCP	AMR_VCP		V_{VREG} – 0.6 to 40	V
BOOT1	AMR_BOOT1		V_{LX1} – 0.3 to V_{LX1} + 7	V
BOOT2	AMR_BOOT2		V_{LX2} – 0.3 to V_{LX2} + 7	V
VLDOP1, VLDOP2	AMR_VLDOPx		−0.3 to 40	V
PGND	AMR_PGND		−0.3 to 0.3	V
All Other Pins			−0.3 to 7	V
Maximum Junction Temperature	$T_{J(MAX)}$		165	°C
Storage Temperature Range	T_{stg}		−40 to 150	°C

[2] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only. Functional operation of the device at these conditions or any conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[3] All absolute maximum ratings (AMRs) shall be measured with respect to the GND pin.

ESD CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions	Min	Typ.	Max.	Unit
ESD HBM Robustness	$V_{ESD,HBM}$	ESD susceptibility to GND on all pins	–2	–	2	kV
ESD CDM Robustness	$V_{ESD,CDM}$	ESD susceptibility to GND on all pins	–500	–	500	V
	$V_{ESD,CDM,CORNER}$	ESD susceptibility to GND on corner pins	–750	–	750	V

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [4]	Value	Unit
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	QFN, 40 pin (EV) package, 4-layer printed circuit board (PCB) based on JEDEC standard	27	°C/W

[4] Additional thermal information is available on the Allegro website.

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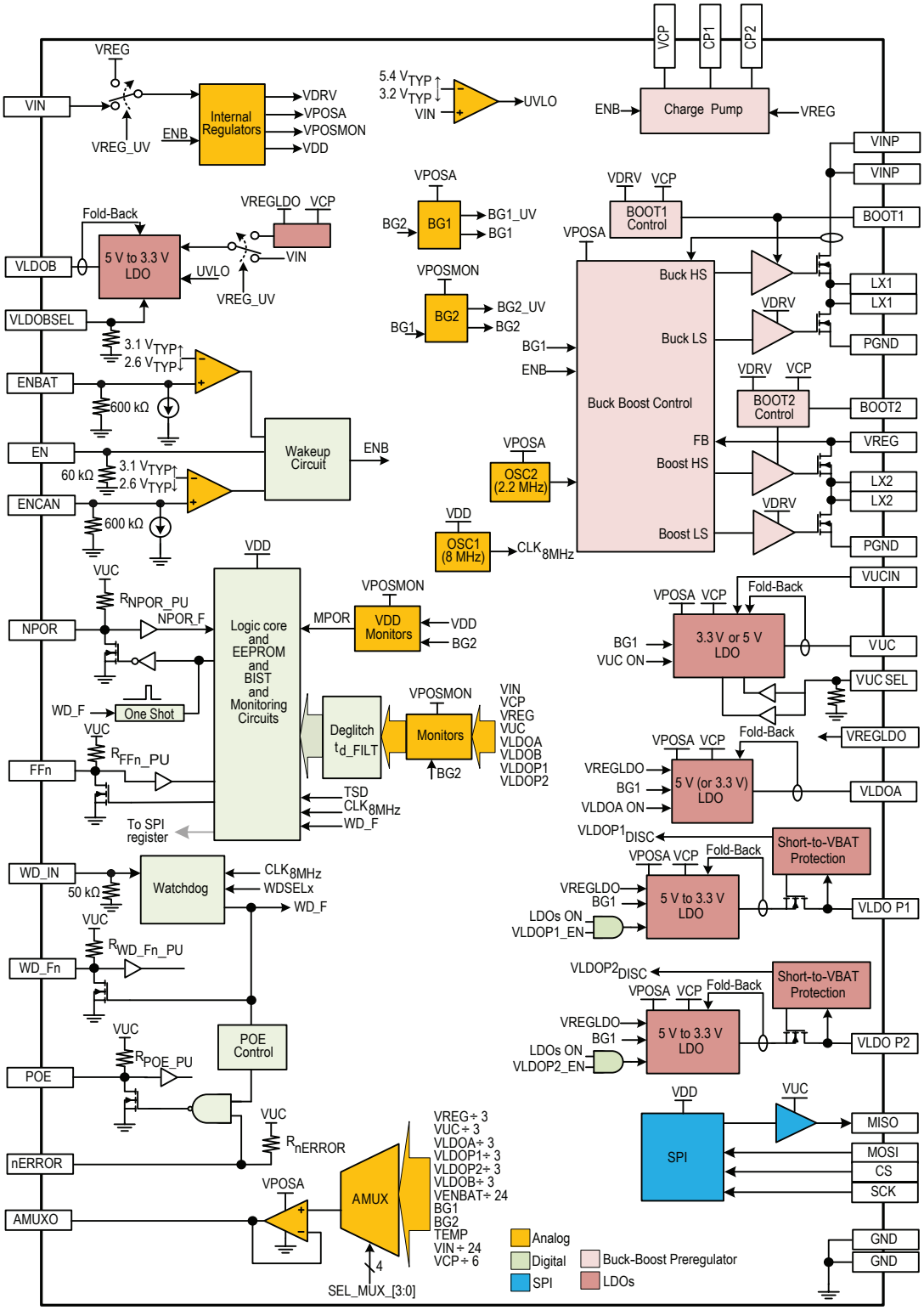
FUNCTIONAL BLOCK DIAGRAM



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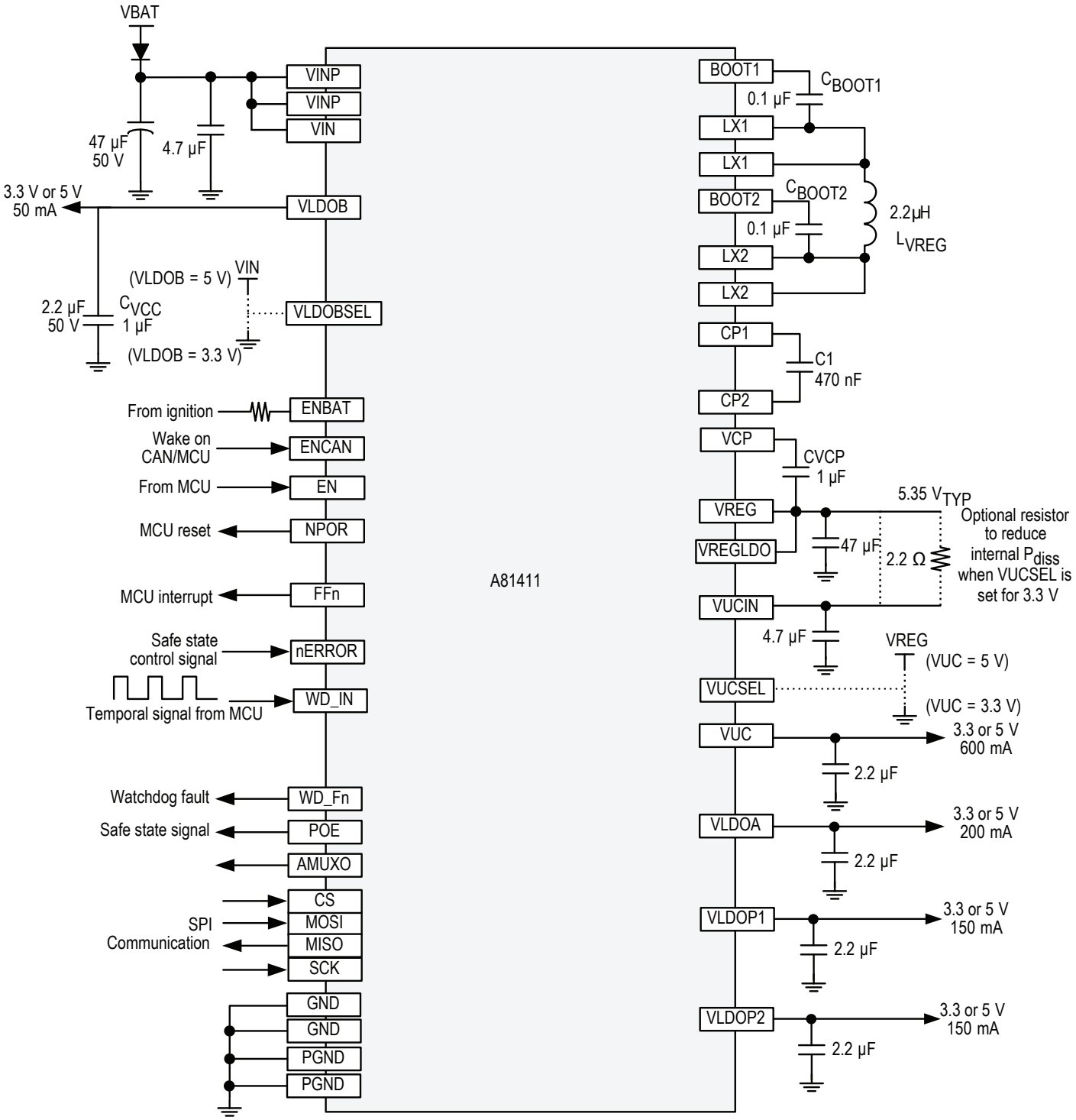
TYPICAL SCHEMATIC



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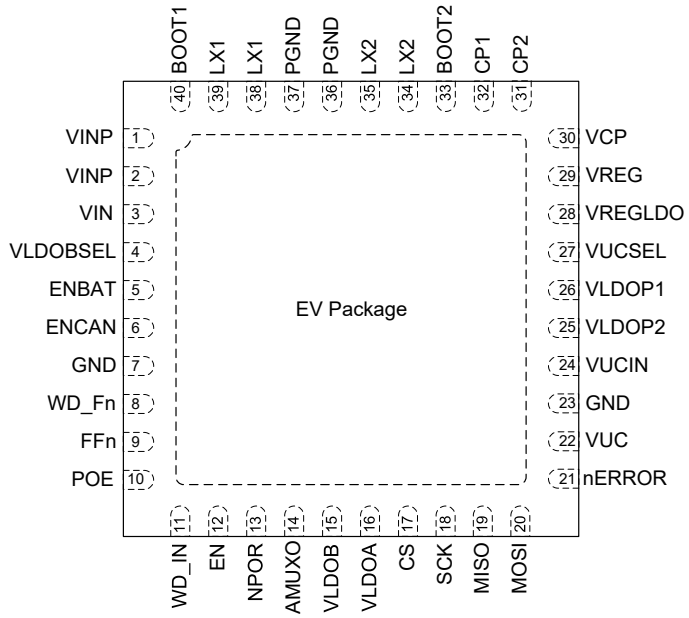
PINOUT DIAGRAMS AND TERMINAL LIST TABLE



NOTE: Pinout is subject to change. Before using pinout, contact factory.

EV Package Pinouts: 40-Pin QFN with Wettable Flank

Terminal List Table

Number	Name	Function
1,2	VINP	Input voltage pins for buck drain connection: Connect high-frequency capacitors between this pin and the PGND pin
3	VIN	Input-voltage pin for control circuits
4	VLDOBSEL	VLDOBSEL voltage selector: For 5 V output, Connect to VIN; for 3.3 V output, connect to GND or leave open Status is latched at start up
5	ENBAT	Ignition-enable input from the key, or switch, via a series resistor
6	ENCAN	High-level enable for wake by CAN
7	GND	Signal ground
8	WD_Fn	Active low, watchdog fault flag: If there is a watchdog fault, pin pulls low
9	FFn	Active low, open drain fault flag: If any fault detected, pin pulls low Signal can be used as an interrupt to MCU
10	POE	Power-on enable: Latches low to put the system into a safe state
11	WD_IN	Watchdog refresh input from MCU
12	EN	Logic-level enable: ORed with other enable pins
13	NPOR	Active-low, VUC fault detection output: If SPI programming is used, watchdog (WD) fault and/or VLDOA can be added to NPOR logic.
14	AMUXO	Analog multiplexer output
15	VLDOB	Always-on LDO 5 V or 3.3 V regulator output: Voltage selected using VLDOBSEL pin
16	VLDOA	5 V (or 3.3 V factory option) regulator output
17	CS	SPI chip-select input from the microcontroller
18	SCK	SPI clock input from the microcontroller
19	MISO	SPI data output to the microcontroller (controller input, peripheral output; MISO)
20	MOSI	SPI data input from the microcontroller (controller output, peripheral input; MOSI)
21	nERROR	Active low input that can be used to drive POE low: If not used, leave it open
22	VUC	3.3 V or 5 V regulator output: Voltage selected using VUCSEL pin
23	GND	Signal ground
24	VUCIN	Input to VUC regulator: Connect to VREG through optional external power resistor to reduce power dissipation of A81411
25	VLDOP2	5 V or 3.3 V short-to-battery protected regulator, enabled through SPI
26	VLDOP1	5 V or 3.3 V short-to-battery protected regulator, enabled through SPI
27	VUCSEL	VUC voltage selector: For 5 V output, connect to VREG; for 3.3 V output, connect to GND or leave open Status is latched at the end of VREG startup
28	VREGLDO	Voltage input to the VLDOA, VLDOPx, and VLDOB (when VREG > VREG_UV) regulators
29	VREG	Voltage feedback input of the preregulator and voltage input to the charge-pump regulator: Connect high-frequency capacitors between this pin and the PGND pins.
30	VCP	Charge-pump reservoir capacitor connection for LDO bias and boost high MOSFET at 100% on.
31	CP2	Charge-pump flying-capacitor connection, terminal 2
32	CP1	Charge-pump flying-capacitor connection, terminal 1
33	BOOT2	Boost boot capacitor
34, 35	LX2	Boost switch node
36, 37	PGND	Power ground for buck side switch. Connect high-frequency capacitors between this pin and the VIN pin
38, 39	LX1	Buck switch node
40	BOOT1	Buck boot capacitor
–	PAD	Exposed thermal pad

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ELECTRICAL CHARACTERISTICS [1]: Valid at 3.2 V ≤ V_{VIN} ≤ 36 V, –40°C ≤ T_J ≤ 150°C, V_{ENCAN} or V_{ENBAT} or V_{EN} high, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL SPECIFICATIONS						
Operating Input Voltage [2]	V_{VIN}	After both V_{VIN} > V_{VIN_START} and VREG regulating	3.2	13.5	36	V
VIN Supply Quiescent Current	I_Q	V_{VIN} = 13. 5 V, V_{VREG} = 6 V (PWM not used)	–	18	–	mA
VIN Supply Sleep Current	I_{Q_SLEEP}	V_{VIN} = 13. 5 V, V_{ENB} = low [3]; T_J = 25°C [2]; I_{VLDOB} = 0 µA	–	–	60	µA
VIN VLDOB Start Voltage	$V_{VIN\_START\_VLDOB}$	V_{VIN} rising and ENB = 0 [3]	5.7	6	6.3	V
VIN UVLO Start Voltage	V_{VIN_START}	V_{VIN} rising and ENB = 1 [3]	5.72	5.88	6.12	V
VIN VLDOB Stop Voltage	$V_{VIN\_STOP\_VLDOB}$	V_{VIN} falling and ENB = 0 [3]	4	–	5	V
VIN UVLO Stop Voltage	V_{VIN_STOP}	V_{VIN} falling and ENB = 1 [3]	2.65	2.9	3.15	V
VIN UVLO Hysteresis	V_{VIN_HYS}	V_{VIN_START} – V_{VIN_STOP}	–	2.5	–	V
VIN UVLO Detection Delay [2]	t_{d_UVLO}		7	10	13	µs
VIN Overvoltage Rising Threshold	$V_{VIN\_OV\_H}$	V_{VIN} rising	33	–	36	V
VIN Overvoltage Falling Threshold	$V_{VIN\_OV\_L}$	V_{VIN} falling	32	–	35	V
VIN Overvoltage Hysteresis	$V_{VIN\_OV\_HYS}$	$V_{VIN\_OV\_H}$ – $V_{VIN\_OV\_L}$	–	1	–	V
VIN Overvoltage Detection Delay [2]	t_{d_OV}		10	–	40	µs
VIN Input Ceramic Capacitance Range [2]	$C1_{VIN}$		2.3	4.7	–	µF
	ESR_{C1VIN}		–	–	20	mΩ
VIN Input Electrolytic Capacitance Range [2]	$C2_{VIN}$		20	47	–	µF
	ESR_{C2VIN}		250	–	–	mΩ
Internal Clock Frequency	f_{CLOCK}		7.6	8	8.4	MHz
ENABLE INPUTS: ENABLE (ENBAT AND ENCAN) INPUTS						
Enable Upper Threshold	V_{ENABLE_H}	V_{ENBAT} or V_{ENCAN} rising	2.7	3.2	3.5	V
Enable Lower Threshold	V_{ENABLE_L}	V_{ENBAT} or V_{ENCAN} falling	2.2	2.6	2.9	V
Enable Hysteresis	V_{ENABLE_HYS}	V_{ENABLE_H} – V_{ENABLE_L}	–	500	–	mV
Enable Bias Current	I_{ENABLE_BIAS}	V_{ENABLE} = 3. 5 V	–	6	50	µA
		V_{ENABLE} = 40 V	–	–	500	µA
Enable Pulldown Resistance	R_{ENABLE}	When V_{ENABLE} < 1.2 V	360	600	840	kΩ
ENBAT Delay Time	t_{d_ENBAT}	Rising and falling, time from ENBAT to ENB [3]	1	1.25	1.65	ms
ENCAN Delay Time	t_{d_ENCAN}	Rising and falling, time from ENCAN to ENB [3]	0.1	0.23	0.35	ms
ENABLE INPUTS: LOGIC ENABLE (EN) INPUT						
EN Upper Thresholds	V_{EN_H}	V_{EN} rising	–	–	2	V
EN Lower Thresholds	V_{EN_L}	V_{EN} falling	0.8	–	–	V
EN Bias Current	I_{EN_IN}	V_{EN} = 3.3 V	–	–	175	µA
EN Pulldown Resistance	R_{EN}		35	60	85	kΩ
EN Delay Time	t_{d_EN}		8	15	22	µs

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing); positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization; not production tested.
[3] ENB is the internal startup shutdown signal.

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ELECTRICAL CHARACTERISTICS (continued) [1]: Valid at 3.2 V ≤ V_{VIN} ≤ 36 V, –40°C ≤ T_J ≤ 150°C, V_{ENCAN} or V_{ENBAT} or V_{EN} high, unless otherwise specified.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VREG BUCK BOOST						
VREG Output Voltage [2]	V_{VREG}	0.1 A < I_{VREG} ≤ 1.2 A	5.25	5.35	5.45	V
		5. 5 V ≤ V_{VIN} ≤ 36 V, 0.1 A < I_{VREG} ≤ 1.6 A	5.25	5.35	5.45	V
VREG Coil [2]	L_{VREG}	Part number (P/N) XGL6030-222MEC or XEL6030-222MEC	–	2.2	–	µH
	DCR_{VREG}		–	–	20	mΩ
VREG Output Capacitor [2]	C_{VREG}	P/N KCM55QC71E476KH13	30	47	–	µF
	ESR_{CVREG}		–	–	50	mΩ
Boot Cap [2]	$C_{BOOT1\_}$ C_{BOOT2}		50	100	130	nF
	ESR_{CBOOT}		–	–	20	mΩ
Switching Frequency	f_{sw_VREG}	Dithering off, V_{VIN} falling and V_{VIN} ≤ 18 V	2	2.2	2.4	MHz
		Dithering off, V_{VIN} rising and V_{VIN} ≥ 19 V	1	1.1	1.2	MHz
Frequency Dithering	Δf_{sw_VREG}	As a percentage of f_{SW_REG}	–10	–	10	%
LX1 and LX2 Rising Slew Rate [2]	SR_{LX_RISE}	V_{VIN} = 13. 5 V, 10% to 90%, I_{VREG} = 1 A	1.5	3	4.5	V/ns
LX1 and LX2 Falling Slew Rate [2]	SR_{LX_FALL}	V_{VIN} = 13. 5 V, 90% to 10%, I_{VREG} = 1 A	1.5	3	4.5	V/ns
Buck HS MOSFET On Resistance	$R_{DS\_ON\_BUCK\_HS}$	T_J = 150°C	–	–	155	mΩ
Buck LS MOSFET On Resistance	$R_{DS\_ON\_BUCK\_LS}$	T_J = 150°C	–	–	210	mΩ
Boost LS MOSFET On Resistance	$R_{DS\_ON\_BST\_LS}$	T_J = 150°C	–	–	220	mΩ
Boost HS MOSFET On Resistance	$R_{DS\_ON\_BST\_HS}$	T_J = 150°C	–	–	155	mΩ
Soft Start Ramp Time [2]	t_{SS_VREG}		400	600	800	µs
SS PWM Frequency Foldback		V_{VREG} < 1.34 V typical	–	$f_{sw\_VREG}/4$	–	–
		1.34 V ≤ V_{VREG} < 2.68 V typical	–	$f_{sw\_VREG}/2$	–	–
		V_{VREG} ≥ 2.68 V typical	–	f_{sw_VREG}	–	–
Hiccup Recovery Time [2]	t_{HIC_REC}		–	5	–	ms
Hiccup OCP PWM Counts [2]	t_{HIC_OCP}	V_{VIN} ≤ 18 V	–	120	–	PWM cycles
		V_{VIN} ≥ 19 V	–	60	–	PWM cycles
Pulse-By-Pulse Current Limit	$I_{LIM\_ton\_min}$	Boost mode	3.3	4.085	4.8	A
		Buck mode	2.3	3	3.3	A
LX Short-Circuit Current Limit	I_{LIM_LX}	Latch off after second detection	5	7.1	–	A
VREG Overvoltage Threshold	$V_{VREG\_OV\_H}$	V_{VREG} rising, LX PWM is to be disabled	5.65	5.82	6	V
	$V_{VREG\_OV\_L}$	V_{VREG} falling, LX PWM is to be enabled	–	5.62	–	V
VREG Overvoltage Hysteresis	$V_{VREG\_OV\_HYS}$	$V_{VREG\_OV\_H}$ – $V_{VREG\_OV\_L}$	–	200	–	mV
VREG Overvoltage Detection Delay [2]	$t_{d\_VREG\_OV}$		10	–	40	µs

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing); positive current is defined as going into the node or pin (sinking).
[2] Ensured by design and characterization; not production tested.
[3] ENB is the internal startup shutdown signal.

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VREG BUCK BOOST (continued)						
VREG Undervoltage Thresholds	$V_{VREG\_UV\_H}$	V_{VREG} rising	4.5	4.75	5	V
	$V_{VREG\_UV\_L}$	V_{VREG} falling	–	4.55	–	V
VREG Undervoltage Hysteresis	$V_{VREG\_UV\_HYS}$	$V_{VREG\_UV\_H} – V_{VREG\_UV\_L}$	–	200	–	mV
VREG UV Detection Delay [2]	$t_{d\_VREG\_UV}$		10	–	40	µs
BOOTx Undervoltage Thresholds	V_{BOOT_UVH}		2.5	–	3.3	V
	V_{BOOT_UVL}		2	–	2.6	V
BOOTx Overvoltage Thresholds	V_{BOOT_OVH}		5.5	–	6.5	V
	V_{BOOT_OVL}		5	–	5.9	V
BOOTx UV Detection Delay [2]	$t_{d\_BOOT\_UV}$		–	16	–	PWM cycles
BOOTx OV Detection Delay [2]	$t_{d\_BOOT\_OV}$		–	4	–	PWM cycles
CHARGE PUMP						
CP Output Voltage	V_{VCP}	$V_{VCP} – V_{VREG}$, I_{VCP} > = –4 mA	4.1	4.7	5.4	V
CP Flying Capacitor [2]	C_{PUMP}		220	470	611	nF
	ESR_{CPUMP}		–	–	20	mΩ
VCP Output Capacitor [2]	C_{VCP}		0.7	1	1.3	µF
	ESR_{VCP}		–	–	20	mΩ
VCP Switching Frequency	f_{CPx}		–	62.5	–	kHz
VCP Startup Time	t_{VCP_START}	$V_{REG} = V_{VREG\_UV\_H}$, high to VCP = $V_{VCP\_UV\_H}$ C_{VCP} = 1 µF	–	–	2.5	ms
VCP Undervoltage Thresholds	$V_{VCP\_UV\_H}$	V_{VCP} rising, $V_{VCP} – V_{VREG}$	2.9	3.15	3.4	V
	$V_{VCP\_UV\_L}$	V_{VCP} falling	–	2.7	–	V
VCP Undervoltage Hysteresis	$V_{VCP\_UV\_HYS}$	$V_{VCP\_UV\_H} – V_{VCP\_UV\_L}$	200	400	800	mV
VCP Overvoltage Thresholds	$V_{VCP\_OV\_H}$	V_{VCP} rising, $V_{VCP} – V_{VREG}$	6	7	8	V
	$V_{VCP\_OV\_L}$	V_{VCP} falling	–	6.8	–	V
VCP Overvoltage Hysteresis	$V_{VCP\_OV\_HYS}$	$V_{VCP\_OV\_H} – V_{VCP\_OV\_L}$	160	315	470	mV
VCP UV Detection Delay [2]	$t_{d\_VCP\_UV}$		10	–	40	µs
VCP OV Detection Delay [2]	$t_{d\_VCP\_OV}$		10	–	40	µs
THERMAL SENSOR AND PROTECTION						
Thermal Warning Threshold [2]	T_{WARN}	T_J rising	150	157.5	165	°C
Thermal Shutdown Threshold [2]	T_{TSD}	T_J rising	175	–	–	°C
Thermal Warning/Shutdown Hysteresis [2]	T_{HYS}		–	15	–	°C
Thermal Warning Detection Delay [2]	t_{d_TWARN}		–	12	–	µs
Thermal Shutdown Detection Delay [2]	t_{d_TSD}		–	12	–	µs

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Characteristic	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
LDO LINEAR REGULATORS							
General							
VUC Output Voltage	V_{VUC}	10 mA ≤ I_{VUC} ≤ 600 mA	5 V	4.9	5	5.1	V
			3.3 V	3.23	3.3	3.37	V
VUCIN Input Capacitance Range [2]	C_{VUCIN}			2.3	4.7	–	µF
	ESR_{CVUCIN}			–	–	20	mΩ
VUC Output Capacitance Range [2]	C_{VUC}			1	–	50	µF
	ESR_{CVUC}			–	–	20	mΩ
VLDOA Output Voltage	V_{VLDOA}	5 mA ≤ I_{VLDOA} ≤ 200 mA	5 V	4.9	5	5.1	V
		5 mA ≤ I_{VLDOA} ≤ 200 mA, A81411KEVTR-T-1	3.3 V	3.23	3.3	3.37	V
VLDOA Output Capacitance Range [2]	C_{VLDOA}			1	–	15	µF
	ESR_{CVLDOA}			–	–	20	mΩ
VLDOB Output Voltage	V_{VLDOB}	1 mA < I_{VLDOB} ≤ 50 mA	5 V	4.9	5	5.1	V
			3.3 V	3.23	3.3	3.37	V
		0.1 mA < I_{VLDOB} ≤ 10 mA, after V_{VIN} > V_{VIN_START} V_{VIN} ≥ 5.2 5 V and V_{VREG} < $V_{VREG\_UV\_L}$	5 V	4.5	5	5.25	V
			3.3 V	3.05	3.3	3.55	V
VLDOB Output Capacitance Range [2]	C_{VLDOB}			1	–	15	µF
	ESR_{CVLDOB}			–	–	20	mΩ
VLDOPx Output Voltage	V_{VLDOPx}	5 mA < I_{VLDOPx} ≤ 150 mA	5 V	4.9	5	5.1	V
			3.3 V	3.23	3.3	3.37	V
VLDOPx Output Capacitance Range [2]	C_{VLDOPx}			1	–	15	µF
	ESR_{CVLDOP}			–	–	20	mΩ
VUC Overcurrent Protection							
VUC Current Limit	I_{VUC_LIM}			–700	–900	–1100	mA
VUC Foldback Current	I_{VUC_FBK}	V_{VUC} = 0 V		–60	–125	–220	mA
VUC Overcurrent Detection	I_{VUC_OC}			–650	–790	–930	mA

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
LDO LINEAR REGULATORS (continued)						
VLDOA Overcurrent Protection						
VLDOA Current Limit	I_{VLDOA_LIM}		–250	–350	–450	mA
VLDOA Foldback Current	I_{VLDOA_FBK}	V_{VLDOA} = 0 V	–25	–50	–75	mA
VLDOA Overcurrent Detection	I_{VLDOA_OC}		–240	–305	–370	mA
VLDOB Overcurrent Protection						
VLDOB Current Limit	I_{VLDOB_LIM}		–57	–80	–105	mA
		V_{VIN} = 13. 5 V, V_{ENB} = low [3], and V_{VREG} < $V_{VREG\_UV\_L}$	–	–40	–	mA
VLDOB Foldback Current	I_{VLDOB_FBK}	V_{VLDOB} = 0 V, V_{VREG} > $V_{VREG\_UV\_H}$	–2	–5	–15	mA
VLDOB Overcurrent Detection	I_{VLDOB_OC}		–50	–74	–98	mA
VLDOPx Overcurrent Protection (x = 1, 2)						
VLDOPx Current Limit	I_{VLDOPx_LIM}		–175	–250	–325	mA
VLDOPx Foldback Current	I_{VLDOPx_FBK}	V_{VLDOPx} = 0 V	–25	–40	–70	mA
VLDOPx Overcurrent Detection	I_{VLDOPx_OC}		–170	–218	–266	mA
VUC, VLDOA, VLDOPx Startup Timing (x = 1, 2)						
VUC Startup Time (5 V OUT) [2]	t_{VUC_START}	C_{VUC} = 2.2 µF ± 20%, load = 13 Ω ± 10%	–	0.15	1	ms
VUC Startup Time (3.3 V OUT) [2]	t_{VUC_START}	C_{VUC} = 2.2 µF ± 20%, load = 9 Ω ± 10%	–	0.13	0.65	ms
VLDOA Startup Time [2]	t_{VLDOA_START}	C_{VLDOA} = 2.2 µF ± 20%, load = 34 Ω ± 10%	–	0.15	1	ms
VLDOPx Startup Time [2]	t_{VLDOPx_START}	C_{VLDOPx} = 2.2 µF ± 20%, load = 42 Ω ± 10%	–	0.15	1	ms
VUC, VLDOA, VLDOPx Shutdown Delay (x = 1, 2)						
VUC Shutdown Delay Time	$t_{VUC\_OFF\_DLY}$		10	–	–	µs
VLDOx Shutdown Delay Time	$t_{VLDOx\_OFF\_DLY}$		10	–	–	µs

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
LDO ENABLES AND MONITORS						
VUC/VLDOB Voltage Select (VUCSEL/VLDOBSEL)						
VUCSEL High Threshold	V_{VUCSEL_H}	V_{UC} = 5 V	–	–	2	V
VUCSEL Low Threshold	V_{VUCSEL_L}	V_{UC} = 3.3 V	0.8	–	–	V
VUCSEL Pull-Down Resistor	R_{VUCSEL}		–	50	–	kΩ
VLDOBSEL High Threshold	$V_{VLDOBSEL\_H}$	V_{LDOB} = 5 V	–	–	2	V
VLDOBSEL Low Threshold	$V_{VLDOBSEL\_L}$	V_{LDOB} = 3.3 V	0.8	–	–	V
VLDOBSEL Pull-Down Current	$I_{VLDOBSEL}$	V_{VIN} = 13.5 V and ENx = 0	–	–	2	µA
VUC, VLDOA, VLDOB, VLDOPx Undervoltage Detection Thresholds (x = 1, 2)						
VUC, VLDOA, VLDOB and VLDOPx 5 V Undervoltage Thresholds	$V_{5\_UV\_H}$	V_{VLDOx} rising	–	4.68	–	V
	$V_{V5\_UV\_L}$	V_{VLDOx} falling	4.5	4.65	4.8	V
VUC, VLDOA, VLDOB and VLDOPx 5 V Undervoltage Hysteresis	$V_{V5\_UV\_HYS}$	$V_{V5\_UV\_H} – V_{V5\_UV\_L}$	–	30	–	mV
VUC, VLDOA, VLDOB and VLDOPx 3.3 V Undervoltage Thresholds	$V_{3V3\_UV\_H}$	V_{3V3} rising	–	3.12	–	V
	$V_{3V3\_UV\_L}$	V_{3V3} falling	3.01	3.1	3.19	V
VUC, VLDOA, VLDOB and VLDOPx 3.3 V Undervoltage Hysteresis	$V_{3V3\_UV\_HYS}$	$V_{3V3\_UV\_H} – V_{3V3\_UV\_L}$	–	20	–	mV
LDO Undervoltage Detection Delay [2]	t_{d_UV}		10	–	40	µs
VUC, VLDOA, VLDOB, VLDOPx Overvoltage Detection Thresholds (x = 1, 2)						
VUC, VLDOA, VLDOB, and VLDOPx 5 V Overvoltage Thresholds	$V_{V5\_OV\_H}$	5 V LDO output voltage rising	5.15	5.3	5.45	V
	$V_{V5\_OV\_L}$	5 V LDO output voltage falling	–	5.27	–	V
VUC, VLDOA, VLDOB, and VLDOPx 5 V Overvoltage Hysteresis	$V_{V5\_OV\_HYS}$	$V_{V5\_OV\_H} – V_{V5\_OV\_L}$	–	30	–	mV
VUC, VLDOA, VLDOB, and VLDOPx 3.3 V Overvoltage Thresholds	$V_{3V3\_OV\_H}$	3.3 V LDO output voltage rising	3.39	3.49	3.59	V
	$V_{3V3\_OV\_L}$	3.3 V LDO output voltage falling	–	3.47	–	V
VUC, VLDOA, VLDOB, and VLDOPx 3.3 V Overvoltage Hysteresis	$V_{3V3\_OV\_HYS}$	$V_{3V3\_OV\_H} – V_{3V3\_OV\_L}$	–	20	–	mV
LDO Overvoltage Detection Delay [2]	t_{d_OV}		10	–	40	µs
VUC AMR Overvoltage Thresholds	$V_{VUC\_AMR\_OV\_H}$	V_{UC} voltage rising	6	6.3	6.6	V
	$V_{VUC\_AMR\_OV\_L}$	V_{UC} voltage falling	–	6.15	–	V
VUC AMR Overvoltage Hysteresis	$V_{VUC\_AMR\_OV\_HYS}$		50	175	300	mV
VUC AMR Overvoltage Detection Delay [2]	$t_{d\_VUC\_AMR\_OV}$		–	5	–	µs

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ANALOG MULTIPLEXER (AMUXO)						
AMUXO Output Source Current	I_{AMUXO_SRC}		–3.5	–	–	mA
AMUXO Output Sink Current	I_{AMUXO_SINK}		0.13	–	–	mA
AMUX Output Voltage Range	V_{AMUXO}		0.1	–	2	V
AMUX Ratio 1/1 Voltage Accuracy	Acc_R1	BG1, BG2 voltages	–1	–	1	%
AMUX Ratio 1/3 Voltage Accuracy	Acc_R3	VREG, LDO voltages	–1	–	1	%
AMUX Ratio 1/6 Voltage Accuracy	Acc_R6	VCP voltages	–2.5	–	2.5	%
AMUX Ratio 1/24 Voltage Accuracy	Acc_R24	VIN, VENBAT voltages	–2.6	–	2.6	%
AMUX Ratio TEMP Accuracy [2]	Acc_TEMP	IC junction temperature sensor	–3	–	3	%
AMUX Output Offset	AMUX_OFF		–22	–	31	mV
NPOR AND FFN OUTPUTS						
NPOR Output Low Voltage	V_{NPOR_L}	I_{NPOR} = 4 mA	–	150	400	mV
		V_{VIN} = 5. 5 V, I_{NPOR} = 2 mA	–	–	200	mV
NPOR Internal Pull-Up	R_{NPOR_PU}	Pull up to VUC	7	10	13	kΩ
NPOR Leakage Current	I_{NPOR_LKG}	V_{NPOR} = VUC	–	–	2	µA
NPOR One-Shot Low Time After Watchdog Fault [2]	t_{WD_FAULT}	Enabled via SPI using the NPOR_KEY	1.6	2	2.4	ms
NPOR One-Shot Low Time After MCU Self-Reset [2]	$t_{MIN\_NPOR\_LOW}$		1.6	2	2.4	ms
NPOR Turn-On Delay [2]	$t_{d\_NPOR\_ON}$	Time from VUC > $V_{3V3\_UV\_H}$ (or $V_{V5\_UV\_H}$) to when the NPOR pin becomes high impedance	1.6	2	2.4	ms
FFn Output Voltage	V_{FFn_L}	FFn is tripped, I_{FFn} = 2 mA	–	150	400	mV
FFn Leakage Current	I_{FFn_LKG}	V_{FFn} = 3.3 V or 5 V	–	–	2	µA
FFn Internal Pull-Up	R_{FFn_PU}	Pull up to VUC	7	10	13	kΩ

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
WATCHDOG, POE, NERROR, BIST						
WD_Fn Output Voltage	$V_{WD\_Fn\_L}$	WD_Fn is tripped, I_{WD_Fn} = 2 mA	–	150	400	mV
WD_Fn Leakage Current	$I_{WD\_Fn\_LKG}$	V_{WD_Fn} = VUC	–	–	2	µA
WD_Fn Internal Pull-Up	$R_{WD\_Fn\_PU}$	Pull up to VUC	7	10	13	kΩ
WD_IN Upper Threshold	V_{WDIN_H}	V_{WD_IN} rising	–	–	2	V
WD_IN Lower Threshold	V_{WDIN_L}	V_{WD_IN} falling	0.8	–	–	V
WD_IN Pull-Down Resistance	$R_{WD\_IN\_PU}$		30	50	70	kΩ
Watchdog Configuration Timeout [2]	t_{CONFIG_WD}	Can be bypassed by setting WD_SEL bits	–	250	–	ms
POE Output Voltage	V_{POE_L}	I_{POE} = 4 mA	–	150	400	mV
POE Internal Pull-Up	R_{POE_PU}	Pull up to VUC	7	10	13	kΩ
POE Leakage Current	I_{POE_LKG}	V_{NPOR} = VUC	–	–	2	µA
nERROR Enable High Threshold	V_{nERROR_H}		–	–	2	V
nERROR Enable Low Threshold	V_{nERROR_L}		0.4	–	–	V
nERROR Enable Pull-Up Resistance	R_{nERROR_PU}		38.5	55	71.5	kΩ
Logic BIST Duration [2]	t_{LBIST}		15	16	17	ms
Analog BIST Duration [2]	t_{ABIST}		–	–	0.2	ms

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SERIAL INTERFACE (SPI)						
Input Low Voltage (CSn, MOSI, SCK)	V_{IL}		–	–	0.8	V
Input High Voltage (CSn, MOSI, SCK)	V_{IH}	All logic inputs	2	–	–	V
Input Hysteresis (CSn, MOSI, SCK)	V_{hys}	All logic inputs	100	–	400	mV
MOSI Input Internal Pull-Down	R_{MOSI_PD}		30	50	70	kΩ
SCK Input Internal Pull-Down	R_{SCK_PD}		30	50	70	kΩ
CSn Input Internal Pull-Up	$R_{WD\_IN\_PU}$	Pull up to VUC	30	50	70	kΩ
MISO Output Low Voltage	V_{OL}	I_{OL} = 1 mA [2]	–	–	0.4	V
MISO Output High Voltage	V_{OH}	I_{OH} = –1 mA [2]	0.8 × V_{VUC}	–	–	V
SPI Clock Frequency [2]	f_{SCK}	MISO pins, CL = 20 pF	0.1	–	10	MHz
SPI Frame Rate [2]	f_{SPI}		2.94	–	294	kHz
Clock High Time	t_{SCK_H}	A in Figure 1	50	–	–	ns
Clock Low Time	t_{SCK_L}	B in Figure 1	50	–	–	ns
Chip-Select Lead Time	t_{CS_LD}	C in Figure 1	30	–	–	ns
Chip-Select Lag Time	t_{CS_LG}	D in Figure 1	30	–	–	ns
Chip-Select High Time	t_{CS_H}	E in Figure 1	400	–	–	ns
Data Out (MISO) Enable Time [2]	t_{MISO_EN}	F in Figure 1	–	–	40	ns
Data Out (MISO) Disable Time [2]	t_{MISO_D}	G in Figure 1	–	–	30	ns
Data Out (MISO) Valid Time from SCK Falling [2]	t_{MISO_V}	H in Figure 1	–	–	40	ns
Data Out (MISO) Hold Time from SCK Falling [2]	t_{MISO_H}	J in Figure 1	5	–	–	ns
Data In (MOSI) Setup Time to SCK Rising	t_{MOSI_SU}	K in Figure 1	15	–	–	ns
Data In (MOSI) Hold Time from SCK Rising	t_{MOSI_H}	L in Figure 1	10	–	–	ns

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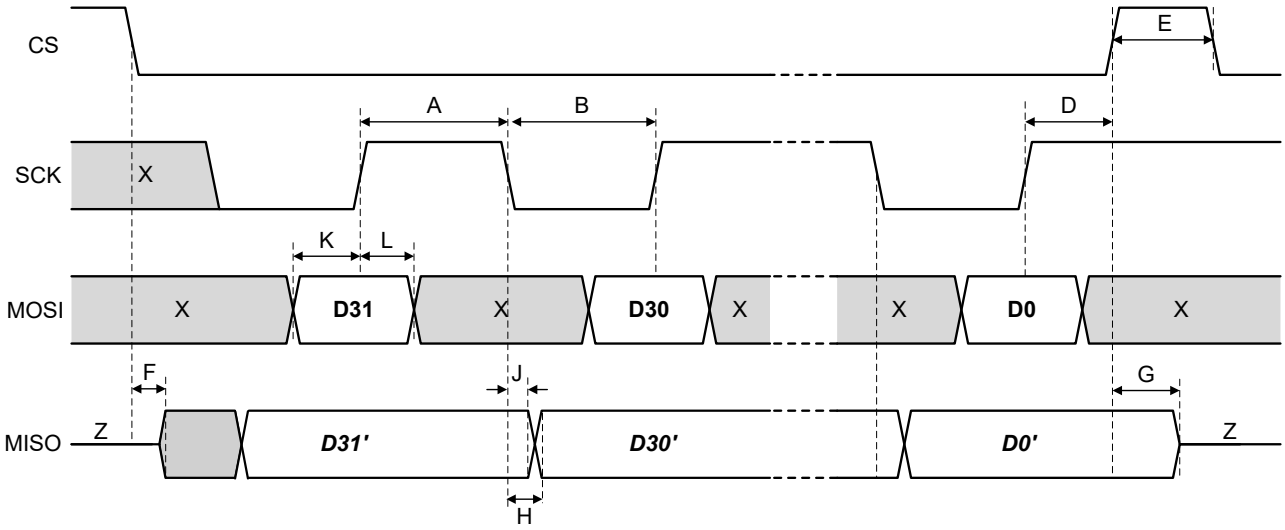

MISO activity assumes the CHIP_ID from the previous frame is correct.

Figure 1: Serial Interface Timing for Write and Read Cycles

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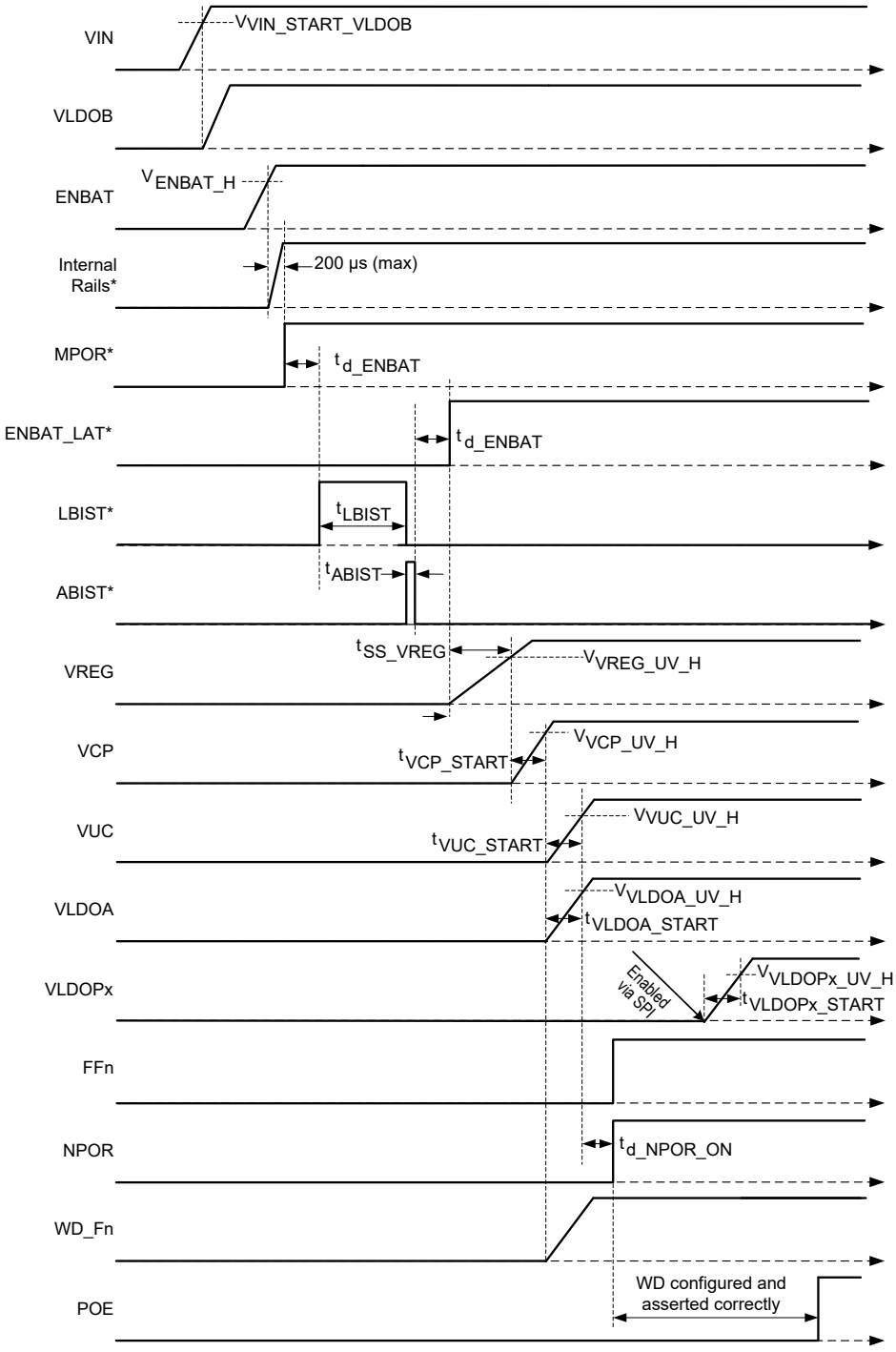
CHARACTERISTIC PERFORMANCE

Timing Diagrams



*** = Internal signal**

Figure 2: Startup by ENBAT, Timing Diagram

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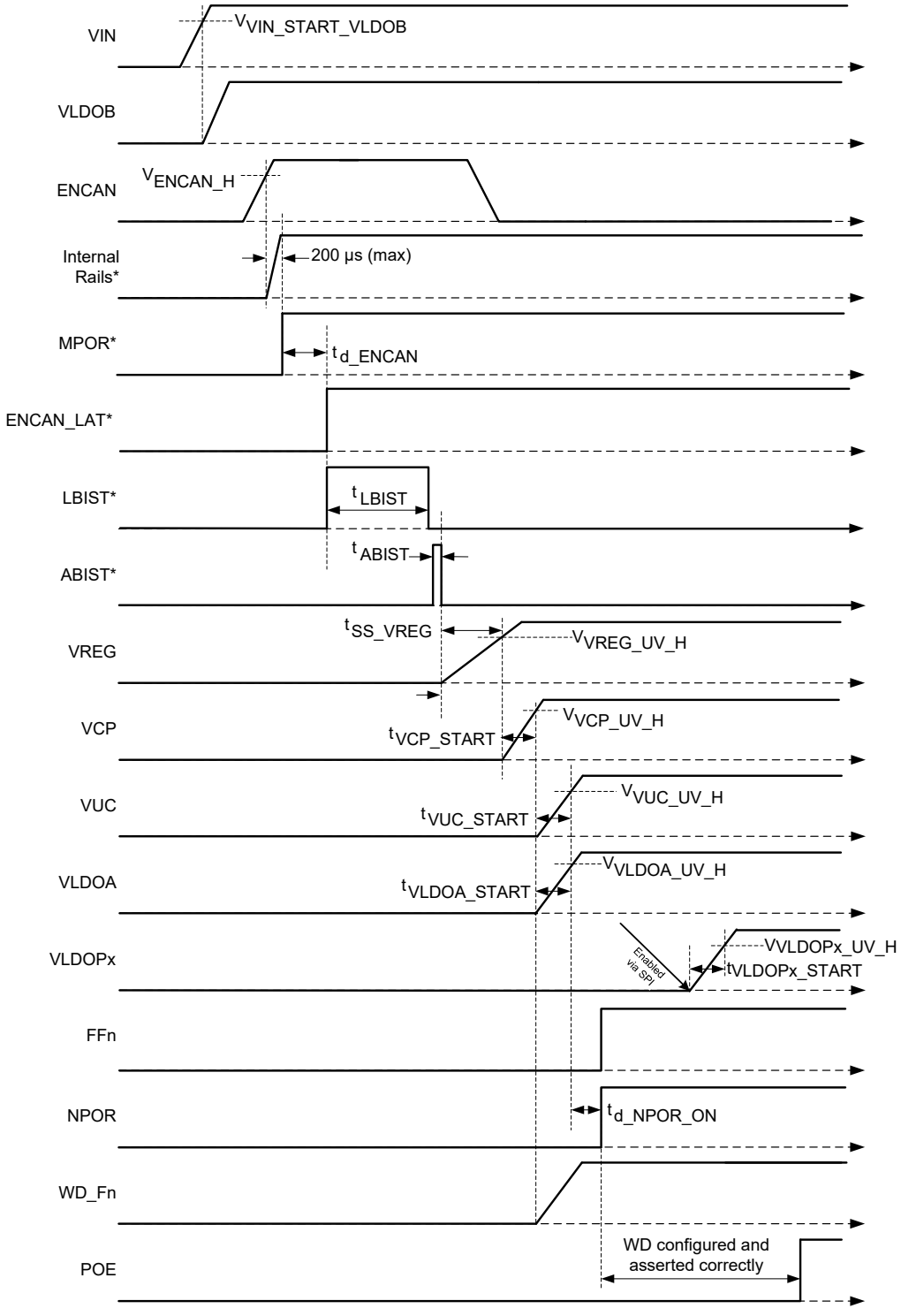

*** = Internal signal**

Figure 3: Startup by ENCAN, Timing Diagram

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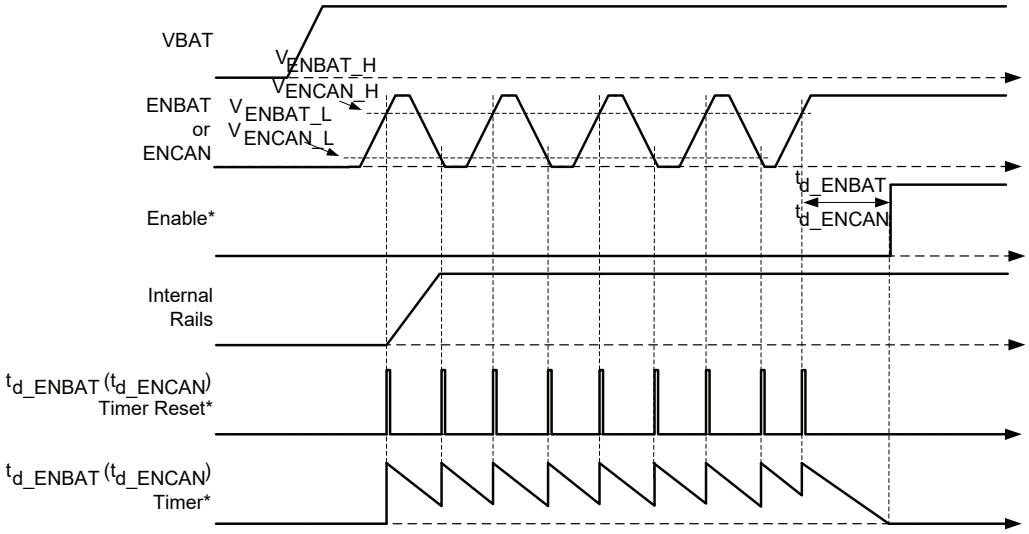
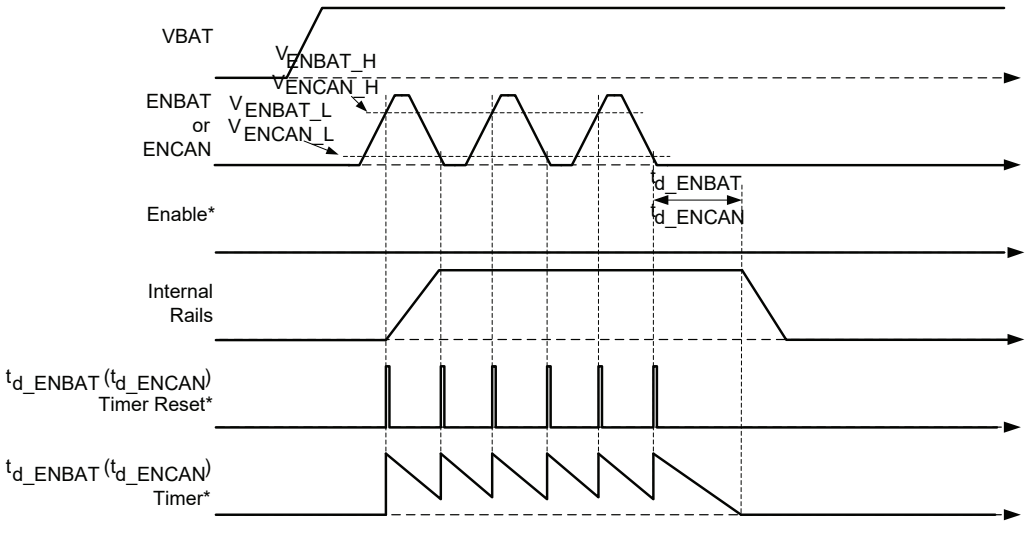


* = Internal signal

Figure 4: Oscillating ENBAT (ENCAN) Signal With Startup



* = Internal signal

Figure 5: Oscillating ENBAT (ENCAN) Signal Without Startup

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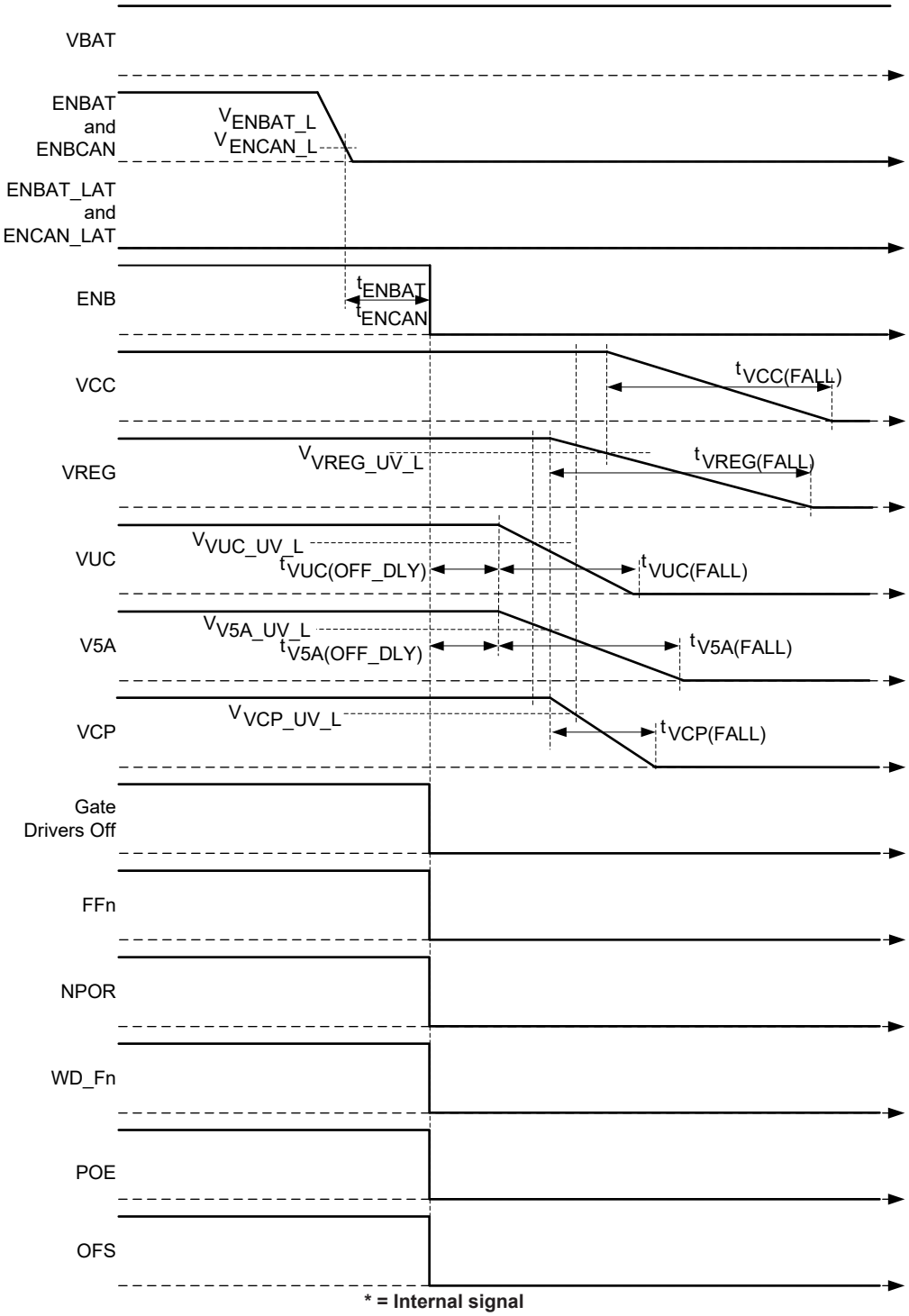

*** = Internal signal**

The time for an output to decay to zero, t_{x_FALL}, varies for each output and depends on the load and output capacitance.

Figure 6: Shutdown Timing Diagram

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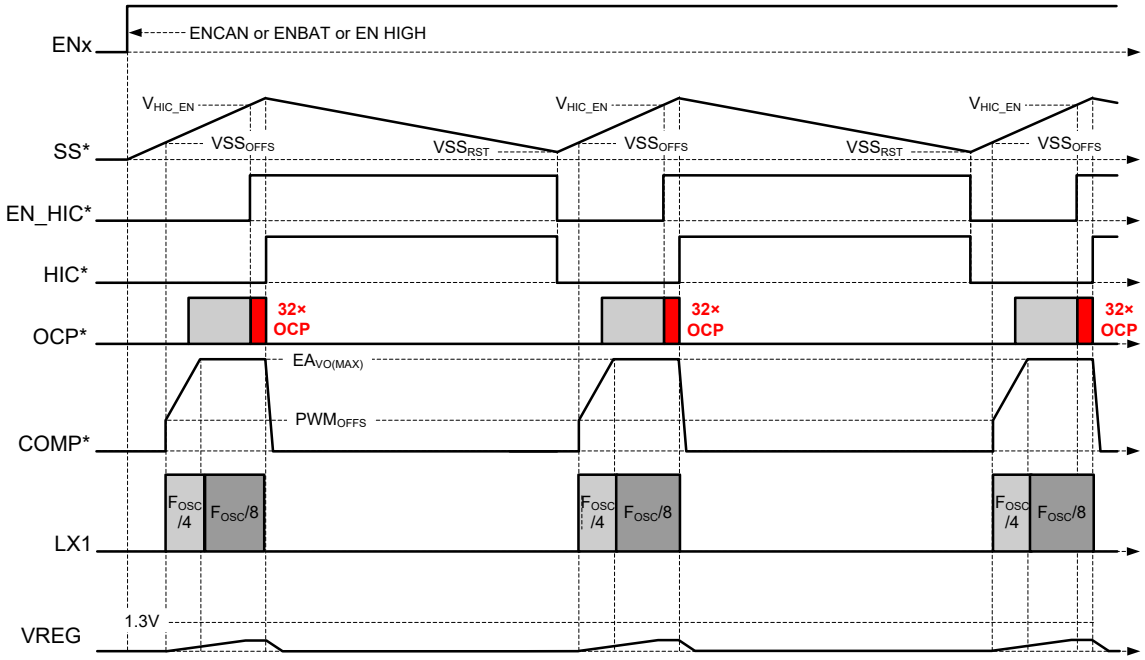
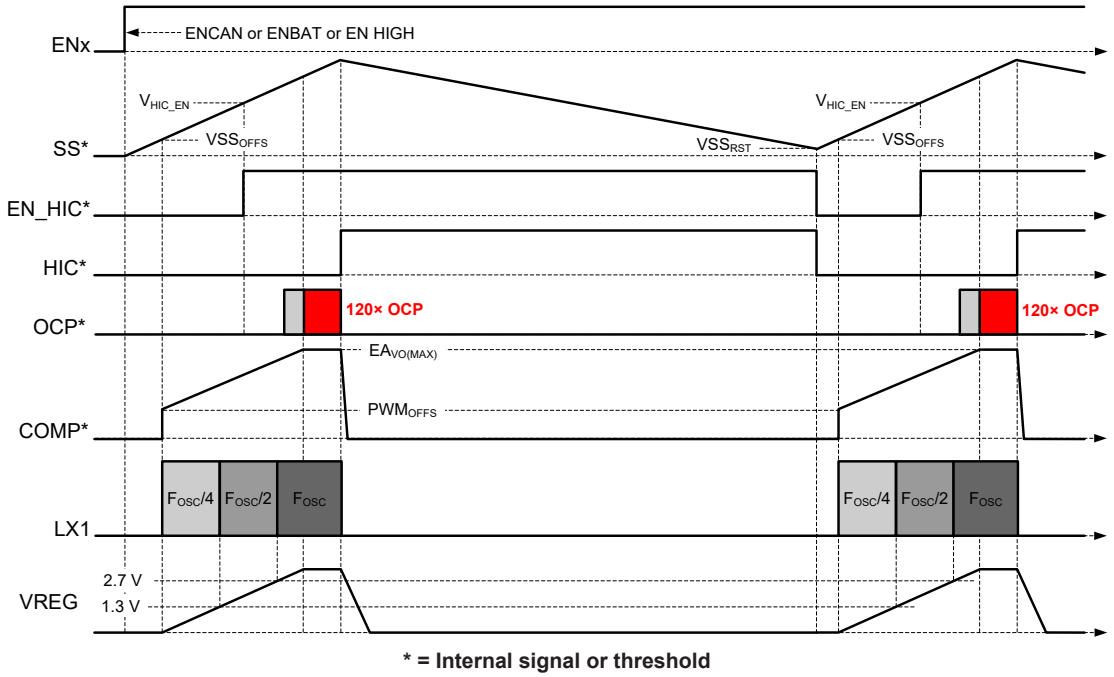


* = Internal signal or threshold

Figure 7: Hiccup Mode Operation with VREG Shorted to GND (R_{LOAD} < 50 mΩ)



* = Internal signal or threshold

Figure 8: Hiccup Mode Operation with VREG Overloaded (R_{LOAD} ≈ 0.5 Ω)

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FAULT MODE OPERATION [1][2][3]

Fault	A81411 Response (SPI Configuration)	VCP	VREG	VUC	VLDOA	VLDOB	VLDOPx	FFn	NPOR	POE	WD_Fn	SPI	WD	Reset (Recovery) Method
VIN UV	Device in power off	Off	Off	Off	Off	Off	Off	Hi_Z	VVUC	Hi_Z	V_{VUC}	Off	Off	Increase VIN
VCP UV	VLDOB supplied by VIN	UV	–	Off	Off	–	Off	Low	–	–	Low	On, no comms	Off	Remove UV factor
VREG UV	VLDOB supplied by VIN	Off	UV	Off	Off	–	Off	Low	–	–	Low	On, no comms	Off	
VUC UV		–	–	UV	–	–	–	Low	Low	Low	V_{VUC}	On, no comms	Off	
VLDOA UV	Inform the MCU (NPOR_KEY.VLDOA_UV = 0)	–	–	–	UV	–	–	Low	–	–	–	–	–	
	NPOR = Low (NPOR_KEY.VLDOA_UV = 1)	–	–	–	UV	–	–	Low	Low [4]	Low	V_{VUC}	–	Off	
VLDOB UV		–	–	–	–	UV	–	Low	–	–	–	–	–	
VLDOPx UV		–	–	–	–	–	UV	Low	–	–	–	–	–	
BOOT1 UV		Off	Off	Off	Off	–	Off	Low	–	–	V_{VUC}	On, no comms	Off	
BOOT2 UV		Off	Off	Off	Off	–	Off	Low	–	–	V_{VUC}	On, no comms	Off	
VIN OV	NPOR = Low (NPOR_KEY.VIN_OV = 1)	–	–	–	–	–	–	Low	Low	Low	V_{VUC}	–	Off	Remove OV factor
	Inform the MCU (NPOR_KEY.VIN_OV = 0)	–	–	–	–	–	–	Low	–	–	–	–	–	
VCP OV	CP pulse-skipping mode	OV	–	–	–	–	–	Low	–	–	–	–	–	
VREG OV	VREG switched off	–	OV	–	–	–	–	Low	–	–	–	–	–	
VUC OV	NPOR = Low (NPOR_KEY.VUC_OV = 1)	–	–	OV	–	–	–	Low	Low	Low	V_{VUC}	–	Off	
	Inform the MCU (NPOR_KEY.VUC_OV = 0)	–	–	OV	–	–	–	Low	–	–	–	–	–	
VLDOA OV	NPOR = Low (NPOR_KEY.VLDOA_OV = 1)	–	–	–	OV	–	–	Low	Low	Low	V_{VUC}	–	Off	
	Inform the MCU (NPOR_KEY.VLDOA_OV = 0)	–	–	–	OV	–	–	Low	–	–	–	–	–	
VLDOB OV		–	–	–	–	OV	–	Low	–	–	–	–	–	
VLDOPx OV		–	–	–	–	–	OV	Low	–	–	–	–	–	
BOOT1 OV	Latch off	Off	Off	Off	Off	–	Off	Low	–	–	V_{VUC}	On, no comms	Off	
BOOT2 OV	Latch off	Off	Off	Off	Off	–	Off	Low	–	–	V_{VUC}	On, no comms	Off	
VREG STG	VREG hiccup mode, VLDOB supplied by VIN	Off	OC	Off	Off	–	Off	Low	–	–	V_{VUC}	On, no comms	Off	Remove STG factor
VUC STG	VUC ILIM or foldback ILIM	–	–	OC	–	–	–	Low	–	–	–	–	–	
VLDOA STG	VLDOA ILIM or foldback ILIM	–	–	–	OC	–	–	Low	–	–	–	–	–	
VLDOB STG	VLDOB foldback ILIM	–	–	–	–	OC	–	Low	–	–	–	–	–	
VLDOPx STG	VLDOPx ILIM or foldback ILIM	–	–	–	–	–	OC	Low	–	–	–	–	–	
LX1 STG	Hiccup mode after 2× f_{SW_VREG}, VLDOB supplied by VIN	Off	LX1 STG	Off	Off	–	Off	Low	–	–	V_{VUC}	On, no comms	Off	Remove STG factor
LX2 STG	Hiccup mode after 2× f_{SW_VREG}, VLDOB supplied by VIN	Off	LX2 STG	Off	Off	–	Off	Low	–	–	V_{VUC}	On, no comms	Off	Remove STG factor
VCP STG	VCP high current and fusing, without LDO drive	UV	–	Off	Off	–	Off	Low	–	–	V_{VUC}	On, no comms	Off	Replace the IC
Watchdog Fault	NPOR = Low (NPOR_KEY.WD_F = 1)	–	–	–	–	–	–	– [5]	Low [6]	Low	Low	–	–	Input proper WD feedback
	Inform the MCU (NPOR_KEY.WD_F = 0)	–	–	–	–	–	–	– [5]	–	Low	Low	–	–	
ABIST Fault	Set POE low, MCU reads	–	–	–	–	–	–	Low	–	Low	–	–	–	Restart/Replace the IC
LBIST Fault	Inform the MCU and set POE low	–	–	–	–	–	–	Low	–	Low	–	–	–	Restart/Replace the IC
EEPROM Fault	Inform the MCU and set POE low	–	–	–	–	–	–	Low	–	Low	–	–	–	Restart/Replace the IC

[1] "–" = no affect; typical operation.
[2] MPOR = controller power-on reset.
[3] STG = short to ground; STB = short to battery.
[4] By default, VLDOA UV does not affect NPOR. However, an option available via SPI programming can be used to allow NPOR to transition low if VLDOA is undervoltage (UV).
[5] By default, a WD fault does not affect FFn. However, an option available via SPI programming can be used to allow FFn to latch low.
[6] By default, a WD fault does not affect NPOR. However, an option available via SPI programming can be used to allow NPOR to transition low for 2 ms to reset the MCU.

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Fault	A81411 Response (SPI Configuration)	VCP	VREG	VUC	VLDOA	VLDOB	VLDOPx	FFn	NPOR	POE	WD_Fn	SPI	WD	Reset (Recovery) Method
Internal Logic Error	Inform the MCU and set POE low	–	–	–	–	–	–	Low	–	Low	–	–	–	Replace the IC
SE Fault	Inform the MCU	–	–	–	–	–	–	Low	–	–	–	–	–	Replace the IC
SPI CS Timeout	Inform the MCU	–	–	–	–	–	–	Low	–	–	–	–	–	Restore communications with device
Pin Checker Fault	Inform the MCU	–	–	–	–	–	–	Low	–	–	–	–	–	Remove external fault or replace the IC
Controller Clock Stuck High or Low	Shutdown VLDOB supplied by VIN	Off	Off	Off	Off	–	Off	Low	Low	Low	V_{VUC}	On, no comms	Off	Replace the IC
PWM Clock Stuck High or Low	VREG shutdown VLDOB supplied by VIN	–	Off	–	–	–	–	Low	–	Low	–	–	–	Replace the IC
One Clock Out of Range	Inform the MCU	–	–	–	–	–	–	Low	–	Low	–	–	–	Replace the IC
LVREG Missing	VREG cannot rise, VLDOB supplied by VIN	Off	UV	Off	Off	–	Off	Low	–	–	V_{VUC}	On, no comms	Off	Replace missing component
CPUMP Missing	VCP_UV, no LDO bias	UV	–	Off	Off	–	Off	Low	–	–	V_{VUC}	On, no comms	Off	
CVCP Missing	VCP_UV, no LDO bias	UV	–	Off	Off	–	Off	Low	–	–	V_{VUC}	On, no comms	Off	
LVREG Shorted	LX1 fault, latch off after 2× VLDOB supplied by VIN	Off	LX1 STG	Off	Off	–	Off	Low	–	–	V_{VUC}	On, no comms	Off	Remove short circuit and toggle VIN or ENx
CPUMP Shorted	VCP_UV, no LDO bias	UV	–	Off	Off	–	Off	Low	–	–	V_{VUC}	On, no comms	Off	Remove short circuit and replace the IC
CVCP Shorted	VCP_UV, no LDO bias	UV	–	Off	Off	–	Off	Low	–	–	V_{VUC}	On, no comms	Off	
Thermal Warning	Inform the MCU	–	–	–	–	–	–	Low	–	–	–	–	–	If the MCU clears the fault, FFn returns to the high state, which allows communication of other faults during operation at high temperature
TSD	Stop PWM, maintain SPI (TSD_F_MSK = 0)	Off	Off	Off	Off	Off	Off	Low	–	Low	V_{VUC}	On, no comms	Off	IC cooldown
	Continue operation, inform the MCU via thermal warning flag (TSD_F_MSK = 1)	–	–	–	–	–	–	Low	–	–	–	–	–	

[1] "–" = no affect; typical operation.
[2] MPOR = controller power-on reset.
[3] STG = short to ground; STB = short to battery.
[4] By default, VLDOA UV does not affect NPOR. However, an option available via SPI programming can be used to allow NPOR to transition low if VLDOA is undervoltage (UV).
[5] By default, a WD fault does not affect FFn. However, an option available via SPI programming can be used to allow FFn to latch low.
[6] By default, a WD fault does not affect NPOR. However, an option available via SPI programming can be used to allow NPOR to transition low for 2 ms to reset the MCU.

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FUNCTIONAL DESCRIPTION

Overview

The A81411 is a power management IC designed for safety-critical applications. It contains one switching regulator and five linear post-regulators to create the voltages necessary for a wide range of automotive applications such as electrical power steering, transmission control units, advanced braking systems, and emissions-control modules.

The A81411 preregulator uses a synchronous buck-boost converter topology. This preregulator generates a fixed 5.35 V (VREG) and is used to power the internal post-regulators and, eventually, external regulators if needed. The post-regulators generate the various voltage levels for the end system.

Power-Up and Power-Down

The A81411 is powered up as soon as one of the enable pins (ENx) is high and the VIN voltage exceeds the UVLO upper threshold. The powerup sequence is shown in Figure 2. During the power-up sequence, if an enable pin does not remain high for a duration longer than the respective deglitch filter time, the device immediately switches to the off state.

If an enable signal latches when all the ENx pins are forced low, the device does not power-down. However, during this condition, if a fault causes NPOR to assert, the enable signal latches clear- and the device powers down. The power-down sequence begins when all ENx pins are low and the microcontroller sends the SPI command to clear the enable-signal latches.

During any state, the device powers down upon detection of the VIN UVLO lower threshold.

Preregulator (VREG)

The preregulator incorporates four internal switches. To complete the buck-boost converter, an external inductor and output capacitors are required.

Preregulator protection and diagnostic functions provided are:

- Pulse-by-pulse and hiccup mode current limit
- Undervoltage and overvoltage detection and reporting
- Shorted switch node-to-ground protection
- High-voltage rating for load dump

The switching frequency is fixed at 2.2 MHz (typical). If the VIN voltage increases to greater than 19 V, the switching frequency decreases to 1.1 MHz (typical). As soon as the VIN voltage decreases to less than 18 V on VIN, the switching frequency returns to 2.2 MHz.

Internal Bias Supply (VDRV, VPOSA, VPOSMON, VDD)

The internal bias supplies are generated by internal linear regulators. These supplies are the first rails to start up as soon as the VIN and one ENx pin are high; during power-up, they are supplied directly from VIN. Most of the internal control circuitry is powered by these supplies. To ensure safe operation of the A81411, unique features of the bias supplies include:

- VIN input undervoltage lockout
- Overvoltage and undervoltage detection
- Dual-input operation: VIN or VREG, for low-battery-voltage operation

Crossover Switches

The A81411 incorporates the crossover switch feature, which changes the input supply of the internal regulators from VIN to VREG, and vice versa.

Once the VREG preregulator is in regulation (V_{REG} > $V_{VREG\_UV\_H}$), the crossover switch changes the input supply from VIN to the VREG preregulator output. If the VREG voltage reduces to less than $V_{VREG\_UV\_L}$, the input supply switches back to VIN.

BOOT Circuits (BOOT1, BOOT2)

Two boot circuits provide the voltage necessary to drive the two high-side N-channel MOSFETs in the preregulator. To ensure correct operation, each boot circuit requires an external 0.1 µF capacitor.

Charge Pump (VCP)

The A81411 incorporates a charge-pump circuit, VCP. This circuit provides bias voltage for the linear post-regulators.

Two external capacitors are required for charge-pump operation. The charge pump is only active when VREG exceeds its UV threshold.

During the first cycle of the charge pump, the flying capacitor, C_{PUMP}, is charged from VREG. During the second cycle, the voltage on the flying capacitor charges a reservoir capacitor, C_{VCP}. The charge pump incorporates safety features, including:

- Undervoltage and overvoltage detection and reporting
- Overcurrent safe mode protection

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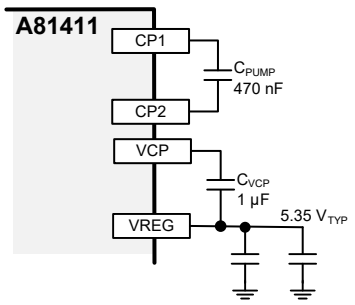

Figure 9: Charge-Pump Connections

Bandgaps (BG1, BG2)

Dual bandgaps are implemented within the A81411. One bandgap is dedicated to the voltage-regulation loops within each regulator, VCP, VREG, and five post-regulators. The other bandgap is dedicated to the undervoltage and overvoltage monitoring functions of all the regulators. This improves safety coverage and fault reporting from the A81411.

If the regulation bandgap fails, the output voltages are out of specification and the monitoring bandgap reports the fault.

If the monitoring bandgap fails, the output voltages remain in regulation, but the monitoring circuitry reports that the outputs are out of specification and trips the fault flag.

The bandgap circuits include two smaller, secondary bandgaps that are used to monitor the undervoltage state of the main bandgaps.

Enable Inputs (ENCAN, ENBAT, EN)

Three enable pins are available on the A81411. Two of the enable pins, ENBAT and ENCAN, are battery-level rated and can be connected to the ignition switch through a low-pass filter. The third enable pin, EN, is a logic-level enable.

As soon as an enable pin is forced high, the internal regulators activate and the power-up sequence initiates.

After the internal ABIST/LBIST, if the ENBAT pin is high at the end of the t_{d_ENBAT} filter time, the ENBAT_LAT signal automatically latches to 1; if ENCAN is high at the end of the t_{d_ENCAN} filter time, ENCAN_LAT also automatically latches to 1.

After the power-up sequence completes and the MCU reset releases (NPOR high), the MCU determines if it should latch to 1 or clear the latch of the ENBAT_LAT and/or ENCAN_LAT signals by SPI command. In this way, the MCU controls when the power-down sequence requires an independent startup on the ENCAN and ENBAT signal status. See Table 1.

Table 1: Truth Table for Enable Inputs

ENCAN	ENBAT	ENCAN_LAT	ENBAT_LAT	EN	ENB
0	0	0	0	0	0
1	x	x	x	x	1
x	1	x	x	x	1
x	x	1	x	x	1
x	x	x	1	x	1
x	x	x	x	1	1

Linear Regulators

The A81411 has five linear regulators:

- VUC regulator (qty. 1) provides 3.3 V or 5 V based on the VUCSEL pin
- Fixed regulator (qty. 1) at 5 V (or 3.3 V factory option, VLDOA)
- Always-on regulator (qty. 1) at 5 V or 3.3 V based on VLDOBSEL pin (VLDOB)
- Short-to-battery protected regulators (qty. 2: VLDOP1 and VLDOP2) programmed (5 V or 3.3 V) and enabled via SPI.

The preregulator supplies 5.35 V (VREG) to the linear regulators, which reduces power dissipation and temperature.

A separate input to the VUC regulator (VUCIN) is provided to allow the use of an external voltage-drop resistor. This helps reduce power dissipation in the A81411 when VUC is set to 3.3 V. The suggested value for this external resistor is 1.7 V/I_{VUCmax}, where I_{VUCmax} is the maximum load current on VUC.

The VUCSEL pin is monitored and latched at the end of VREG power-up. The VLDOBSEL pin is monitored and latched upon device power-up. These pins also include an internal pulldown resistor: If either pin is open, the respective voltage becomes set to 3.3 V; if the pin opens during operation, the respective voltage is not affected. For the VUCSEL pin, one redundant and identical input buffer has been added to assure the right selection of the VUC voltage. The output signals of the two buffers are compared immediately before the value is latched: If the two output buffer values match, the VUCSEL value is latched; otherwise, VUC and VLDOA are not enabled and the FFn pin remains low. If the two output signals do not match after the latch, only the SPI bit (VUCSEL_F) is set; thus, the LDOs do not turn off and FFn does not change.

All linear regulators provide the following protection features:

- Current limit with foldback
- Overcurrent detection and reporting
- Undervoltage and overvoltage detection and reporting

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Fault Detection and Reporting (FFn, NPOR, POE)

In addition to the previously discussed fault protections, the extensive fault detection within the A81411 includes two fault reporting mechanisms: one through hard-wired pins and the other through the SPI. The three hard-wired pins used for fault reporting, FFn, NPOR, and POE, are detailed next.

FFN

FFn (open-drain, active low) reports on all detected faults. When a fault is detected, FFn transitions low. The FFn output can be used as an interrupt pin to the processor. This alerts the processor to check the A81411 status and to take appropriate action if a fault occurs. By default, FFn does not report a watchdog fault, but it may be added to the FFn logic via SPI programming.

NPOR

NPOR (open-drain with internal pull-up, active low) reports on the status of the VUC output. By default, this signal transitions low only if VUC is out of regulation (undervoltage or overvoltage). However, options are available to:

- Report a watchdog fault by setting NPOR low for 2 ms.
- Indicate if VLDOA is out of regulation.
- Report if VIN is in an overvoltage condition.

These additional reporting options are selectable through SPI using the NPOR_KEY or mask bits. For details, see the Register Mapping section. The logic setup for the NPOR signal is shown in Figure 10.

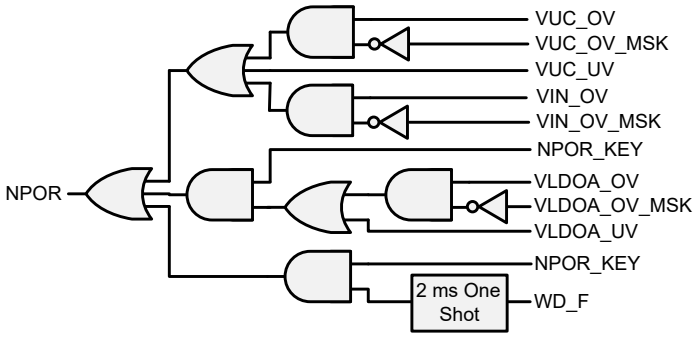

Figure 10: NPOR Generation Logic

POE

Power-on enable (POE) is a safe-state flag that reports faults observed by the watchdog circuits. These faults signal a processor malfunction. The POE pin should be used to put the system in a safe state. This pin is a push-pull output. The A81411 continuously monitors the state of this pin and compares it to the demanded states.

The nERROR input allows the user to feed other safe-state signals into the A81411 and to set POE low. If nERROR is not used, it can remain open or it can be connected to VUC.

Analog Multiplexer Output

The AMUX pin is the output of an analog multiplexer to monitor the voltages shown in Table 2. The output of the MUX is selected through AMUX_SEL [3:0] in register 0x08. The accuracy of the multiplexer is reported in Table 2. The driving capability of this output is 5 mA, and the maximum voltage is 2 V. The typical response time from the write to AMUX_SEL [3:0] to the AMUX output change is 20 µs.

If TEMP output is selected on the analog multiplexer, the internal temperature of the device is provided. It is measured as:

Equation 1:

$$\text{TEMP (V)} = 1.4131\ 5\ \text{V} - 3.986\ \text{mV/ºC} \times T_J\ (\text{ºC})$$

Table 2: Analog Multiplexer Outputs

Node	Signal Divide Ratio	Tolerance (Reference)
VREG	1/3	±1%
VUC	1/3	±1%
VLDOA	1/3	±1%
VLDOB	1/3	±1%
VLDOP1	1/3	±1%
VLDOP2	1/3	±1%
VENBAT	1/24	±2.5%
VCP	1/6	±2.5%
BG1	1/1	±1%
BG2	1/1	±1%
VIN	1/24	±2.6%
TEMP	1/1	±3%

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Built-In Self-Tests

The A81411 includes an analog built-in self-test (ABIST) and a logic built-in self-test (LBIST). ABIST and LBIST are performed only during the startup sequence. ABIST verifies the operation of the undervoltage and overvoltage monitor circuits for the main outputs and the overtemperature shutdown circuitry; it also includes self-testing of the NPOR, POE, WD_Fn and FFn fault-generation circuits. LBIST performs tests of the on-the-chip logic, state machine, and registers, including the watchdog circuits.

At startup, LBIST is performed immediately after the ENBAT or ENCAN filtered signal is high (after t_{d_ENBAT} or t_{d_ENCAN}). Once LBIST is completed, the ABIST is performed. After the ABIST completes, the VREG and the LDOs start.

The MCU must read the verification register and clear any faults to reset the FFn flag. Also, the MCU can verify if BIST passed via reads of the relevant bits in the verification registers.

In the event of a self-test failure, the A81411 reports the failure through SPI.

Undervoltage Detect Self-Test

The undervoltage (UV) detection circuits are verified during startup of the A81411. A voltage that is less than the undervoltage threshold is applied to each UV comparator; this should cause the corresponding undervoltage bit in the diagnostic register to change state: 0→1; this indicates a fault. If a diagnostic UV register bit does not change state, the corresponding verify result register bit latches high. Thus, when self-test completes, if any bit in the verify result register is high, verification failed. The UV comparators that are tested are VREG, VUC, VLDOA, VLDOB, VLDOPx, and VCP.

Overvoltage Detect Self-Test

The overvoltage (OV) detection circuits are verified during startup of the A81411.

A voltage that exceeds the overvoltage threshold is applied to each OV comparator; this should cause the corresponding overvoltage bit in the diagnostic register to change state: 0→1; this indicates a fault. If a diagnostic OV register bit does not change state, the corresponding verify result register bit latches high. Thus, when the self-test completes, if any bit in the verify result register is high, verification failed. The OV comparators that are tested are VREG, VUC, VLDOA, VLDOB, VLDOPx, VIN, and VCP.

Overtemperature Shutdown Self-Test

The overtemperature shutdown (TSD) detector is verified during startup of the A81411.

A voltage that exceeds the overvoltage threshold is applied to the TSD comparator; this should cause the overtemperature bit in the diagnostic register to change state: 0→1; this indicates a fault. If the TSD register bit does not change state, the TSD verify result register bit latches high. Thus, when the self-test completes, if the TSD bit in the verify result registers is high, verification failed.

Power-On Enable (POE) Self-Test

The A81411 incorporates continuous self-testing of the power-on enable (POE) output. It compares the status of the POE pin (POE_S) with the internal, expected status. If these differ, the FFn output pin is set low and POE_ERR in the status register is set high.

MCU Self-Reset

MCU can assert its reset by pulling the NPOR pin low. If A81411 detects NPOR low and an internal condition to force NPOR low is not present:

- NPOR_MCU latched bit is set high.
- Minimum NPOR low timer starts $t_{MIN\_NPOR\_LOW}$
- Watchdog state machine moves to the NPOR_LOW state, then waits for the duration of $t_{MIN\_NPOR\_LOW}$ and the release of the NPOR pin.

Once the minimum NPOR low duration, $t_{MIN\_NPOR\_LOW}$, expires and MCU releases the NPOR pin WD, the state machine moves to the configuration (CONFIG) state.

The MCU must clear the NPOR_MCU bit because it controls POE during the configuration state.

The WD configuration is not affected unless it is changed via SPI. When the WD state machine exits the configuration state, the WD configuration latches again.

Logic Built-In Self-Test (LBIST)

The logic for the watchdogs, fault reporting, registers, EEPROM interface, and SPI interface are verified with LBIST. A 26-bit linear feedback shift register (LFSR) exercises internal scan chains for 16 ms, and a 26-bit multi-input signature register (MISR) compresses the results into a 26-bit signature. If the calculated signature does not match the expected value, a logic error is detected.

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While LBIST is active, inputs are ignored and outputs are frozen. For example, the A81411 does not respond to SPI transactions and faults are not recorded. When LBIST completes, the logic is reset and the shadow registers are again loaded from the on-chip EEPROM memory.

Output Pin Checker

To ensure the pin status matches the internal signal value, the device monitors the voltage directly on the NPOR, POE, FFn, and WD_Fn pins. If an external or internal fault causes a mismatch between pin and internal signal, the corresponding SPI flag is set (DIAGNOSTIC_2 register 0x06, bits [12:15]).

Watchdog

The A81411 contains three different watchdogs. The selection and configuration of each watchdog is performed through SPI. After a watchdog is selected and is in the run state, reconfiguration is not possible until it undergoes a secure SPI procedure. When the state machine leaves the configuration mode, the watchdog circuits update and latch. After leaving the configuration state, modifications to the watchdog registers do not take effect unless a configuration (CONFIG) or restart command is issued.

The three types of watchdogs are:

- Pulse-width watchdog (PWWD)
- Window watchdog (WWD)
- Question-and-answer watchdog (QAWD) (default)

The question-and-answer watchdog is the default watchdog. It automatically starts if the default settings are used and the following conditions are met:

- NPOR transitions high;
- Watchdog is not selected: WD_SEL [2:0] = [0,0,0]; and
- The t_{CONFIG_WD} configuration timer expires.
  - To force the configuration timer to expire, use the WD_SEL [2:0] bits to select a watchdog.

The watchdog can be restarted by the microcontroller by sending either a restart command or a configuration command via the three-word WD_KEYs

If a watchdog fault occurs, POE is set low and the respective bit in the diagnostic register (WWD_F, QAWD_F, or PWWD_F) latches high.

By default, a watchdog fault does not affect NPOR. However, at any time, the microcontroller can configure the device by SPI to force low also the NPOR after a watchdog fault. This is accomplished through a write of three secure words to the SPI NPOR_KEY register. In this case, a watchdog fault sets NPOR low for $t_{WD,FAULT}$ (2 ms) to reset/restore the microcontroller.

When NPOR goes high after the toggle cycle, the t_{CONFIG_WD} timer starts. The MCU can reconfigure and select the WD type through a write to WD_SEL [2:0] to ensure proper synchronization, especially of the question-and-answer watchdog. If WD_SEL [2:0] is not written and t_{CONFIG_WD} expires, the WD configuration latches when the state machine exits the configuration mode.

By default, a watchdog fault does not affect FFn. However, at any time, the microcontroller can modify how FFn behaves after a watchdog fault. If configuration bit WDF_2_FFn is set and a watchdog fault is detected, FFn transitions low and remains low until the diagnostic registers are cleared.

PULSE-WIDTH WINDOW WATCHDOG (PWWD)

The pulse-width watchdog circuit monitors an external clock applied to the WD_IN pin. This clock should be generated by the primary microcontroller or digital signal processor (DSP). The PWWD watchdog measures the time between two clock edges, either rising or falling; thus, the watchdog effectively measures both the “high” and “low” pulse widths, as shown in Figure 11:

- The default nominal WD_IN pulse width (PWWD_PW) of 1 ms can be modified to 0.5, 1.5, or 2 ms via SPI.
- If an incorrect pulse width is detected, the watchdog increments its fault counter by 10 (default).
- If a correct pulse width is detected, the watchdog decrements its fault counter by 2 (default).
- If the watchdog fault counter exceeds 160 (default), the POE pin transitions low.

Operation of the PWWD is shown in Figure 11 and Figure 12. The increment value (PWWD_INC), decrement value (PWWD_DEC), and maximum fault count (PWWD_MAX) all have alternate values that can be accessed via SPI.

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The watchdog default values are loaded when:

- The internal rails transition low (i.e., VIN is removed, or ENCAN and ENBAT are both low); or
- The bandgap, BG1, transitions low.

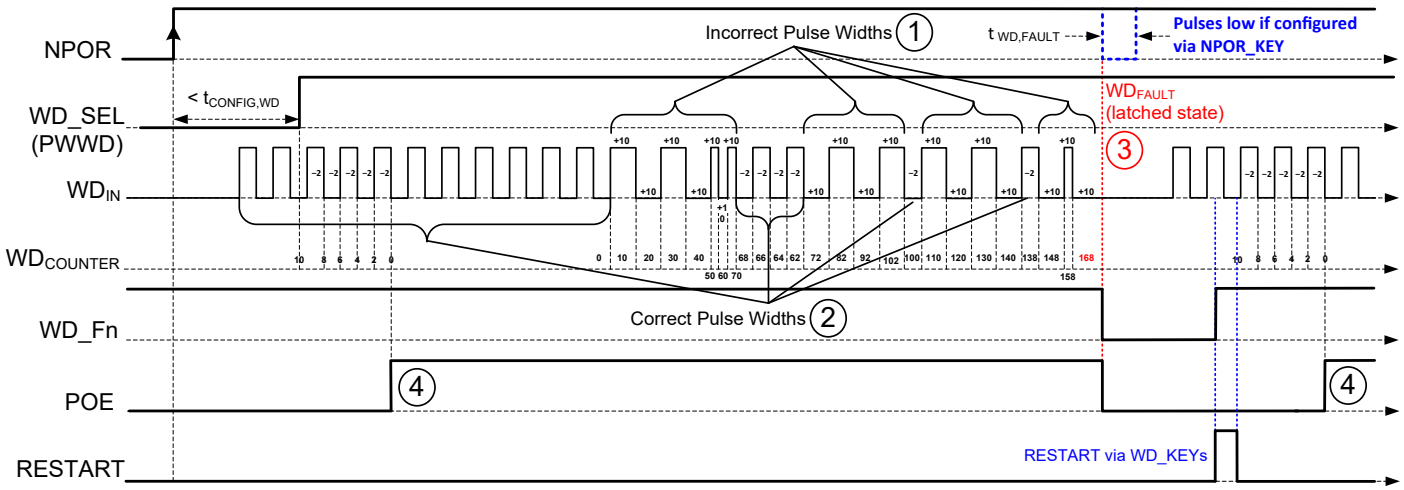
Clock pulses from the microcontroller must be applied to the WD_IN pin before the watchdog is selected (via WD_SEL) or restarted (via the three-word WD_KEY command). The PWWD error counter can be preloaded to a value set by PWWD_POE_DLY (default value is 2). Preloading the error counter forces the microcontroller to send valid pulses before POE transitions high; this effectively prequalifies the performance of the microcontroller. Prequalification with PWWD_POE_DLY set to a value of 10 is shown in Figure 11 and Figure 12; this value requires 5 V valid clock pulses (–2 counts per valid clock pulse) before POE transitions high.

After moving into typical operation, if a clock edge is not detected at WD_IN for PWWD_EDGE_TO, the POE pin transitions low. The default PWWD_EDGE_TO of 5 ms can be modified to 2.5, 10, or 15 ms via SPI. The “edge timeout” condition is shown as (1) in Figure 12.

While in the typical state, if clock activity at WD_IN terminates for at least PWWD_ACT_TO, the POE pin transitions low. The default PWWD_ACT_TO of 16 ms can be modified to 8, 24, or 32 ms via SPI. The “loss of clock activity” condition is shown as (2) in Figure 12.

The pulse widths generated by a microcontroller or DSP depend on many factors and exhibit some pulse-to-pulse variation. The A81411 accommodates pulse-width variations by allowing the designer to select a window (period) of allowable variations. The default window tolerance (PWWD_WIN_TOL) of ±13% can be modified to ±8%, ±18%, and ±23% via SPI.

The watchdog performs calculations based on an internally generated clock. The accuracy of the internal clock is typically ±2.5% at 25°C; however, due to IC process shifts and temperature variations, this accuracy may vary by as much as ±5%. Variations in the watchdog clock result in a shift of the “OK region” (i.e., the expected pulse width) at WD_IN.



1. Each incorrect pulse width increments the WD counter by 10.
2. Each correct pulse width decrements the WD counter by 2.
3. If the total fault count exceeds 160, a WD fault occurs.
4. PWWD_POE_DLY is set to 10: Before POE can transition high, five valid pulse widths (10 ÷ 2 counts per valid pulse) must be observed.

Figure 11: Watchdog (WD) Operation With Correct Pulse Widths and Incorrect Pulse Widths

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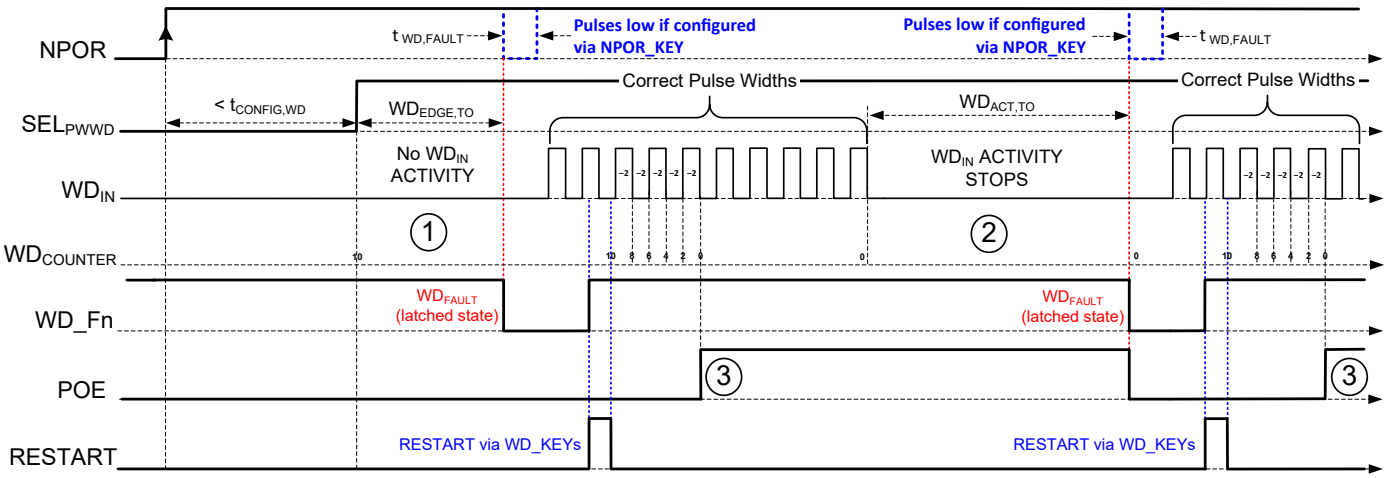

1. WD_IN not active for WD_{EDGE_TO}.
2. WD_IN activity stops.
3. PWWD_POE_DLY is set to 10: Before POE can transition high, five valid pulse widths (10 ÷ 2 counts per valid pulse) must be observed.

Figure 12: Watchdog Operation With Faults From Sources Noted

WINDOW WATCHDOG (WWD)

The window watchdog monitors the time between rising edges of an external clock applied to the WD_IN pin. This clock should be generated by the microcontroller or DSP. If the time between rising edges (i.e., the frequency) of the clock is not within an acceptable window, a watchdog fault is generated. In general, before POE transitions high, valid watchdog clock(s) must be present at WD_IN for a duration of at least t_{WD_SLOW}.

After NPOR transitions high, the processor must:

- Program the configuration registers WWD_TIMER [3:0] to select and initiate valid WD pulses on the WD_IN pin; and
- Select the WWD: Set WD_SEL [2:0] = [010] or [011].

Both tasks must complete before t_{CONFIG_WD} expires.

To initiate valid WD pulses on the WD_IN pin, it is strongly recommended for the processor to produce valid clock pulses at WD_IN prior to selection of the watchdog or issuance of the restart command.

If the time between rising clock edges is too short (i.e., a “fast” fault) or too long (i.e., a “slow” fault), a window watchdog fault occurs. If a WD fault occurs: the POE signal is driven low; the WWD_F bit in the diagnostic register latches high; and, if selected, the NPOR toggles for 2 ms.

Before POE is allowed to transition high, valid watchdog clocks should be present at the WD_IN pin for a duration of at least t_{WD_SLOW}. This “prequalifies” correct operation of the microcontroller before the gate driver is enabled (via POE). During the prequalification time (t_{WD_SLOW}), at least one complete clock cycle must occur. For prequalification, the maximum WD_IN clock frequency ($f_{WD\_IN\_MAX}$) and the selected value of WWD_TIMER [3:0} must satisfy the following:

Equation 2:

$$t_{WWD\_SLOW} > 1.5/f_{WD\_IN\_MAX}$$

The minimum and maximum values of the t_{WWD_SLOW} and t_{WWD_FAST} parameters depend on the tolerance of the internal clock frequency (f_{CLOCK_TOL}). Starting from this value as a percentage, the tolerances of t_{WWD_SLOW} and t_{WWD_FAST} can be calculated as:

Equation 3:

$$t_{WWD\_X\_TOL}|max = [100/(100 - f_{CLOCK\_TOL})] - 1$$

Equation 4:

$$t_{WWD\_X\_TOL}|min = [100/(100 + f_{CLOCK\_TOL})] - 1$$

Typical watchdog operation with both fast and slow fault events, along with the recommended restart conditions, are shown in Figure 13 and Figure 14.

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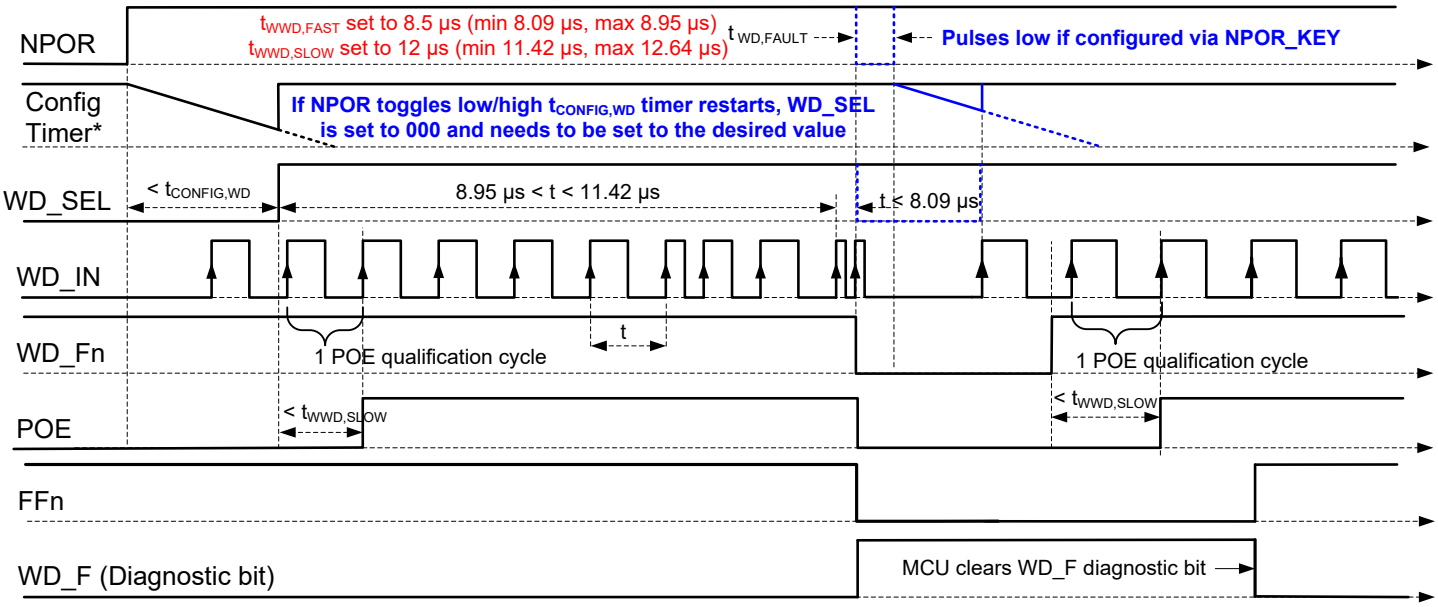
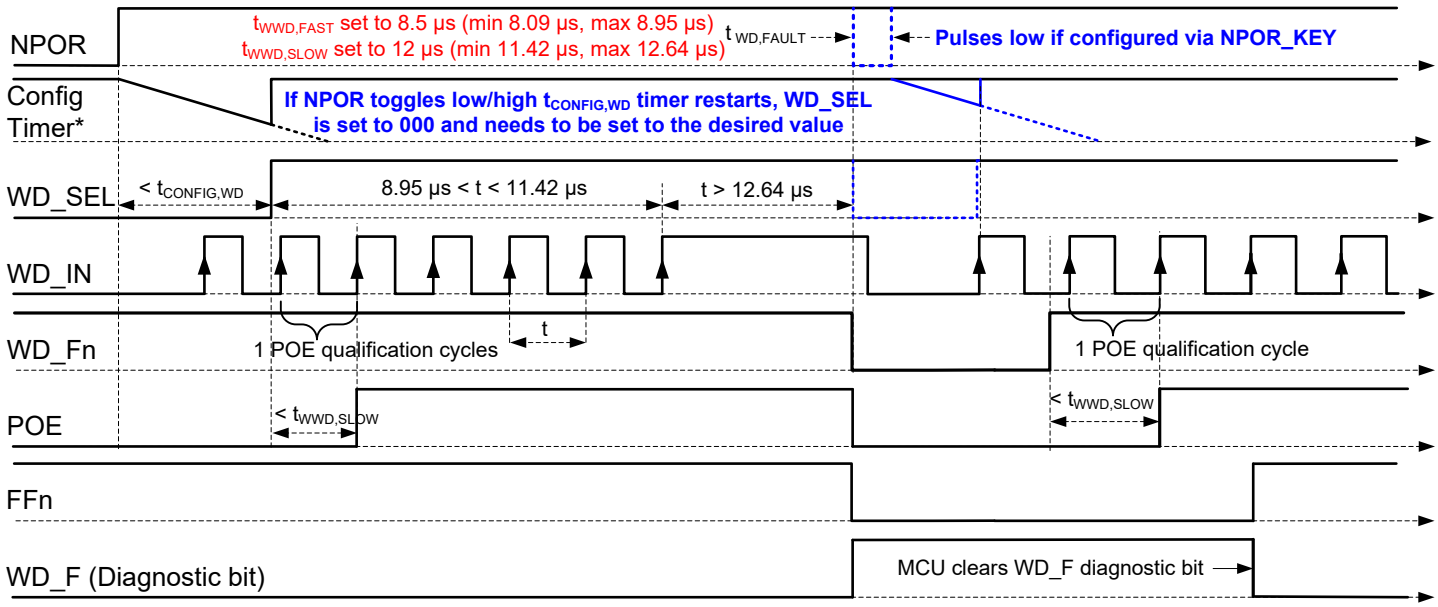


A watchdog fault occurs when the WD_IN period (t) is too short.
*** Signal is internal to A81411.**

Figure 13: Window Watchdog (WWD) Operation



A watchdog fault occurs when the WD_IN period (t) is too long.
*** Signal is internal to A81411.**

Figure 14: Window Watchdog (WWD) Operation

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QUESTION-AND-ANSWER WATCHDOG (QAWD)

The question-and-answer watchdog (QAWD) requires the MCU to read a 6-bit word from a register within the A81411. The MCU must then generate four answer words based on the word read. If the QAWD_TIMERS bit is 0, all four answer words must be written in the correct sequence, within two timed windows or one timed window. The A81411 periodically generates the random word.

Before the question-and-answer watchdog becomes active via WD_SEL [2:0], the QAWD must be fully configured through SPI. For example, the minimum and maximum time limits for each window (t_{QA_MIN1}, t_{QA_MAX1}, t_{QA_MIN2}, and t_{QA_MAX2}) must be selected from a list of 16 possibilities using the following SPI bits: QAWD_TIMER1_MIN1[3:0], QAWD_TIMER1_MAX1 [3:0], QAWD_TIMER2_MIN [3:0], and QAWD_TIMER2_MAX [3:0].

For invalid configurations such as QAWD_TIMER1_MIN [3:0] ≥ QAWD_TIMER1_MAX [3:0] or QAWD_TIMER2_MIN [3:0] ≥ QAWD_TIMER2_MAX [3:0], the QAWD function is not guaranteed.

Any time POE is low, the microcontroller must successfully complete a question-and-answer session before POE transitions high.

After the question-and-answer watchdog is activated via WD_SEL [2:0], the A81411 generates a 6-bit random word, QAWD_RAND [5:0] and starts the first internal timer. The microcontroller must synchronize its own timer when it selects the question-and-answer watchdog via WD_SEL [2:0]. Then, the microcontroller must read the random word and allow enough time, with margin, to generate the four answer words and write the answer words back to the watchdog.

The write-back for word 1 and 2 must not occur before the first minimum timer limit (t_{QA_MIN1}) expires, nor after the first maximum time limit (t_{QA_MAX1}) expires. Once word 1 and word 2 are received, even if they are incorrect, the second set of minimum and maximum timers start. The MCU must then write answer 3 and answer 4 back after t_{QA_MIN2} expires and before t_{QA_MAX2} expires. Upon receipt of the answer words, a new question-and-answer watchdog session starts. The MCU should synchronize its timers with the writes of the answer words.

The microcontroller uses a 6-bit linear feedback shift register (LFSR) to generate the next four 6-bit words in the sequence. The random word received from the A81411 is used to seed the LFSR.

The MCU must wait for the first minimum time limit to elapse (t_{QA_MIN1}). After the minimum time limit expires, the microcontroller must write the four 6-bit words back to the A81411 using two frames. The first two words are written to QAWD_ANS_1 and QAWAD_ANS_0 in the first frame. The first frame write must complete before the first maximum time limit expires (t_{QA_MAX1}), with margin.

Answer words 3 and 4 are written in the second frame. The second frame write must be completed after the second minimum timer (t_{QA_MIN2}) expires and before the second maximum time (t_{QA_MAX2}) limit expires, with margin.

To start the next question-and-answer session, both the question-and-answer watchdog and the microcontroller must again synchronize their internal timers (i.e., they must be set to zero and counting must begin) immediately after the second write-back occurs.

The microcontroller is allowed to retry the question-and-answer sequence a number of times before a watchdog fault is declared. The number of retries can be selected by a 3-bit word, QAWD_RETRY [2:0]. A question-and-answer watchdog fault occurs only after the retry counter reaches zero, as shown in Figure 19. During a question-and-answer watchdog session, the retry counter is decremented by 1 if one or more of the following occur:

- An answer is received before the respective minimum time limit expires (t_{QA_MIN1} or t_{QA_MIN2}).
- An answer is not received before the respective maximum time limit expires (t_{QA_MAX1} or t_{QA_MAX2}).
- An incorrect answer is received from the microcontroller.

If a successful watchdog session is completed, the retry counter increments by 1. The maximum increments are limited by the content of the QAWD_RETRY configuration register.

The following example is illustrated in Figure 15. The MCU reads the question (seed) from the A81411 register; here, the seed is 0b101001. The MCU implements an LFSR with polynomial $x^5 + x^4 + 1$. The MCU seeds its LFSR with this word. The MCU clocks the LFSR, which returns 0b010011, answer word 1. The MCU again clocks the LFSR to return 0b100111, answer word 2. Two further clocks cycles give 0b001111 (answer word 3) and 0b011110 (answer word 4).

The MCU puts answer word 1 and answer word 2 in a 32-bit SPI frame; answer word 1 uses bits [D20:D15] and answer word 2 uses [D10:D5]. The MCU writes this frame to the A81411 answer register. A81411 determines if the answers received are correct and if they arrived within the timer window. The MCU repeats the process with answer words 3 and 4.

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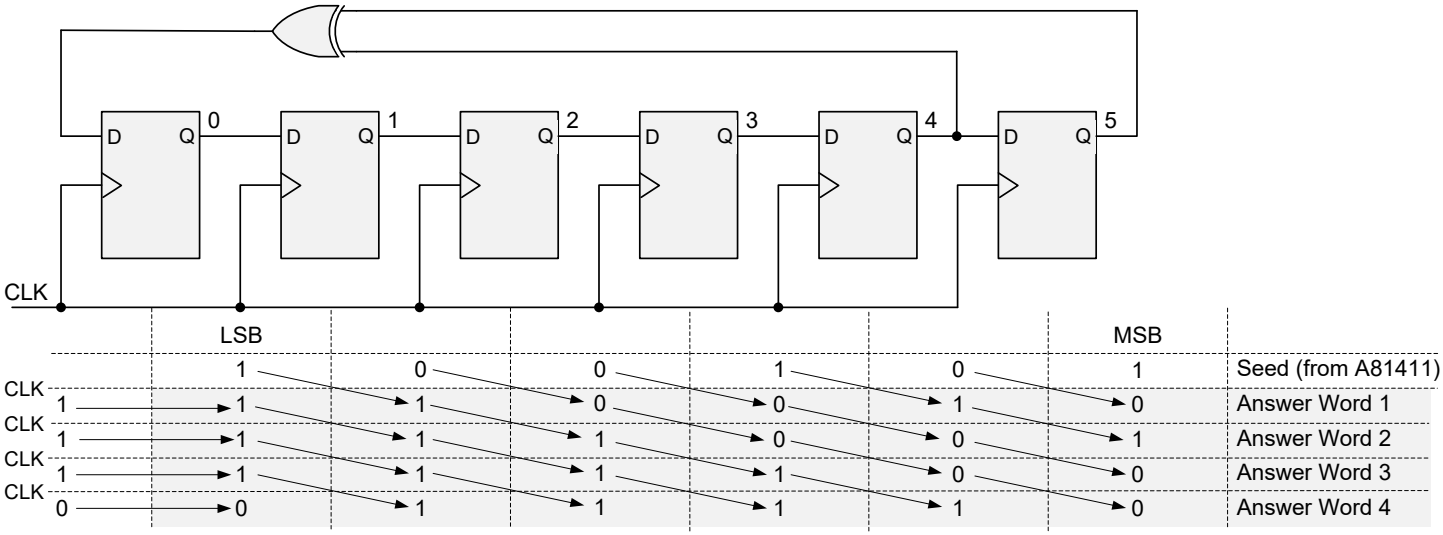

Figure 15: 6-Bit Question-and-Answer Linear-Feedback Shift Register Using Polynomial $x^5 + x^4 + 1$

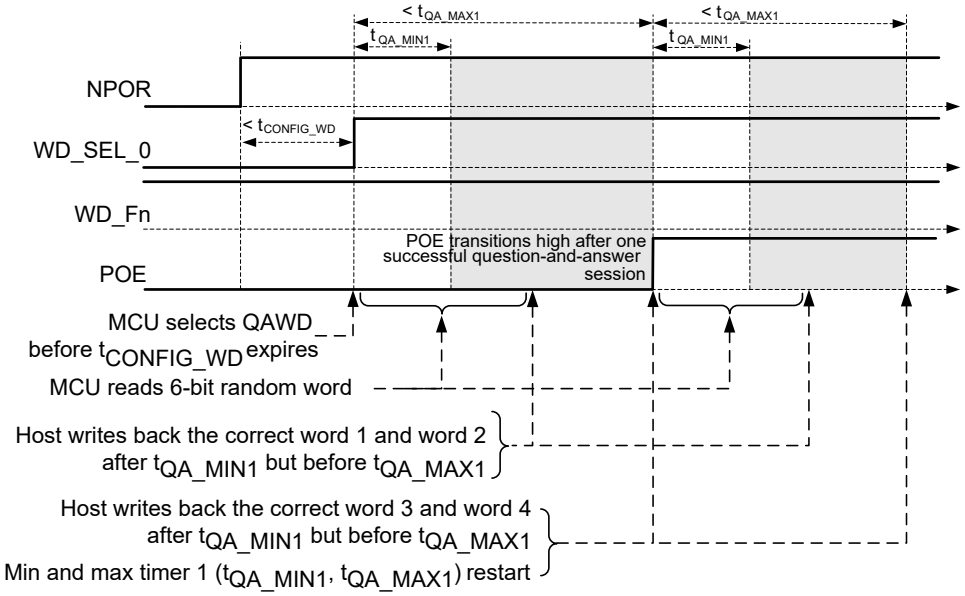

Figure 16: Question-and-Answer Watchdog Selection, Operation and Successful Session SPI (QAWD_TIMERS) = 0

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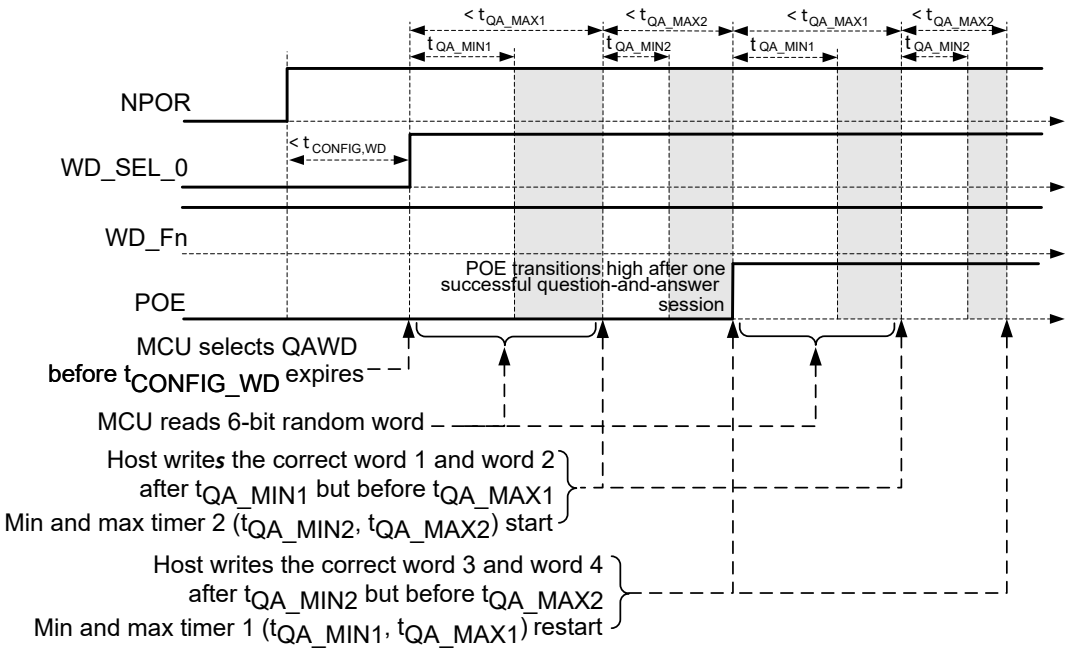

Figure 17: Question-and-Answer Watchdog Selection, Operation and Successful Session SPI (QAWD_TIMERS) = 1

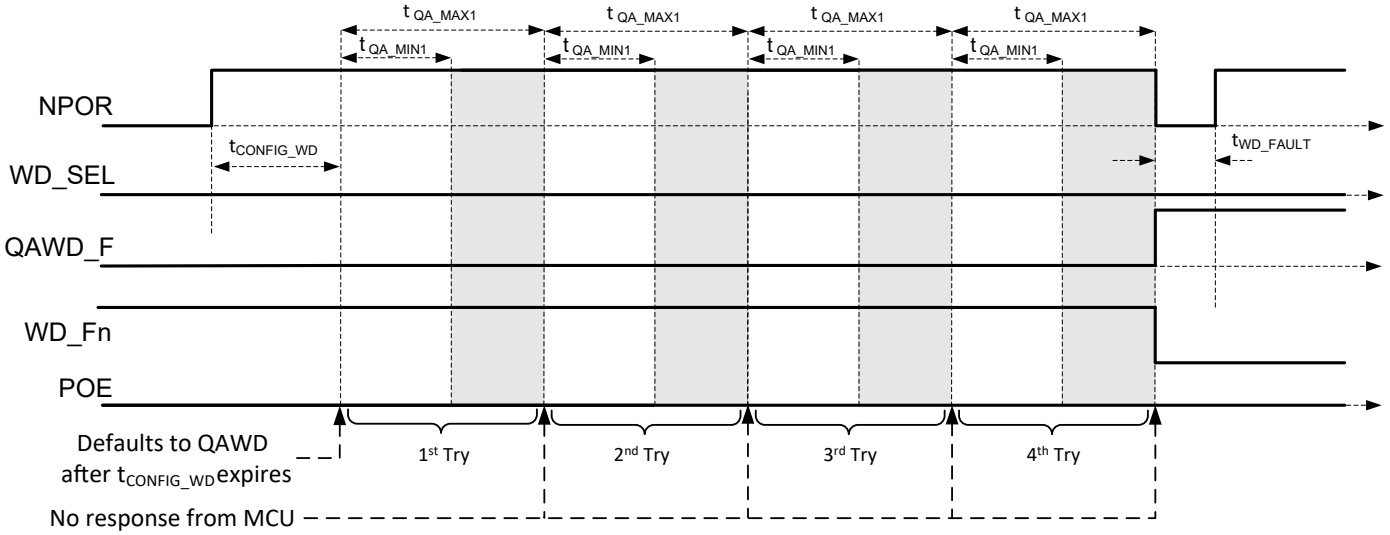

Figure 18: Watchdog Fault Behavior When WD Selection Is Not Performed By MCU

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Watchdog Flow Charts

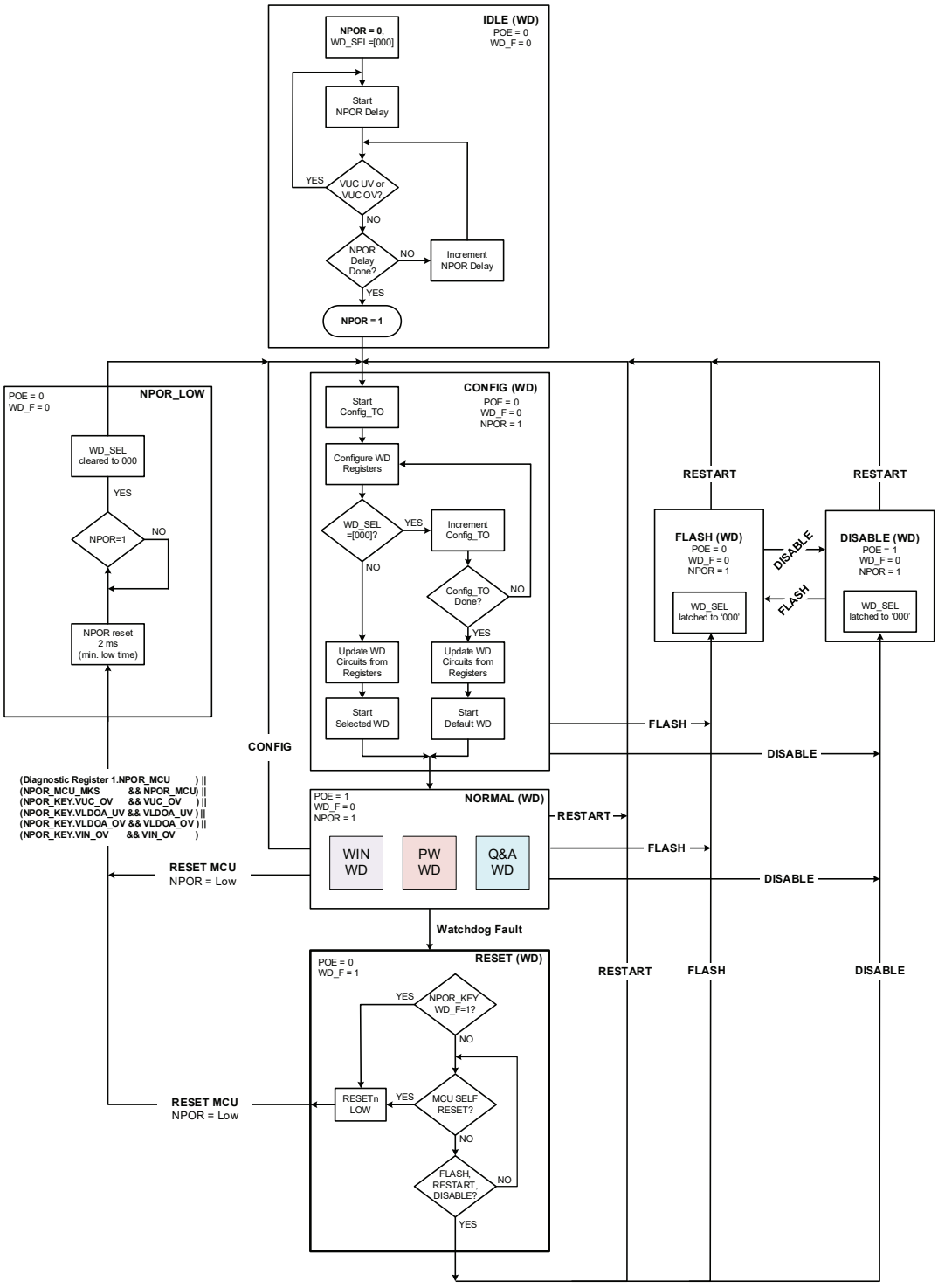

Figure 19: State Diagram of Watchdog Operation

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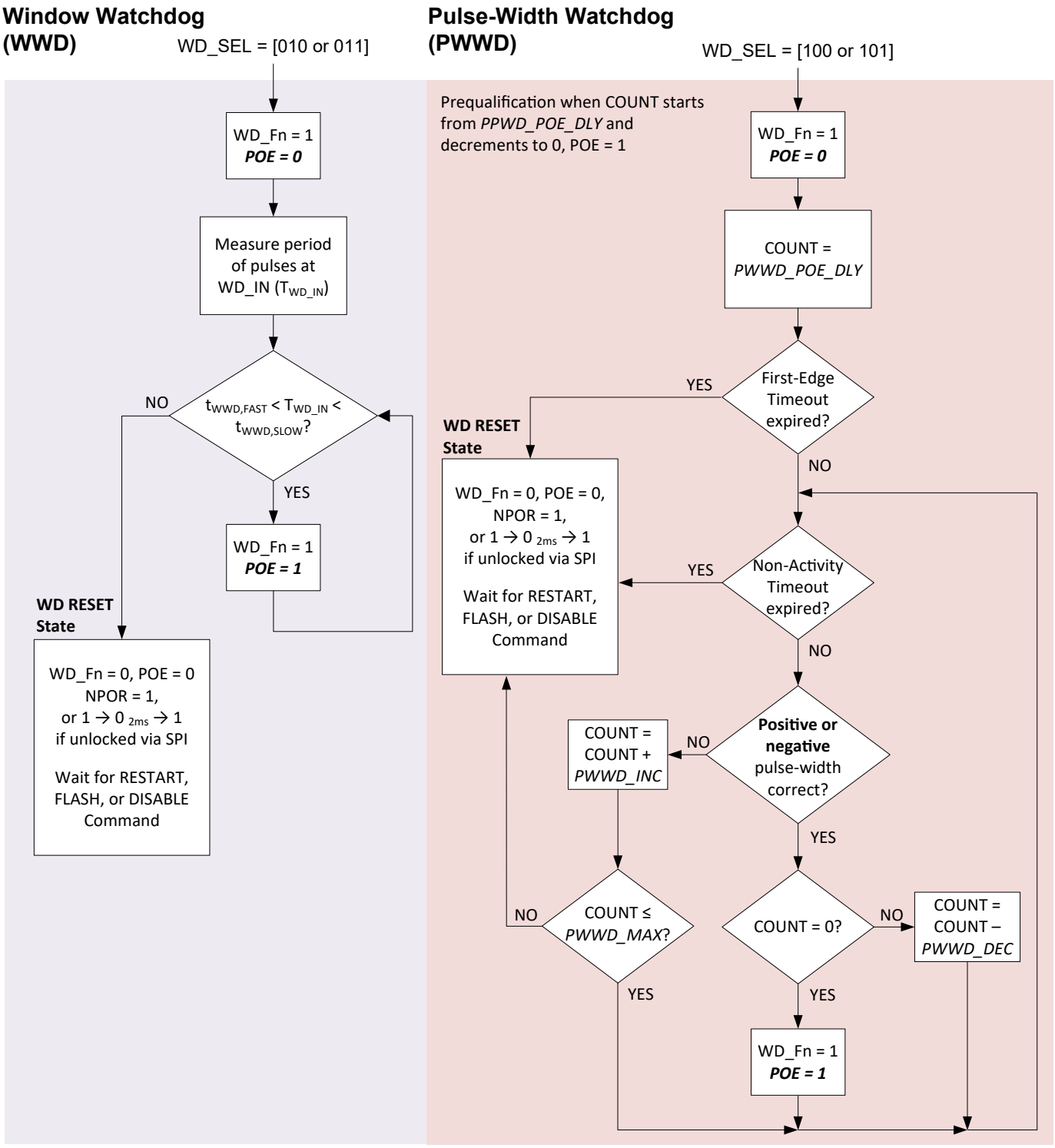

Figure 20: WWD and PWWD Flow Charts

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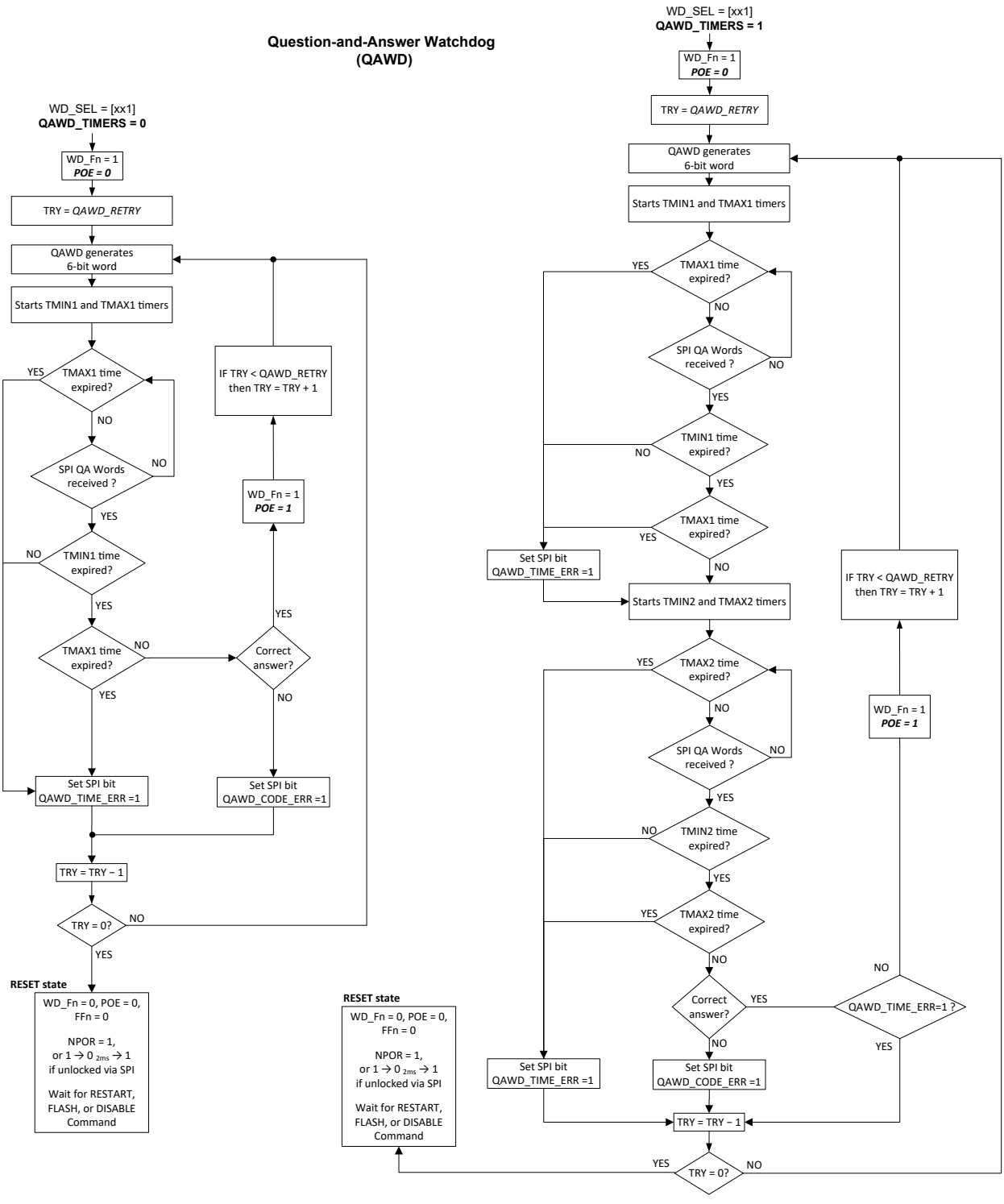

Figure 21: QAWD Flow Charts

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SERIAL COMMUNICATION INTERFACE

The A81411 provides the user with a full-duplex, four-wire, synchronous serial interface. It is compatible with the serial peripheral interface (SPI) standard using mode 3 (CPOL = 1, CPHA = 1). The SPI interface uses an out-of-frame communication protocol. This means that the logical response of the peripheral is within the next frame of the controller, as shown Figure 22. The serial interface timing requirements are specified in the Electrical Characteristics table and are illustrated in Figure 1.

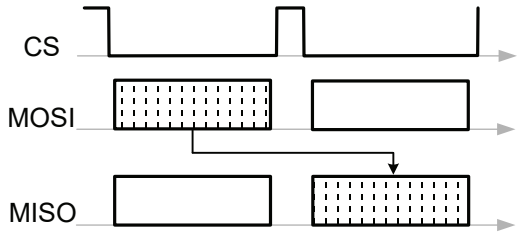

Figure 22: Out-of-Frame SPI Communication

Each 32-bit frame has a read/write bit (WR, bit [30]). To enable writes of subsequent bits into the selected register, this bit must be set to 1. If WR is set to 0 (read), the data bits [21:6] are ignored. The state of the WR bit also determines the data output on MISO. If WR is set to 1, general diagnostic data is output. If WR is set to 0, the contents of the register selected by the address bits is output.

MOSI

The controller output, peripheral input (MOSI; data input from the controller) uses a 32-bit word, sent and received most-significant bit (MSB) first. When CS is low, data from the controller is received on this pin. The peripheral reads and latches the data on the rising edge of SCK. The controller advances to the next bit on the falling edge of SCK.

MISO

The controller input, peripheral output (MISO; data output from the peripheral, or A81411) uses a 32-bit word, sent and received MSB first. If CS is high or the CHIP_ID bit [22] from the previous frame) is incorrect, this pin is high impedance. If CS is low, data from the peripheral is sent on this pin. The controller reads/latches the data on the rising edge of SCK. The peripheral advances to the next bit on the falling edge of SCK.

SCK

The serial clock (SCK; input) from the controller requires 32 rising clock edges per frame. During each clock cycle, a full duplex data transmission occurs. The controller sends a bit on the MOSI line and the peripheral reads it; meanwhile, the peripheral sends a bit on the MISO line and the controller reads it. This sequence is maintained even when only single-directional data transfer is intended. Data changes state on the falling edge of SCK and latches on the rising edge of SCK. Before CS transitions, SCK must be set high.

CS

When the chip-select (CS; input) from the controller is high, MISO is high impedance and activity on MOSI and SCK is ignored. This allows multiple SPI peripherals to have common MISO, SCK, and MOSI connections. However, each peripheral must have a dedicated CS signal. CS is brought low to initiate a serial transfer. When 32 data bits have been clocked into the shift register, CS must be taken high to latch the data into the selected register. When this occurs, the internal control circuits act on the new data.

If CS transitions high and there are fewer than 32 rising edges on SCK, the write is canceled and data is not written to the registers. Similarly, if there are more than 32 rising edges on SCK while CS is low, the write is canceled and data is not written. In both cases, the serial error (SE) and fault flag (FF) bits are set high, and FFn pin (microcontroller interrupt) is pulled low to indicate a data-transfer error.

The device also integrates a timeout that checks for inactivity on the SPI CS pin. This additional check is enabled and disabled using the SPI bit CSN_TO_EN. If the CS pin is inactive for longer than the timeout threshold (configured by SPI CSN_TO_THR), the latched bit is set, which asserts FFn low and puts MISO to high-impedance (Hi-Z) until the bit is cleared.

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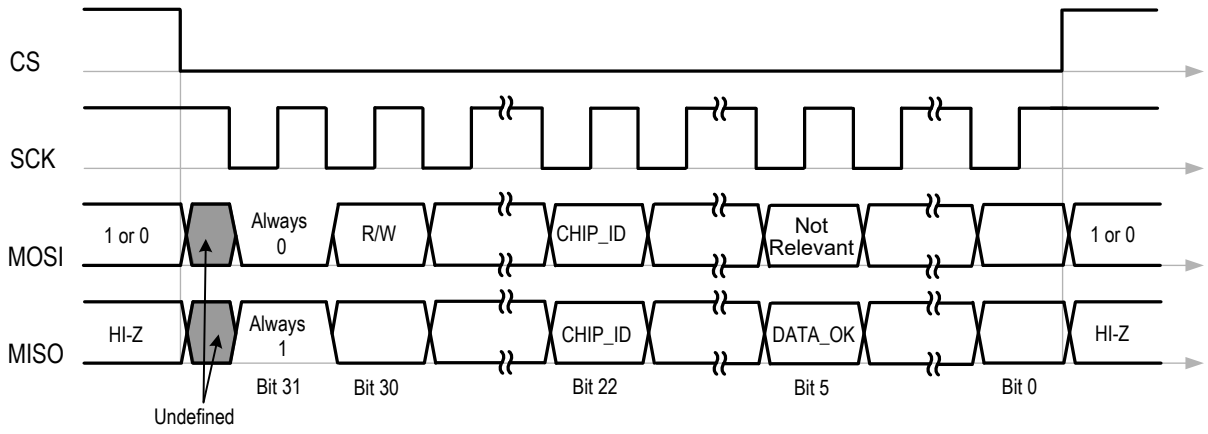

Data changes on the falling edge of SCK. Data latches on the rising edge of SCK.

Figure 23: Example SPI Communications

SPI FRAME DEFINITIONS

1. Request register ID is the address of the host command, from the previous SPI message.
2. When the A81411 shares SPI with a second device, the CHIP_ID bit, bit [22] in both the MISO and MOSI frames, ensures that the A81411 only accepts commands intended for it. The CHIP_ID for the A81411 is internally fixed at 0. The CHIP_ID for the second device on SPI should be internally fixed at 1.
3. MOSI and MISO frames include a 5-bit CRC calculated from bits [30] through [5].
   A. Because the MSB is static, it does not need to be included in the CRC calculation; rather, it can be checked at the host-side or device-side independently.
   B. The polynomial of 0x12 ($x^5 + x^2 + 1$) is used with a start value of 11111b and a target of 00000b.
   C. All single-bit and dual-bit errors are covered.
   D. Hamming distance of 3 is achieved.
   E. Every four consecutive bit errors.
   F. Line stuck low or high is detected.
   G. If a CRC error occurs, the SE and FF bits are set to 1, and the FFn pin is pulled low.
4. MISO frame includes a 5-bit request register ID [30:26].
5. MISO frame includes a 3-bit frame counter [25:23]. It is a simple modulo-8 (0 → 1 → 2 → … → 7 → 0 → …) counter value that increments at every SPI message.
6. SPI integrity is checked via writes and reads of 2-bit patterns to the read-back register.

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HOST COMMANDS

- Bit [31] is static, fixed at 0.
- Bit [30] indicates a write or a read: 1 = Write, 0 = Read.
- Bit [22], the CHIP_ID, is fixed at 0 for the A81411.
- For a read command, the data bits are considered not relevant (NR).

Write Command from Host to MOSI Pin

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	5-bit address					NR		0	16-bit data																NR	5-bit CRC				

Read Command from Host to MOSI Pin

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	5-bit address					NR		0	16-bit data																NR	5-bit CRC				

DEVICE RESPONSES

- Bit [31] is static, fixed at 1.
- Bit [22], CHIP_ID, is fixed at 0 for the A81411.
- Bit [5], DATA_OK, indicates if the 16-bit data is valid:
  - □ 1 = Valid data, errors not detected.
  - □ 0 = Typical response after detection of a MOSI write or an error (i.e., SE or CRC); general status bits are sent.

Pattern at MISO Pin After MOSI Read Where 16-Bit Data Is Valid (Errors Not Detected)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	Request Register ID	Frame Counter							0	16-bit data																1	5-bit CRC				

Pattern at MISO Pin After MOSI Read Where Error Is Detected or Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	Request Register ID					Frame Counter			0	Status Register 0																0	5-bit CRC				

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STATUS UPDATES AND SPI PROCEDURE IF FFN→0

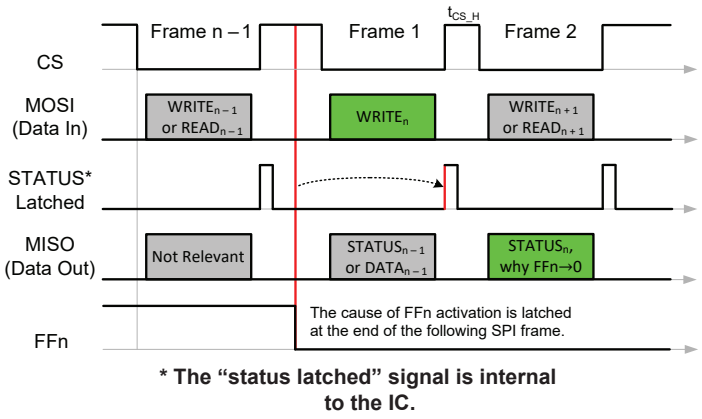
The SPI diagnostic status bits of the A81411 are updated at the end of each SPI frame (i.e., when CS transitions high). This is shown by the "status latched" signal in Figure 24.

If the FFn signal transitions low, the MCU must perform a diagnostic on the A81411. This diagnostic can be accomplished by obtaining a device response via a simple write command to the read-back register (see Figure 27).

NOTE: Any other register can be used for this diagnostic. However, the read-back register is the safest because it does not change any functionality.

Because the A81411 uses out-of-frame communication, the actual response is available on the next frame.

Alternatively, a read of the status/diagnostic registers can be performed.



*** The "status latched" signal is internal to the IC.**

Figure 24: Recommended SPI Operations after FFn→0.

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Register Mapping

STATUS REGISTERS

The A81411 provides three status registers. These registers are read only. They provide real-time status of various functions within the A81411.

These registers report on the status of the five system rails: VUC, VLDOA, VLDOB, VLDOP1, and VLDOP2. They also report on the internal rail status, which includes VREG and the charge pump, VCP. The general fault flag (FF), watchdog fault flag (WD_F), and watchdog state (WD_STATE) are found in these status registers. The fault-signal NPOR, POE, and WD_Fn pins are monitored and reported if they do not match the internally generated signal. At startup, the undervoltage faults are masked.

CONFIGURATION REGISTERS

Six registers in the A81411 are used for configuration. Four of these registers are dedicated to watchdog parameters.

The watchdog registers can only be configured in the configuration state. This occurs after the A81411 is first enabled or after the watchdog receives a secure SPI restart command.

The watchdog configuration register allows the user to:

- Select the type of watchdog via WD_SEL [2:0]. The default watchdog is the question-and-answer watchdog (QAWD).
- Set the timer for the question-and-answer watchdog.
- Set the allowed number of retries.
- Read the 6-bit random word.
- Write the QAWD answers.
- Set the parameters and timers for the pulse-width watchdog.

Two other configuration registers allow the user to:

- Disable the PWM dither feature.
- Modify the response to a watchdog fault (at pins FFn).
- Mask thermal shutdown.
- Disable and enable the 5 V (or 3.3 V) rails, VLDOA, VLDOP1 and VLDOP2.

By default, VLDOP1 and VLDOP2 are in the off state. They can be enabled via SPI. If an LDO is disabled, its output decays to 0 V. Typically, this causes a UV fault to occur. However, because this condition is expected and is internally masked, the fault flags (both FF and FFn) do not register a fault. When any LDO is disabled, both the UV and OV faults are masked. This allows the system to disable one of the LDOs and it still maintains interrupt functionality to the microcontroller via the fault flag (FFn) pin. Also, if an LDO is disabled or off, the corresponding SPI diagnostic status bits (VLDOA_F, VLDOP1_F or VLDOP2_F) indicate a failure did not occur.

Control Bits		Status Bits		FF Bit	FFn Pin
VLDOPx_EN_1	VLDOPx_EN_0	VLDOPx_UV	VLDOPx_OV		
0	0	Not relevant	Not relevant	Mask UV and OV	
0	1	If previous state was off		Mask UV and OV	
1	0	If previous state was off		Mask UV and OV	
1	1	1	0	1	0
1	1	0	1	1	0

WATCHDOG MODE KEY REGISTER

At times, it may be necessary to reflash or restart the processor. To do this, the user should put the watchdog into flash mode. To put the watchdog into flash mode, write a sequence of key words to the WD_CMD_KEY register. If the correct word sequence is not received, the sequence must restart. While in flash mode, the A81411 sets NPOR high and POE low.

Upon completion of flash, to exit flash mode, the processor must send the restart sequence of keywords for the watchdog. If VIN has not been removed, the watchdog restarts with the new configuration.

NPOR INPUT KEY AND CONFIGURATION

The NPOR input key allows the user to modify which faults generate an NPOR. It also allows the MCU to toggle NPOR for 2 ms. Any change to this register requires a write of three specific words in the correct order.

VERIFY-RESULT REGISTERS

At power-up, the A81411 performs a self-test of the UV and OV detection circuits. This test should cause the states of the respective diagnostic registers to toggle. If any diagnostic register does not change state, the corresponding verify-result register latches high and FFn becomes set low.

Upon completion of power-up, the system microcontroller might be interrupted by FFn. At that time, the microcontroller should examine the verify result registers to determine which self-test failed. If a register contains a 1, the microcontroller should make note of the failure and determine how to proceed.

Last, to clear the flag and regain functionality of FFn, the microcontroller should write a 1 to the failed register bits (RW1C).

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REGISTER MAPS

HEX	DEC	Register Name	Type	D21 / D13	D20 / D12	D19 / D11	D18 / D10	D17 / D9	D16 / D8	D15 / D7	D14 / D6
0x00	0	STATUS_0	RO	FF	SE_S	WD_F_S	POE_S	NPOR_S	TSD_F_S	EEPROM_F	VUCSEL_F
				VMON_F	POE_ERR	NPOR_ERR	TSD_WARN	ENCAN_S	ENBAT_S	ENCAN_LAT_S	ENBAT_LAT_S
0x01	1	STATUS_1	RO	VREG_F	VUC_F	VLDOA_F	VLDOB_F	VLDOP1_F	VLDOP2_F	VCP_F	VUCSEL_S
				BIST_F	NPOR_INPUT [4:0]					WD_F_ERR	FFn_ERR
0x02	2	STATUS_2	RO	PWWD_CNT7:0)							
				QAWD_RETRY_CNT [2:0]			WD_STATE [2:0]			QAWD_WINDOW_OPEN	QAWD_CURR_WINDOW
0x03	3	STATUS_3 [1]	RO	QAWD_WINDOW_TIMER [7:0]							
				QAWD_TIME_ERR	QAWD_CODE_ERR	QAWD_RAND [5:0]					
0x04	4	DIAGNOSTIC_0	RW1C	VREG_OV	VREG_UV	VUC_OV	VUC_UV	VLDOA_OV	VLDOA_UV	VLDOB_OV	VLDOB_UV
				VLDOP1_OV	VLDOP1_UV	VLDOP2_OV	VLDOP2_UV	VCP_OV	VCP_UV	TSD_F	VIN_OV
0x05	5	DIAGNOSTIC_1	RW1C	VUC_OC	VLDOA_OC	VLDOB_OC	VLDOP1_OC	VLDOP2_OC	VREG_OC	–	–
				–	–	TWARN_F	VUC_AMR_OV	BOOT1_UV	BOOT2_UV	LX1_STG	LX2_STG
0x06	6	DIAGNOSTIC_2	RW1C	SE	PWM_F	CLK_OOR	WWD_F	QAWD_F	PWWD_F	POE_FAIL	NPOR_FAIL
				WD_F_FAIL	FFN_FAIL	NPOR_F	NPOR_REQ	NPOR_MCU	NPOR_PWR	–	SPI_CSN_TO
0x07	7	WD_CMD_KEYS NPOR_INPUTS_KEY	WO	WD_KEY [7:0]							
				NPOR_KEY [7:0]							
0x08	8	CONFIG_0	RW	–	VLDOP2_EN [1:0]		VLDOP1_EN [1:0]		VLDOA_EN	WDF_2_FFN	DITH_DIS
				TSD_F_MSK	POE_FORCE	–	AMUX_SEL [3:0]				FFN_PIN_CHCK_LAT_EN
0x09	9	CONFIG_1	RW	ENCAN_LAT [7:0]							
				ENBAT_LAT [7:0]							
0x0A	10	CONFIG_2: LDO OUT AND WD [1]	RW	–	VLDOP1_OUT	VLDOP2_OUT	–	QAWD_TIMERS	QAWD_RETRY [2:0]		
				WD_SEL [2:0]			–	WWD_TIMER [3:0]			
0x0B	11	CONFIG_3: WD [1]	RW	QAWD_TIMER1_MAX [3:0]				QAWD_TIMER1_MIN [3:0]			
				QAWD_TIMER2_MAX [3:0]				QAWD_TIMER2_MIN [3:0]			
0x0C	12	CONFIG_4: WD [1]	RW	QAWD_ANS_2_4 [5:0]						–	–
				–	–	QAWD_ANS_1_3 [5:0]					
0x0D	13	CONFIG_5: WD [1]	RW	PWWD_EDGE_TO [1:0]		PWWD_ACT_TO [1:0]		PWWD_WIN_TOL [1:0]		PWWD_PW [1:0]	
				PWWD_DEC [1:0]		PWWD_INC [1:0]		PWWD_MAX [1:0]		PWWD_POE_DLY [1:0]	
0x0E	14	CONFIG_6	RW	ABIST_ON	–	–	–	–	SPI_CSN_TO_EN	SPI_CSN_TO_THR [9:8]	
				SPI_CSN_TO_THR [7:0]							
0x0F	15	READ-BACK	RW	READ–BACK [15:8]							
				READ–BACK [7:0]							
0x10	16	VERIFY_RESULT_0	RW1C	VUC_OV_FAIL	VLDOA_OV_FAIL	VLDOB_OV_FAIL	VLDOP1_OV_FAIL	VLDOP2_OV_FAIL	VREG_OV_FAIL	VCP_OV_FAIL	VIN_OV_FAIL
				VUC_UV_FAIL	VLDOA_UV_FAIL	VLDOB_UV_FAIL	VLDOP1_UV_FAIL	VLDOP2_UV_FAIL	VREG_UV_FAIL	VCP_UV_FAIL	TSD_BIST_FAIL
0x11	17	VERIFY_RESULT_1	RW1C	ABIST_FAIL	LBIST_FAIL	INT_LOGIC_ERR	–	–	–	–	–
				–	–	–	–	–	–	–	–

[1] Except for QAWD_RAND, the watchdog (WD) registers only take effect after the state machine exits the configuration (CONFIG) mode.

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0x00: Status Register 0

Address: 00000b; Type: Read Only (RO)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	FF	SE_S	WD_F_S	POE_S	NPOR_S	TSD_F_S	EEPROM_F	VUCSEL_F
Data Bit/ Name	D13	D12	D11	D10	D9	D8	D7	D6
	VMON_F	POE_ERR	NPOR_ERR	TSD_WARN	ENCAN_S	ENBAT_S	ENCAN_ LAT_S	ENBAT_LAT_S

FF [D21]

Fault flag:

- 0: Fault not detected
- 1: Fault detected (default)

SE_S [D20]

Serial communications error:

- 0: No error (default)
- 1: Fault detected—Less than or more than 32 rising SCK edges occurred in a frame, or there is a CRC error

WD_F_S [D19]

Watchdog fault status:

- 0: Fault not detected or watchdog is disabled (default)
- 1: Fault detected

POE_S [D18]

Power-on enable internal logic status:

- 0: POE is low (default)
- 1: POE is high

NPOR_S [D17]

Power-on reset internal logic status:

- 0: NPOR is low (default)
- 1: NPOR is high

TSD_F_S [D16]

Thermal shutdown status:

- 0: Temperature is OK (default)
- 1: Overtemperature event

EEPROM_F [D15]

EEPROM error:

- 0: Fault not detected (default)
- 1: Fault detected

VUCSEL_F [D14]

VUCSEL is terminated incorrectly:

- 0: Fault not detected (default)
- 1: Fault detected

VMON_F [D13]

Monitor supply fault. UV/OV is not communicated:

- 0: Fault not detected (default)
- 1: Fault detected

POE_ERR [D12]

Power-on enable (POE) error. POE output pin does not match the demand of the A81411:

- 0: Fault not detected (default)
- 1: Fault detected

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NPOR_ERR [D11]

NPOR output pin does not match the demand of the A81411:

- 0: Fault not detected (default)
- 1: Fault detected

TSD_WARN [D10]

Thermal warning:

- 0: Temperature is less than 155°C (default)
- 1: Temperature exceeds 155°C

ENCAN_S [D9]

Status of the CAN enable input pin (ENCAN):

- 0: ENCAN is low (default)
- 1: ENCAN is high

ENBAT_S [D8]

Status of the high-voltage enable input pin (ENBAT):

- 0: ENBAT is low (default)
- 1: ENBAT is high

ENCAN_LAT_S [D7]

Status of the internal SPI CAN enable (ENCAN_LAT):

- 0: ENCAN_LAT is low (default)
- 1: ENCAN_LAT is high

ENBAT_LAT_S [D6]

Status of the internal high-voltage enable (ENBAT_LAT):

- 0: ENBAT_LAT is low (default)
- 1: ENBAT_LAT is high

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0x01: Status Register 1

Address: 00001b; Type: Read Only (RO)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	VREG_F	VUC_F	VLDOA_F	VLDOB_F	VLDOP1_F	VLDOP2_F	VCP_F	VUCSEL_S
Data Bit/ Name	D13	D12	D11	D10	D9	D8	D7	D6
	BIST_F	NPOR_VUC_OV	NPOR_VLDOA_ UV	NPOR_VLDOA_ OV	NPOR_WD_F	NPOR_VIN_ OV	WD_F_ ERR	FFn_ERR

VREG_F [D21]

Indicates if the voltage at the preregulator output pin is within regulation:

- 0: Fault not detected (default)
- 1: Fault detected

VUC_F [D20]

Indicates if the voltage at the VUC pin is within regulation:

- 0: Fault not detected (default)
- 1: Fault detected

VLDOA_F [D19]

Indicates if the voltage at the VLDOA output is within regulation:

- 0: Fault not detected (default)
- 1: Fault detected

VLDOB_F [D18]

Indicates if the voltage at the VLDOB output is within regulation:

- 0: Fault not detected (default)
- 1: Fault detected

VLDOP1_F [D17]

Indicates if the voltage at the VLDOP1 output is within regulation:

- 0: Fault not detected (default)
- 1: Fault detected

VLDOP2_F [D16]

Indicates if the voltage at the VLDOP2 output is within regulation:

- 0: Fault not detected (default)
- 1: Fault detected

VCP_F [D15]

Indicates if the voltage at the VCP pin is within regulation:

- 0: Fault not detected (default)
- 1: Fault detected

VUCSEL_S [D14]

Indicates the voltage setting for VUC:

- 0: VUC is set to 3.3 V
- 1: VUC is set to 5 V

BIST_F [D13]

LBIST or ABIST failure:

- 0: LBIST and ABIST report that a fault is not detected (default)
- 1: LBIST or ABIST report that a fault is detected

NPOR_VUC_OV [D12]

Reports status on the NPOR configuration register:

- 0: VUC OV fault is excluded from NPOR generation
- 1: VUC OV fault is included in NPOR generation (default)

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NPOR_VLDOA_UV [D11]

Reports status on the NPOR configuration register:

- 0: VLDOA UV fault is excluded from NPOR generation (default)
- 1: VLDOA UV fault is included in NPOR generation

NPOR_ VLDOA_OV [D10]

Reports status on the NPOR configuration register:

- 0: VLDOA OV fault is excluded from NPOR generation (default)
- 1: VLDOA OV fault is included in NPOR generation

NPOR_WD_F [D09]

Reports status on the NPOR configuration register:

- 0: WD fault is excluded from NPOR generation (default)
- 1: WD fault is included in NPOR generation

NPOR_VIN_OV [D08]

Reports status on the NPOR configuration register:

- 0: VIN OV fault is excluded from NPOR generation (default)
- 1: VIN OV fault is included in NPOR generation

WD_F_ERR [D7]

WD_Fn pin does not match the demand of the A81411:

- 0: Fault not detected (default)
- 1: Fault detected

FFn_ERR [D6]

FFn pin does not match the demand from the A81411:

- 0: Fault not detected (default)
- 1: Fault detected

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0x02: Status Register 2

Address: 00010b; Type: Read Only (RO)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	PWWD_CNT [7:0]							
Data Bit/ Name	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**
	QAWD_RETRY_CNT [2:0]			WD_STATE [2:0]			QAWD_ WINDOW_OPEN	QAWD_CURR_ WINDOW

PWWD_CNT [D21:D14]

Indicates the value of the error counter of the pulse-width watchdog:

- 00000000 = 0, starting value
- …
- 10100000 = 160, default maximum value
- …
- 11011100 = 220, alternate maximum value selectable via SPI

QAWD_RETRY_CNT [D13:D11]

Question-and-answer watchdog remaining retries:

- 000 = 0 retries remaining
- 001 = 1 retry remaining
- 010 = 2 retries remaining
- 011 = 3 retries remaining
- 100 = 4 retries remaining
- 101 = 5 retries remaining
- 110 = 6 retries remaining
- 111 = 7 retries remaining

WD_STATE [D11, D10, D8]

Watchdog state:

WD_STATE [D10]	WD_STATE [D11]	WD_STATE [D8]	Watchdog State
0	0	0	Idle
0	0	1	Configuration
0	1	0	Reset
0	1	1	Typical
1	0	0	Flash
1	0	1	Disabled
1	1	0	Reserved/Future Use
1	1	1	Reserved/Future Use

QAWD_WINDOW_OPEN [D7]

When the minimum time elapses and the maximum time is counting, the content is 1:

- 0 = Question-and-answer window excluding zone
- 1 = Question-and-answer window valid zone

QAWD_CURR_WINDOW [D6]

Reports which answer window is currently active. Valid only is QAWD_WIN_OPEN = 1:

- 0 = QAWD is waiting for answer words 1 and 2
- 1 = QAWD waits for answer words 3 and 4

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0x03: Status Register 3 (QAWD)

Address: 00011b; Type: Read Only (RO)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	QAWDWINDOW_TIMER							
Data Bit/ Name	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**
	QAWD_TIME_ ERR	QAWD_ CODE_ERR	QAWD_RAND [5:0]					

QAWD_WINDOW_TIMER [D21:D14]

The 8 MSBs [17:10] of the QAWD window 8-bit counter, resolution = $2^{10} \times t$.

QAWD_TIME_ERR [D13]

At least one timing error occurred in the last question-and-answer cycle.

QAWD_CODE_ERR [D12]

At least one data error occurred in last question-and-answer cycle

QAWD_RAND [D11:D6]

Randomly generated 6-bit word for the question-and-answer watchdog.

To generate the answer words, these bits must be read (questioned) from the microcontroller during the typical mode of operation.

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0x04: Diagnostic Register 0

Address: 00100b; Type: Read, or Write 1 to Clear (RW1C); Faults are not latched until NPOR ceases to release.

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	VREG_OV	VREG_UV	VUC_OV	VUC_UV	VLDOA_OV	VLDOA_UV	VLDOB_OV	VLDOB_UV
Data Bit/ Name	D13	D12	D11	D10	D9	D8	D7	D6
	VLDOP1_OV	VLDOP1_UV	VLDOP2_OV	VLDOP2_UV	VCP_OV	VCP_UV	TSD_F	VIN_OV

VREG_OV [D21]

Indicates if an overvoltage occurs at the preregulator output:

- 0: Fault not detected (default)
- 1: Fault detected

VREG_UV [D20]

Indicates if an undervoltage occurs at the preregulator output:

- 0: Fault not detected (default)
- 1: Fault detected

VUC_OV [D19]

Indicates if an overvoltage occurs at the VUC LDO output:

- 0: Fault not detected (default)
- 1: Fault detected

VUC_UV [D18]

Indicates if an undervoltage occurs at the VUC LDO output:

- 0: Fault not detected (default)
- 1: Fault detected

VLDOA_OV [D17]

Indicates if an overvoltage occurs at the VLDOA LDO output:

- 0: Fault not detected (default)
- 1: Fault detected

VLDOA_UV [D16]

Indicates if an undervoltage occurs at the VLDOA LDO output:

- 0: Fault not detected (default)
- 1: Fault detected

VLDOB_OV [D15]

Indicates if an overvoltage occurs at the VLDOB LDO output:

- 0: Fault not detected (default)
- 1: Fault detected

VLDOB_UV [D14]

Indicates if an undervoltage occurs at the VLDOB LDO output:

- 0: Fault not detected (default)
- 1: Fault detected

VLDOP1_OV [D13]

Indicates if an overvoltage occurs at the VLDOP1 LDO output:

- 0: Fault not detected (default)
- 1: Fault detected

VLDOP1_UV [D12]

Indicates if an undervoltage occurs at the VLDOP1 LDO output:

- 0: Fault not detected (default)
- 1: Fault detected

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VLDOP2_OV [D11]

Indicates if an overvoltage occurs at the VLDOP1 LDO output:

- 0: Fault not detected (default)
- 1: Fault detected

VLDOP2_UV [D10]

Indicates if an undervoltage occurs at the VLDOP2 LDO output:

- 0: Fault not detected (default)
- 1: Fault detected

VCP_OV [D9]

Indicates if an overvoltage occurs at the VCP pin:

- 0: Fault not detected (default)
- 1: Fault detected

VCP_UV [D8]

Indicates if an undervoltage occurs at the VCP pin:

- 0: Fault not detected (default)
- 1: Fault detected

TSD_F [D7]

Indicates if a thermal fault occurs:

- 0: Fault not detected (default)
- 1: Fault detected

VIN_OV [D6]

Indicates if an overvoltage occurs at the VIN pin:

- 0: Fault not detected (default)
- 1: Fault detected

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0x05: Diagnostic Register 1

Address: 00101b; Type: Read, or Write 1 to Clear (RW1C); Faults are not latched until NPOR is released.

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	VUC_OC	VLDOA_OC	VLDOB_OC	VLDOP1_OC	VLDOP2_OC	VREG_OC	UNUSED	UNUSED
Data Bit/ Name	D13	D12	D11	D10	D9	D8	D7	D6
	UNUSED	UNUSED	TWARN_F	VUC_AMR_OV	BOOT1_UV	BOOT2_UV	LX1_STG	LX2_STG

VUC_OC [D21]

Indicates if the VUC regulator undergoes an overcurrent condition:

- 0: In the time since the register was last cleared, an overcurrent event did not occur (default)
- 1: An overcurrent event occurred

VLDOA_OC [D20]

Indicates if the VLDOA regulator undergoes an overcurrent condition:

- 0: In the time since the register was last cleared, an overcurrent event did not occur (default)
- 1: An overcurrent event occurred

VLDOB_OC [D19]

Indicates if the VLDOB regulator undergoes an overcurrent condition:

- 0: In the time since the register was last cleared, an overcurrent event did not occur (default)
- 1: An overcurrent event occurred

VLDOP1_OC [D18]

Indicates if the VLDOP1 regulator undergoes an overcurrent condition:

- 0: In the time since the register was last cleared, an overcurrent event did not occur (default)
- 1: An overcurrent event occurred

VLDOP2_OC [D17]

Indicates if the VLDOP2 regulator undergoes an overcurrent condition:

- 0: In the time since the register was last cleared, an overcurrent event did not occur (default)
- 1: An overcurrent event occurred

VREG_OC [D16]

Indicates if a VREG overcurrent occurs:

- 0: Fault not detected (default)
- 1: Fault detected

UNUSED[D15]

Unused

UNUSED[D14]

Unused

UNUSED [D13]

Unused

UNUSED [D12]

Unused

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TWARN_F [D11]

Indicates if a temperature warning is flagged to the MCU:

- 0: Fault not detected (default)
- 1: Fault detected

VUC_AMR_OV [D10]

Indicates if an absolute maximum rate overvoltage occurs at the VUC LDO output:

- 0: Fault not detected (default)
- 1: Fault detected

BOOT1_UV [D9]

Indicates if the buck boot is undervoltage:

- 0: Fault not detected (default)
- 1: Fault detected

BOOT2_UV [D8]

Indicates if the boost boot is undervoltage:

- 0: Fault not detected (default)
- 1: Fault detected

LX1_STG [D7]

Indicates if LX1 is shorted to ground:

- 0: Fault not detected (default)
- 1: Fault detected

LX2_STG [D6]

Indicates if LX2 is shorted to ground:

- 0: Fault not detected (default)
- 1: Fault detected

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0x06: Diagnostic Register 2

Address: 00110b; Type: Read, or Write 1 to Clear (RW1C); Faults are not latched until NPOR is not released.

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	SE	PWM_F	CLK_OOR	WWD_F	QAWD_F	PWWD_F	POE_FAIL	NPOR_FAIL
Data Bit/ Name	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**
	WD_F_FAIL	FFn_FAIL	NPOR_F	NPOR_REQ	NPOR_MCU	NPOR_PWR	UNUSED	SPI_CSN_TO

SE [D21]

Indicates if there is a serial communications error:

- 0: Error not detected (default)
- 1: Fault detected—There were less than or more than 32 rising SCK edges in a frame, or a CRC error occurred

PWM_F [D20]

Indicates if there is a PWM oscillator fault:

- 0: Fault not detected (default)
- 1: Stuck fault detected

CLK_OOR [D19]

Indicates if there is a main and/or PWM oscillator fault:

- 0: Fault not detected (default)
- 1: Out-of-range fault detected

WWD_F [D18]

Indicates if there is a window watchdog fault:

- 0: Fault not detected (default)
- 1: Fault detected

QAWD_F [D17]

Indicates if there is a question-and-answer watchdog fault:

- 0: Fault not detected (default)
- 1: Fault detected

PWWD_F [D16]

Indicates if there is a pulse-width watchdog fault:

- 0: Fault not detected (default)
- 1: Fault detected

POE_FAIL [D15]

Indicates if there is a POE output pin fault:

- 0: No fault (default)
- 1: Fault detected—The POE output pin does not match the demand from the A81411

NPOR_FAIL [D14]

Indicates if there is an NPOR fault. The NPOR output value is 1, even if the A81411 demands a value of 0:

- 0: Fault not detected (default)
- 1: Fault detected

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WD_F_FAIL [D13]

Indicates if the WD_Fn pin does not match the demand from the A81411:

- 0: Fault not detected (default)
- 1: Fault detected

FFn_FAIL [D12]

Indicates if the FFn pin does not match the demand from the A81411:

- 0: Fault not detected (default)
- 1: Fault detected

NPOR_F [D11]

Indicates if the A81411 resets the MCU because of an internal fault:

- 0: Reset did not occur (default)
- 1: MCU reset by a fault; refer to the NPOR key configuration

NPOR_REQ [D10]

Indicates if the MCU requests a reset by SPI command:

- 0: Request not received (default)
- 1: MCU reset itself by NPOR input key (NPOR_VAL = 0)

NPOR_MCU [D9]

Indicates if MCU self-reset occurs by pulling the NPOR pin low. The value of the NPOR output is 0, even if the A81411 demands the value to be 1:

- 0: Reset did not occur (default)
- 1: MCU pulled the NPOR pin low, which triggered a self-reset sequence

NPOR_PWR [D8]

Indicates if the A81411 resets the MCU because of an internal reset:

- 0: NPOR_PWR bit is cleared by the MCU via SPI
- 1: MCU reset is caused by powerup (default)

UNUSED [D7]

Unused

SPI_CSN_TO [D6]

SPI CSN timeout

- 0: Timeout not reached (default)
- 1: Timeout occurred

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0x07: WD and NPOR Input Keys

Address: 00111b; Type: Write Only (WO)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	WD_KEY [7:0]							
Data Bit/ Name	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**
	NPOR_KEY [7:0]							

WD_KEY [D21:D14]

Watchdog mode key. To enable flash mode or to restart the watchdog, three 8-bit words (WORD1 – WORD3) must be sent in the correct order. If an incorrect word is received, the register resets and the first word must be resent. The third 8-bit word (WORD3) is the command to force the watchdog to transition from state to state.

		WD_KEY [D21]	WD_KEY [D20]	WD_KEY [D19]	WD_KEY [D18]	WD_KEY [D17]	WD_KEY [D16]	WD_KEY [D15]	WD_KEY [D14]
WORD1 (Key)		1	1	0	1	0	0	1	1
WORD2 (Key)		0	0	1	1	0	0	1	1
WORD3 (Command)	**Flash**	1	1	0	0	1	1	0	0
	Configuration	1	1	0	0	1	1	0	1
	Restart	1	1	0	0	1	1	1	0
	Disable	1	1	0	0	1	1	1	1

NPOR_KEY [D13:D6]

NPOR key. To unlock the NPOR configuration register, two 8-bit words (WORD1, WORD2) must be sent in the correct order. If an incorrect word is received, the register resets and the first word must be resent. A third 8-bit word (WORD3) can modify which signals are used for the NPOR logic; it also allows the MCU to command the NPOR to toggle low for 2 ms. If the A81411 experiences a controller power-on reset (MPOR), it transitions back to the default state.

	NPOR_ KEY [D13]	NPOR_ KEY [D12]	NPOR_ KEY [D11]	NPOR_ KEY [D10]	NPOR_ KEY [D9]	NPOR_ KEY [D8]	NPOR_ KEY [D7]	NPOR_ KEY [D6]	
WORD1 (Key)	1	1	0	1	0	1	0	0	
WORD2 (Key)	0	0	1	0	1	0	1	1	
WORD3 (Command)	NPOR_ VAL	FIXED	FIXED	VUC_OV	VLDOA_ UV	VLDOA_ OV	WD_F	VIN_OV	
	0	1	1	X	X	X	X	X	Initiate MCU reset by setting NPOR low for 2 ms. Bits [D10:D6] do not change.
	1	1	1	VUC_OV value [1]	VLDOA_ UV value [1]	VLDOA_ OV value [1]	WD_F value [1]	VIN_OV value [1]	Set new value for buts [D10:D6]
	X	0	X	X	X	X	X	X	Invalid command; does not have an effect
	X	X	0	X	X	X	X	X	Invalid command; does not have an effect

[1] Note: 0 = fault is excluded from NPOR generation; 1 = fault is included in NPOR generation. VUC_OV default value is 1, while it is 0 for all the other bits [D9:D6].

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0x08: Configuration Register 0

Address: 01000b; Type: Read or Write (RW)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	UNUSED	VLDOP2_EN [1:0]		VLDOP1_EN [1:0]		VLDOA_EN	WDF_2_FFn	DITH_DIS
Data Bit/ Name	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**
	TSD_F_MSK	POE_ FORCE	UNUSED	AMUX_SEL [3:0]				FFN_PIN_CHCK_ LAT_EN

UNUSED [D21]

Unused

VLDOP2_EN [D20:D19]

Controls the on and off states of the VLDOP2 linear regulator:

[D20]	[D19]	Description
0	0	Disabled or off (default)
0	1	Maintains previous state
1	0	Maintains previous state
1	1	Enabled or on

VLDOP1_EN [D18:D17]

Controls the on and off states of the VLDOP1 linear regulator:

[D18]	[D17]	Description
0	0	Disabled or off (default)
0	1	Maintains previous state
1	0	Maintains previous state
1	1	Enabled or on

VLDOA_EN [D16]

Controls the on and off states of the VLDOA linear regulator:

- 0: VLDOA linear regulator is off
- 1: VLDOA linear regulator is on (default)

WDF_2_FFn [D15]

Determines if FFn is to be forced low by a watchdog fault:

- 0: FFn does not transition low if a watchdog fault occurs (default)
- 1: FFn transitions low if a watchdog fault occurs

DITH_DIS [D14]

Controls the status of PWM frequency dithering:

- 0: Dithering is enabled (default)
- 1: Dithering is disabled

TSD_F_MSK [D13]

Controls the mask of the TSD_F fault:

- 0: A81411 shuts down upon detection of a TSD fault (default)
- 1: FFn is set low and A81411 does not shut down upon detection of a TSD fault

POE_FORCE [D12]

POE force bit:

- 0: POE control is not affected
- 1: Forces POE low

UNUSED [D11]

Unused

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AMUX_SEL [D10:D7]

AMUX output:

AMUX_SEL [D10]	AMUX_SEL [D9]	AMUX_SEL [D8]	AMUX_SEL [D7]	AMUX Output
0	0	0	0	VREG ÷ 3
0	0	0	1	VUC ÷ 3
0	0	1	0	VLDOA ÷ 3
0	0	1	1	VLDOB ÷ 3
0	1	0	0	VLDOP1 ÷ 3
0	1	0	1	VLDOP2 ÷ 3
0	1	1	0	VIN ÷ 24
0	1	1	1	VENBAT ÷ 24
1	0	0	0	VCP ÷ 6
1	0	0	1	VBG1 (default)
1	0	1	0	VBG2
1	0	1	1	VTEMP
1	1	0	0	Unused
1	1	0	1	Unused
1	1	1	0	Unused
1	1	1	1	Unused

FFN_PIN_CHCK_LAT_EN [D6]

Determines if the status or latched pin checker faults are to be used for FFn:

- 0: Use pin checker status bits
- 1: Use pin checker latched bits (default)

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0x09: Configuration Register 1 (EN_LAT)

Address: 01001b; Type: Read or Write (RW)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	ENCAN_LAT [7:0]							
Data Bit/ Name	D13	D12	D11	D10	D9	D8	D7	D6
	ENBAT_LAT [7:0]							

ENCAN_LAT [D21:D14]

ENCAN latch reset word:

- 0x00 = ENCAN latch ENCAN_LAT output is low (default).
- 0x01 to 0xA9 = Previous state.
- 0xAA = ENCAN latch signal (ENCAN_LAT) is set to 1. If ENCAN is 0, the MCU keeps A81411 in the on state.
- 0xAB to 0xFF = Previous state.

ENBAT_LAT [D13:D6]

ENBAT latch reset word:

- 0x00 = ENBAT latch ENBAT_LAT output is low (default).
- 0x01 to 0x54 = Previous state.
- 0x55 = ENBAT latch signal (ENBAT_LAT) is set to 1. If ENBAT is 0, the MCU keeps A81411 in the on state.
- 0x56 to 0xFF = Previous state

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0x0A: Configuration Register 2 (VLDOPx and WD)

Address: 01010b; Type: Read or Write (RW)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	UNUSED	VLDOP1_OUT	VLDOP2_OUT	UNUSED	QAWD_TIMERS	QAWD_RETRY [2:0]		
Data Bit/ Name	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**
	WD_SEL [2:0] WD_SEL, WD_SEL_0			UNUSED	WWD_TIMER [3:0] WWD_TIMER_2, WWD_TIMER_1, WWD_TIMER_0			

UNUSED [D21]

Unused

VLDOP1_OUT [D20]

VLDOP1 regulator output voltage:

- 0 = Output is 5 V (default)
- 1 = Output is 3.3 V

VLDOP2_OUT [D19]

VLDOP2 regulator output voltage:

- 0 = Output is 5 V (default)
- 1 = Output is 3.3 V

UNUSED [D18]

Unused

QAWD_TIMERS [D17]

Selects the number of windows for the question-and-answer watchdog:

- 0 (default) = One window selected, programmed using QAWD timer 1
- 1 = Two windows selected

QAWD_RETRY [D16:D14]

Acceptable number of retries:

QAWD_ RETRY [D16]	QAWD_ RETRY [D15]	QAWD_ RETRY [D14]	Acceptable Number of Retries
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

■ Default

WD_SEL [D13:D11]

Type of active watchdog:

WD_SEL [D13]	WD_SEL [D12]	WD_SEL [D11]	Type of Active Watchdog
0	0	0	None; reset value for WD_SEL [2:0]
0	0	1	Question-and-answer watchdog (QAWD) (default, after t_{CONFIG_WD})
0	1	0	Window watchdog (WWD)
0	1	1	Question-and-answer watchdog and window watchdog
1	0	0	Pulse-width watchdog
1	0	1	Question-and-answer watchdog and pulse-width watchdog
1	1	x	None; default to QAWD after t_{CONFIG_WD}

UNUSED [D10]

Unused

WWD_TIMER [D9:D2]

Watchdog timers:

WWD_ TIMER [D9]	WWD_ TIMER [D8]	WWD_ TIMER [D7]	WWD_ TIMER [D6]	t_{WWD_FAST}	t_{WWD_SLOW}
0	0	0	0	0.5 ms	4 ms
0	0	0	1	1 ms	8 ms
0	0	1	0	2 ms	16 ms
0	0	1	1	4 ms	32 ms
0	1	0	0	6 ms	42 ms
0	1	0	1	8 ms	64 ms
0	1	1	0	10 ms	80 ms
0	1	1	1	12.5 ms	100 ms
1	0	0	0	4.25 µs	6.00 µs
1	0	0	1	8.50 µs	12 µs
1	0	1	0	17 µs	24 µs
1	0	1	1	34 µs	48 µs

■ Default

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0x0B: Configuration Register 3 (QAWD_TIMER)

Address: 01011b; Type: Read or Write (RW)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	QAWD_TIMER1_MAX [3:0]				QAWD_TIMER1_MIN [3:0]			
Data Bit/ Name	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**
	QAWD_TIMER2_MAX [3:0]				QAWD_TIMER2_MIN [3:0]			

QAWD_TIMER1_MAX [D21:D18]

Maximum timeout:

QAWD_ TIMER1_ MAX [D21]	QAWD_ TIMER1_ MAX [D20]	QAWD_ TIMER1_ MAX [D19]	QAWD_ TIMER1_ MAX [D18]	MAX_ TIMEOUT t_{QA_MAX2} (ms)
0	0	0	0	1
0	0	0	1	1.5
0	0	1	0	2
0	0	1	1	2.5
0	1	0	0	2.75
0	1	0	1	3
0	1	1	0	3.25
0	1	1	1	3.5
1	0	0	0	3.75
1	0	0	1	4
1	0	1	0	4.25
1	0	1	1	4.5
1	1	0	0	8
1	1	0	1	16
1	1	1	0	24
1	1	1	1	32

■ Default

For invalid configurations, the question-and-answer watchdog function cannot be guaranteed. Invalid configurations include:

- QAWD_TIMER1_MIN [3:0] ≥ QAWD_TIMER1_MAX [3:0]
- QAWD_TIMER2_MIN [3:0] ≥ QAWD_TIMER2_MAX [3:0].

QAWD_TIMER1_MIN [D17:D14]

Minimum timeout:

QAWD_ TIMER1_ MIN [D17]	QAWD_ TIMER1_ MIN [D16]	QAWD_ TIMER1_ MIN [D15]	QAWD_ TIMER1_ MIN [D14]	MIN_ TIMEOUT t_{QA_MIN1} (ms)
0	0	0	0	0.5
0	0	0	1	1
0	0	1	0	1.5
0	0	1	1	2
0	1	0	0	2.25
0	1	0	1	2.5
0	1	1	0	2.75
0	1	1	1	3
1	0	0	0	3.25
1	0	0	1	3.5
1	0	1	0	3.75
1	0	1	1	4
1	1	0	0	5
1	1	0	1	8
1	1	1	0	12
1	1	1	1	16

■ Default

For invalid configurations, the question-and-answer watchdog function cannot be guaranteed. Invalid configurations include:

- QAWD_TIMER1_MIN [3:0] ≥ QAWD_TIMER1_MAX [3:0]
- QAWD_TIMER2_MIN [3:0] ≥ QAWD_TIMER2_MAX [3:0].

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QAWD_TIMER2_MAX [D13:D10]

Maximum timeout:

QAWD_TIMER2_MAX [D13]	QAWD_TIMER2_MAX [D12]	QAWD_TIMER2_MAX [D11]	QAWD_TIMER2_MAX [D10]	MAX_TIMEOUT t_{QA_MAX2} (ms)
0	0	0	0	1
0	0	0	1	1.5
0	0	1	0	2
0	0	1	1	2.5
0	1	0	0	2.75
0	1	0	1	3
0	1	1	0	3.25
0	1	1	1	3.5
1	0	0	0	3.75
1	0	0	1	4
1	0	1	0	4.25
1	0	1	1	4.5
1	1	0	0	8
1	1	0	1	16
1	1	1	0	24
1	1	1	1	32

■ Default

For invalid configurations, the question-and-answer watchdog function cannot be guaranteed. Invalid configurations include:
- QAWD_TIMER1_MIN [3:0] ≥ QAWD_TIMER1_MAX [3:0]
- QAWD_TIMER2_MIN [3:0] ≥ QAWD_TIMER2_MAX [3:0].

QAWD_TIMER2_MIN [D9:D6]

Minimum timeout:

QAWD_TIMER2_MIN [D9]	QAWD_TIMER2_MIN [D8]	QAWD_TIMER2_MIN [D7]	QAWD_TIMER2_MIN [D6]	MIN_TIMEOUT t_{QA_MIN1} (ms)
0	0	0	0	0.5
0	0	0	1	1
0	0	1	0	1.5
0	0	1	1	2
0	1	0	0	2.25
0	1	0	1	2.5
0	1	1	0	2.75
0	1	1	1	3
1	0	0	0	3.25
1	0	0	1	3.5
1	0	1	0	3.75
1	0	1	1	4
1	1	0	0	5
1	1	0	1	8
1	1	1	0	12
1	1	1	1	16

■ Default

For invalid configurations, the question-and-answer watchdog function cannot be guaranteed. Invalid configurations include:
- QAWD_TIMER1_MIN [3:0] ≥ QAWD_TIMER1_MAX [3:0]
- QAWD_TIMER2_MIN [3:0] ≥ QAWD_TIMER2_MAX [3:0].

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0x0C: Configuration Register 4 (QAWD_ANS)

Address: 01100b; Type: Read or Write (RW)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	QAWD_ANS_2_4 [5:0]						UNUSED	
Data Bit/ Name	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**
	UNUSED		QAWD_ANS_1_3 [5:0]					

QAWD_ANS_1_3 [D22:D16]

MCU writes question-and-answer watchdog answer word 2 and word 4 here.

UNUSED [D15:D13]

Unused.

QAWD_ANS_2_4 [D12:D6]

MCU writes question-and-answer watchdog answer word 1 and word 3 here.

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0x0D: Configuration Register 5 (PWWD)

Address: 01101b; Type: Read or Write (RW)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	PWWD_EDGE_TO [1:0]		PWWD_ACT_TO [1:0]		PWWD_WIN_TOL [1:0]		PWWD_PW [1:0]	
Data Bit/ Name	D13	D12	D11	D10	D9	D8	D7	D6
	PWWD_DEC [1:0]		PWWD_INC [1:0]		PWWD_MAX [1:0]		PWWD_POE_DLY [1:0]	

PWWD_EDGE_TO [D21:D20]

First-edge timeout:

PWWD_EDGE_TO [D21]	PWWD_EDGE_TO [D20]	First-Edge Timeout (ms)
0	0	2.5
0	1	5 (default)
1	0	10
1	1	15

PWWD_ACT_TO [D19:D18]

Nonactivity timeout:

PWWD_ACT_TO [D19]	PWWD_ACT_TO [D18]	Nonactivity Timeout (ms)
0	0	8
0	1	16 (default)
1	0	24
1	1	32

PWWD_WIN_TOL [D17:D16]

Window tolerance:

PWWD_WIN_TOL [D17]	PWWD_WIN_TOL [D16]	Window Tolerance (%)
0	0	±8
0	1	±13 (default)
1	0	±18
1	1	±23

PWWD_PW [D15:D14]

Pulse width:

PWWD_PW [D15]	PWWD_PW [D14]	Pulse Width (ms)
0	0	0.5
0	1	1 (default)
1	0	1.5
1	1	2

PWWD_DEC [D13:D12]

Decrement amount:

PWWD_DEC [D13]	PWWD_DEC [D12]	Decrement Amount (counts)
0	0	1
0	1	2 (default)
1	0	3
1	1	4

PWWD_INC [D11:D10]

Increment amount:

PWWD_INC [D11]	PWWD_INC [D10]	Increment Amount (counts)
0	0	5
0	1	10 (default)
1	0	20
1	1	30

PWWD_MAX [D9:D8]

Maximum fault counter value:

PWWD_MAX [D9]	PWWD_MAX [D8]	Maximum Fault Counter Value
0	0	80
0	1	120
1	0	160 (default)
1	1	220

PWWD_POE_DLY [D7:D6]

Sets the value preloaded into the PWWD error counter. This value is used to prequalify the WD_IN clock before POE is allowed to transition high:

PWWD_POE_DLY [D7]	PWWD_POE_DLY [D6]	Value
0	0	2 (default)
0	1	4
1	0	10
1	1	16

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0x0E: Configuration Register 6 (ABIST and CSN_TO)

Address: 01110b; Type: Read or Write (RW)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	ABIST_ON	UNUSED	UNUSED	UNUSED	UNUSED	SPI_CSN_TO_EN	SPI_CSN_TO_THR [9:8]	
Data Bit/ Name	D13	D12	D11	D10	D9	D8	D7	D6
	SPI_CSN_TO_THR [7:0] ENBAT_LAT_6 ENBAT_LAT_5 ENBAT_LAT_4 ENBAT_LAT_3 ENBAT_LAT_2 ENBAT_LAT_1 ENBAT_LAT_0							

ABIST_ON [D21]

Runs internal analog self-test:

- 0: ABIST only runs at startup (default)
- 1: ABIST runs on this command; cleared when ABIST is complete

SPI_CSN_TO_EN [D16]

CSN timeout enable:

- 0: Disabled
- 1: Enabled (default)

SPI_CSN_TO_THR [D15:D6]

CSN timeout threshold

- 0x000 to 0x3FF: 10-bit threshold compared with CSN timeout counter. If the counter reaches the threshold, SPI_CSN_TO is asserted. The CSN timeout counter is incremented each 1 ms, and it is asynchronous to SPI; thus, if the CSN timeout threshold is set to 1, the actual timeout fault bit is set to a value between 0 and 1 ms. The default value is 0x12C (this means the timeout occurs between 299 ms and 300 ms).

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0x0F: Read-Back Register

Address: 01111b; Type: Read or Write (RW)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	Read-Back [15:8]							
Data Bit/ Name	D13	D12	D11	D10	D9	D8	D7	D6
	Read-Back [7:0]							

Read-Back [D21:D6]

The host microcontroller can implement a loop-back test with this register. The host should write a specific pattern (value) to this register, read it back, and compare the two results. To ensure a bit is not stuck, the host should use at least two different write patterns.

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0x10: Verify Result Register 0

Address: 10000b; Type: Read, or Write 1 to Clear (RW1C)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	VUC_OV_FAIL	VLDOA_OV_FAIL	VLDOB_OV_FAIL	VLDOP1_OV_FAIL	VLDOP2_OV_FAIL	VREG_OV_FAIL	VCP_OV_FAIL	VIN_OV_FAIL
Data Bit/ Name	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**
	VUC_UV_FAIL	VLDOA_UV_FAIL	VLDOB_UV_FAIL	VLDOP1_UV_FAIL	VLDOP2_UV_FAIL	VREG_UV_FAIL	VCP_UV_FAIL	TSD_BIST_FAIL

VUC_OV_FAIL [D21]

Indicates if the VUC overvoltage circuit fails its self-test:

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. FFn set low. To clear and regain FFn functionality, write the value 1.

VLDOA_OV_FAIL [D20]

Indicates if the VLDOA overvoltage circuit fails its self-test:

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. FFn set low. To clear and regain FFn functionality, write the value 1.

VLDOB_OV_FAIL [D19]

Indicates if the VLDOB overvoltage circuit fails its self-test:

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. FFn set low. To clear and regain FFn functionality, write the value 1.

VLDOP1_OV_FAIL [D18]

Indicates if the VLDOP1 overvoltage circuit fails its self-test:

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. FFn set low. To clear and regain FFn functionality, write the value 1.

VLDOP2_OV_FAIL [D17]

Indicates if the VLDOP2 overvoltage circuit fails its self-test:

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. FFn set low. To clear and regain FFn functionality, write the value 1.

VREG_OV_FAIL [D16]

Indicates if the VREG overvoltage circuit fails its self-test:

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. FFn set low. To clear and regain FFn functionality, write the value 1.

VCP_OV_FAIL [D15]

Indicates if the VCP overvoltage circuit fails its self-test:

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. FFn set low. To clear and regain FFn functionality, write the value 1.

VIN_OV_FAIL [D14]

Indicates if the VIN overvoltage circuit fails its self-test:

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. FFn set low. To clear and regain FFn functionality, write the value 1.

VUC_UV_FAIL [D13]

Indicates if the VUC undervoltage circuit fails its self-test:

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. FFn set low. To clear and regain FFn functionality, write the value 1.

VLDOA_UV_FAIL [D12]

Indicates if the VLDOA undervoltage circuit fails its self-test:

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. FFn set low. To clear and regain FFn functionality, write the value 1.

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VLDOB_UV_FAIL [D11]

Indicates if the VLDOB undervoltage circuit fails its self-test:

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. FFn set low. To clear and regain FFn functionality, write the value 1.

VLDOP1_UV_FAIL [D10]

Indicates if the VLDOP1 undervoltage circuit fails its self-test:

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. FFn set low. To clear and regain FFn functionality, write the value 1.

VLDOP2_UV_FAIL [D9]

Indicates if the VLDOP2 undervoltage circuit fails its self-test:

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. FFn set low. To clear and regain FFn functionality, write the value 1.

VREG_UV_FAIL [D8]

Indicates if the VREG undervoltage circuit fails its self-test:

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. FFn set low. To clear and regain FFn functionality, write the value 1.

VCP_UV_FAIL [D7]

Indicates if the VCP undervoltage circuit fails its self-test

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. FFn set low. To clear and regain FFn functionality, write the value 1.

TSD_BIST_FAIL [D6]

Indicates if the TSD circuit fails its self-test

- 0: Self-test passed (default value at powerup).
- 1: Self-test failed. FFn set low. To clear and regain FFn functionality, write the value 1.

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0x11: Verify Result Register 1

Address: 10001b; Type: Read, or Write 1 to Clear (RW1C)

Data Bit/ Name	D21	D20	D19	D18	D17	D16	D15	D14
	ABIST_FAIL	LBIST_FAIL	INT_LOGIC_ERR	–	–	–	–	–
Data Bit/ Name	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**
	–	–	–	–	–	–	–	–

ABIST_FAIL [D21]

Indicates if the A81411 fails ABIST:

- 0: ABIST passed (default value at powerup).
- 1: ABIST failed. FFn set low. To clear and regain FFn functionality, write the value 1.

LBIST_FAIL [D20]

Indicates if the A81411 failed LBIST:

- 0: LBIST passed (default value at powerup).
- 1: LBIST failed. FFn set low. To clear and regain FFn functionality, write the value 1.

INT_LOGIC_ERR [D19]

Indicates if an internal logic error occurs:

- 0: The digital logic function is OK.
- 1: An internal logic error occurred.

UNUSED [D18:D6]

Unused

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PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference DWG-0000378, Rev. 3)
Dimensions in millimeters
NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown

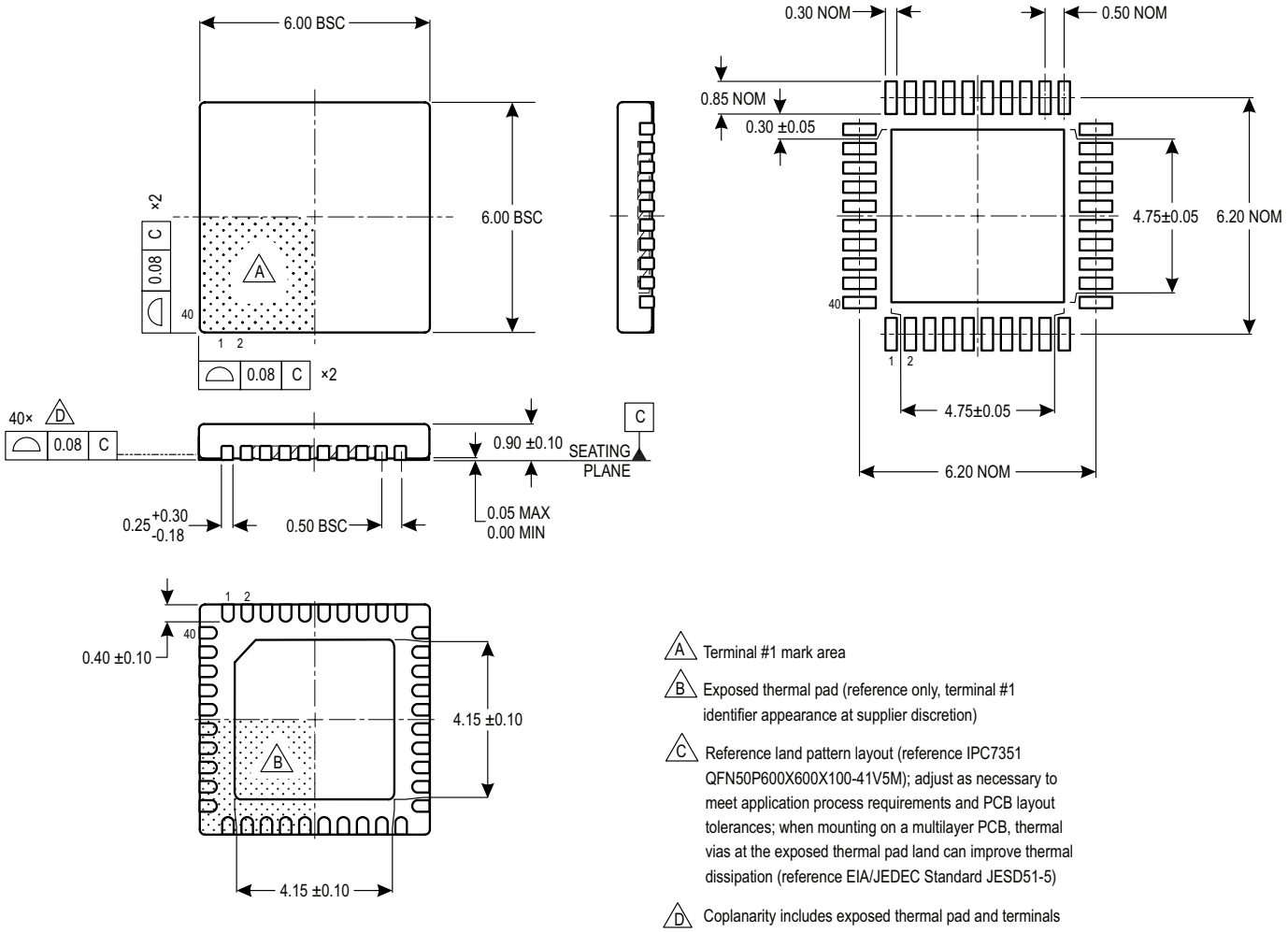

Figure xx: Package Title

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Revision History

Number	Date	Description
–	January 13, 2025	Initial release
1	January 21, 2025	Removed confidentiality watermark (all pages), Updated Application and Features and Benefits sections (page 1), added ESD Characteristics table (page 3)
2	January 31, 2025	Updated ASIL logo (page 1), updated Electrical Characteristics table (page 7, page 12)
3	February 10, 2025	Created short-form datasheet

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