Dual-Channel Hall-Effect Direction Detection Sensor IC

FEATURES AND BENEFITS

- AEC-Q100 automotive qualified
- ISO 26262 compliant
- ASIL Ready: possesses device features for safety-critical systems

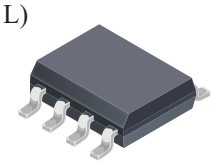
ISO 26262 ASIL Ready

- Precisely aligned dual Hall elements
- Tightly matched magnetic switchpoints
- Speed and direction outputs
- Individual Hall element outputs (L package)
- Output short-circuit protection

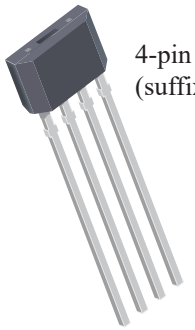
Continued on the next page…

PACKAGES

8-pin SOIC
(suffix L)



4-pin SIP
(suffix K)



Not to scale

DESCRIPTION

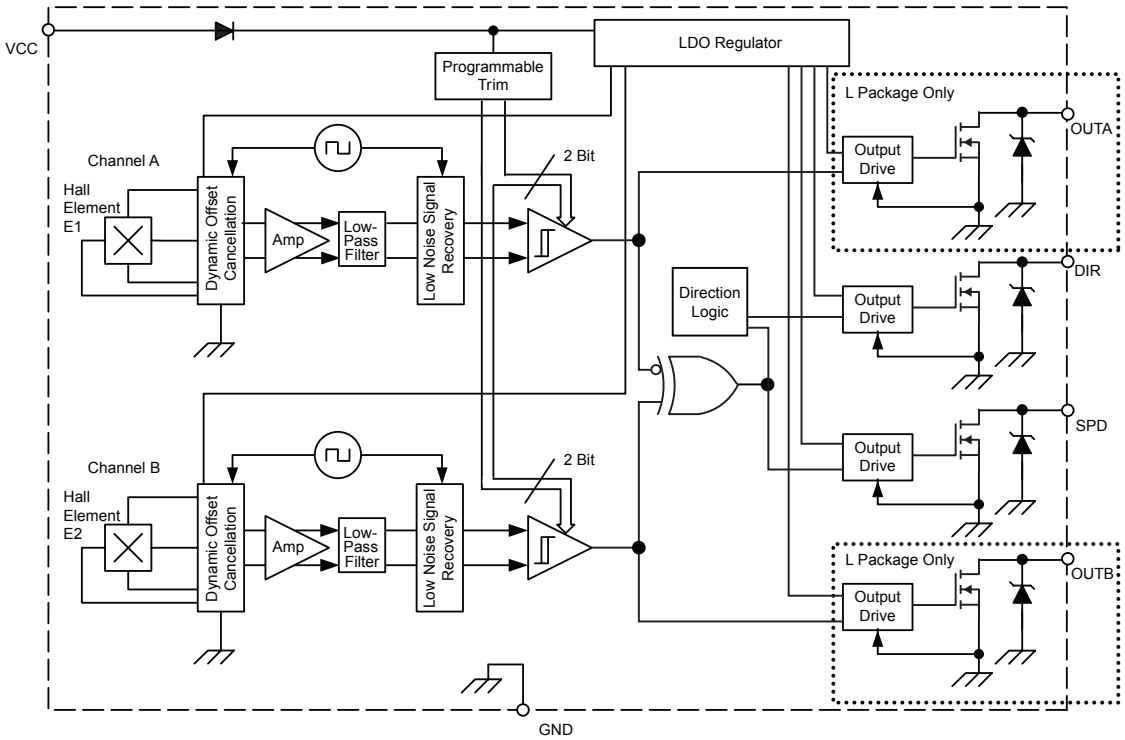
The A1233 is a dual-channel Hall-effect sensor IC ideal for use in speed and direction sensing applications incorporating encoder ring-magnet targets. The A1233 provides various output signals that indicate speed and direction of target rotation. The Hall elements are both photolithographically aligned to better than 1 µm. Maintaining accurate displacement between the two active Hall elements eliminates the major manufacturing hurdle encountered in fine-pitch detection applications. The A1233 is a highly sensitive, temperature-stable magnetic device ideal for use in harsh automotive and industrial environments.

The Hall elements of the A1233 are spaced 1.63 mm apart, which provides excellent speed and direction information for small-geometry targets. Extremely low-drift amplifiers guarantee symmetry between the switches to maintain signal quadrature. An on-chip regulator allows the use of this device over a wide operating voltage range of 3.5 to 24 V.

End-of-line trimming of the Hall element switchpoints provides tight matching capability. The Allegro™ high-frequency chopper stabilization technique cancels offsets in each channel, providing stable operation over the full specified temperature and voltage ranges.

Continued on the next page…

Functional Block Diagram



FEATURES AND BENEFITS (continued)

- Operation from an unregulated power supply
- Wide operating temperature range
- Wide operating voltage range
- Integrated EMC-ESD protection
- Superior temperature stability and industry-leading jitter performance through use of advanced chopper stabilization topology

DESCRIPTION (continued)

The A1233 has integrated protection against transients on the supply and output pins and short-circuit protection on all outputs.

The A1233 is available in a 4-pin SIP and a plastic 8-pin SOIC surface-mount package. Both packages are lead (Pb) free, with 100% matte-tin leadframe plating.

SELECTION GUIDE

Part Number	Package	Packing [1]	T_A (°C)
A1233LK-T	4-pin through hole SIP	Bulk bag, 500 pieces/bag	–40 to 150
A1233LLTR-T	8-pin surface mount SOIC	Tape and reel, 3000 pieces/reel	

[1] Contact Allegro for additional packing options.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage [2]	V_{CC}		26.5	V
Reverse Battery Voltage [2]	V_{RCC}		–18	V
Output Off Voltage [2]	V_{OUTPUT}		V_{CC}	V
Reverse Output Voltage [2]	V_{ROUT}		–0.5	V
Reverse Output Current	I_{ROUT}		–10	mA
Output Sink Current	$I_{OUTPUT(Sink)}$		30	mA
Magnetic Flux Density [3]	B		Unlimited	–
Operating Ambient Temperature	T_A	Range L	–40 to 150	°C
Maximum Junction Temperature	$T_{J(max)}$		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

[2] This rating does not apply to extremely short voltage transients such as Load Dump and/or ESD. Those events have individual ratings, specific to the respective transient voltage event.

[3] Guaranteed by design.

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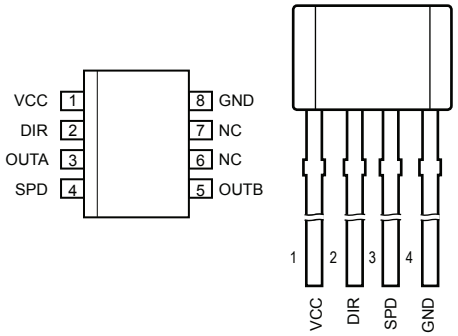
PINOUT DIAGRAMS AND TERMINAL LIST

Pinout Diagrams



L Package K Package

Terminal List Table

Number		Name	Description
K	L		
1	1	VCC	Input power supply; tie to GND with bypass capacitor
2	2	DIR	Output signal indicating direction of target movement
–	3	OUTA	Output from E1 via a Schmitt circuit
3	4	SPD	Output signal indicating speed of target movement
–	5	OUTB	Output from E2 via a Schmitt circuit
–	6, 7	NC	No connection
4	8	GND	Ground connection

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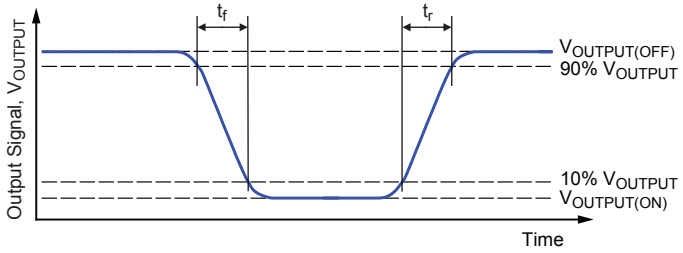
OPERATING CHARACTERISTICS: Valid over operating voltage and temperature ranges, unless otherwise noted; typical data applies to V_{CC} = 12 V, and T_A = 25°C

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit [1]
ELECTRICAL CHARACTERISTICS						
Supply Voltage [2]	V_{CC}	Operating, $T_A \le 150°C$	3.5	–	24	V
Output Leakage Current	$I_{OUTPUT(OFF)}$	All outputs, $V_{OUT} \le V_{CC}$(max)	–	< 1	10	µA
Supply Current	$I_{CC(OFF)}$, $I_{CC(ON)}$	$B < B_{RP(A)}$ and $B < B_{RP(B)}$, or $B > B_{OP(A)}$ and $B > B_{OP(B)}$	2.5	4.5	8.0	mA
Low Output Voltage	$V_{OUTPUT(ON)}$	All outputs, Output = On, $I_{OUTPUT(SINK)}$ = 20 mA	–	160	500	mV
Output Current Limit	I_{OUTLIM}	All outputs	30	–	70	mA
Chopping Frequency	f_C		–	520	–	kHz
Output Rise Time	t_r	C_{LOAD} = 20 pF, R_{LOAD} = 820 Ω	–	0.3	–	µs
Output Fall Time	t_f	C_{LOAD} = 20 pF, R_{LOAD} = 820 Ω	–	0.2	–	µs
Speed Output Delay	Δt_{DIRSPD}	Delay between direction output changing and speed output transition, V_{CC} = 5 V, C_{LOAD} = 12 pF, R_{LOAD} = 820 Ω, R_{LOAD} connected to 5 V	–	2	5	µs
Power-On Time	t_{ON}	$B > B_{OP}$ + 10 G or $B < B_{RP}$ – 10 G	–	35	–	µs
Power-Off Time	t_{OFF}	$B > B_{OP}$ + 10 G or $B < B_{RP}$ – 10 G	–	36	–	µs
Power-On State	POS	B = 0 G (reference Typical Application diagram)	–	High	–	–
TRANSIENT PROTECTION CHARACTERISTICS						
Supply Zener Voltage	V_Z	$I_{CC} = I_{CC}$(max) + 3 mA, T_A = 25°C	28	–	–	V
Supply Zener Current [3]	I_Z	V_S = 28 V	–	–	11	mA
Reverse-Battery Current	I_{RCC}	V_{RCC} = –18 V, $T_J < T_{J(max)}$	–	2	15	mA
Undervoltage Lockout	V_{UVLO}		–	–	3.4	V
MAGNETIC CHARACTERISTICS [4]						
Operate Point (Channel A and Channel B)	B_{OP}	$B_{(A)} > B_{OP(A)}$, $B_{(B)} > B_{OP(B)}$	–35	15	55	G
Release Point (Channel A and Channel B)	B_{RP}	$B_{(A)} < B_{OP(A)}$, $B_{(B)} < B_{OP(B)}$	–55	–15	35	G
Hysteresis (Channel A and Channel B)	B_{hys}	$B_{OP} - B_{RP}$	10	30	60	G
Operate Symmetry	$SYM_{OP(AB)}$	$B_{OP(A)} - B_{OP(B)}$	–50	–	50	G
Release Symmetry	$SYM_{RP(AB)}$	$B_{RP(A)} - B_{RP(B)}$	–50	–	50	G

[1] 1 G (gauss) = 0.1 mT (millitesla).
[2] When operating at maximum voltage, never exceed maximum junction temperature, T_J(max). Refer to power derating curve charts.
[3] Maximum specification limit is equivalent to $I_{CC(max)}$ + 3 mA.
[4] Magnetic flux density, B, is indicated as a negative value for north-polarity magnetic fields, and as a positive value for south-polarity magnetic fields. This so-called algebraic convention supports arithmetic comparison of north and south polarity values, where the relative strength of the field is indicated by the absolute value of B, and the sign indicates the polarity of the field (for example, a –100 G field and a 100 G field have equivalent strength, but opposite polarity).



Definition of Output Fall Time, t_f, and Output Rise Time, t_r

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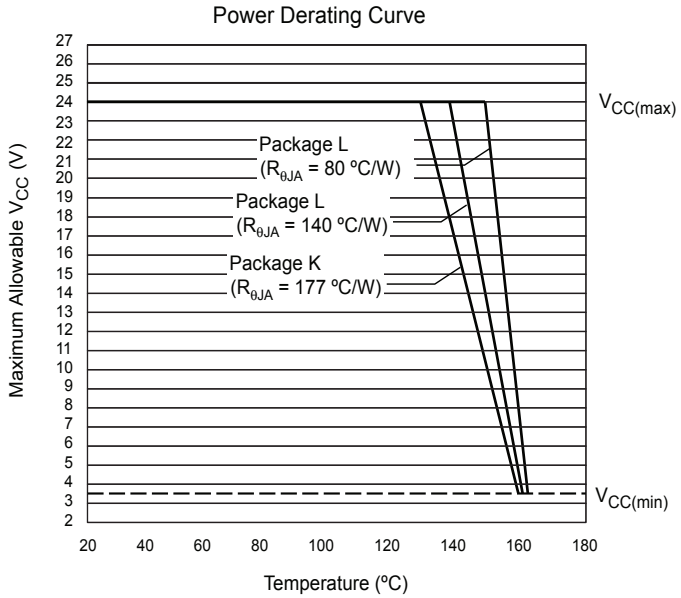
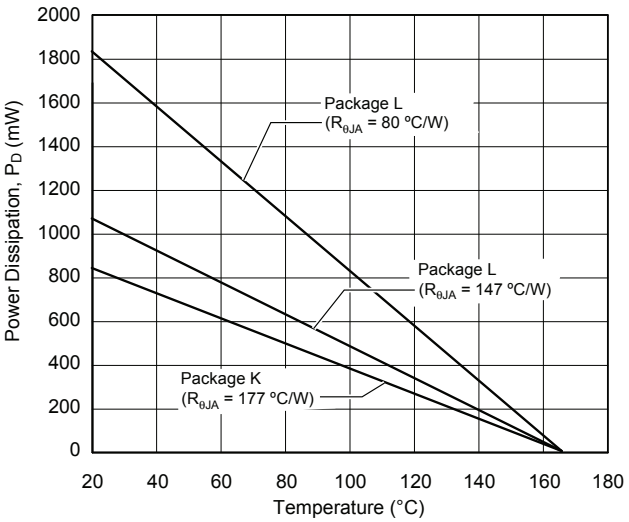
THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Package K, single-sided PCB with copper limited to solder pads	177	°C/W
		Package L, single-sided PCB with copper limited to solder pads	140	°C/W
		Package L, 4-layer PCB based on JEDEC standard	80	°C/W

*Additional thermal information available on Allegro website.



Power Dissipation versus Ambient Temperature



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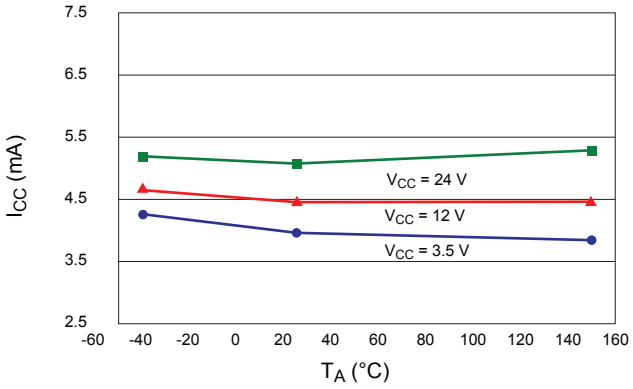
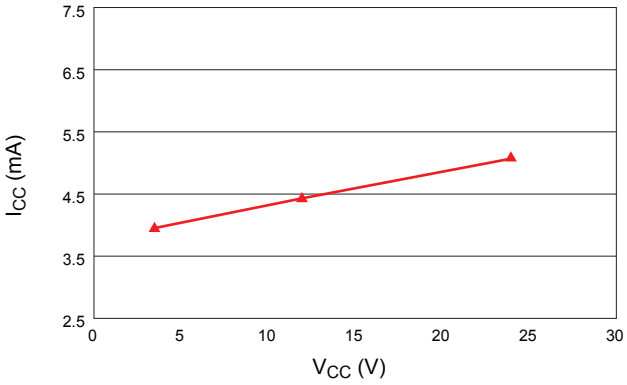
CHARACTERISTIC PERFORMANCE DATA

Supply Current versus Ambient Temperature



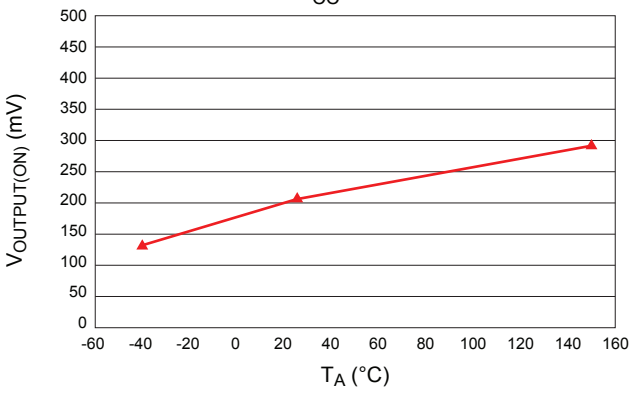
Supply Current versus Supply Voltage

T_A = 25°C

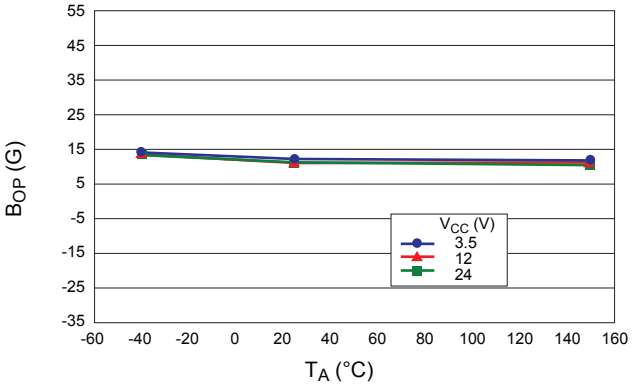


Low Output Voltage versus Ambient Temperature

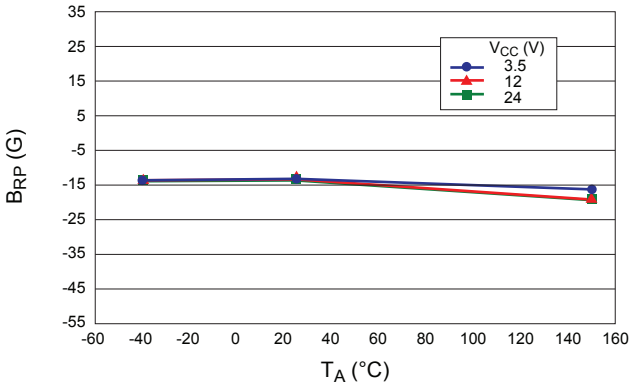
V_{CC} = 12 V



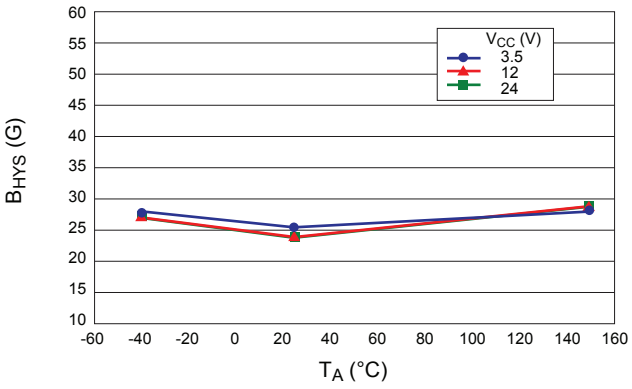
Operate Point versus Ambient Temperature



Release Point versus Ambient Temperature



Switchpoint Hysteresis versus Ambient Temperature



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FUNCTIONAL DESCRIPTION

The integrated circuit contains an internal voltage regulator that powers the Hall elements and both the analog and digital circuitry. This regulator allows operation over a wide supply voltage range and provides some immunity to supply noise. The device also contains logic circuitry that decodes the direction of rotation of the ring magnet.

Quadrature/Direction Detection Internal logic circuitry provides outputs representing the speed and direction of the magnetic field across the face of the package. For the direction signal to be appropriately updated, a quadrature relationship must be maintained between the target magnetic pole width, the pitch between the two Hall elements (E1 and E2) in the device, and, to a lesser extent, the magnetic switchpoints.

For optimal design, the device should be actuated by a ring magnet that presents to the front of the device a field with a pole width two times the Hall element-to-element spacing. This will produce a sinusoidal magnetic field whose period (denoted as *T*) is then four times the element-to-element spacing. A quadrature relationship can also be maintained for a ring magnet with fields having a period that satisfies the relationship:

$$n\mathrm{T}/4 = 1.63 \text{ mm},$$

where *n* is any odd integer. Therefore, ring magnets with pole-pair spacing equal to 6.52 mm ($n = 1$), 2.17 mm ($n = 3$), 1.3 mm ($n = 5$), and so forth, are permitted. The response of the device to the magnetic field produced by a rotating ring magnet is shown in figure 1. Note the phase shift between the two integrated Hall elements.

Outputs The device provides up to four outputs: target direction (DIR pin), E1 element output (OUTA pin), E2 element output (OUTB pin), and target speed (SPD pin).

DIR provides the direction output of the device and is defined as off (high) for targets moving in the direction from E1 to E2 and on (low) for the direction E2 to E1. SPD provides an XORed output of the two Hall elements (see figure 1). Because of internal delays, DIR is always updated before SPD and is updated at every transition of OUTA and OUTB (internal) allowing the use of up-down counters without the loss of pulses.

Power-on State At power on, the logic circuitry is reset to provide an off (high) state for all the outputs. If any of the channels is subjected to a field greater than B_{OP}, the internal logic will set accordingly, and the outputs will switch to the expected state.

Power-on Time This characteristic, t_{ON}, is the elapsed time from when the supply voltage reaches the device supply minimum until the device output becomes valid (see figure 2).

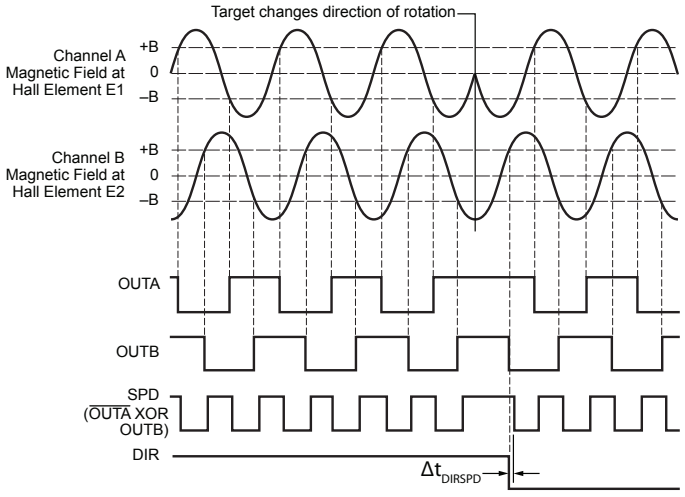

Figure 1

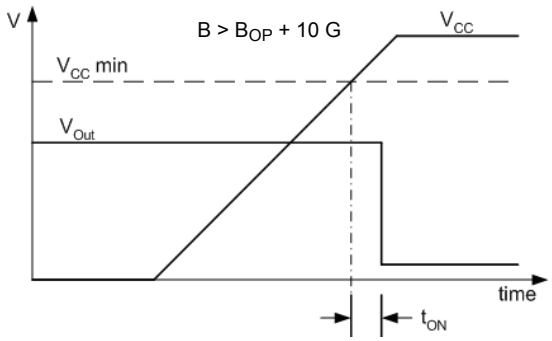

Figure 2

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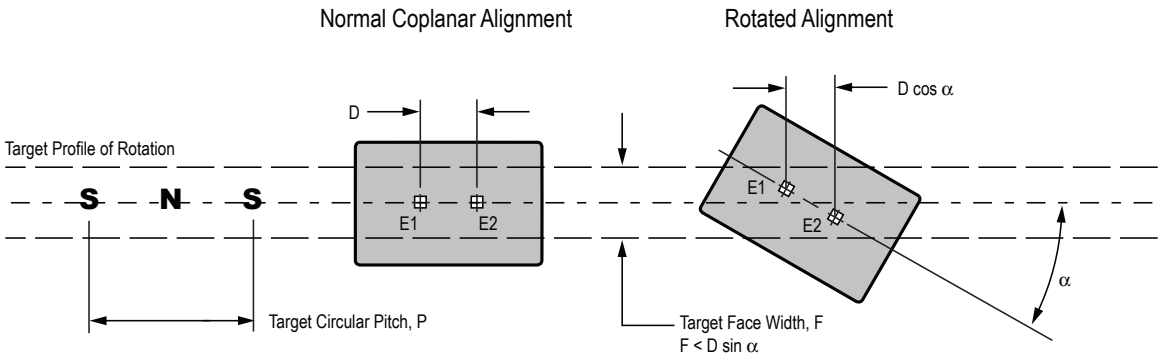
APPLICATION INFORMATION

Operation with Fine-Pitch Ring Magnets. For targets with a circular pitch of less than 4 mm, a performance improvement can be observed by rotating the front face of the device (see below). This rotation decreases the effective Hall element-to-element spacing, provided that the Hall elements are not rotated beyond the width of the target.

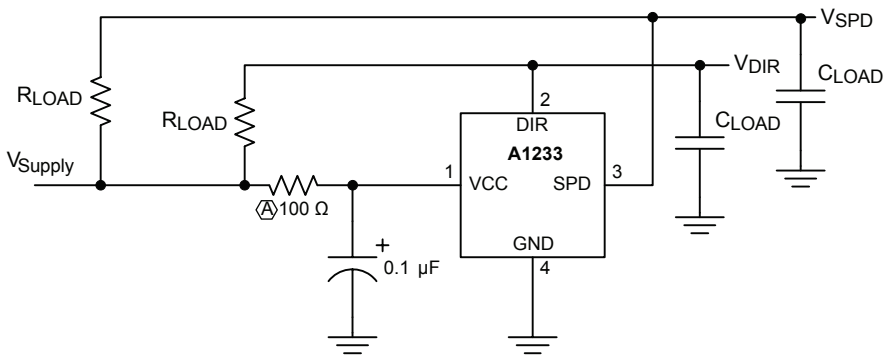
Applications. It is strongly recommended that an external 0.1 µF bypass capacitor be connected (in close proximity to the device) between the supply and ground of the device to reduce both external noise and noise generated by the internal logic.

The simplest form of magnet that will operate these devices is a ring magnet. Other methods of operation, such as linear magnets, are possible. Extensive applications information on magnets and Hall-effect sensor ICs is also available in the "Hall-Effect IC Applications Guide" which can be found on the Allegro website, www.allegromicro.com.



Typical Application

(Using regulated supply; K package configuration shown)



Ⓐ Resistor is optional, depending on Conducted Immunity requirements

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POWER DERATING

The device must be operated below the maximum junction temperature of the device, $T_{J(max)}$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems website.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: T_A= 25°C, V_{CC} = 12 V, I_{CC} = 4.5 mA, and $R_{\theta JA}$ = 177°C/W, then:

$$P_D = V_{CC} \times I_{CC} = 12\ V \times 4.5\ mA = 54\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 54\ mW \times 177°C/W = 9.6°C$$

$$T_J = T_A + \Delta T = 25°C + 9.6°C = 34.6°C$$

A worst-case estimate, $P_{D(max)}$, represents the maximum allowable power level, without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at T_A=150°C.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$=177°C/W, $T_{J(max)}$=165°C, $V_{CC(max)}$ = 24 V, and $I_{CC(max)}$ = 8 mA.

Calculate the maximum allowable power level, $P_{D(max)}$. First, invert equation 3:

$$\Delta T_{(max)} = T_{J(max)} - T_A = 165\,°C - 150\,°C = 15\,°C$$

This provides the allowable increase to T_J resulting from internal power dissipation.

Then, invert equation 2:

$$P_{D(max)} = \Delta T_{(max)} \div R_{\theta JA} = 15°C \div 177°C/W = 84.7\,mW$$

Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_{D(max)} \div I_{CC(max)} = 84.7\ mW \div 8\,mA = 10.59\ V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages ≤$V_{CC(est)}$.

Compare $V_{CC(est)}$ to $V_{CC(max)}$. If $V_{CC(est)} \leq V_{CC(max)}$, then reliable operation between $V_{CC(est)}$ and $V_{CC(max)}$ requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \geq V_{CC(max)}$, then operation between $V_{CC(est)}$ and $V_{CC(max)}$ is reliable under these conditions.

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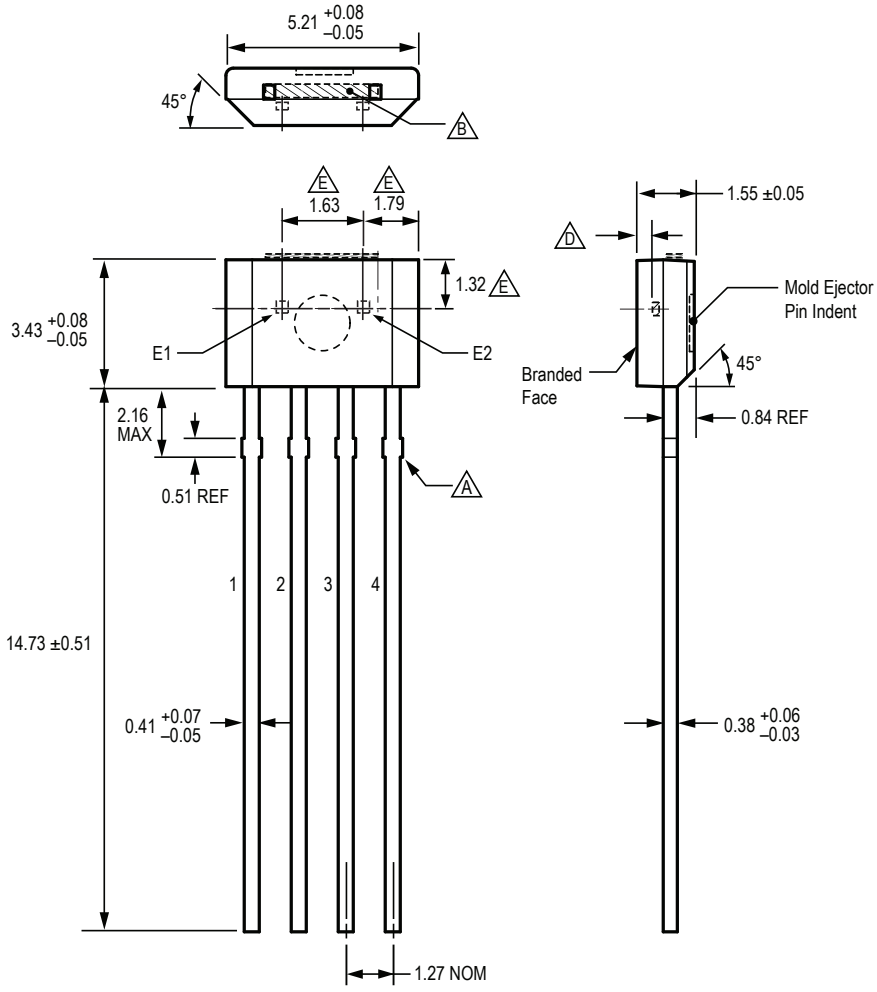
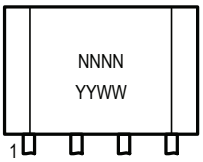
Package K, 4-Pin SIP





D Standard Branding Reference View

N = Device part number
Y = Last two digits of year of manufacture
W = Week of manufacture

For Reference Only; not for tooling use (reference Allegro DWG-0000395)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Dambar removal protrusion (8×)

B Gate and tie bar burr area

C Branding scale and appearance at supplier discretion

D Active Area Depth, 0.42 mm

E Hall elements (E1 and E2); not to scale

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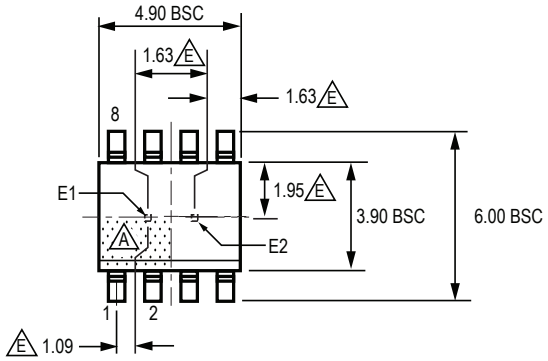
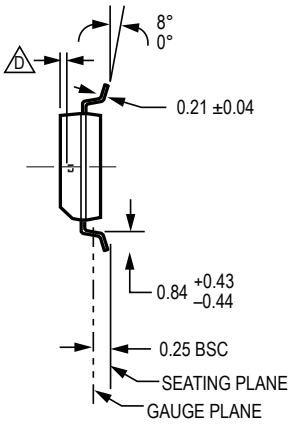
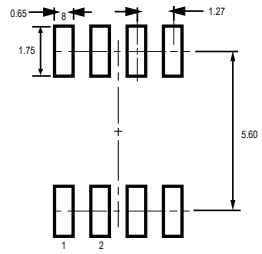
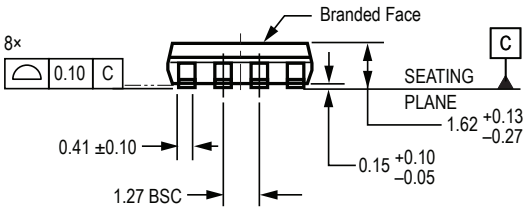
Package L, 8-Pin SOIC

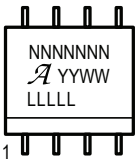






C PCB Layout Reference View





For Reference Only; not for tooling use
(reference Allegro DWG-0000385, Rev. 2 or JEDEC MS-012AA)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Branding scale and appearance at supplier discretion

C Reference land pattern layout (reference IPC7351 SOIC127P600X175-8M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

D Active Area Depth 0.40 NOM

E Hall elements (E1 and E2); not to scale

B Standard Branding Reference View

N = Device part number
A = Supplier emblem
Y = Last two digits of year of manufacture
W = Week of manufacture
L = Lot number

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Revision History

Number	Date	Description
–	January 15, 2013	Initial Release
1	September 21, 2015	Added AEC-Q100 qualification under Features and Benefits
2	September 26, 2017	Added Functional Safety information; added footnote to Absolute Maximum Ratings table
3	October 12, 2018	Added footnote to Magnetic Flux Density (page 2); minor editorial updates
4	November 21, 2019	Minor editorial updates
5	November 9, 2022	Updated “ISO 26262:2011” to “ISO 26262” (pages 1, 8); updated package drawings (pages 10-11)
6	October 13, 2025	Updated ASIL branding and text (page 1) and removed functional safety section (page 8)

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