AMT49105

ISO 26262 ASIL Compliant

Three-Phase MOSFET Driver System IC

FEATURES AND BENEFITS

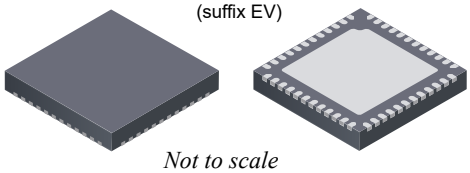
- 3-phase bridge MOSFET driver
- Bootstrap gate drive for N-channel MOSFET bridge
- Cross-conduction protection with adjustable dead time
- Charge pump for low supply voltage operation
- Programmable gate drive voltage and strength
- 5.5 to 50 V supply voltage operating range
- Integrated logic supply
- Current sense amplifier with programmable gain and offset
- SPI-compatible serial interface
- Bridge control by direct logic inputs or serial interface
- Integrated bemf state comparators
- LIN/PWM physical interface with Wake
- Programmable logic supply regulator with current limit
- MCU Window watchdog and reset
- Ignition switch interface
- Diagnostics, status, voltage, and temperature feedback
- ASIL Compliant: ASIL A safety element out-of-context (SEooC) developed in accordance with ISO 26262, when used as specified in the safety manual

APPLICATIONS

- Automotive fuel, oil, and urea pumps
- Automotive fans and blowers

PACKAGE

48-pin QFN with exposed thermal pad and wettable flank (suffix EV)



Not to scale

DESCRIPTION

The AMT49105 is an N-channel power MOSFET driver capable of controlling MOSFETs connected in a three-phase bridge arrangement and is specifically designed for automotive applications with high-power inductive loads such as BLDC motors. Full control over all six power MOSFETs in the three-phase bridge is provided, allowing motors to be driven with block commutation or sinusoidal excitation.

The AMT49105 is designed to provide the gate drive, supply, and peripheral functions in a system where a small microcontroller provides the motor control, communication interface to a central ECU and intelligent fault and status handling. The AMT49105 provides the supply and watchdog for the microcontroller and the high voltage interfaces between the microcontroller and the central ECU and ignition switch. An ISO17987 (LIN 2.X) and SAE J2602 compliant physical interface is provided for systems using LIN bus communications. This can also operate as a PWM interface for PWM communication systems.

A unique charge pump regulator provides the supply for the MOSFET gate drive for battery voltages down to 7 V and allows the AMT49105 to operate with a reduced gate drive down to 5.5 V. A bootstrap capacitor is used to provide the above-battery supply voltage required for N-channel MOSFETs.

A single sense amplifier with programmable gain and offset provides current sensing using a single low-side resistive shunt.

Integrated diagnostics provide indication of undervoltage, overtemperature, and power bridge faults and can protect the power switches under most short-circuit conditions.

The AMT49105 is supplied in a 48-terminal wettable flank QFN package (suffix EV). This package is lead (Pb) free with 100% matte-tin leadframe plating.

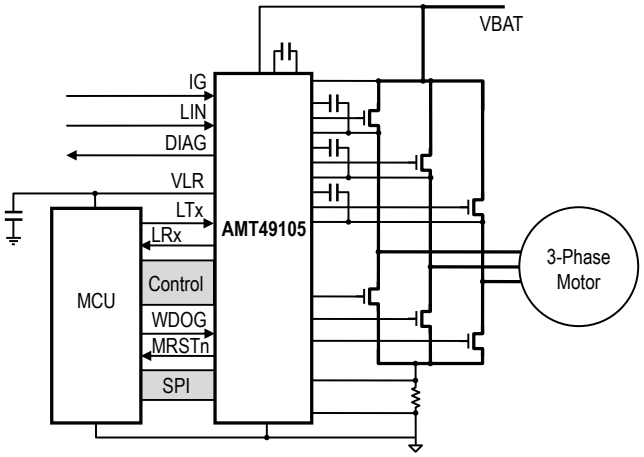


Figure 1: Typical Application

SELECTION GUIDE

Part Number	Packing	Package
AMT49105KEVTR-J	1000 pieces per 7-inch reel	7 mm × 7 mm, 0.9 mm nominal height 48-terminal QFN with exposed thermal pad and wettable flank

Table of Contents

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ABSOLUTE MAXIMUM RATINGS [1][2]

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{BB}	VBB	–0.3 to 50	V
Between Ground Terminals	–	Connect GND terminals together at package	–0.1 to 0.1	V
Pumped Regulator Terminal	V_{REG}	VREG	–0.3 to 16	V
Charge Pump Capacitor Terminal	V_{CP1}	CP1	–0.3 to 16	V
Charge Pump Capacitor Terminal	V_{CP2}	CP2	–0.3 to 16	V
Logic Regulator Output	V_{LR}	VLR	–0.3 to 6	V
LIN Bus Interface	V_{LIN}	LIN	–40 to 50	V
Logic Inputs	–	All logic inputs except IG	–0.3 to 6	V
Logic Input	V_{IG}	IG	–4 to 50	V
Logic Outputs	–	All logic outputs except DIAG	–0.3 to 6	V
Logic Output	V_{DIAG}	DIAG	–0.3 to 50	V
Bridge Drain Monitor Terminals	V_{BRG}	VBRG	–5 to 55	V
Switched Bridge Terminal	V_{BRS}	BRSW	–0.3 to 55	V
Bootstrap Supply Terminals	V_{Cx}	CA, CB, CC	–0.3 to V_{REG}+50	V
High-Side Gate Drive Output Terminals	V_{GHx}	GHA, GHB, GHC	V_{CX} – 16 to V_{Cx} + 0.3	V
		GHA, GHB, GHC (Transient)	–18 to V_{Cx} + 0.3	V
Motor phase terminals	V_{Sx}	SA, SB, SC	V_{CX} – 16 to V_{Cx} + 0.3	V
		SA, SB, SC (Transient)	–18 to V_{Cx} + 0.3	V
Low-side gate drive output terminals	V_{GLx}	GLA, GLB, GLC	V_{REG} – 16 to 18	V
		GLA, GLB, GLC (Transient)	–18 to V_{Cx} + 0.3	V
Bridge low-side source terminals	V_{LSS}	LSSA, LSSB, LSSC	V_{REG} – 16 to 18	V
		LSSA, LSSB, LSSC (Transient)	–8 to 18	V
Sense Amplifier Inputs	V_{CSI}	CSP, CSM	–4 to 6.5	V
Sense Amplifier Output	V_{CSI}	CSO	–0.3 to 6.5	V
Ambient Operating Temperature Range	T_A		–40 to 150	°C
Maximum Continuous Junction Temperature	$T_{J(max)}$		165	°C
Transient Junction Temperature	T_{Jt}	Over temperature event not exceeding 10 seconds, lifetime duration not exceeding 10 hours, guaranteed by design characterization.	180	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

[1] With respect to GND. Ratings apply when no other circuit operating constraints are present.
[2] Lowercase “x” in terminal names and symbols indicates a variable sequence character.

THERMAL CHARACTERISTICS: May require derating at maximum conditions

Characteristic	Symbol	Test Conditions [4]	Value	Unit
EV Package Thermal Resistance	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	24	°C/W
		2-layer PCB with 3.8 in.^{2} of copper area each side	44	°C/W
	$R_{\theta JP}$		2	°C/W

[4] Additional thermal information available on the Allegro website.

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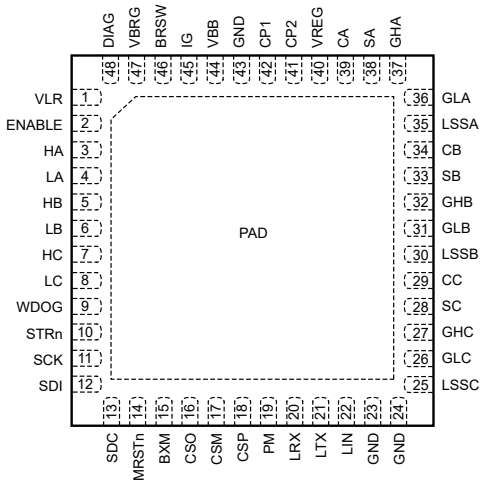

QFN-48 (EV) Package Pinout Diagram

Terminal List Table

Name	Number	Function
BRSW	46	Switched Bridge connection
BXM	15	Multiplexed bemf output
CA	39	Bootstrap Capacitor Phase A
CB	34	Bootstrap Capacitor Phase B
CC	29	Bootstrap Capacitor Phase C
CP1	42	Pump Capacitor
CP2	41	Pump Capacitor
CSM	17	Current Sense Amp 1 –Input
CSO	16	Current Sense Amp 1 Output
CSP	18	Current Sense Amp 1 +Input
DIAG	48	Programmable diagnostic output
ENABLE	2	Direct Output Activity Control
GHA	37	High-side Gate Drive Phase A
GHB	32	High-side Gate Drive Phase B
GHC	27	High-side Gate Drive Phase C
GLA	36	Low-side Gate Drive Phase A
GLB	31	Low-side Gate Drive Phase B
GLC	26	Low-side Gate Drive Phase C
GND	43	Ground
GND	23	Ground
GND	24	Ground
HA	3	Control Input A High Side
HB	5	Control Input B High Side
HC	7	Control Input C High Side
PAD	Pad	Connect To Ground

Name	Number	Function
IG	45	Ignition Input
LA	4	Control Input A Low Side
LB	6	Control Input B Low Side
LC	8	Control Input C Low Side
LIN	22	LIN Bus connection
LRX	20	LIN Receive output
LTX	21	LIN Transmit input
LSSA	35	Low-side Source Phase A
LSSB	30	Low-side Source Phase B
LSSC	25	Low-side Source Phase C
MRSTn	14	MCU Reset output
PM	19	Program mode input
SA	38	Motor Connection Phase A
SB	33	Motor Connection Phase B
SC	28	Load Connection Phase C
SCK	11	Serial Clock Input
SDI	12	Serial Data Input
SDO	13	Serial Data output
STRn	10	Serial Strobe (chip select) Input
VBB	44	Main Power Supply
VBRG	47	High-side Drain voltage sense
VREG	40	Gate Drive Supply Output
VLR	1	LDO Regulator Output
WDOG	9	Watchdog Input

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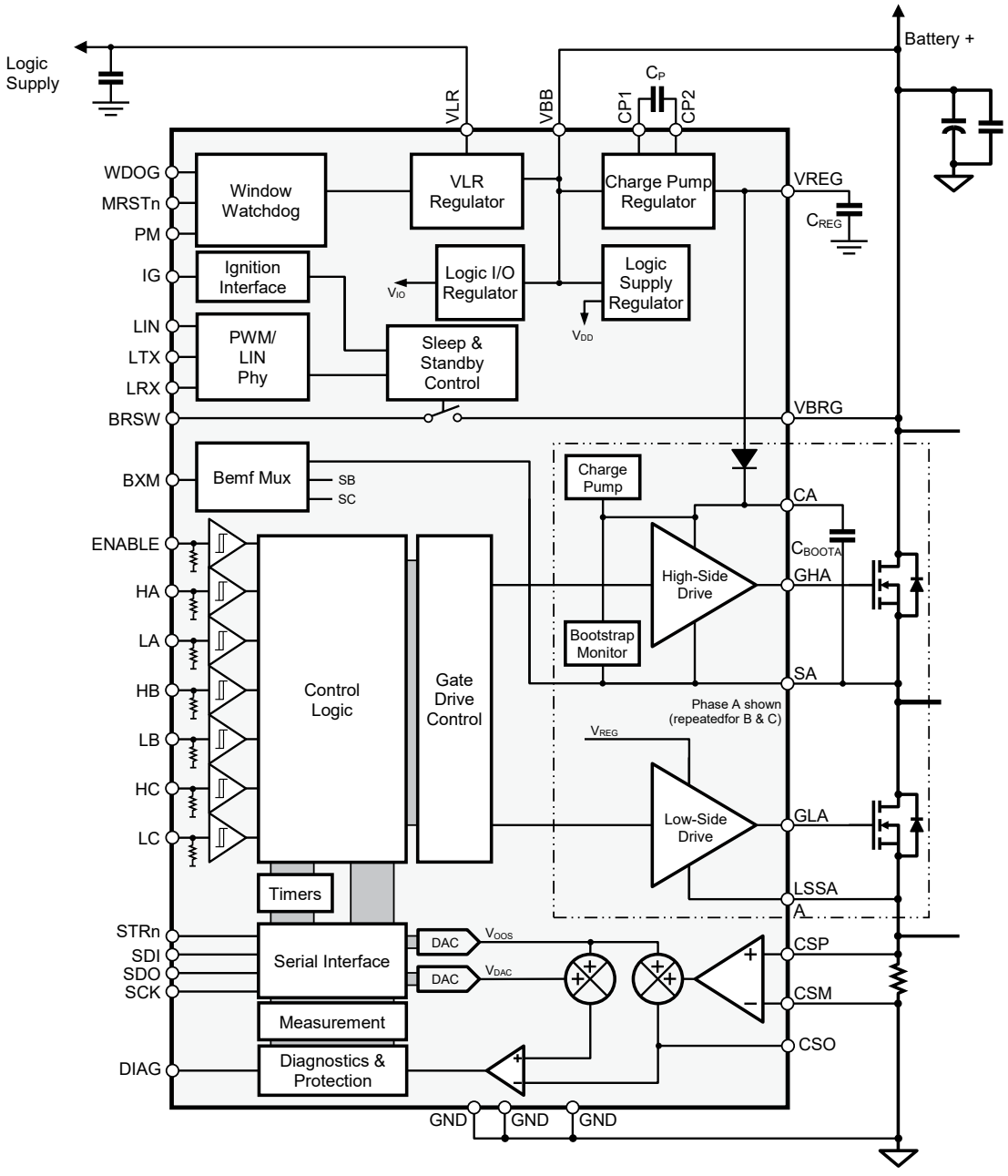
FUNCTIONAL BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS: Valid at T_J = –40°C to 150°C, V_{BB} = 5.5 to 50 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY AND REFERENCE						
VBB Functional Operating Range	V_{BB}	Operating; outputs active	5.5	–	50	V
		Functional; no POR, outputs disabled	3.5	–	50	V
		No unsafe states	0	–	50	V
VBB Quiescent Current	I_{BBQ}	V_{BB} = 12 V, all gate drive outputs low	–	25	28	mA
	I_{BBS}	V_{LIN} = V_{BB} = 12 V, in sleep state	–	–	10	µA
VREG Output Voltage	V_{REG}	VRG = 0, V_{BB} ≥ 8.5 V, I_{VREG} = 0 to 35 mA	7.5	8	8.5	V
		VRG = 0, 7.5 V ≤ V_{BB} < 8.5 V, I_{VREG} = 0 to 30 mA	7.5	8	8.5	V
		VRG = 0, 6 V ≤ $_{VBB}$ < 7.5 V, I_{VREG} = 0 to 13 mA	7.5	8	8.5	V
		VRG = 0, 5.5 V ≤ V_{BB} < 6 V, I_{VREG} ≤ 8 mA	7.5	8	8.5	V
		VRG = 1, V_{BB} ≥ 9 V, I_{VREG} = 0 to 33 mA	9	11	11.7	V
		VRG = 1, 7.5 V ≤ V_{BB} < 9 V, I_{VREG} = 0 to 23 mA	9	11	11.7	V
		VRG = 1, 6 V ≤ V_{BB} < 7.5 V, I_{VREG} = 0 to 13 mA	7.9	–	–	V
		VRG = 1, 5.5 V ≤ V_{BB} < 6 V, I_{VREG} ≤ 5 mA	7.9	9.5	–	V
Logic I/O Regulator Voltage	V_{IO}	VLR = 0, V_{BB} > 4.5 V	3.1	3.3	3.5	V
		VLR = 1, V_{BB} > 6 V	4.8	5.0	5.2	V
VLR Output Voltage	V_{LR}	VLR = 0, I_{VLR} < 70 mA, V_{BB} > 6 V	3.1	3.3	3.5	V
		VLR = 0, 25 mA ≤ I_{VLR} ≤ 50 mA, 6.5 V ≤ V_{BB} ≤ 20 V	3.2	3.3	3.4	V
		VLR = 1, I_{VLR} < 70 mA, V_{BB} > 6.5 V	4.8	5.0	5.2	V
		VLR = 1, 25 mA ≤ I_{VLR} ≤ 50 mA, 6.5 V ≤ V_{BB} ≤ 20 V	4.84	5.0	5.16	V
VLR Regulator Current Limit	I_{LROC}		130	–	300	mA
VLR Regulator Enable Voltage Threshold	V_{LROE}	V_{LR} rising	–	–	1.5	V
VLR Regulator Shutdown Voltage Threshold	V_{LROSD}	V_{LR} falling	1.2	–	–	V
VLR Regulator Shutdown Lockout Period	t_{LRLO}		–	2	–	ms
VLR Regulator Pilot Current	I_{LROP}		–	2	–	mA
BRSW Switch Impedance [1]	R_{BRSW}	I_{BRSW} = –5 mA	50	–	250	Ω
BRSW Current Limit [1][8]	I_{BRLIM}	V_{BRSW} = 0 V, V_{BRG} = 50 V	–30	–	–8	mA
BRSW Switched Bridge Output Leakage	I_{BRSWL}	Switch disabled, 0 < V_{BRS} < V_{BRG}	–1	–	1	µA
Bootstrap Diode Forward Voltage	V_{fBOOT}	I_D = 10 mA	0.4	0.7	1.0	V
		I_D = 100 mA	1.5	2.2	2.8	V
Bootstrap Diode Resistance	r_D	$r_{D(100\ mA)}$ = ($V_{fBOOT(150\ mA)}$ – $V_{fBOOT(50mA)}$) / 100 mA	6	11	24	Ω
Bootstrap Diode Current Limit	I_{DBOOT}		250	500	850	mA
Top-Off Charge Pump Current Limit	I_{TOCPM}		35	100	550	µA
High-Side Gate Drive Static Load Resistance	R_{GSH}	V_{REG} > 7 V	300	–	–	kΩ
System Clock Period	t_{OSC}		47.5	50	52.5	ns

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ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 5.5 to 50 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GATE OUTPUT DRIVE						
Turn-On Time	t_r	Switched mode, C_{LOAD} = 10 nF, 20% to 80%	–	190	–	ns
Turn-Off Time	t_f	Switched mode, C_{LOAD} = 10 nF, 80% to 20%	–	120	–	ns
Pull-Up On-Resistance	$R_{DS(on)UP}$	T_J = 25°C, I_{GH} = –150 mA [1]	5	8	11	Ω
		T_J = 150°C, I_{GH} = –150 mA[1]	10	15	20	Ω
Pull-Up Peak Source Current [1][8]	I_{PUPK}	V_{GS} = 0 V	–1500	–450	–200	mA
Pull-Down On-Resistance	$R_{DS(on)DN}$	T_J = 25°C, I_{GL} = 150 mA	1.5	2.4	3.1	Ω
		T_J = 150°C, I_{GL} = 150 mA	2.9	4	5	Ω
Pull-Down Peak Sink Current [8]	I_{PDPK}	V_{GS} > 9 V	425	800	1330	mA
Turn-On Current 1	I_{R1}	V_{GS} = 0 V, VRG = 1, IR1 = 15	–144	–82.5	–48	mA
		Programmable Range, DT[5:0] > 0	–5.5	–	–82.5	mA
Turn-On Current 2	I_{R2}	V_{GS} = 0 V, VRG = 1, IR2 = 15	–144	–82.5	–48	mA
		Programmable Range DT[5:0] > 0	–5.5	–	–82.5	mA
Turn-Off Current 1	I_{F1}	V_{GS} = 9 V, VRG = 1, IF1 = 15	48	79.5	136	mA
		Programmable Range DT[5:0] > 0	5.3	–	79.5	mA
Turn-Off Current 2	I_{F2}	V_{GS} = 9 V, VRG = 1, IF2 = 15	48	79.5	136	mA
		Programmable Range DT[5:0] > 0	5.3	–	79.5	mA
GHx Output Voltage High	V_{GHH}	Bootstrap capacitor fully charged	V_{Cx} – 0.2	–	–	V
GHx Output Voltage Low	V_{GHL}	–10 µA < I_{GH} < 10 µA	–	–	V_{Sx} + 0.3	V
GLx Output Voltage High	V_{GLH}		V_{REG} – 0.2	–	–	V
GLx Output Voltage Low	V_{GLL}	–10 µA < I_{GL} < 10 µA	–	–	V_{LSS} + 0.3	V
GHx Passive Pull-Down	R_{GHPD}	V_{BB} = 0 V, I_{GHx} = 500 µA	–	4	10	kΩ
GLx Passive Pull-Down	R_{GLPD}	V_{BB} = 0 V, I_{GLx} = 500 µA	–	4	10	kΩ
Turn-Off Propagation Delay [2]	$t_{P(off)}$	Input change to unloaded gate output change; DT[5:0] = 0	60	90	140	ns
		Input change to unloaded gate output change, excluding jitter[12]; DT[5:0] > 0	135	165	215	ns
Turn-On Propagation Delay [2]	$t_{P(on)}$	Input change to unloaded gate output change; DT[5:0] = 0	50	80	130	ns
		Input change to unloaded gate output change, excluding jitter[12]; DT[5:0] > 0	125	155	205	ns
Propagation Delay Matching (Phase-to-Phase)	Δt_{PP}	Same state change, DT[5:0] = 0	–	5	15	ns
Propagation Delay Matching (On-to-Off)	Δt_{OO}	Single phase, DT[5:0] = 0	–	15	30	ns
Propagation Delay Matching (GHx-to-GLx)	Δt_{HL}	Same state change, DT[5:0] = 0	–	–	20	ns
Dead Time (Turn-Off To Turn-On Delay) [2]	t_{DEAD}	Default power-up value	1.52	1.6	1.68	µs
		Programmable Range	0.1	–	3.15	µs

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ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 5.5 to 50 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
LOGIC INPUTS & OUTPUTS						
Input Low Voltage	V_{IL}	All digital inputs except IG, VIO = 0	–	–	1.05	V
		All digital inputs except IG, VIO = 1	–	–	1.56	V
Input High Voltage	V_{IH}	All digital inputs except IG, VIO = 0	2.17	–	–	V
		All digital inputs except IG, VIO = 1	3.36	–	–	V
Input Hysteresis	V_{Ihys}	All digital inputs except IG	250	550	–	mV
Input Pull-Down Resistor	R_{PD}	SCK, SDI, WDOG, Hx, Lx, ENABLE, PM	30	50	75	kΩ
		IG	–	300	–	kΩ
Input Pull-Up Resistor	R_{PU}	STRn, LTX	30	50	75	kΩ
Input Low Voltage	V_{IL}	IG	–	–	2.5	V
Input High Voltage	V_{IH}	IG	4.8	–	–	V
Input Hysteresis	V_{Ihys}	IG	250	–	–	mV
Input Current	I_G	IG	–	–	100	µA
Output Low Voltage	V_{OL}	SDO, MRSTn, BXM, LRX, I_{OL} = 1 mA	–	–	0.4	V
Output High Voltage	V_{OH}	SDO, MRSTn, BXM, LRX, I_{OL} = –1 mA [1]	V_{IO} – 0.4	–	–	V
Output Leakage [1]	I_O	SDO, 0 V < V_O < V_{IO}, STRn = 1	–1	–	1	µA
Output Low Voltage	V_{OLD}	DIAG, I_{OD} = 3 mA, DIAG active	–	0.2	0.4	V
Output Current Limit	I_{ODLIM}	DIAG, 0 V < V_{OD} < 18 V, DIAG active	–	10	17	mA
		DIAG, 18 V ≤ V_{OD} < 50 V, DIAG active	–	–	2.5	mA
Output Leakage Current [1]	I_{OD}	DIAG, 0 V < V_{OD} < 6 V, DIAG inactive	–1	–	1	µA
		DIAG, 6 V ≤ V_{OD} < 50, DIAG inactive	–	–	2.5	mA
WATCHDOG – TIMING PARAMETERS						
Minimum Watchdog Time	t_{WM}	Default power-up value	0.95	1	1.05	ms
		Programmable range	1	–	63	ms
Watchdog Window Time	t_{WW}	Default power-up value	9.5	10	10.5	ms
		Programmable range	10	–	320	ms
Watchdog Detect to MRSTn Low	t_{WDET}		100	–	200	ms
MRSTn Low	t_{MRST}		9.5	10	10.5	ms

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SERIAL INTERFACE – TIMING PARAMETERS [11]						
Clock High Time	t_{SCKH}	A in Figure 4	50	–	–	ns
Clock Low Time	t_{SCKL}	B in Figure 4	50	–	–	ns
Strobe Lead Time	t_{STLD}	C in Figure 4	100	–	–	ns
Strobe Lag Time	t_{STLG}	D in Figure 4	30	–	–	ns
Strobe High Time	t_{STRH}	E in Figure 4	350	–	–	ns
Data Out Enable Time	t_{SDOE}	F in Figure 4	–	–	40	ns
Data Out Disable Time	t_{SDOD}	G in Figure 4	–	–	30	ns
Data Out Valid Time From Clock Falling	t_{SDOV}	H in Figure 4	–	–	40	ns
Data Out Hold Time From Clock Falling	t_{SDOH}	I in Figure 4	5	–	–	ns
Data In Set-Up Time To Clock Rising	t_{SDIS}	J in Figure 4	15	–	–	ns
Data In Hold Time From Clock Rising	t_{SDIH}	K in Figure 4	10	–	–	ns
STRn Delay From POR	t_{EN}	$V_{BB} > V_{BBR}$ to STRn low	500	–	–	µs
LIN/PWM INTERFACE LOGIC I/O [11]						
Transmitter Input Low Voltage (LTX)	V_{IL}	VIO = 0	–	–	1.05	V
		VIO = 1	–	–	1.56	V
Transmitter Input High Voltage (LTX)	V_{IH}	VIO = 0	2.17	–	–	V
		VIO = 1	3.36	–	–	V
Transmitter Input Hysteresis (LTX)	V_{Ihys}		250	550	–	mV
Transmitter Input Pull-Up Resistor (LTX)	R_{PU}		30	50	75	kΩ
Receiver Output Low Voltage (LRX)	V_{OL}	I_{OL} = 1 mA, V_{BUS} = 0 V	–	–	0.4	V
Receiver Output High Voltage (LRX)	V_{OH}	I_{OL} = –1 mA [1], $V_{BUS} = V_{BB}$	V_{IO} – 0.4	–	–	V
LIN/PWM INTERFACE BUS TRANSMITTER [11]						
Bus Recessive Output Voltage	V_{BUSRO}	LTX High, Bus open load	0.8 × V_{BB}	–	–	V
Bus Dominant Output Voltage	V_{BUSDO}	LTX Low, R_{LIN} = 500 Ω, V_{BB} = 7 V	–	–	1.4	V
		LTX Low, R_{LIN} = 500 Ω, V_{BB} = 18 V	–	–	2.0	V
Bus Short Circuit Current	I_{BUSLIM}	V_{BUS} = 13.5 V	40	–	100	mA
Leakage Current – Dominant	$I_{BUS\_PAS\_dom}$	V_{BB} = 12 V, V_{BUS} = 0 V	–1	–	–	mA
Leakage Current – Recessive	$I_{BUS\_PAS\_rec}$	7 V < V_{BB} < 18 V, 7 V < V_{BUS} < 18 V, $V_{BUS} \geq V_{BB}$	–	–	20	µA
Leakage Current – Ground Disconnect	$I_{BUS\_NO\_GND}$	V_{BB} = 12 V, 0 V < V_{BUS} < 18 V	–1	–	1	mA
Leakage Current – Supply Disconnect	$I_{BUS\_NO\_BAT}$	V_{BB} = 0 V, 0 V < V_{BUS} < 18 V	–	–	100	µA
Bus Pull-Up Resistance	R_{SLAVE}	Normal operation	20	30	60	kΩ
		Sleep state	–	2	–	MΩ
Termination Diode Forward Voltage	$V_{SerDiode}$		0.4	0.7	1	V
LIN/PWM INTERFACE BUS RECEIVER [11]						
Receiver Center Voltage	V_{BUSCNT}		0.475 × V_{BB}	0.5 × V_{BB}	0.525 × V_{BB}	V
Receiver Dominant State	V_{BUSdom}		–	–	0.4 × V_{BB}	V
Receiver Recessive State	V_{BUSrec}		0.6 × V_{BB}	–	–	V
Receiver Hysteresis	V_{HYS}		0.05 × V_{BB}	–	0.175 × V_{BB}	V
Receiver Wake-Up Threshold Voltage	V_{BUSwk}		0.4 × V_{BB}	0.5 × V_{BB}	0.6 × V_{BB}	V

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
LIN/PWM INTERFACE – TIMING PARAMETERS [11]						
Receiver Propagation Delay H → L	t_{rx_pdf}	Bus dominant to LRX low	–	–	6	µs
Receiver Propagation Delay L → H	t_{rx_pdr}	Bus recessive to LRX high	–	–	6	µs
Receiver Delay Symmetry	t_{rx_sym}	$t_{rx\_pdf} - t_{rx\_pdr}$	–2	–	2	µs
Bus Dominant Time For Wake	t_{BUSWK}		30	–	160	µs
Wake Up Delay	t_{WL}	LIN Wake up to V_{REG} 90%, C_{REG} = 4.7 µF	–	3	–	ms
Transmit Dominant Time-Out	t_{TXTO}	OPM = 0	–	15	–	ms
Duty Cycle D1 (worst case at 20 kbps) [9]	D1	7 V < V_{BB} < 18 V, t_{BIT} = 50 µs, $V_{THRec(max)}$ = 0.744 × V_{BB}, $V_{THDom(max)}$ = 0.581 × V_{BB}, D1 = $t_{BUS\_rec(min)}$ / (2 × t_{BIT})	0.396	–	–	–
Duty Cycle D2 (worst case at 20 kbps) [9]	D2	7 V < V_{BB} < 18 V, t_{BIT} = 50 µs, $V_{THRec(min)}$ = 0.422 × V_{BB}, $V_{THDom(min)}$ = 0.284 × V_{BB}, D2 = $t_{BUS\_rec(max)}$ / (2 × t_{BIT})	–	–	0.581	–
Duty Cycle D3 (worst case at 10.4 kbps) [9]	D3	7 V < V_{BB} < 18 V, t_{BIT} = 96 µs, $V_{THRec(max)}$ = 0.778 × V_{BB}, $V_{THDom(max)}$ = 0.616 × V_{BB}, D3 = $t_{BUS\_rec(min)}$ / (2 × t_{BIT})	0.417	–	–	–
Duty Cycle D4 (worst case at 10.4 kbps) [9]	D4	7 V < V_{BB} < 18 V, tBIT = 96 µs, $V_{THRec(min)}$ = 0.389 × V_{BB}, $V_{THDom(min)}$ = 0.251 × V_{BB}, D4 = $t_{BUS\_rec(max)}$ / (2 × t_{BIT})	–	–	0.590	–

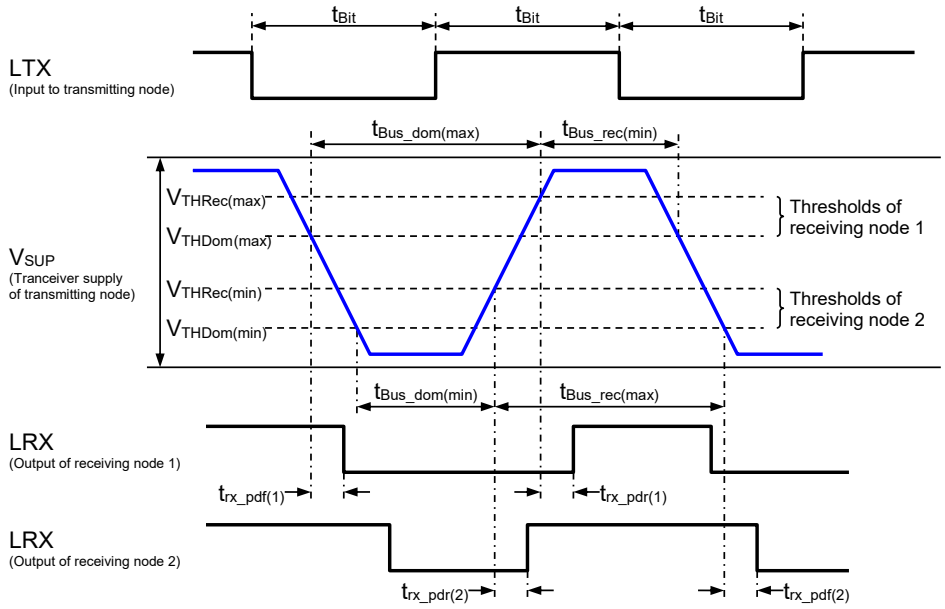

Figure 2: LIN bus timing

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ELECTRICAL CHARACTERISTICS (continued): Valid at T_J = –40°C to 150°C, V_{BB} = 5.5 to 50 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
CURRENT SENSE AMPLIFIER						
Input Offset Voltage	V_{IOS}		–2	–	2	mV
Input Offset Voltage Drift	ΔV_{IOS}		–20	–	20	µV/°C
Input Bias Current [1]	I_{BIAS}	VID = 0, V_{CM} in range	–50	–	50	µA
Input Offset Current [1]	I_{OS}	VID = 0, V_{CM} in range	–1	–	1	µA
Input Common-Mode Range (DC)	V_{CM}	V_{ID} = 0 V	–1.8	–	2	V
Gain	A_V	Default power-up value	–	20	–	V/V
Gain Error	E_A	V_{CM} in range	–1.6	–	1.6	%
Gain Drift [8]	E_{AD}	V_{CM} in range	–60	–	15	ppm/°C
Output Offset	V_{OOS}	Default power-up value	–	1.65	–	V
Output Offset Error	E_{VO}	V_{CM} in range, V_{OOS} = 2.5 V	–75	±25	75	mV
Output Offset Drift	V_{OOSD}	V_{CM} in range, V_{OOS} = 2.5 V	–135	–	135	µV/°C
Small Signal –3 dB Bandwidth (at Gain = 20)	BW	V_{IN} = 10 mVpp	2	–	–	MHz
Output Settling Time (to within 40 mV)	t_{SET}	V_{CSO} = 1 Vpp square wave, Gain = 20 V/V, C_{OUT} = 50 pF	0.2	–	1	µs
Output Dynamic Range	V_{CSOUT}	–100 µA < I_{CSO} < 100 µA	0.3	–	4.8	V
Output Voltage Clamp	V_{CSC}	I_{CSO} = –1 mA	4.8	5.2	5.6	V
Output Current Sink	I_{CSsink}	V_{ID} = 0 V, V_{CSO} = 1.5 V, Gain = 20 V/V	240	–	470	µA
Output Current Sink (Boosted) [13]	$I_{CSsinkb}$	V_{OOS} = 1.5 V, V_{ID} = –50 mV, Gain = 20 V/V, V_{CSO} = 1.5 V	1.9	–	4.4	mA
Output Current Source [1]	$I_{CSsource}$	V_{ID} = 0 V, V_{CSO} = 1.5 V, Gain = 20 V/V	–15.1	–	–1.6	mA
VBB Supply Ripple Rejection	PSRR	V_{ID} = 0 V, 100 kHz, Gain = 20 V/V [8]	–	75	–	dB
		V_{CSP} = V_{CSM} = 0 V, DC, Gain = 20 V/V	75	–	–	dB
DC Common-Mode Rejection	CMRR	V_{CM} step from 0 to 200 mV, Gain = 20 V/V	53	75	–	dB
AC Common-Mode Rejection [8]	CMRR	V_{CM} = 200 mVpp, 100 kHz, Gain = 20 V/V	–	62	–	dB
		V_{CM} = 200 mVpp, 1 MHz, Gain = 20 V/V	–	43	–	dB
		V_{CM} = 200 mVpp, 10 MHz, Gain = 20 V/V	–	25	–	dB
Common-Mode Recovery Time (to within 100 mV)	t_{CMrec}	V_{CM} step from –4 V to 1 V, Gain = 20 V/V, C_{OUT} = 50 pF	–	–	2.1	µs
Output Slew Rate 10% to 90%	SR	V_{ID} step from 0 to 175 mV, Gain = 20 V/V, C_{OUT} = 50 pF	2.1	–	5.3	V/µs
Input Overload Recovery (to within 40 mV)	t_{IDrec}	V_{ID} step from 250 mA to 0 V, Gain = 20 V/V, C_{OUT} = 50 pF	0.4	–	2.1	µs
Offset Calibration Time	t_{Cal}	From STRn rising edge	–	–	100	µs

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
MEASUREMENT SYSTEM						
Supply Voltage (VBRG): Measurement Range	V_{VM}		0	–	50.4	V
Supply Voltage (VBRG): Measurement Accuracy	E_{VM}	V_{BRG} ≤ 30 V	–	±0.5	–	V
VLR Output Voltage: Measurement Accuracy	E_{VLM}		–2	–	2	%
Temperature Measurement Range	T_J		–50	–	190	C
Temperature Measurement Accuracy	E_{TJ}		–	±5	–	C
BEMF DETECTION						
BEMF Filter Time	t_{BF}	Default power-up value	0.19	0.2	0.21	ms
		Programmable range	0	–	20	ms
BEMF Comparator Offset	V_{BO}	5.5 V < V_{BB} < 28 V	–60	±40	60	mV
NVM – PROGRAMMING PARAMETERS						
Programming Voltage	V_{PP}	Applied to VBB when programming	24	–	–	V
Programming Supply Setup Time	t_{PRS}	V_{PP} > $V_{PP(min)}$ to start of NVM write	10	–	–	ms
DIAGNOSTICS AND PROTECTION						
VBB Undervoltage Lockout	V_{BBON}	V_{BB} rising, VLR = 0	4.3	–	4.8	V
		V_{BB} rising, VLR = 1	5.75	–	6.4	V
	V_{BBOFF}	V_{BB} falling, VLR = 0	4.05	–	4.5	V
		V_{BB} falling, VLR = 1	5.24	–	5.80	V
VBB Undervoltage Lockout Hysteresis	V_{BBHys}	VLR = 0	–	300	–	mV
		VLR = 1	–	500	–	mV
VBB Startup Voltage [8]	V_{BBSU}	V_{BB} rising	–	–	5.0	V
VBB POR Voltage	V_{BBR}	V_{BB} falling	–	3.2	3.7	V
VPP Undervoltage	V_{PPUV}		20	–	22	V
VLR Undervoltage Reset (3.3 V)	V_{LRON}	V_{LR} rising, VLR = 0	2.73	2.90	3.00	V
	V_{LROFF}	V_{LR} falling, VLR = 0	2.67	2.80	2.95	V
VLR Undervoltage Reset Hysteresis (3.3 V)	$V_{LRUVHys}$	VLR = 0	–	70	–	mV
VLR Undervoltage Reset (5 V)	V_{LRON}	V_{LR} rising, VLR = 1	4.15	4.40	4.55	V
	V_{LROFF}	V_{LR} falling, VLR = 1	4.10	4.30	4.50	V
VLR Undervoltage Reset Hysteresis (5 V)	$V_{LRUVHys}$	VLR = 1	–	50	–	mV
VIO Undervoltage Reset (3.3 V)	V_{IOON}	V_{IO} rising, VIO = 0	2.73	2.90	3.00	V
	V_{IOOFF}	V_{IO} falling, VIO = 0	2.65	2.80	2.95	V
VIO Undervoltage Reset Hysteresis (3.3 V)	$V_{IOUVHys}$	VIO = 0	–	70	–	mV

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
DIAGNOSTICS AND PROTECTION (continued)						
VIO Undervoltage Reset (5 V)	V_{IOON}	V_{IO} rising, VIO = 1	4.1	4.40	4.55	V
	V_{IOOFF}	V_{IO} falling, VIO = 1	4.05	4.30	4.50	V
VIO Undervoltage Reset Hysteresis (5 V)	$V_{IOUVHys}$	VIO = 1	–	50	–	mV
VREG Undervoltage	V_{RON}	V_{REG} rising, VRG = 0	6.4	6.6	6.8	V
		V_{REG} rising, VRG = 1	7.6	7.9	8.2	V
	V_{ROFF}	V_{REG} falling, VRG = 0	5.5	5.7	5.9	V
		V_{REG} falling, VRG = 1	6.9	7.2	7.4	V
Bootstrap Undervoltage	V_{BCUV}	V_{BOOT} falling, $V_{BOOT} = V_{Cx} – V_{Sx}$	55	–	71	$\%V_{REG}$
Bootstrap Undervoltage Hysteresis	$V_{BCUVHys}$		–	8	–	$\%V_{REG}$
ENABLE Input Timeout	t_{ETO}		90	100	110	ms
VBRG Input Voltage	V_{BRG}	When VDS monitor is active	5.5	VBB	50	V
VBRG Input Current	I_{VBRG}	V_{DST} = default, V_{BB} = 12 V, 0 V < V_{BRG} < V_{BB}	–	–	500	µA
	I_{VBRGQ}	Sleep mode $V_{BB} = V_{BRG}$ < 35 V	–	–	5	µA
VDS Threshold	V_{DST}	Default power-up level	1.0	1.2	1.4	V
		V_{BRG} ≥ 8 V [10]	–	–	3.15	V
		5.5 V ≤ V_{BRG} < 8 V [10]	–	–	1.55	V
VDS Threshold Offset [3][4]	V_{DSTO}	V_{DST} > 1 V	–200	±100	200	mV
		V_{DST} ≤ 1 V	–150	±50	150	mV
VDS Qualifier Time [5]	t_{VDQ}	Default power-up value	1.52	1.6	1.68	µs
		Programmable range	0.6	–	6.3	µs
Overcurrent Threshold Voltage	V_{OCT}	Default power-up value	492	600	708	mV
Overcurrent Threshold Offset	V_{OCTO}	V_{OCT} ≤ 400 mV	–40	–	40	%
		600 mV ≤ V_{OCT} ≤ 1000 mV	–18	–	18	%
		V_{OCT} ≥ 1200 mV	–10	–	10	%
SDO Output: Clock Division Ratio	N_D	CKS = 1		280000		–
DIAG Output: Fault Pulse Period	t_{FP}	DG = 1	95	100	105	ms
DIAG Output: Fault Pulse Duty Cycle	D_{FP}	DG = 1: No Fault present		80		%
		DG = 1: Fault present		20		%
DIAG Output: Clock Division Ratio	N_D	DG = 3		280000		–

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Temperature Warning Threshold	T_{JW}	Temperature increasing	125	135	145	°C
Temperature Warning Hysteresis	T_{JWhys}		–	15	–	°C
Overtemperature Threshold	T_{JF}	Temperature increasing	170	175	180	°C
Overtemperature Hysteresis	T_{Jhys}	Recovery = $T_{JF} – T_{Jhys}$	–	15	–	°C

[1] For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device terminal.
[2] See Figure 5 for gate drive output timing.
[3] As V_{SX} decreases, high-side fault occurs if $V_{BAT} – V_{SX} > V_{DST} + V_{DSTO}$.
[4] As V_{SX} increases, low-side fault occurs if $V_{SX} > V_{DST} + V_{DSTO}$.
[5] See Figure 6 and Figure 7 for V_{DS} monitor timing.
[6] Current limit threshold voltage error is the difference between the target threshold voltage and the actual threshold voltage, referred to maximum full scale (100%) current: $E_{ILIM} = 100 \times (V_{ILIMActual} – V_{ILIM}) / 200\%$ (V_{ILIM} in mV).
[7] Slew rate is controlled during both transitions and will not exceed specified limits at any point between test limits.
[8] Ensured by design and characterization.
[9] LIN bus load conditions (C_{BUS}, R_{BUS}): 1 nF; 1 kΩ / 6.8 nF; 660 Ω / 10 nF; 500 Ω
[10] Maximum value of V_{DS} threshold that should be set in the configuration registers for correct operation when V_{BB} is within the stated range.
[11] Parameters are not guaranteed above or below the LIN 2.2 A operating limits V_{BB} = 7 to 18 V.
[12] For DT[5:0] > 0, jitter of ±25 ns must be added to the limits shown.
[13] If the amplifier output voltage (V_{CSO}) is more positive than the value demanded by the applied differential input (V_{ID}) and output offset (V_{OOS}) conditions, then output current sink capability is boosted to enhance negative going transient response.

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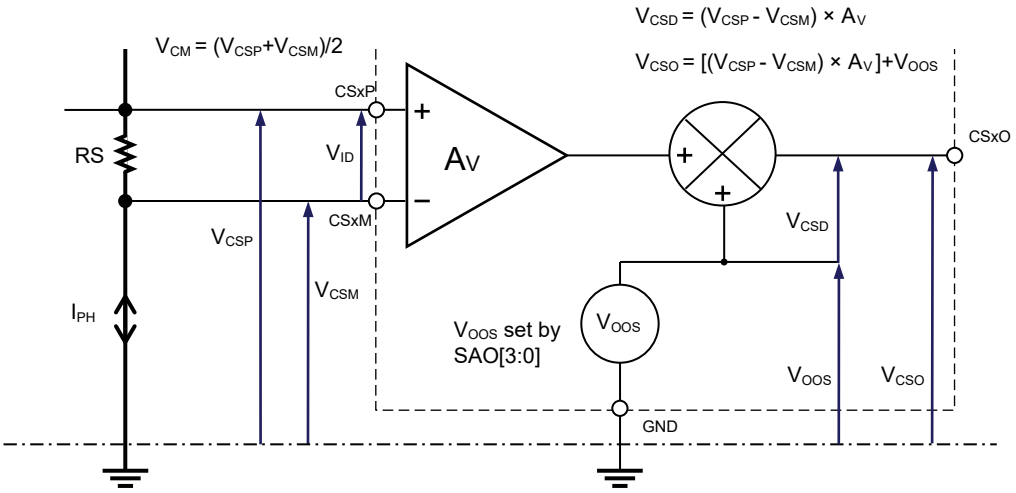
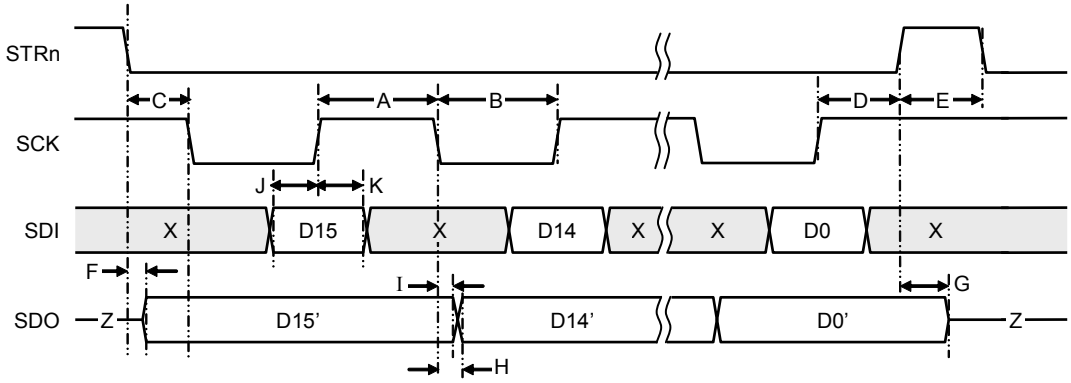


Figure 3: Sense Amplifier Voltage Definitions



X=don't care, Z=high impedance (tri-state)

Figure 4: Serial Interface Timing

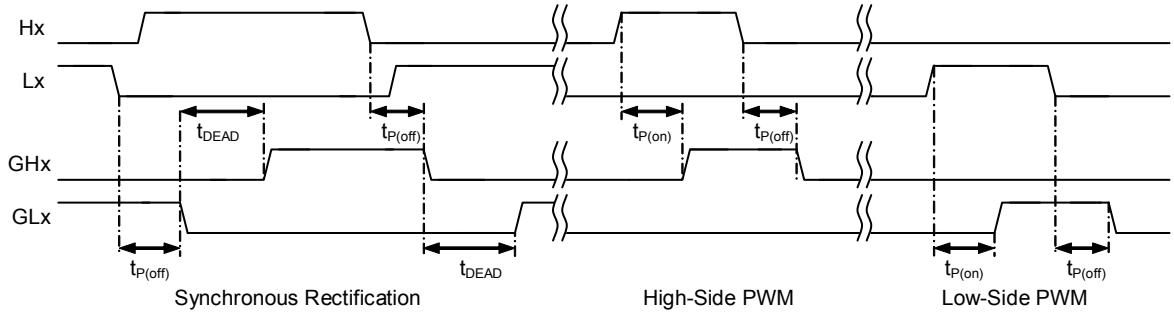


Figure 5: Gate Drive Timing, Phase Logic Inputs

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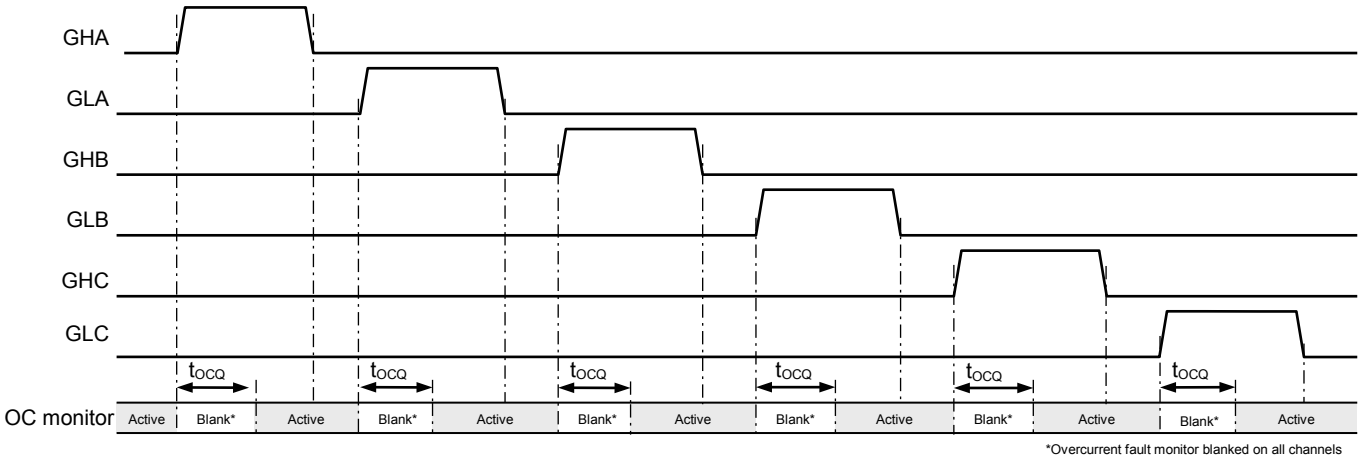

Figure 6: Overcurrent Fault Monitor – Blank Mode Timing (OCQ = 1)

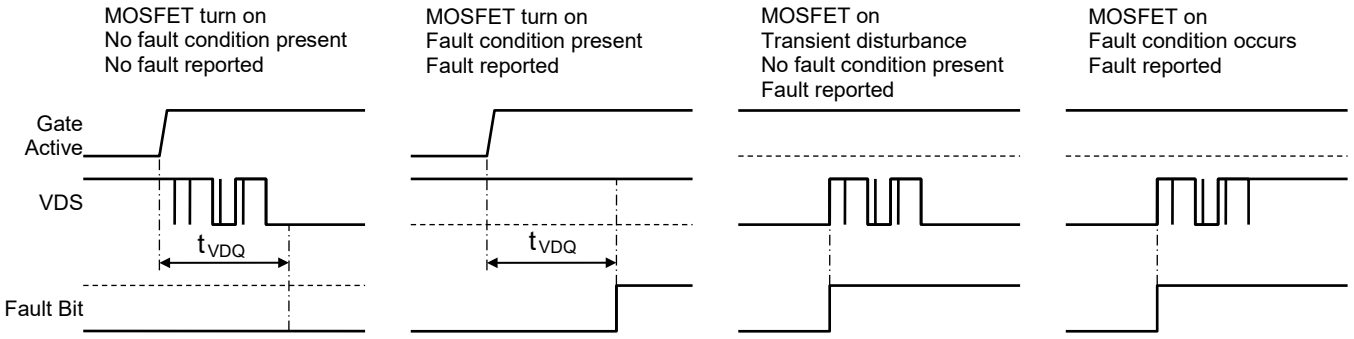

Figure 7: VDS Fault Monitor – Blank Mode Timing (VDQ = 1)

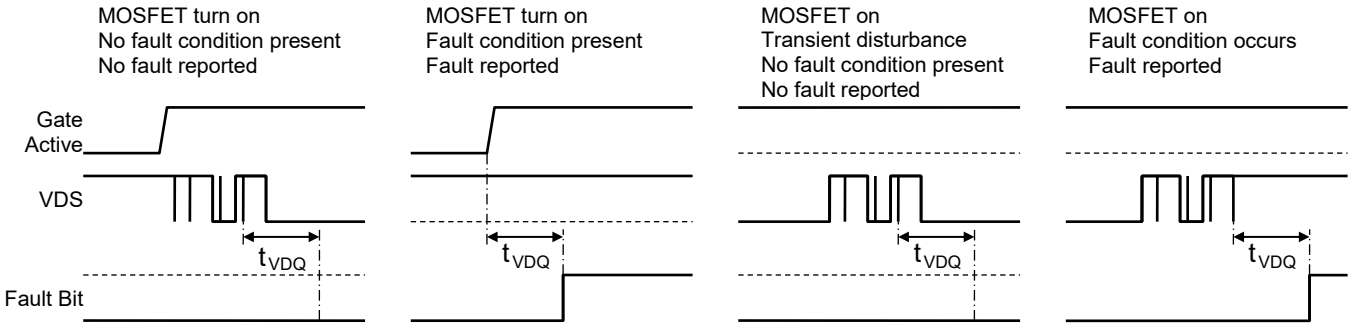

Figure 8: VDS Fault Monitor – Debounce Mode Timing (VDQ = 0)

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LOGIC TRUTH TABLES

Table 1: Control Logic – Logic Inputs

Phase A					Phase B					Phase C				
HA	LA	GHA	GLA	SA	HB	LB	GHB	GLB	SB	HC	LC	GHC	GLC	SC
0	0	LO	LO	Z	0	0	LO	LO	Z	0	0	LO	LO	Z
0	1	LO	HI	LO	0	1	LO	HI	LO	0	1	LO	HI	LO
1	0	HI	LO	HI	1	0	HI	LO	HI	1	0	HI	LO	HI
1	1	LO	LO	Z	1	1	LO	LO	Z	1	1	LO	LO	Z

HI = high-side FET active, LO = low-side FET active
Z = high impedance, both FETs off
All control register bits set to 0. Gate drive outputs active.

Table 2: Control Logic – Serial Register

Phase A					Phase B					Phase C				
AH	AL	GHA	GLA	SA	BH	BL	GHB	GLB	SB	CH	CL	GHC	GLC	SC
0	0	LO	LO	Z	0	0	LO	LO	Z	0	0	LO	LO	Z
0	1	LO	HI	LO	0	1	LO	HI	LO	0	1	LO	HI	LO
1	0	HI	LO	HI	1	0	HI	LO	HI	1	0	HI	LO	HI
1	1	LO	LO	Z	1	1	LO	LO	Z	1	1	LO	LO	Z

HI = high-side FET active, LO = low-side FET active
Z = high impedance, both FETs off
Logic 0 input on HA, LA, HB, LB, HC, and LC. Gate drive outputs active.

Table 3: Control Combination Logic – Logic Inputs and Serial Register

Terminal	Register	Internal
Hx	xH	HIx
0	0	0
0	1	1
1	0	1
1	1	1

Terminal	Register	Internal
Lx	xL	LOx
0	0	0
0	1	1
1	0	1
1	1	1

The three phases are controlled independently.

Internal control signals (HIx, LOx) are derived by combining the logic states applied to the control input terminals (Hx, Lx) with the bit patterns held in the Control register (xH, xL).

Normally the input terminals or the Control register method is used for control with the other being held inactive (all terminals or bits at logic 0).

HIx	LOx	GHx	GLx	Sx	Comment
0	0	LO	LO	Z	Phase disabled
0	1	LO	HI	LO	Phase sinking
1	0	HI	LO	HI	Phase sourcing
1	1	LO	LO	Z	Phase disabled

Gate drive outputs active.
When gate drive outputs are disabled, GHx and GLx are held low.

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FUNCTIONAL DESCRIPTION

The AMT49105 provides many of the key elements to allow a microcontroller to drive a motor and communicate with a central ECU allowing a high-performance cost-effective motor control solution with reduced component count.

It provides six high current gate drives capable of driving a wide range of N-channel power MOSFETs. The gate drives are configured as three half bridges, each with a high-side drive and a low-side drive. The three half bridges can be operated independently or together as a three-phase bridge driver for BLDC or PMSM motors.

Gate drives have programmable drive voltage and drive strength and can be controlled individually with logic inputs or through the SPI-compatible serial interface. The control logic inputs provide a very flexible solution for many motor control applications. Independent control over each MOSFET allows each driver to be driven with an independent PWM signal for full sinusoidal excitation. All logic inputs are standard CMOS levels and can be programmed to be compatible with 3.3 or 5 V logic.

The AMT49105 requires a single unregulated supply of 5.5 to 50 V and includes a charge-pump regulator, a logic supply linear regulator for external use, and two internal integrated linear regulators. The charge pump regulator provides the regulated gate drive voltage used for the low-side gate drive and to charge the bootstrap capacitors. The logic supply linear regulator can be used to provide power for an external microcontroller and sensors. The output voltage, V_{LR}, can be programmed to 3.3 or 5 V. One internal linear regulator provides the internal logic supply voltage, V_{DD}, and a second independent internal regulator provides the supply and reference, V_{IO}, for the digital input and output terminals.

Circuit functions are provided within the AMT49105 to ensure that, under normal operating conditions, all external power MOSFETs are fully enhanced at supply voltages down to 5.5 V. For extreme battery voltage drop conditions, the AMT49105 is guaranteed not to reset any internal states at supply voltages down to 3.5 V. However, below 5.5 V it is possible that the gate drive outputs may fall below a safe level and be disabled.

A low-power sleep state initiated by a register setting through the serial interface allows the AMT49105, the power bridge, and the load to remain connected to a vehicle battery supply without the need for an additional supply switch.

An ISO17987 (LIN 2.x) and SAE J2602 compliant physical interface is provided for systems using LIN bus communications. This can also operate as a PWM interface for simpler PWM communication systems. In addition to the IG input, this physical interface can be used in either LIN mode or in PWM mode to wake the circuit from the sleep state and activate the microcontroller.

For systems requiring a potential divider to be able measure the motor bridge voltage, a switch from the VBRG terminal is provided on the BRSW terminal. This helps to minimize the VBR current drawn from the motor supply in power down or sleep states.

The AMT49105 also includes an integrated bemf crossing detector with a multiplexed output that can be used to detect motor motion before activation of any drive outputs.

The integrated linear regulator, programmable to 3.3 or 5 V, can provide power to the local microcontroller and additional circuits. A programmable window watchdog, operating in conjunction with the regulator and the sleep control circuits, is available to monitor the microcontroller activity.

A number of diagnostic features are included to provide indication of and/or protection against undervoltage, overtemperature, and power bridge faults. A single diagnostic output pin can be programmed to provide optional diagnostic outputs. Detailed diagnostic information is available through the serial interface, which also allows programming of the control and configuration parameters and the user-defined power-up parameters can be stored in nonvolatile memory.

An integrated data acquisition system provides digitized feedback of the bridge voltage and chip temperature.

Specific functions are described more fully in following sections.

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Input and Output Terminal Functions

VBB: Main power supply for internal regulators and charge pump. The main power supply should be connected to VBB through a reverse voltage protection circuit and should be decoupled with ceramic capacitors connected close to the supply and ground terminals.

CP1, CP2: Pump capacitor connection for charge pump. Connect a 470 nF ceramic capacitor between CP1 and CP2.

VREG: Regulated voltage, selectable as 8 or 11 V, used to supply the low-side gate drivers and to charge the bootstrap capacitors. A sufficiently large storage capacitor of at least 4.7 µF (X7R, 50 V) must be connected to this terminal to provide the transient charging current.

VLR: VLR regulator output. External logic can be powered by this node. The voltage can be selected as 3.3 or 5 V. A ceramic capacitor of at least 1 µF with an ESR of no more than 250 mΩ should be fitted between the VLR output and GND to ensure stability.

GND: Analog reference, digital, and power ground. Connect all GND terminals together to supply ground—see Layout Recommendations.

VBRG: Sense input to the top of the external MOSFET bridge. Allows accurate measurement of the voltage at the drain of the high-side MOSFETs in the bridge.

BRSW: A switched version of the voltage at the VBRG terminal. High impedance in sleep mode. Can also be switched off via the serial interface.

CA, CB, CC: High-side connections for the bootstrap capacitors and positive supply for high-side gate drivers.

GHA, GHB, GHC: High-side gate-drive outputs for external N-channel MOSFETs.

SA, SB, SC: Motor phase connections. These terminals sense the voltages switched across the load. They are also connected to the negative side of the bootstrap capacitors and are the negative supply connections for the floating high-side drivers.

GLA, GLB, GLC: Low-side gate-drive outputs for external N-channel MOSFETs.

LSSA, LSSB, LSSC: Low-side return path for discharge of the capacitance on the MOSFET gates, connected to the common sources of the low-side external MOSFETs independently through a low-impedance track.

HA, HB, HC: Logic inputs to control the high-side gate drive outputs. A pull-down is connected to each input.

LA, LB, LC: Logic inputs to control the low-side gate drive outputs. A pull-down is connected to each input.

ENABLE: Disables all gate drive outputs when pulled low in direct mode or after a timeout in watchdog mode. In direct mode, it provides an independent output disable, directly to the gate drive outputs, to allow a fast disconnect on the power bridge.

CSP, CSM: Differential current sense amplifier inputs. Connect directly to each end of the sense resistor using separate PCB traces.

CSO: Current sense amplifier outputs.

LIN: LIN bus connection compliant with ISO17987 (LIN 2.x). This input can also be used as a PWM that can be passed to the LRX output.

LTX: LIN or FAULT transmit logic level input.

LRX: LIN or PWM receive logic level output.

IG: Ignition switch input, with resistor pull-down, to wake up the AMT49105 and enable the logic regulator for the microcontroller. When not used, IG should be tied to ground to minimize the effect on the supply current in the sleep state. The input thresholds allow for ±2 V ground difference between the switch ground and the IC ground.

DIAG: Programmable diagnostic output. Can be shorted to ground or VBB without damage.

WDOG: External microcontroller watchdog logic input with resistor pull-down. Window watchdog with programmable minimum and maximum clock period.

MRSTn: Microcontroller reset control output. Holds the microcontroller in reset until supplies are available. Resets the microcontroller in case of watchdog failure.

PM: Program mode logic input disables watchdog and MRSTn.

SDI: Serial data input with resistor pull-down. 16-bit serial word input msb first.

SDO: Serial data output. High impedance or clock output when STRn is high. Outputs bit 15 of the Status register, the fault flag, as soon as STRn goes low.

SCK: Serial clock input with resistor pull-down. Data is latched in from SDI on the rising edge of CLK.

STRn: Serial data strobe and serial access enable input with resistor pull-up. When STRn is high, any activity on SCK or SDI is ignored and SDO is high impedance or a clock output.

BXM: BEMF zero crossing multiplex output. Logic level outputs representing the state of a selected phase relative to the center (average) voltage of the three phases.

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Supplies and Regulators

Main Power Supply

A single power supply voltage is required. The main power supply should be connected to VBB through a reverse voltage protection circuit. A 100 nF ceramic decoupling capacitor must be connected close to the supply and ground terminals of the AMT49105.

Four regulator circuits are included: a pump regulator for the gate drive, an externally connected linear regulator to provide power for an external microcontroller and associated circuits, and two internally connected linear regulators—one for the core logic and one for the I/O interface.

The output voltage of the externally connected linear regulator, V_{LR}, available at the VLR terminal, is selected as 3.3 or 5 V using the VLR bit.

The core logic is guaranteed to operate correctly to below the VBB POR level, ensuring that the AMT49105 will continue to operate safely until all logic is reset when a power-on-reset state is present.

The voltage of the I/O regulator is selected as 3.3 or 5 V using the VIO bit.

The AMT49105 will operate within specified parameters with V_{BB} from 5.5 to 50 V. Below 5.5 V, the gate drive outputs may be inactive but the AMT49105 will continue to function with a supply down to 3.5 V. It will remain in a safe state between 0 and 50 V under all supply switching conditions. This provides a very rugged solution for use in the harsh automotive environment.

At power-up, the logic inputs will be forced to their inactive state until V_{IO} rises above the rising undervoltage threshold, V_{IOON}.

If the WD mask bit is saved as 0 in nonvolatile EEPROM (NVM), the MRSTn output will remain low for 10 ms after V_{LR} rises above the rising undervoltage threshold, V_{LRON}. If the WD mask bit is saved as 1 in NVM, the MRSTn output will remain low for 10 ms after V_{LR} rises above the rising undervoltage threshold, V_{LRON}, or until the first valid serial transfer (whichever occurs first). After the MRSTn output goes high, the gate drive outputs can be activated as described in the Fault Action and Output Enable/Disable sections.

VLR Regulator

An integrated programmable linear regulator is provided to supply external logic level circuits such as a microcontroller or interface circuit. The output of the regulator on the VLR terminal is derived from V_{BB} and the output can be selected as 3.3 or 5 V using the VLR bit.

If not used, the VLR regulator output can be disabled by setting VLRD = 1.

The regulator includes current limit, undervoltage, and short protection. The current limiting circuit will reduce the output voltage to ensure that the output current does not exceed the current limit, I_{LROC}. If the output voltage drops below the falling undervoltage threshold, V_{LROFF}, the MRSTn output will go low and can be used to reset an external microcontroller.

If the output voltage falls below the regulator shutdown threshold, V_{LROSD}, for a period exceeding the shutdown lockout period, t_{LRLO}, the regulator is turned off. In this state, a small pilot current, I_{LROP}, is driven through the regulator output to detect load resistance. If the resultant voltage rises above the regulator enable threshold, V_{LROE}, the regulator immediately attempts to restart.

At power-up, or when the regulator restarts, full output current is delivered for a period equal to the shutdown lockout period. During this time, the output voltage is not monitored for short circuit conditions in order to ensure reliable regulator startup.

If ESF = 1 and the AMT49105 internal junction temperature, T_J, rises above the overtemperature threshold, T_{JF}, the VLR regulator is immediately shut down and MRSTn will go low. All AMT49105 functions other than the regulator remain active. When T_J drops by more than the overtemperature threshold ($T_J < T_{JF} - T_{Jhys}$) there are two possible sequences depending on the state of the WD mask bit.

If the WD mask bit is 0, i.e. watchdog is active, the VLR regulator will be re-enabled when T_J drops by more than the overtemperature threshold ($T_J < T_{JF} - T_{Jhys}$). MRSTn will remain low for 10 ms after V_{LR} rises above the rising undervoltage threshold, V_{LRON}. MRSTn will then go high and the watchdog timer will be reset. The watchdog timer will remain reset for 100 ms during which time the WDOG input will be ignored. The gate drive outputs will remain disabled until the first valid watchdog is detected.

If the WD mask bit is 1, i.e. watchdog is inactive, the VLR regu-

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lator will be re-enabled when T_J drops by more than the overtemperature threshold ($T_J < T_{JF} - T_{Jhys}$). MRSTn will remain low for 10 ms after V_{LR} rises above the rising undervoltage threshold, V_{LRON}. The gate drive outputs will be re-enabled 10 ms after MRSTn goes high. A valid serial transfer will immediately terminate this timeout, set MRSTn high, and allow the gate drive outputs to be activated.

If an undervoltage shutdown and an overtemperature warning occur simultaneoulsy, both must be cleared to allow the regulator to restart.

Internal AMT49105 logic circuitry is not powered from the VLR regulator and remains fully operational regardless of whether the VLR regulator is running normally or shut down.

A ceramic capacitor of at least 1 µF with an ESR of no more than 250 mΩ should be fitted between the VLR terminal and GND to guarantee stability during oscillation and voltage excursions outside the specified output voltage range. In some applications, the use of redundant output capacitors may be advisable to avoid such a condition in the event of a single-point capacitor high-impedance failure.

Pump Regulator

The gate drivers are powered by a programmable voltage internal regulator which limits the supply to the drivers and therefore the maximum gate voltage. At low input supply voltage the regulated supply is maintained by a charge pump boost converter which requires a pump capacitor, typically 470 nF, connected between the CP1 and CP2 terminals.

The regulated voltage, V_{REG}, can be programmed to 8 or 11 V and is available on the VREG terminal. The voltage level is selected by the value of the VRG bit. When VRG = 1, the voltage is set to 11 V; when VRG = 0, the voltage is set to 8 V. A sufficiently large storage capacitor (see Layout Recommendations section) must be connected to this terminal to provide the transient charging current to the low-side drivers and bootstrap capacitors.

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Operating Modes

The AMT49105 provides a sleep state and two operating modes related to the selected use of the LIN bus terminal: LIN mode and PWM mode. All configuration settings and basic control functions can be programmed through the serial interface in both LIN and PWM modes.

LIN Mode

When operating in LIN mode (OPM = 0), the LIN terminal complies with the requirements of the LIN standard regarding dominant timeout and wake on LIN.

PWM Mode

When operating in PWM mode (OPM = 1), the LIN dominant timeout is disabled and the wake mode is changed to wake on a simple rising or falling edge.

Programming Mode

The PM logic input terminal provides the ability, when high, to disable the window watchdog and any related actions. It also forces the MRSTn output into a high-impedance state. This can be used to permit exclusive access to the reset input of the external microcontroller, for example, during flash programming using an external programmer. When the PM input is low, the window watchdog and the MRSTn output function is as described in the Microcontroller Reset and Watchdog section.

Low Power Sleep State

The AMT49105 provides a low-power sleep state where the consumption from the supply is reduced to a minimum by disabling all normal operation including the charge pump regulator, the internal logic regulator, the external regulator, and the internal clock. To achieve the minimum supply current in the sleep state, the LIN terminal must be at the same voltage as the supply terminal, VBB, and the IG terminal should be tied to ground.

The AMT49105 can be commanded to go into the sleep state using the serial interface to change the GTS bit from 0 to 1. The sleep state is also entered following a watchdog cycle count failure as described in the Microcontroller Watchdog section.

The sequence to wake the AMT49105 is determined by the operating mode defined by the OPM bit. When LIN mode is selected (OPM = 0), the AMT49105 will wake up according to the LIN protocol.

When the PWM mode is selected (OPM = 1), the AMT49105 will wake up on any valid transition of the signal at the LIN terminal. These sequences are fully described and defined in the LIN Physical Interface section.

Table 4: Operating and Wake Mode Features

	Operating Mode			
	LIN		PWM	
OPM	0		1	
Sleep (SPI) Command	SPI (GTS 0→1)			
Sleep (IG) Command	No			
IGP	0	1	0	1
Wake (IG)	IG L→H			
Wake (LIN)	First L→H transition on LIN terminal after LIN terminal low for $>t_{BUSWK}$	No	Any transition on LIN terminal present for $>t_{BUSWK}$	No

Wake up on the LIN terminal can be disabled by setting the IGP bit to 1.

In either operating mode, the AMT49105 will also wake up on a low to high transition of the signal on the IG terminal.

In the sleep state, the MRSTn output is held low, latched faults are cleared and the Diagnostic and Status registers are reset to zero.

When coming out of the sleep state, all registers are reset to the user-defined values held in the nonvolatile memory and the AMT49105 follows the same procedure as for a full power-on reset. The logic inputs will be forced to their inactive state until V_{IO} rises above the rising undervoltage threshold, V_{IOON}.

If the WD mask bit is saved as 0 in nonvolatile memory, i.e. watchdog is active, the MRSTn output will remain low for 10 ms after the external logic supply, V_{LR}, rises above the rising undervoltage threshold, V_{LRON}. MRSTn will then go high and the watchdog timer will be reset. The watchdog timer will remain reset for 100 ms during which time the WDOG input will be ignored. The gate drive outputs will remain disabled until the first valid watchdog is detected.

If the WD mask bit is saved as 1 in nonvolatile memory, i.e. watchdog is inactive, the MRSTn output will remain low for 10 ms, after the external logic supply, V_{LR}, rises above the rising undervoltage threshold, V_{LRON}. The gate drive outputs can be activated 10 ms after MRSTn goes high. A valid serial transfer will terminate this timeout, set MRSTn high, and allow the gate drive outputs to be activated. The VLRU fault bit remains in the Diagnostic register until cleared.

In addition, the charge pump output monitor ensures that the gate drive outputs are off until the charge pump reaches its correct operating condition. The charge pump will stabilize in approximately 2 ms under nominal conditions.

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Microcontroller Reset and Watchdog

Microcontroller Reset

The microcontroller reset output, MRSTn, can be used to reset and reinitialize an external microcontroller if a V_{LR} undervoltage, watchdog fault, or power-on-reset (POR) occurs. The MRSTn output will be active low when the V_{LR} regulator undervoltage or POR fault state is present and will remain low for 10 ms after the V_{LR} undervoltage condition is removed.

Microcontroller Watchdog

The AMT49105 includes a programmable window watchdog that can be used to determine if the external microcontroller is operating in an adverse state. After any transition (high-to-low or low-to-high) on the WDOG input, the WDOG input must be held at a DC level for the duration of the minimum watchdog time, t_{WM}, set by the WM variable. Following the end of the minimum watchdog time, a transition on the WDOG input must then be detected before the end of the watchdog window time, t_{WW}, set by the WW variable in order to reset the watchdog timer. This means that the time between each transition on the WDOG input must be longer than t_{WM} and shorter than $t_{WM} + t_{WW}$.

If a subsequent transition is detected before t_{WM} or if a transition is not detected within $t_{WM} + t_{WW}$, then the WD bit will be set in the Status register and the MRSTn output will go active low for 10 ms in order to reset the microcontroller.

In all fault cases (POR, undervoltage or watchdog), when MRSTn goes high after the 10 ms low period, the watchdog timer will be reset and remain reset for 100 ms. During this time, the WDOG input is ignored. The first transition must then be detected within $t_{WM} + t_{WW}$ or the micro-reset cycle will repeat. There is no minimum watchdog time, t_{WM}, following a micro reset. The micro reset and watchdog timing is shown in Figure 9. The WD bit will remain set in the Status register until cleared.

When a watchdog failure is detected, the gate drive outputs are disabled (low) and any attached motor will coast. The gate drive outputs remain disabled until a valid watchdog transition is detected. Once a valid watchdog has been detected, the AMT49105 will re-enable the gate drive outputs.

If the watchdog function is not required, it is possible to disable the function by setting the WD bit in the mask register to 1. This will completely disable the watchdog monitor and any possible actions that it may take.

If the microcontroller has completely stopped working, it is possible to put the AMT49105 into the sleep state after a num-

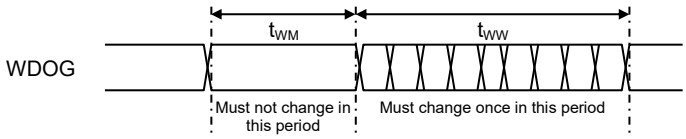

Figure 9a: Watchdog Timing Requirements

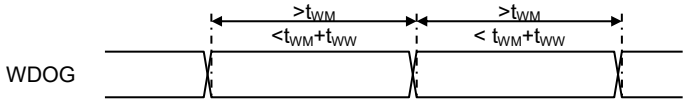

Figure 9b: Suitable Watchdog Signal

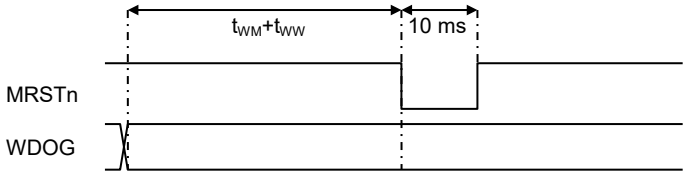

Figure 9c: Reset after Missing Watchdog Edge

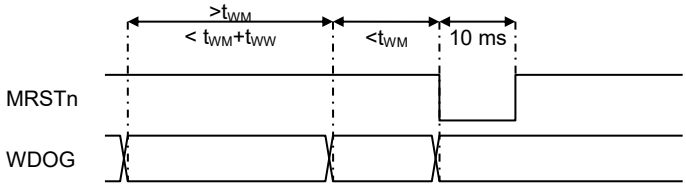

Figure 9d: Reset after Early Watchdog Edge

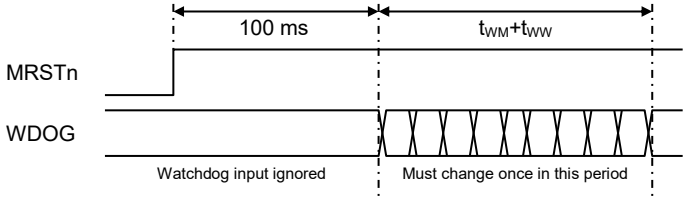

Figure 9e: Timing after Reset

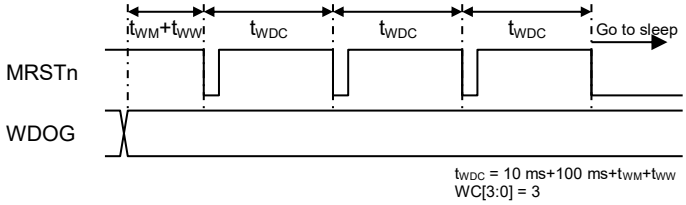

Figure 9f: Sleep after Fail Cycle Count

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ber of reset cycles using the watchdog fail cycle count variable, WC[3:0]. The value in WC[3:0] sets the number of watchdog fail/reset cycles that can occur before the AMT49105 goes into the sleep state. A value of 1 will allow one fail-reset cycle and will go to sleep on the next watchdog failure if no valid transitions are detected on the WDOG input. A value of 8 will allow 8 fail-reset cycles and will go to sleep on the 9th watchdog failure if no transitions are detected on the WDOG input. The counter is reset if any valid transition is detected on the WDOG input. A valid transition is one that occurs after the initial 100 ms following a microcontroller reset and before the end of the initial watchdog window time, $t_{WM} + t_{WW}$. Figure 9f shows the fail-cycle operation when WC[3:0] is set to 3. A value of zero in WC[3:0] will disable this feature and permit unlimited fail-reset cycles.

The sequence to wake the AMT49105 from the sleep state is described in the Low Power Sleep State section.

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LIN Physical Interface

The AMT49105 includes a physical interface to drive and monitor a single wire LIN Bus as a slave node that complies with the ISO17987 (LIN 2.x) and SAE J2602 standards. The LIN terminal can withstand voltages from –40 to 50 V with respect to the ground pin without adversely affecting LIN bus communications between other devices. LIN protocol handling is not included.

The LIN terminal meets all voltage, timing, and slew limitation requirements of LIN 2.2 when actively transmitting and receiving. When operating in LIN mode (OPM=0), a timer is included to ensure that the LIN output does not remain dominant when a fault occurs. If the LIN terminal is driven in the dominant state for longer than the transmit dominant timeout period, t_{TXTO}, then the output is disabled and allowed to return to the recessive state in order to avoid locking the LIN bus for other messages. The dominant timeout function is disabled in the PWM operating mode (OPM = 1) or when the LIN interface is in the standby state (LEN = 0).

The data to be transmitted is input to the LTX terminal and converted to LIN bus signals. A logic high on the LTX input produces a recessive bus (high) state while a logic low produces a dominant bus (low) state. The LTX input has an internal pull-up resistor to ensure a recessive state if the pin is not connected or becomes disconnected.

The logic state of the LIN bus is determined by the receiver and output as a logic level on the LRX terminal. LRX will be low when the LIN bus is in the dominant (low) state and high when the LIN bus is in the recessive (high) state. In the sleep state, LRX is not active and will be low.

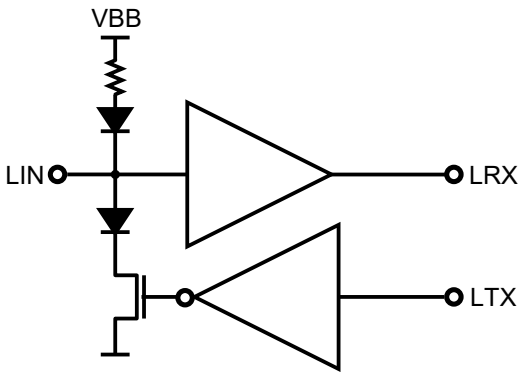

Figure 10: LIN Physical Interface

In PWM mode, the LIN terminal can also be used as a PWM interface to the external microcontroller. The level of the PWM signal applied to the LIN terminal will be output as a logic level on the LRX terminal. When operating in PWM mode, the LTX input can be used to pull the PWM signal low in order to indicate a fault to the external ECU. Alternatively, the DIAG output can be connected directly to the LIN terminal to indicate a fault to the external ECU. See Diagnostics section for additional detail.

When the AMT49105 is in the sleep state, the LIN terminal changes to a passive input and the resistance of the pull-up resistor on the LIN terminal increases to approximately 2 MΩ. This ensures that the LIN terminal is unable to affect the LIN bus signal. When IGP = 0, the LIN terminal continues to be monitored in the normal sleep state in order to detect a wake request.

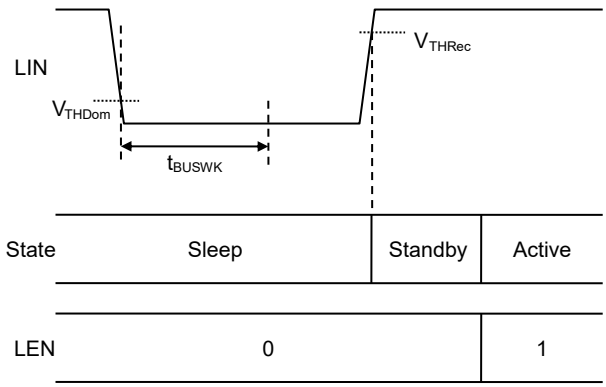

Figure 11a: LIN Wake Sequence and Timing

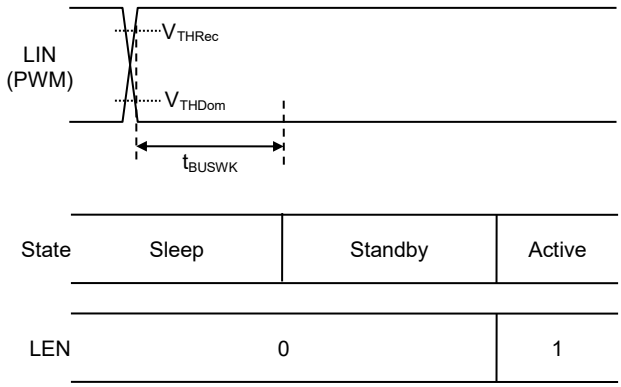

Figure 11b: PWM Wake Sequence and Timing

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Two wake sequence modes are possible, selected by the operating mode.

In LIN mode (OPM = 0), the AMT49105 will wake up according to the LIN protocol. In this mode, the wake request is valid on the first low-to-high transition on the LIN terminal after the LIN terminal is in a dominant (low) state for longer than the wake time, t_{BUSWK}, as shown in Figure 11a. If the LIN terminal changes to recessive (high) within t_{BUSWK}, then the AMT49105 returns to the sleep state.

In PWM mode (OPM = 1), the AMT49105 will wake up on any valid transition of the signal at the LIN terminal. In this mode, the wake signal is valid when the signal on the LIN terminal changes state, high to low or low-to high, and remains in the changed state for longer than the wake time, t_{BUSWK}, as shown in Figure 11b. If the LIN terminal does not remain in the changed state for longer than the wake time, t_{BUSWK}, then the AMT49105 returns to the sleep state.

When a valid wake request is detected on the LIN terminal, with IGP = 0, or the IG terminal transitions from low to high, the AMT49105 will exit the sleep state normally, turn on all regulators and control circuits, and commence operation.

At this time, if the LEN bit is 0, the LIN interface will remain in the standby state where the LIN terminal is a passive input. The LRX output will indicate the state of the LIN terminal but the signal on the LTX terminal is ignored. The LIN interface becomes fully active when LEN is set to 1. If the default value of LEN is 1 then the standby state is bypassed and the LIN interface is fully active as soon as the internal regulators are fully active.

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Gate Drives

The AMT49105 is designed to drive external low on-resistance power N-channel MOSFETs. It will supply the large transient currents necessary to quickly charge and discharge the external MOSFET gate capacitance in order to reduce dissipation in the external MOSFET during switching. The charge current for the low-side drives and the recharge current for the bootstrap capacitors are provided by the capacitor on the VREG terminal. The charge current for the high-side drives is provided by the bootstrap capacitors connected between the Cx and Sx terminal, one for each phase. The MOSFET gate charge and discharge rate can be controlled using an external resistor in series with the connection to the gate of the MOSFET or by selecting the gate drive current and timing using a group of parameters set via the serial interface.

Gate Drive Voltage Regulation

The gate drivers are powered by an integrated programmable voltage regulator which limits the supply to the drivers and therefore the maximum gate voltage. At low supply voltage, the regulated supply is maintained by a charge pump boost converter which requires a pump capacitor, typically 470 nF, connected between the CP1 and CP2 terminals.

The regulated voltage, V_{REG}, can be programmed to 8 or 11 V and is available on the VREG terminal. The voltage level is selected by the value of the VRG bit. When VRG = 1, the voltage is set to 11 V; when VRG = 0, the voltage is set to 8 V. A sufficiently large storage capacitor must be connected to this terminal to provide the transient charging current to the low-side drivers and the bootstrap capacitors (see Layout Recommendations section).

Bootstrap Supply

When a high-side driver is active, the reference voltage, V_{Sx}, will rise close to the bridge supply voltage. The supply to the driver then must be above the bridge supply voltage to ensure that the driver remains active. This temporary high-side supply is provided by bootstrap capacitors, one for each high-side driver. These three bootstrap capacitors are connected between the bootstrap supply terminals, CA,CB, CC, and the corresponding high-side reference terminal, SA, SB, SC.

The bootstrap capacitors are independently charged to approximately V_{REG} when the associated reference terminal, Sx, is low. When the output swings high, the voltage on the bootstrap supply terminal, V_{Cx}, rises with the output to provide the boosted gate voltage needed for the high-side N-channel power MOSFETs.

Bootstrap Charge Management

The AMT49105 monitors the individual bootstrap capacitor charge voltages to ensure sufficient high-side drive. It also includes an optional bootstrap capacitor charge management system (bootstrap manager) to ensure that the bootstrap capacitor remains sufficiently charged under all conditions. The bootstrap manager is enabled by default, but may be disabled by setting the DBM bit to 1. This may be required in systems where the output MOSFET switching must only be allowed by the controlling processor.

Before a high-side drive can be turned on, the bootstrap capacitor voltage must be higher than the turn-on voltage threshold, $V_{BCUV} + V_{BCUVhys}$. If this is not the case, then the AMT49105 will attempt to charge the bootstrap capacitor by activating the complementary low-side drive. Under normal circumstances, this will charge the capacitor above the turn-on voltage in a few microseconds and the high-side drive will then be enabled. The bootstrap voltage monitor remains active while the high-side drive is active, and if the voltage drops below the turn-off voltage threshold, V_{BCUV}, a charge cycle is also initiated.

The bootstrap charge management circuit may actively charge the bootstrap capacitor regularly when the PWM duty cycle is very high, particularly when the PWM off-time is too short to permit the bootstrap capacitor to become sufficiently charged.

In some safety systems, the gate driver is not permitted to turn on a MOSFET without a direct command from the controller. In this case, the bootstrap manager may be disabled by setting the DBM bit to 1. If the bootstrap manager is disabled, then the user must ensure that the bootstrap capacitor does not become discharged below the bootstrap undervoltage threshold, V_{BCUV}, or a bootstrap fault will be indicated and the outputs disabled. This can happen with very high PWM duty cycles when the charge time for the bootstrap capacitor is insufficient to ensure a sufficient recharge to match the MOSFET gate charge transfer during turn on.

If, for any reason, the bootstrap capacitor cannot be sufficiently charged, a bootstrap fault will occur—see Diagnostics section for further details.

Top-Off Charge Pump

An additional “top-off” charge pump is provided for each phase, which will allow the high-side drive to maintain the gate voltage on the external MOSFET indefinitely, ensuring so-called 100% PWM if required. This is a low-current trickle charge pump and is only operated after a high side has been signaled to turn on. There is a small amount of bias current drawn from the Cx ter-

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minal to operate the floating high-side circuit (<40 µA), and the charge pump simply provides enough drive to ensure the bootstrap voltage, and hence the gate voltage, will not drop due to this bias current.

In some applications, a safety resistor is added between the gate and source of each MOSFET in the bridge. When a high-side MOSFET is held in the on-state, the current through the associated high-side gate-source resistor (R_{GSH}) is provided by the high-side driver, and therefore appears as a static resistive load on the top-off charge pump. The minimum value of R_{GSH} for which the top-off charge pump can provide current, without dropping below the bootstrap undervoltage threshold, is defined in the Electrical Characteristics table.

In all cases, the charge required for initial turn-on of the high-side gate is always supplied by the bootstrap capacitor. If the bootstrap capacitor becomes discharged, the top-off charge pump alone will not provide sufficient current to allow the MOSFET to turn on.

High-Side Gate Drive

High-side gate-drive outputs for external N-channel power MOSFETs are provided on terminals GHA, GHB, and GHC. GHx = 1 (or “high”) means that the upper half of the driver is turned on and its drain will source current to the gate of the high-side MOSFET in the external motor-driving bridge, turning it on. GHx = 0 (or “low”) means that the lower half of the driver is turned on and its drain will sink current from the external MOSFET’s gate circuit to the respective Sx terminal, turning it off.

The reference points for the high-side drives are the load phase connections, SA, SB, and SC. These terminals sense the voltages at the load connections. These terminals are also connected to the negative side of the bootstrap capacitors and are the negative supply reference connections for the floating high-side drivers. The discharge current from the high-side MOSFET gate capacitance flows through these connections which should have low-impedance traces to the MOSFET bridge.

MOSFET gate charge and discharge rates may be controlled via the serial interface as detailed in the Gate Drive Control section.

Low-Side Gate Drive

The low-side, gate-drive outputs on GLA, GLB, and GLC are referenced to the corresponding LSSx terminal. These outputs are designed to drive external N-channel power MOSFETs. GLx = 1 (or “high”) means that the upper half of the driver is turned on and its drain will source current to the gate of the low-side MOSFET in the external power bridge, turning it on. GLx = 0 (or “low”) means that the lower half of the driver is turned on and its drain will sink current from the external MOSFET’s gate circuit to the LSSx terminal, turning it off.

The LSSx terminals provide the return paths for discharge of the capacitance on the low-side MOSFET gates. These terminals are connected independently to the common sources of the low-side external MOSFETs through low-impedance tracks.

MOSFET gate charge and discharge rates may be controlled via the serial interface as detailed in the Gate Drive Control section below.

Gate Drive Passive Pull-Down

Each gate drive output includes a discharge circuit to ensure that any external MOSFET connected to the gate drive output is held off when the power is removed. This discharge circuit appears as a variable resistance pull-down, but is not active when the AMT49105 is in normal operating mode. At low gate source voltage, the resistance is approximately 950 kΩ to ensure that any charge accumulated on the MOSFET gate has a discharge path. This resistance reduces rapidly as the voltage increases such that any MOSFET gate that becomes charged by external means is rapidly discharged to below the turn-on threshold. In some applications, this can eliminate the requirement for a permanent external gate source resistor.

Gate Drive Control

In some applications, it may be necessary to limit the rate of change of the voltage at the motor phase connections to help comply with EMC emission requirements. This is usually achieved by controlling the MOSFET gate charge and discharge rates.

The conventional approach is to add an external resistor between the gate drive output and the gate connection to each MOSFET and possibly an additional small value capacitor between the gate and source of the external MOSFET.

In addition to operating in this basic switch mode drive, the AMT49105 gate drive output can be programmed to provide control of the slew rate of the drain-source voltage of the external power MOSFET. This is achieved by controlling the gate sink or source current during the time when the drain-source voltage is changing. This occurs during the Miller region when the gate-drain capacitance of the external MOSFET is being charged or discharged. This capacitance is referred to as the Miller capacitor and the period of time as the Miller time.

MOSFET gate drives are controlled according to the values set in the slew control variables IR1, IR2, IF1, IF2, TRS, and TFS.

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The off-to-on transition is controlled by IR1, IR2, and TRS. The on-to-off transition is controlled by IF1, IF2, and TFS.

There are two gate drive control modes, switched and slew control. All gate drives operate in the same mode.

In switched mode, the gates are driven at the full capability of the pull-up or pull-down switches in the gate drive, as shown in Figure 12b. If both IR1 and IR2 are set to zero, the gate drive operates in full switched mode for the off-to-on transition. If both IF1 and IF2 are set to zero, the gate drive operates in full switched mode for the on-to-off transition. If the dead time is set to zero by setting the DT variable to zero, then the gate drive can only operate in switched mode.

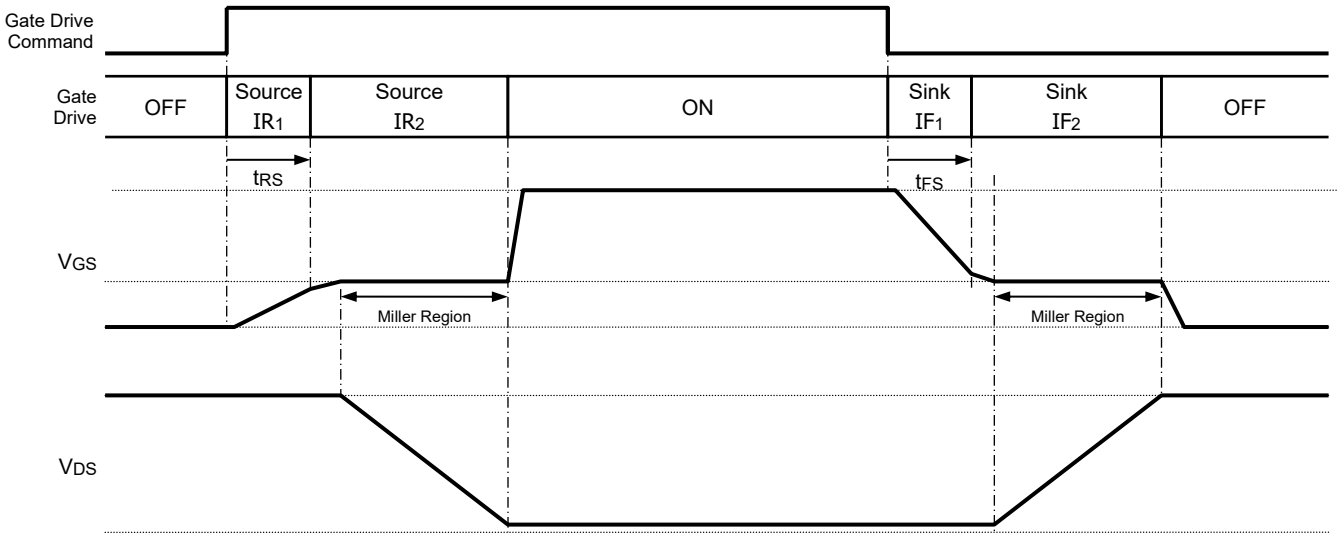

Figure 12a: Off-to-On and On-to-Off Transitions with Gate Drive Control Enabled

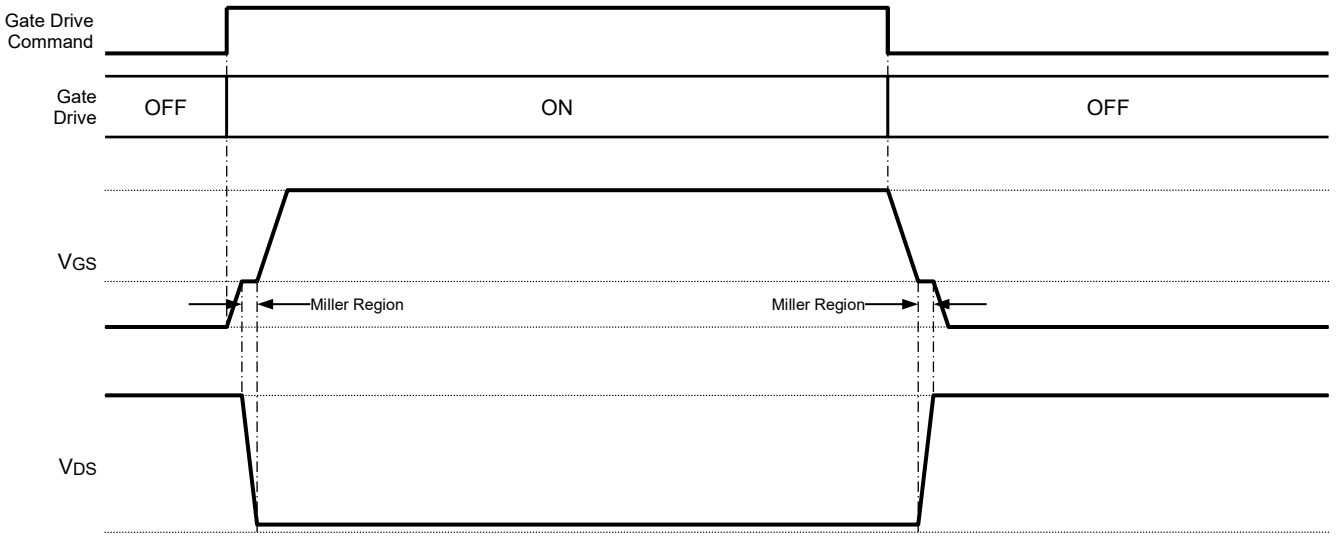

Figure 12b: Off-to-On and On-to-Off Transitions with Gate Drive Control Disabled

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In slew-control mode, the gates are driven using programmable currents to provide some control over the slew rate of the motor phase connection as shown in Figure 12a. To operate in slew-control mode for the off-to-on transition, both IR1 and IR2 must be non-zero. To operate in slew-control mode for the on-to-off transition, both IF1 and IF2 must be non-zero. If any of the drive currents are set to zero, then the output will operate in switched mode for the period of time when that current is active.

The basic principle of the slew rate mode is to drive the gate with a controlled current for a fixed time to quickly get the MOSFET to the Miller region where the drain-source voltage, V_{DS}, starts to change. Then to follow this with a second, usually lower current to control the V_{DS} slew rate. Finally the gate drive changes to switch mode once V_{DS} has completed its transition.

In slew control mode, when a gate drive is commanded to turn on, a current, I_{R1} (defined by IR1[3:0]) is sourced from the relevant gate drive output for a duration, t_{RS} (defined by TRS[3:0]). These parameters should typically be set to quickly charge the MOSFET input capacitance such that the gate-source voltage rises close to the Miller voltage of the MOSFET. The drain-source voltage of the MOSFET will not start to change until the gate-source voltage reaches this level. After this time, the current sourced on the gate drive output is set to a value of I_{R2} (as defined by IR2[3:0]) and remains at this value while the MOSFET transitions through the Miller region. I_{R2} should be selected to achieve the required slew rate of the drain-source voltage by setting the charge time of the drain-gate (Miller) capacitor.

When the MOSFET reaches the fully-on state, the gate drive output changes from current drive to voltage drive to hold the MOSFET in the on state.

A high-side MOSFET is considered to be in the fully-on state when the drain-source voltage, V_{DS} (= $V_{BB} – V_{Sx}$), drops below the programmed V_{DS} threshold voltage, V_{DST}.

A low-side MOSFET is considered to be in the fully-on state when the drain-source voltage, V_{DS} (= $V_{Sx} – V_{GND}$), drops below the programmed V_{DS} threshold voltage, V_{DST}.

When a gate drive is commanded to turn off in slew control mode, a current, I_{F1} (defined by IF1[3:0]) sinks to the relevant gate drive output for a duration, t_{FS} (defined by TFS[3:0]). These parameters should typically be set to quickly discharge the MOSFET input capacitance such that the gate-source voltage drops to close to the Miller voltage of the MOSFET. The drain-source voltage of the MOSFET will not start to change until the gate-source voltage reaches this level. After this time, the current sourced on the gate drive output is set to a value of I_{F2} (as defined by IF2[3:0]) and remains at this value while the MOSFET transitions through the Miller region. I_{F2} should be selected to achieve the required slew rate of the drain-source voltage by setting the discharge time of the drain-gate (Miller) capacitor.

When the MOSFET reaches the fully-off state, the gate drive output changes from current drive to voltage drive to hold the MOSFET in the off state.

A high-side MOSFET is considered to be in the fully-off state when the drain-source voltage of its complementary low-side MOSFET, V_{DS} (= $V_{Sx} – V_{GND}$), drops below the programmed V_{DS} threshold voltage, V_{DST}.

A low-side MOSFET is considered to be in the fully-off state when the drain-source voltage of its complementary high-side MOSFET, V_{DS} (= $V_{BB} – V_{Sx}$), drops below the programmed V_{DS} threshold voltage, V_{DST}.

Dead Time

To prevent shoot through (transient cross-conduction) in any phase of the power MOSFET bridge, it is necessary to have a dead-time delay between a high- or low-side turn off and the next complementary turn-on event. The potential for cross-conduction occurs when any complementary high-side and low-side pair of MOSFETs is switched at the same time, for example, at the PWM switch point. In the AMT49105, the dead time for all three phases is set by the contents of the DT[5:0] bits. These six bits contain a positive integer that determines the dead time by division from the system clock.

The dead time is defined as:

$$t_{DEAD} = n \times 50\ ns$$

where n is a positive integer defined by DT[5:0] and t_{DEAD} has a minimum active value of 100 ns.

For example, when

DT[5:0] contains [01 1000] (= 24 in decimal),

then t_{DEAD} = 1.2 µs, typically.

The accuracy of t_{DEAD} is determined by the accuracy of the system clock as defined in the Electrical Characteristics table. The range of t_{DEAD} is 100 ns to 3.15 µs. A value of 1 or 2 in DT[5:0] sets the minimum active dead time of 100 ns.

If DT[5:0] is set to zero, the dead timer is disabled and no minimum dead time is generated by the AMT49105. The logic that prevents permanent cross-conduction is, however, still active. Adequate dead time must be generated externally by, for

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example, the microcontroller producing the drive signals applied to the AMT49105 logic inputs or control register. When the dead time is set to zero, the gate drive slew control is disabled and the gate drive output operates only in switched mode.

The value of the dead time should be selected such that the gate-source voltage of any pair of complementary MOSFETs is never above the threshold voltage for both MOSFET at the same time as shown in Figure 13. This applies in either the slew control mode or the switch mode. In the slew control mode, the dead time must be increased to accommodate the extended switching times.

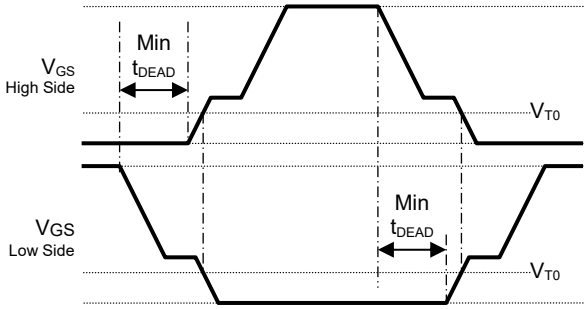

Figure 13: Minimum Dead Time

The internally generated dead time is only present if the on command for one MOSFET occurs within one dead time after the off command for its complementary partner. In the case where one side of a phase drive is permanently off, for example when using diode rectification with slow decay, then the dead time does not occur. In this case, the gate drive turns on within the specified propagation delay after the corresponding phase input goes high. (See Figure 5).

Logic Control Inputs

Six logic level digital inputs, HA, LA, HB, LB, HC, LC, provide direct control for the gate drives, one for each drive. The Hx inputs correspond to the high-side drives and the Lx inputs correspond to the low-side drives. All logic inputs are standard CMOS levels referenced to the voltage of the logic I/O regulator, V_{IO}. Logic inputs have a typical hysteresis of 550 mV to improve noise performance.

The operation of the inputs are shown in the Control Logic Table of Table 1. A pull-down resistor is connected to each input to ensure a safe state if the control becomes disconnected.

The gate drive outputs can also be controlled through the serial interface by setting the appropriate bit in the control register. In the control register, all bits are active high. The logical relationship between the register bit setting and the gate drive outputs is defined in Table 2.

The logic inputs are combined, using logical OR, with the corresponding bits in the serial interface control register to determine the state of the gate drive. The logical relationship between the combination of logic input and register bit setting and the gate drive outputs is defined in Table 3. In most applications, either the logic inputs or the serial control will be used. When using only the logic inputs to control the bridge, the serial register should be left in the reset condition with all control bits set to 0. When using only the serial interface to control the bridge, the inputs should be connected to GND. The internal pull-down resistors on these inputs then ensure that they go to the inactive state should they become disconnected from the control signal level.

Internal lockout logic ensures that the high-side gate drive output and low-side gate drive output drive on the same phase cannot be active (high) simultaneously. If the control inputs request both the high-side and the low-side gate drives to be active at the same time, then both high-side and low-side gate drives are switched into the inactive (low) state.

Output Enable / Disable

The ENABLE input can be configured to operate as a direct logic level output control or as a time-qualified output control.

When the ETO mask bit is set to 1, ENABLE is connected directly to the gate drive output command signal, bypassing the main synchronous logic block on the chip (including all phase control logic). This input can be used to provide a fast output disable (emergency cutoff) or to provide nonsynchronous fast decay PWM.

When ETO = 0, the transitions on ENABLE are monitored by a timer. In this mode, the signal is routed through the synchronous logic block on the chip before connecting to the gate drive output command signal. The first change of state on the ENABLE input will activate the gate drive outputs under command from the corresponding phase control signals and a timer is started. The ENABLE input must then change state before the end of the ENABLE timeout period, t_{ETO}. If the ENABLE input does not change before the end of the timeout period and ESF = 1, then all gate drive outputs will be driven low and the ETO bit will be set in the Status register. Any following change of state on the ENABLE input will reactivate the gate drive outputs and reset the fault. If ESF = 0, then the outputs are not affected. The ETO bit remains in the Status register until reset.

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Bridge Switch

A switched version of the bridge voltage is available on the BRSW terminal. The switch is always off when the AMT49105 is in the sleep state to remove any conduction path that may be introduced by an external resistor divider between the BRSW and GND terminals. The switch can also be switched off by setting the BRS bit to 0.

BEMF Zero Crossing Multiplex Output

The voltage on the Sx terminal for each phase is compared to a common "center tap" voltage, V_{CT}, generated by the average of the three phase voltages defined as:

$$V_{CT} = (V_{SA} + V_{SB} + V_{SC}) / 3$$

The output from each comparator is fed to a debounce filter with a programmable filter time set by the contents of the BF[3:0] bits. This ensures that any noise at the switching point of each BEMF comparator is filtered to give a clean edge on the output.

The signal output on the BXM terminal is selected by the BXM[2:0] variable as follows:

BXM2	BXM1	BXM0	BXM output
0	0	0	FG speed signal which is the exclusive OR of all three phases.
0	0	1	Phase A comparator output.
0	1	0	Phase B comparator output.
0	1	1	Phase C comparator output.
1	X	X	Output driven low.

Figure 14 provides a functional diagram and Figure 15 shows the output options for a normal motor rotation when the gate drive outputs are disabled and the motor is not being driven. The DIRO bit in the Verification register reports the motor direction. When the motor is being driven, the BXM output can be set low to avoid any unnecessary switching noise.

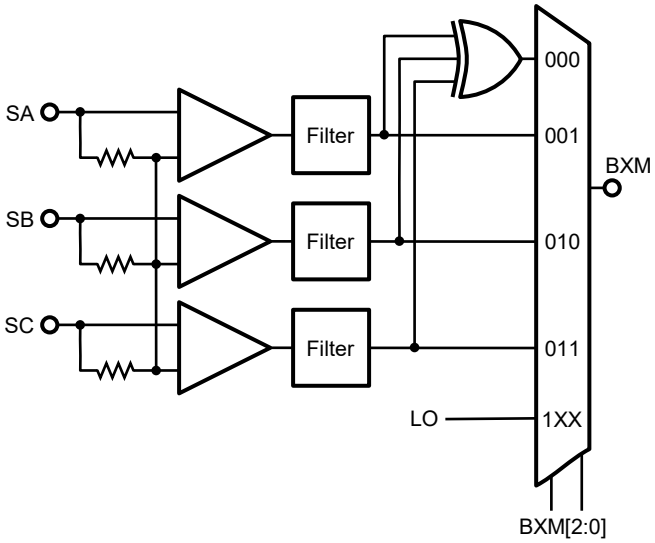

Figure 14: BEMF Detection Multiplexer Diagram

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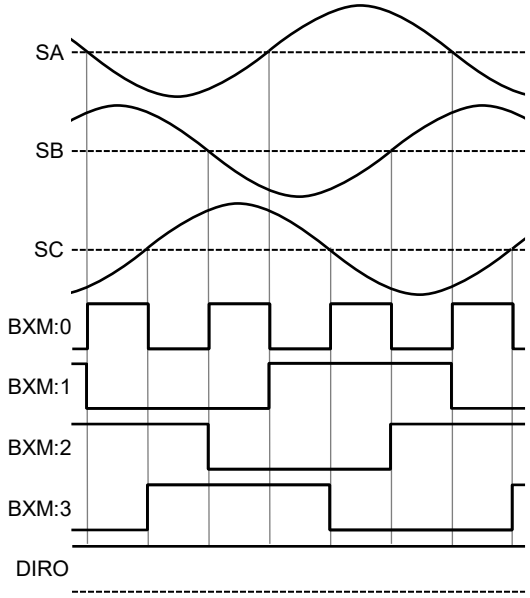

Figure 15a: BEMF Multiplexer Output Selection (DIRO = 1)

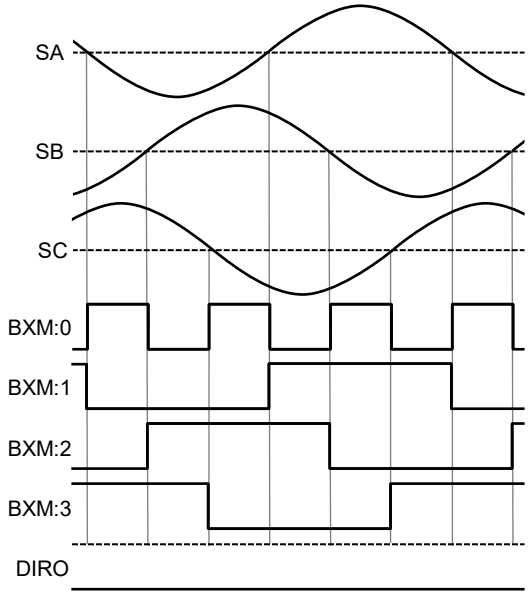

Figure 15b: BEMF Multiplexer Output Selection (DIRO = 0)

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Current Sense Amplifiers

A programmable-gain/programmable-offset differential sense amplifier is provided to allow the use of a low-value sense resistor or current shunt as a current sensing element in connection between the common source connections of the low-side MOSFETS to ground. The input common mode range of the CSP and CSM inputs allows below-ground current sensing typically required for low-side current sense in PWM control of motors or other inductive loads during switching transients. The output of the sense amplifier is available at the CSO output and can be used in peak or average current control systems. The output can drive up to 4.8 V to permit maximum dynamic range with higher input voltage A-to-D converters. Maximum output voltage is clamped to V_{CSC} as defined in the Electrical Characteristics table.

The gain, A_V, of the sense amplifier is programmable and defined by the contents of the SG[2:0] variable as:

SxG	Gain
0	10
1	15
2	20
3	25

SxG	Gain
4	30
5	35
6	40
7	50

The output offset of all three sense amplifiers, V_{OOS}, is defined by the contents of the SAO[3:0] variable as:

SAO	V_{OS}
0	0
1	0
2	100 mV
3	100 mV
4	200 mV
5	300 mV
6	400 mV
7	500 mV

SAO	V_{OS}
8	750 mV
9	1 V
10	1.25 V
11	1.5 V
12	1.65 V
13	2 V
14	2.25 V
15	2.5 V

Equations describing the relationship between sense amplifier gain and output offset are shown in Figure 3.

To achieve the sense amplifier Input Offset Voltage, V_{IOS}, limits detailed in the Electrical Characteristics table, the amplifier must be calibrated and output offset uncertainty must be eliminated.

Current sense amplifier calibration is initiated via the serial interface. Amplifiers are calibrated by writing a 1 to the SAC bit. If the SAC bit is already set to 1, it must first be cleared to 0 before writing 1, otherwise a calibration cycle will not take place. Before initiating a calibration, the OSO bit must be set to 0 and the relevant positive and negative amplifier input terminals (CSP and CSM) must be held at the same potential by ensuring that no current is flowing in the sense resistor. This condition must be maintained until the calibration operation is complete. Calibration starts on the STRn rising edge associated by writing 1 to the SAC bit and is completed within an Offset Calibration Time, t_{Cal}, from this point. After calibration, the amplifier automatically reverts to normal operating mode. During calibration, transient voltage variations may be observed on the CSO terminal.

Calibration is not required to achieve the specified Input Offset Voltage Drift, ΔV_{IOS}, and leaves this parameter unaltered.

Output offset uncertainty is eliminated by carrying out a two-stage voltage measurement on the CSO terminal. First, the OSO bit is set to 0 to make the combined current sense signal plus output offset available on CSO, and this is measured as $V_{CSO(1)} = V_{CSD} + V_{OOS}$. Secondly, the OSO bit is set to 1 to make only the output offset voltage available on CSO, and this is measured as $V_{CSO(2)} = V_{OOS}$. The actual current sense signal is then determined by calculating the difference between the two measurements as follows:

$$V_{CSO(1)} - V_{CSO(2)} = (V_{CSD} + V_{OOS}) - V_{OOS}$$

$$V_{CSO(1)} - V_{CSO(2)} = V_{CSD}$$

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Diagnostics

Multiple diagnostic features provide fault monitoring for basic chip status and for the state of the external bridge. Most of the non-critical diagnostics can be masked by setting the appropriate bit in the mask register. The detectable faults are listed in Table 5. The fault status is available through the serial interface or through the DIAG output.

Serial Status Register

The serial interface allows detailed diagnostic information to be read from the Status register at any time.

Table 5: Diagnostic Functions

Name	Diagnostic	Level
POR	Internal logic supply undervoltage causing power-on reset	Chip
OT	Chip junction overtemperature	Chip
SE	Serial transmission error	Chip
EE	EEPROM error	Chip
VBU	VBB supply undervoltage	Monitor
VRU	VREG output undervoltage	Monitor
VLRU	External supply regulator undervoltage	Monitor
VIOU	Logic I/O regulator undervoltage	Monitor
TW	High chip junction temperature warning	Monitor
WD	Microcontroller window watchdog	Monitor
ETO	ENABLE watchdog timeout	Monitor
OC	Overcurrent	Bridge
VA	Bootstrap undervoltage phase A	Bridge
VB	Bootstrap undervoltage phase B	Bridge
VC	Bootstrap undervoltage phase C	Bridge
AHO	Phase A high-side VDS overvoltage	Bridge
ALO	Phase A low-side VDS overvoltage	Bridge
BHO	Phase B high-side VDS overvoltage	Bridge
BLO	Phase B low-side VDS overvoltage	Bridge
CHO	Phase C high-side VDS overvoltage	Bridge
CLO	Phase C low-side VDS overvoltage	Bridge

The first bit (bit 15) of the Status register contains a common fault flag, FF, which will be high if any of the fault bits in the registers have been set. This allows fault condition to be detected using the serial interface by simply taking STRn low. As soon as STRn goes low, the first bit in the Status register can be read to determine if a fault has been detected at any time since the last Status or Diagnostic register reset. In all cases, the fault bits in the diagnostic registers are latched and only cleared after the associated fault bit is read through the serial interface with DSR = 0. When DSR = 1, no fault bits or states are reset.

Note that FF (bit 15) does not provide the same function as the general fault flag output on the DIAG terminal in the default mode. The fault output on the DIAG terminal provides an indication that either a fault is present or the outputs have been disabled due to a latched fault state. FF provides an indication that a fault has occurred since the last fault reset and one or more fault bits have been set.

Diagnostic Registers

The diagnostic registers provide additional details of any V_{DS} overvoltage, bootstrap undervoltage, or supply undervoltage faults. The status and diagnostic registers are described further in the serial interface section description below.

DIAG Diagnostic Output

The DIAG terminal is a single diagnostic output signal that can be programmed by setting the contents of the DG[1:0] variable through the serial interface to provide one of four dedicated diagnostic signals:

DG = 0, a general fault flag

DG = 1, a pulsed fault flag

DG = 2, a general fault flag

DG = 3, a clock signal derived from the internal chip clock

The general fault flag output option provides a fault flag that remains low while the fault is present or if one of the latched faults has been detected and the outputs disabled. When the general fault flag is reset, the DIAG output will be high.

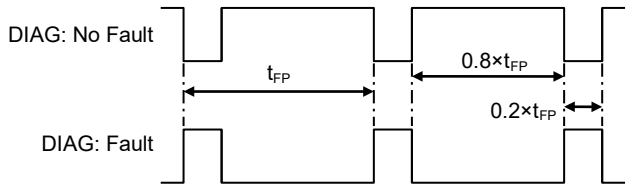

Figure 16: DIAG – Pulsed Output Mode

The pulsed fault output option provides a continuous, low-frequency, low-duty cycle pulsed output when a fault is present or if one of the latched faults has been detected and the outputs disabled. When the general fault flag is reset and no fault is present, the signal output on the DIAG terminal is continuous, low-frequency, high-duty cycle pulses. The period of the DIAG signal

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in pulsed mode is defined by t_{FP} and is typically 100 ms. The two duty cycles are defined by DFP and are typically 20% when a fault is present and 80% when no fault is present.

DIAG is an open drain output. On-state drive capability and off-state leakage current limits are defined in the Electrical Characteristics table by the V_{OL} and I_{ODI} parameters respectively and may be used to calculate a suitable pull-up resistance. In the majority of applications, a resistor in the range 10 to 20 kΩ is acceptable.

Chip-Level Diagnostics

Chip-wide parameters critical for correct operation of the AMT49105 are monitored. These include maximum chip temperature, minimum internal logic supply voltage, EEPROM data integrity, and the serial interface transmission. These four monitors are necessary to ensure that the AMT49105 is able to respond as specified.

Chip Fault State: Internal Logic Undervoltage (POR)

The AMT49105 has an independent integrated logic regulator to supply the internal logic. This ensures that external events other than loss of supply do not prevent the AMT49105 from operating correctly. The internal logic supply regulator will continue to operate with a low supply voltage, for example, if the main supply voltage drops to a very low value during a severe cold crank event. In extreme low supply voltage circumstances, or during power-up or power-down, an undervoltage detector ensures that the AMT49105 operates correctly. The logic supply undervoltage lockout cannot be masked as it is essential to guarantee correct operation over the full supply range.

When power is first applied to the AMT49105, the internal logic is prevented from operating, and all gate drive outputs held in the off state until the internal regulator voltage, V_{DD}, exceeds the logic supply undervoltage lockout threshold, derived from V_{BBR}. At this point, all serial control registers will be reset to their power-on state and all fault states and the general fault flag will be reset. The FF bit and the POR bit in the Status register will be set to one to indicate that a power-on-reset has taken place. The AMT49105 then goes into its fully operational state and begins operating as specified. In general, the VBU, VRU, VLRU, and VIOU bits may also be set following a power-on-reset as the regulators may not have reached their respective rising undervoltage thresholds until after the register reset is completed.

Following a power-on-reset, the logic inputs will be forced to their inactive state until V_{IO} rises above the rising undervoltage threshold, V_{IOON}.

When V_{LR} rises above the rising undervoltage threshold, V_{LRON}, there are two possible sequences depending on the state of the WD mask bit.

If the WD mask bit is 0, i.e. watchdog is active, the MRSTn output will remain low for 10 ms after the external logic supply, V_{LR}, rises above the rising undervoltage threshold, V_{LRON}. After 10 ms, MRSTn will go high and the watchdog timer will be reset. The watchdog timer will remain reset for 100 ms during which time the WDOG input will be ignored. The gate drive outputs will remain disabled until the first valid watchdog is detected.

If the WD mask bit is 1, i.e. watchdog is inactive, the MRSTn output will remain low for 10 ms, after the external logic supply, V_{LR}, rises above the rising undervoltage threshold, V_{LRON}. The gate drive outputs can be activated 10 ms after MRSTn goes high. A valid serial transfer will immediately terminate this timeout, set MRSTn high, and allow the gate drive outputs to be activated. The VLRU fault bit remains in the Diagnostic register until cleared.

Once the AMT49105 is operational, the internal logic supply continues to be monitored. If, during the operational state, V_{DD} drops below logic supply undervoltage lockout threshold, derived from V_{BBR}, then the logical function of the AMT49105 cannot be guaranteed and the outputs will be immediately disabled. The AMT49105 will enter a power-down state and all internal activity, other than the logic regulator voltage monitor will be suspended. If the logic supply undervoltage is a transient event, then the AMT49105 will follow the power-up sequence above as the voltage rises.

Chip Fault State: Overtemperature

If the chip temperature rises above the over temperature threshold, T_{JF}, the general fault flag will be active and the overtemperature bit, OT, will be set in the Status register. If ESF = 1 when an overtemperature is detected, all gate drive outputs will be disabled, the VLR regulator is shut down, and MRSTn will go low. All AMT49105 functions other than the regulator remain active. When T_J drops by more than the overtemperature threshold ($T_J < T_{JF} - T_{Jhys}$), there are two possible sequences depending on the state of the WD mask bit.

If the WD mask bit is 0, i.e. watchdog is active, the VLR regulator will be re-enabled when T_J drops by more than the overtem-

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perature threshold ($T_J < T_{JF} – T_{Jhys}$). MRSTn will remain low for 10 ms after V_{LR} rises above the rising undervoltage threshold, V_{LRON}. After 10 ms, MRSTn will go high and the watchdog timer will be reset. The watchdog timer will remain reset for 100 ms during which time the WDOG input will be ignored. The gate drive outputs will remain disabled until the first valid watchdog is detected.

If the WD mask bit is 1, i.e. watchdog is inactive, the VLR regulator will be re-enabled when T_J drops by more than the overtemperature threshold ($T_J < T_{JF} – T_{Jhys}$). MRSTn will remain low for 10 ms after V_{LR} rises above the rising undervoltage threshold, V_{LRON}. The gate drive outputs can be activated 10 ms after MRSTn goes high. A valid serial transfer will immediately terminate this timeout, set MRSTn high, and allow the gate drive outputs to be activated.

If ESF = 0 when an overtemperature is detected, no circuitry will be disabled and action must be taken by the user to limit the power dissipation in some way so as to prevent overtemperature damage to the chip and unpredictable device operation.

In both cases, the overtemperature bit, OT, remains latched in the Status register until reset.

Chip Fault State: Serial Error

If there are more than 16 rising edges on SCK, or if STRn goes high and there are fewer than 16 rising edges on SCK, or the parity is not odd, or a NVM save sequence is in progress, then the transfer will be cancelled. No data will be written to the registers. In addition, the Status register will not be reset and the SE bit will be set to indicate a data transfer error. If the transfer is a write, then the Status register will not be reset. If the transfer is a diagnostic or verification result read, then the addressed register will not be reset.

Chip Fault State: EEPROM

Configuration and calibration information is stored within internal EEPROM and loaded into working registers to configure the device at power up. As part of this process, a data integrity check is carried out. If the check returns a single bit error, automatic error correction is applied and the part starts up. If the check returns a multiple bit error, all gate drives are disabled, the general fault flag is set low and the EEPROM error bit, EE, is set in the Status register. EEPROM faults can only be cleared by a power-on-reset (POR).

Operational Monitors

Parameters related to the safe operation of the AMT49105 in a system are monitored. These include parameters associated with external active and passive components, power supplies, and interaction with external controllers.

Voltages relating to driving the external power MOSFETs are monitored, specifically V_{REG}, and each bootstrap capacitor voltage. The main supply voltage, V_{BB}, is monitored for undervoltage events.

In addition, a watchdog timer can be applied to the ENABLE input to verify continued operation of the external controller.

Monitor: V_{BB} Supply Undervoltage

The main supply to the AMT49105 on the VBB terminal, V_{BB}, is monitored to indicate if the supply voltage has dropped below its normal operating range (for example, during a load dump event).

The V_{BB} undervoltage lockout threshold value is set according to the state of the VLR bit.

If V_{BB} falls below the V_{BB} undervoltage lockout threshold, V_{BBUV}, then the VBU bit will be set in the Diagnostic register and VSU bit (which indicates the logical OR of the VBU and VRU bits) will be set in the Status register. The general fault flag will be set and if ESF = 1 all gate drive outputs will be driven low. If VRS = 0, the VREG regulator will be disabled. If VLS = 0, the VLR regulator will be disabled.

When V_{BB} moves above the rising V_{BB} undervoltage threshold, $V_{BBUV} + V_{BBhys}$, the gate drive outputs, VLR regulator, and VREG regulator will be re-enabled. The general fault flag will be cleared but the VBU and VSU bits will remain set until the Diagnostic register is reset.

If ESF = 0, the gate drive outputs will not be disabled. If VRS = 1, the VREG regulator will remain enabled. If VLS = 1, the VLR regulator will remain enabled.

Monitor: V_{REG} Undervoltage

The internal charge-pump regulator supplies the low-side gate driver and the bootstrap charge current. It is critical to ensure that the regulated voltage, V_{REG}, at the VREG terminal is sufficiently high before enabling any of the outputs.

If V_{REG} goes below the V_{REG} undervoltage threshold, V_{ROFF}, the general fault flag will be active, the V_{REG} undervoltage bit, VRU, will be set in the Diagnostic register, and all gate drive outputs will go low. When V_{REG} rises above the rising threshold, V_{RON},

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the gate drive outputs are re-enabled and the general fault flag is cleared. The fault bit remains in the Diagnostic register until cleared.

The V_{REG} undervoltage monitor circuit is active during power-up. The general fault flag will be active and all gate drives will be low until V_{REG} is greater than V_{RON}. Note that this is sufficient to turn on standard threshold external power MOSFETs at a battery voltage as low as 5.5 V, but the on-resistance of the MOSFET may be higher than its specified maximum.

The V_{REG} undervoltage monitor can be disabled by setting the VRU bit in the Mask register. Although not recommended, this can allow the AMT49105 to operate below its minimum specified supply voltage level with a severely impaired gate drive. The specified electrical parameters will not be valid in this condition.

Monitor: V_{LR} Undervoltage

The voltage at the VLR terminal, V_{LR}, is monitored to ensure that the supply for any external controller is high enough to permit correct operation of the controller. If V_{LR} drops below the falling undervoltage threshold, V_{LROFF}, the regulator undervoltage bit, VLRU, will be set in the Diagnostic register and the MRSTn output will go low to reset the external microcontroller. If ESF = 1, all gate drive outputs will be disabled. Setting VLRU in the Diagnostic register will also set the VLU bit in the Status register.

When V_{LR} rises above the rising undervoltage threshold, V_{LRON}, there are two possible sequences depending on the state of the WD mask bit.

If the WD mask bit is 0, i.e. watchdog is active, the MRSTn output will remain low for 10 ms after the external logic supply, V_{LR}, rises above the rising undervoltage threshold, V_{LRON}. After 10 ms MRSTn will go high and the watchdog timer will be reset. The watchdog timer will remain reset for 100 ms during which time the WDOG input will be ignored. The gate drive outputs will remain disabled until the first valid watchdog is detected.

If the WD mask bit is 1, i.e. watchdog is inactive, the MRSTn output will remain low for 10 ms, after the external logic supply, V_{LR}, rises above the rising undervoltage threshold, V_{LRON}. The gate drive outputs can be activated 10 ms after MRSTn goes high. A valid serial transfer will immediately terminate this timeout, set MRSTn high, and allow the gate drive outputs to be activated. The VLRU fault bit remains in the Diagnostic register until cleared.

Monitor: V_{IO} Undervoltage

The logic I/O voltage, V_{IO}, is monitored to ensure that the logic interface voltage is high enough to permit correct operation of the logic input buffers. If V_{IO} drops below the falling undervoltage threshold, V_{IOOFF}, the logic inputs are forced to their inactive state, all gate drive outputs will go low, and the regulator undervoltage bit, VIOU, is set in the diagnostic register which will also set the VLU bit in the status register.

When V_{IO} rises above the rising undervoltage threshold, V_{IOON}, the logic inputs are always re-enabled. The gate drive outputs will remain low for 10 ms or until the first valid serial transfer. After this timeout, the gate drive outputs will revert to the commanded state. The VIOU fault bit remains in the diagnostic register until cleared.

Monitor: Temperature Warning

If the chip temperature rises above the temperature warning threshold, T_{JW}, the general fault flag will be active and the hot warning bit, TW, will be set in the Status register. No action will be taken by the AMT49105. When the temperature drops below T_{JW} by more than the hysteresis value, T_{JWhys}, the general fault flag is reset, but the TW bit remains in the Status register until reset.

Monitor: Microcontroller Watchdog

The programmable window watchdog can be used to determine if an external microcontroller is operating in an adverse state. When a watchdog fault is detected, the fault state is latched, the WD bit is set in the Status register, and the MRSTn output goes active low for 10 ms in order to reset the microcontroller. When MRSTn goes high after the 10 ms low period, the watchdog timer will be reset and remain reset for 100 ms. The fault state is cleared and the AMT49105 will re-enable the gate drive outputs on the first valid watchdog transition after the 100 ms timeout. The WD fault bit remains set until cleared. Further details of the microcontroller watchdog operation are provided in the Microcontroller Reset and Watchdog section above.

Monitor: ENABLE Timeout

The ENABLE input provides a direct connection to all gate drive outputs and can be used as a safety override to immediately disable the outputs. The ENABLE input can be programmed to operate as a direct logic control by setting the ETO mask bit to 1 or can be monitored by a watchdog timer by setting ETO to 0. In the direct mode, the input is not monitored. In the timed mode, the first change of state on the ENABLE input will activate the gate drive outputs under command from the corresponding phase control signals and a timer is started. The ENABLE input must then change state before the end of the ENABLE timeout period, t_{ETO}. If the ENABLE input does not change before the end of

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the timeout period, then all gate drive outputs will be driven low, the ETO bit will be set in the Status register, and the general fault flag will be active. Any following change of state on the ENABLE input will re-activate the gate drive outputs and reset the general fault flag. The ETO bit remains in the Status register until reset.

Monitor: IG Input

The state of the IG input is provided directly in the status register as the IG bit. This bit has no effect on the general fault flag output on DIAG or on the state of the FF bit.

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Power Bridge Faults

Bridge: Overcurrent Detect

The output from the sense amplifier is fed into a comparator referenced to the overcurrent threshold voltage, V_{OCT}, to provide indication of overcurrent events. V_{OCT}, is generated by a 4-bit DAC with a resolution of 200 mV and defined by the contents of the OCT[3:0] variable. V_{OCT} is approximately defined as:

$$V_{OCT} = (n + 1) \times 200 \text{ mV}$$

where n is a positive integer defined by OCT[3:0].

Any offset programmed on SAO[3:0] is applied to both the current sense amplifier output and the V_{OCT} threshold and has no effect on the overcurrent threshold, I_{OCT}. In effect, V_{CSD} is compared with V_{OCT} and the relationship between the threshold voltage and threshold current is given by:

$$I_{OCT} = V_{OCT} / (R_S \times A_V)$$

where V_{OCT} is the overcurrent threshold voltage programmed by OCT[3:0], I_{OCT} is the corresponding current value, R_S is the sense resistor value in Ω, and A_V is the sense amplifier gain defined by SAG[2:0].

The output from the overcurrent comparator is filtered by an overcurrent qualifier circuit. This circuit uses a timer to verify that the output from the comparator is indicating a valid overcurrent event. The qualifier can operate in one of two ways, debounce or blanking, selected by the OCQ bit.

In the default debounce mode, a timer is started each time a comparator output indicates an overcurrent detection. This timer is reset when the comparator changes back to indicate normal operation. If the debounce timer reaches the end of the timeout period, set by t_{OCQ}, then the overcurrent event is considered valid and the overcurrent bit, OC, will be set in the Status register.

In the optional blanking mode, a timer is started when any gate drive is turned on or turned off. The output from the comparators is ignored (blanked) for the duration of the timeout period, set by t_{OCQ}. If the comparator output indicates an overcurrent event when the blanking timer is not active, then the overcurrent event is considered valid and the overcurrent bit will be set in the Status register. If any gate drive changes state when a timeout period is in progress, the timeout will be extended to run for a period of t_{OCQ} from the new switching event.

The duration of the overcurrent qualifying timer, t_{OCQ}, is determined by the contents of the TOC[3:0] variable. t_{OCQ} is approximately defined as:

$$t_{OCQ} = n \times 500 \text{ ns}$$

where n is a positive integer defined by TOC[3:0].

When a valid overcurrent is detected, the general fault flag will be active and the associated fault bit, OC, will be set in the Status register. When the overcurrent condition is removed, the general fault flag will go inactive. The OC bit will remain in the Status register until reset.

The overcurrent monitor can be disabled by setting the OC bit in the Mask register.

Bridge: Bootstrap Capacitor Undervoltage Fault

The AMT49105 monitors the individual bootstrap capacitor charge voltages to ensure sufficient high-side drive. It also includes an optional bootstrap capacitor charge management system (bootstrap manager) to ensure that the bootstrap capacitor remains sufficiently charged under all conditions. The bootstrap manager is active by default, but may be disabled by setting the DBM bit to 1. This may be required in systems where the output MOSFET switching must only be allowed by the controlling processor.

If the bootstrap manager is disabled, then the user must ensure that the bootstrap capacitor does not become discharged below the bootstrap undervoltage threshold, V_{BCUV}, or a bootstrap fault will be indicated and the outputs disabled. This can happen with very high PWM duty cycles when the charge time for the bootstrap capacitor is insufficient to ensure a sufficient recharge to match the MOSFET gate charge transfer during turn on.

When the bootstrap manager is active, the bootstrap capacitor voltage must be higher than the turn-on voltage limit before a high-side drive can be turned on. If this is not the case, then the AMT49105 will attempt to charge the bootstrap capacitor by activating the complementary low-side drive. Under normal circumstances, this will charge the capacitor above the turn-on voltage in a few microseconds and the high-side drive will then be enabled. The bootstrap voltage monitor remains active while the high-side drive is active, and if the voltage drops below the turn-off voltage, a charge cycle is also initiated.

If there is a fault that prevents the bootstrap capacitor from charging during the managed recharge cycle, then the charge cycle will timeout after typically 200 µs and the bootstrap undervoltage fault is considered to be valid. If the bootstrap manager is disabled and a bootstrap undervoltage is detected when a high-side MOSFET is active or being switched on, then the bootstrap undervoltage is immediately valid.

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The action taken when a valid bootstrap undervoltage fault is detected and the fault reset conditions depend on the state of the ESF bit.

If ESF = 0, the fault state will be latched, the general fault flag will be active, the associated bootstrap undervoltage fault bit (VA, VB, VC) will be set in the Diagnostic 1 register, and the associated MOSFET will be disabled. The fault state and the general fault flag, but not the bootstrap undervoltage fault bit, will be reset the next time the MOSFET is commanded to switch on. If the MOSFET is being driven with a PWM signal, then this will usually mean that the MOSFET will be turned on again each PWM cycle. If this is the case, and the fault conditions remain, then a valid fault will again be detected after the timeout period and the sequence will repeat. In this case, the general fault flag will only be reset for the duration of the validation timer. The bootstrap undervoltage fault bit will only be reset by a serial read of the Diagnostic register or by a power-on reset.

If ESF = 1, the fault will be latched, the general fault flag will be active, the associated bootstrap undervoltage fault bit (VA, VB, VC) will be set in the Diagnostic register, and all MOSFETs will be disabled. The fault state, bootstrap undervoltage fault bit, and the general fault flag will only be reset by a serial read of the Diagnostic register with DSR = 0 or by a power-on reset.

The bootstrap undervoltage monitor can be disabled for all phases by setting the BSU bit in the Mask register. Although not recommended, this can allow the AMT49105 to operate below its minimum specified supply voltage level with a severely impaired gate drive. The specified electrical parameters may not be valid in this condition.

Bridge: MOSFET V_{DS} Overvoltage Fault

Faults on any external MOSFETs are determined by monitoring the drain-source voltage of the MOSFET and comparing it to a drain-source overvoltage threshold. The threshold, V_{DST}, is generated by an internal DAC and is defined by the values in the VT[5:0] variable. This variables provides the input to a 6-bit DAC with a least significant bit value of typically 50 mV. The output of the DAC produces the threshold voltage approximately defined as:

$$V_{DST} = n \times 50 \text{ mV}$$

where n is a positive integer defined by VT[5:0],

The low-side drain-source voltage for any MOSFET is measured between the adjacent Sx terminal and the adjacent LSSx terminal. Using the LSS terminal rather than the ground connection avoids adding any low-side current sense voltage to the real low-side drain-source voltage and avoids false V_{DS} fault detection.

The high-side drain-source voltage for any MOSFET is measured between the adjacent Sx terminal and the VBRG terminal. Using the VBRG terminal rather than the VBB avoids adding any reverse diode voltage or high-side current sense voltage to the real high-side drain-source voltage and avoids false V_{DS} fault detection.

The VBRG terminal is an independent low-current sense input to the top of the MOSFET bridge. It should be connected independently and directly to the common connection point for the drains of the power bridge MOSFETs at the positive supply connection point in the bridge. The input current to the VBRG terminal is proportional to the drain-source threshold voltage, V_{DSTH}, and is approximately:

$$I_{VBRG} = (0.84 \times V_{BRG}) + (20 \times V_{DST}) + 107$$

where I_{VBRG} is the current into the VBRG terminal in µA and V_{DST} is the drain-source threshold voltage described above.

Note that the VBRG terminal can withstand a negative voltage up to –5 V. This allows the terminal to remain connected directly to the top of the power bridge during negative transients where the body diodes of the power MOSFETs are used to clamp the negative transient. The same applies to the more extreme case where the MOSFET body diodes are used to clamp a reverse battery connection.

The output from each V_{DS} overvoltage comparator is filtered by a V_{DS} fault qualifier circuit. This circuit uses a timer to verify that the output from the comparator is indicating a valid V_{DS} fault. The duration of the V_{DS} fault qualifying timer, t_{VDQ}, is determined by the contents of the VQT[5:0] variable. t_{VDQ} is approximately defined as:

$$t_{VDQ} = n \times 100 \text{ ns}$$

where n is a positive integer defined by VQT[5:0].

The qualifier can operate in one of two ways, debounce mode, or blanking mode, selected by the VDQ bit.

In debounce mode (the default setting), a timer is started each time the comparator output indicates a V_{DS} fault detection when the corresponding MOSFET is active. This timer is reset when the comparator changes back to indicate normal operation. If the debounce timer reaches the end of the timeout period, set by t_{VDQ}, then the V_{DS} fault is considered valid and the corresponding V_{DS} fault bit, ALO, AHO, BLO, BHO, CLO, or CHO will be set in the Diagnostic register.

In blanking mode (optional), a timer is started when any gate drive is turned on or turned off. The outputs from the V_{DS} over-

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voltage comparators for all MOSFETs are ignored (blanked) for the duration of the timer's active period, set by t_{VDQ}. If any gate drive changes state while a blanking period is in progress, the timer will be retriggered, resulting in an extended overall blanking time. If any comparator output indicates a V_{DS} fault and the blanking timer is not active, then the V_{DS} fault is considered valid and the corresponding V_{DS} fault bit, ALO, AHO, BLO, BHO, CLO, or CHO is set in the Diagnostic register.

The action taken when a valid V_{DS} fault is detected and the action then required to clear the fault state depend upon the ESF bit value.

If ESF = 0, the fault state will be latched, the general fault flag will be active, the associated V_{DS} fault bit will be set, and the associated phase will be disabled. The fault state and the general fault flag, but not the V_{DS} fault bit, will be reset the next time the MOSFET on which the fault was detected is commanded to switch on. If the phase is being driven with a PWM signal, then this will usually mean that the phase will be turned on again each PWM cycle. If this is the case, and the fault condition remains, then a valid fault will again be detected after the timeout period and the sequence will repeat. In this case the general fault flag will only be reset for the duration of the validation timer. The V_{DS} fault bit will only be reset by a serial read of the Diagnostic register with DSR = 0 or by a power-on reset.

If ESF = 1, the fault will be latched, the general fault flag will be active, the associated V_{DS} fault bit will be set, and all MOSFETs will be disabled. The fault state, V_{DS} fault bit, and the general fault flag will only be reset by a serial read of the Diagnostic register with DSR = 0 or by a power-on reset.

If ESF = 0, care must be taken to avoid damage to the MOSFET where the V_{DS} fault is detected. Although the MOSFET will be switched off as soon as the fault is detected at the end of the fault validation timeout, it is possible that it could still be damaged by excessive power dissipation and heating. To limit any damage to the external MOSFETs or the motor, the MOSFET should be fully disabled by logic inputs from the external controller.

Fault Action

The action taken when one of the diagnostic functions indicates a fault is listed in Table 6.

Table 6: Fault Actions

Fault Description	Disable Outputs		Fault State Latched
	ESF = 0	ESF = 1	
No Fault	No	No	–
Power-On-Reset	Yes [1]	Yes [1]	No
V_{REG} Undervoltage	Yes [1]	Yes [1]	No
V_{BB} Undervoltage	No	Yes [1]	No
V_{LR} Undervoltage	No	Yes [1]	Yes
V_{IO} Undervoltage	Yes [1]	Yes [1]	Yes
MCU Watchdog	Yes [1]	Yes [1]	Yes
ENABLE Timeout	No	Yes [1]	No
V_{DS} Overvoltage	Yes [2]	Yes [1]	Yes
Bootstrap Undervoltage	Yes [2]	Yes [1]	Yes
Overtemperature	No	Yes [1]	Yes [3]
Temperature Warning	No	No	No
Overcurrent	No	No	No
Serial Transmission Error	No	No	No
EEPROM	Yes [1]	Yes [1]	Yes

[1] All gate drives low, all MOSFETs off.
[2] Gate drive for the affected MOSFET low, only the affected MOSFET off.
[3] Only latched when ESF = 1.

When a fault is detected, a corresponding fault state is considered to exist. In some cases, the fault state only exists during the time the fault is detected. In other cases, when the fault is only detected for a short time, the fault state is latched (stored) until reset. The faults that are latched are indicated in Table 6. Some latched fault states are reset with specific actions. All latched fault states and any fault bits in the status diagnostic registers are always reset when a power-on-reset state is present or when the associated fault bit is read through the serial interface with DSR = 0.

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For many of the faults, the action taken is modified by the ESF (enable stop on fail) bit. In general, this will affect the action on the gate drive outputs and is detailed for each fault in Table 6. Setting the ESF bit to 0 such that the gate drive outputs are not disabled in the event of the corresponding fault being detected means that the AMT49105 will not take any action to protect itself or the external bridge MOSFETs and damage may occur. Appropriate action must be taken by the external controller.

The fault conditions power-on-reset, V_{REG} undervoltage, V_{IO} undervoltage, and EEPROM error are considered critical to the safe operation of the AMT49105 and the system. If these faults are detected then the gate drive outputs are automatically driven low and all MOSFETs in the bridge held in the off state. This state will remain until the fault is removed.

If the ENABLE timeout is active by setting the ETO mask bit to 0 then this fault state is also considered critical to the safe operation of the AMT49105 and the system. If an ENABLE timeout is detected then all gate drive outputs are driven low and all MOSFETs in the bridge held in the off state. This state will remain until the timer is reset.

If the microcontroller watchdog is active by setting the WD mask bit to 0, then this fault state is also considered critical to the safe operation of the AMT49105 and the system. If a microcontroller watchdog failure is detected, then all gate drive outputs are driven low and all MOSFETs in the bridge are held in the off state. This state will remain until a valid watchdog input has been detected and the fault state is cleared.

For overtemperature fault conditions, the action taken depends on the status of the ESF bit. If an overtemperature fault is detected and ESF = 1 when an overtemperature is detected, all gate drive outputs will be disabled, the V_{LR} regulator is shut down, and MRSTn will go low. This state will remain until 10 ms after the fault is removed. If ESF = 0, then neither VLR nor the gate drive outputs will be affected.

If ESF = 0 when an overtemperature is detected, no circuitry will be disabled and action must be taken by the user to limit the power dissipation in some way so as to prevent overtemperature damage to the chip and unpredictable device operation.

V_{BB} undervoltage is not considered critical and the action taken depends on the state of the enable stop on fault bit, ESF. If a V_{BB} undervoltage condition exists and ESF = 1, the gate drive outputs will be disabled and the motor will coast until the condition is removed. If ESF = 0, the gate drive outputs are not affected.

If a V_{DS} overvoltage or bootstrap undervoltage fault is detected, then the action taken will also depend on the status of the ESF bit, but these faults are handled as a special case. If a fault is detected on any of these two diagnostics and ESF = 1, then all the gate drive outputs will be driven low and all MOSFETs in the bridge held in the off state. When ESF = 1, this fault state will be latched and remain until reset. If a V_{DS} overvoltage or bootstrap undervoltage fault is detected and ESF = 0, then only the gate drive output to the MOSFET where the fault was detected will be driven low and the MOSFET will be held in the off state. When ESF = 0, the V_{DS} or bootstrap undervoltage fault state will be latched but will be reset the next time the MOSFET is commanded to switch on.

The remaining faults (temperature warning, overcurrent detect, and serial error) are not considered critical and the gate drive outputs will remain active.

Fault Masks

Individual diagnostics, except power-on reset, serial transmission error, and EEPROM error can be disabled by setting the corresponding bit in the mask registers. Power-on-reset cannot be disabled because the diagnostics and the output control depend on the logic regulator to operate correctly. If a bit is set to one in the mask registers, then the corresponding diagnostic will be completely disabled. No fault states for the disabled diagnostic will be generated, no action will be taken, and no fault flags or diagnostic bits will be set. See Mask Register definition for bit allocation.

Care must be taken when diagnostics are disabled to avoid potentially damaging conditions.

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Diagnostic and System Verification

To comply with various aspects of safe system design, it is necessary for higher level safety systems to verify that any diagnostics or functions used to guarantee safe operation are operating within specified tolerances.

The AMT49105 includes additional verification functions to help the system design comply with safety requirements.

Table 7: Verification Functions

Verification Type	Function Verified	Operation	
		Offline	Online
Monitor	System clock frequency verification		Y
Diagnostic	System clock operation		Y
Diagnostic	All gate drives off	Y	
Monitor	MOSFET active monitor	Y	
Monitor	Motor direction	Y	

On-Line Verification

The following functions are permanently active and can be monitored at any point during normal operation. No other action will be taken by the AMT49105 unless described below.

System Clock Frequency Verification

The SDO output can be set to provide a logic-level square wave output at a ratio of the internal clock frequency to allow verification of the system clock frequency and more precise calibration of the timing settings if required.

When the CKS bit is set to 0, the SDO terminal operates as described in the serial interface description. When the CKS bit is set to 1, the SDO terminal will output the divided clock signal when STRn is held high. The division ratio, ND, is defined in the Electrical Characteristics table. When CKS = 1 and STRn is low, the serial interface will continue to accept data on SDI and output the normal serial data on SDO.

System Clock Operation Verification

The internal system clock is monitored by a watchdog timer. When the watchdog detects that the clock has stopped, the gate drive outputs are disabled. If a serial access is performed, data input through SDI is ignored, no data is written to the serial registers and the addresses registers are clocked out on the SDO terminal. If the internal system clock stops, then the SC bit will be set in the Verification register. When the system clock restarts, the SC bit will be reset and the gate drive outputs and SPI re-enabled.

Off-Line Verification

The following functions can only be completed when the diagnostics are not required and the motor is not being commanded to run.

All Gate Drives Off

The successful propagation of control inputs demanding all-gate drives-off to the gate drive outputs is verified by setting up an appropriate input condition and inspecting the GDO bit in the Verification register. If the input condition has successfully turned off all six gate drives, the GDO bit is set. The control input conditions (i.e. the combinational states of Hx, Lx, xH, xL, and ENABLE) that demand all outputs off (GHx = L, GLx = L) and hence set the GDO bit as a result of a successful verification test can be determined by inspection of Table 1, Table 2, and Table 3. If the ENABLE watchdog mode is selected (EWD = 1) and the watchdog timeout is allowed to expire, the GDO bit will similarly be set as the result of a successful test. Verification of propagation from an appropriate combination of phase logic inputs (Hx, Lx) and serial register bits (xH, xL) to the gate drive outputs does not verify propagation from the ENABLE input to the gate drive outputs and vice versa. Gate drive off events are not latched in the Verification register and the GDO bit returns to 0 as soon as any gate drive is detected to be in the on state.

MOSFET Active Monitor

The state of the external MOSFETs in each phase can be verified using a combination of MOSFET commands.

For the high-side MOSFET test, a high-side MOSFET is switched on using the Control register bits or the logic input terminals. The MOSFET active monitor then determines whether the resultant voltage on the corresponding Sx node is higher than $V_{BRG} - V_{DSTH}$. If this is true, the corresponding SxM bit in the Verification register will be set to 1. If the SxM bit is set to 0, then the high-side MOSFET verification has failed.

For the low-side MOSFET test, a low-side MOSFET is switched on using the Control register bits or the logic input terminals. The MOSFET active monitor then determines whether the resultant voltage on the corresponding Sx node is lower than $V_{LSSx} + V_{DSTL}$. If this is true, the corresponding SxM bit in the Verification register will be set to 0. If the SxM bit is set to 1, then the low-side MOSFET verification has failed.

All six MOSFETs must be tested separately to complete the verification.

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Motor Direction

The DIRO bit in the Verification register reports the motor direction. Forward is defined as DIRO = 1 and reverse is defined as DIRO = 0. The phase state sequence for both directions is defined in Figure 15.

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SERIAL INTERFACE

Table 8: Serial Register Definition*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0: Bridge	0	0	0	0	0	WR	DBM			DT5	DT4	DT3	DT2	DT1	DT0	P
							0	0	0	1	1	1	1	1	1	
1: Overcurrent	0	0	0	0	1	WR	OCQ	OCT3	OCT2	OCT1	OCT0	TOC3	TOC2	TOC1	TOC0	P
							0	0	0	1	0	1	1	1	1	
2: VDS monitor	0	0	0	1	0	WR		VDQ		VQT5	VQT4	VQT3	VQT2	VQT1	VQT0	P
							0	0	0	0	1	0	0	0	0	
3: VDS monitor	0	0	0	1	1	WR				VT5	VT4	VT3	VT2	VT1	VT0	P
							0	0	0	0	1	1	0	0	0	
4: BEMF detect	0	0	1	0	0	WR			BXM2	BXM1	BXM0	BF3	BF2	BF1	BF0	P
							0	0	0	0	0	0	0	0	1	
5: Watchdog	0	0	1	0	1	WR					WM4	WM3	WM2	WM1	WM0	P
							0	0	0	0	0	0	0	0	0	
6: Watchdog	0	0	1	1	0	WR	WC3	WC2	WC1	WC0	WW4	WW3	WW2	WW1	WW0	P
							0	0	0	0	0	0	0	0	0	
7: Sense Amp	0	0	1	1	1	WR	SAC	SAO3	SAO2	SAO1	SAO0	OSO	SAG2	SAG1	SAG0	P
							0	1	1	0	0	0	0	1	0	
8: Gate drive	0	1	0	0	0	WR		IR13	IR12	IR11	IR10	IR23	IR22	IR21	IR20	P
							0	0	0	0	0	0	0	0	0	
9: Gate drive	0	1	0	0	1	WR		IF13	IF12	IF11	IF10	IF23	IF22	IF21	IF20	P
							0	0	0	0	0	0	0	0	0	
10: Gate drive	0	1	0	1	0	WR		TRS3	TRS2	TRS1	TRS0	TFS3	TFS2	TFS1	TFS0	P
							0	0	0	0	0	0	0	0	0	
11: Regulators	0	1	0	1	1	WR								VRS	VLS	P
							0	0	0	0	0	0	0	0	0	
21: Control	1	0	1	0	1	WR	IGP			CH	CL	BH	BL	AH	AL	P
							0	0	0	0	0	0	0	0	0	
22: Diagnostic Select	1	0	1	1	0	WR	DG1	DG0	DSR	ESF		CKS		RBS1	RBS0	P
							0	0	0	1	0	0	0	0	0	

***Default values shown below each input register bit.**

Continued on the next page...

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Table 8: Serial Register Definition*

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
23: System	1	0	1	1	1	WR	GTS	VLR	VRG	VIO	BRS	OPM	LBR	LEN	VLRD	P
							0	0	1	0	1	0	0	0	0	
24: NVM Write	1	1	0	0	0	WR	SAV1	SAV0								P
							0	0	0	0	0	0	0	0	0	
26: Mask 0	1	1	0	1	0	WR	ETO	OC		CHO	CLO	BHO	BLO	AHO	ALO	P
							1	0	0	0	0	0	0	0	0	
27: Mask 1	1	1	0	1	1	WR		VBU	VRU	VLRU	VIOU	WD	OT	TW	BSU	P
							0	0	0	0	0	1	0	0	0	
28: Verification	1	1	1	0	0	0				SC	DIRO	GDO	SCM	SBM	SAM	P
							0	0	0	0	0	0	0	0	0	
29: Diag 0	1	1	1	0	1	0				CHO	CLO	BHO	BLO	AHO	ALO	P
							0	0	0	0	0	0	0	0	0	
30: Diag 1	1	1	1	1	0	0		VBU	VRU	VLRU	VIOU		VC	VB	VA	P
							0	0	0	0	0	0	0	0	0	
31: Data Acquisition	1	1	1	1	1	DO9	DO8	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0	P
						0	0	0	0	0	0	0	0	0	0	
Status	FF	POR	SE	EE	OC	IG	OT	TW		WD	ETO	VSU	VLU	BSU	DSO	P
	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	

*Default values shown below each input register bit.

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A three wire synchronous serial interface, compatible with SPI, is used to control the features of the AMT49105. A fourth wire can be used to provide diagnostic feedback and read back of the register contents. The fourth wire can also be set to provide a logic-level square wave output at a ratio of the internal clock frequency as described in the Diagnostics section. The serial interface provides full access to all the features of the AMT49105.

The serial interface timing requirements are specified in the Electrical Characteristics table and illustrated in Figure 4. Data is received on the SDI terminal and clocked through a shift register on the rising edge of the clock signal input on the SCK terminal. The STRn terminal is normally held high and is only brought low to initiate a serial transfer. No data is clocked through the shift register when STRn is high, allowing multiple slave units to use common SDI, SCK, and SDO connections. Each slave then requires an independent STRn connection.

After 16 data bits have been clocked into the shift register, STRn must be taken high to latch the data into the selected register. When this occurs, the internal control circuits act on the new data and the Status or Diagnostic registers are reset depending on the transfer.

Diagnostic information or the contents of the registers is output on the SDO terminal msb first while STRn is low and changes to the next bit on each falling edge of SCK. The first bit, which is always the FF bit from the Status register, is output as soon as STRn goes low.

The first five bits, D[15:11], in a serial input word are the register address bits providing 32 addressable registers, of which, 20 are used. In addition to these there is a read only Status register.

Register address 31 is a special function register. This is a read only measurement output register and provides a 10-bit integer output from the internal data acquisition system.

The remaining registers provide configuration and control for the AMT49105. Each of these registers has a write bit, WR (bit 10), as the first bit after the register address. This bit must be set to one to write the subsequent bits into the selected register. If WR is zero, then the remaining data bits (bits 9 to 0) are ignored. For these registers, the state of the WR bit also determines the data output on SDO. If WR is set to one, then the Status register is output. If WR is set to zero, then the contents of the register selected by the first five bits on SDI is output.

In all cases, the first six bits output on SDO will always include the FF, POR, SE, EE, OC, and IG bits from the Status register.

The last bit in any serial transfer, D[0], is a parity bit that is set to ensure odd parity in the complete 16-bit word. Odd parity means that the total number of 1s in any transfer should always be an odd number. A parity fault is detected if the total number of logic 1 states in the 16-bit transfer is an even number. This ensures that there is always at least one bit set to 1 and one bit set to 0 and allows detection of stuck-at faults on the serial input and output data connections. The parity bit is not stored but generated on each transfer.

If a parity fault is detected, or there are more than 16 rising edges on SCK, or if STRn goes high and there are fewer than 16 rising edges on SCK, the write will be cancelled without latching data to the registers. In addition, the Status register will not be reset and the FF bit and SE bits will be set to indicate a data transfer error.

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Configuration and Control Registers

The serial data word is 16 bits, input msb first; the first five bits are defined as the register address. This provides 32 addressable registers: 28 are read/write and 4 are read only.

Register 0: Bridge dead time:

- DBM, disable bootstrap management
- DT[5:0], a 6-bit integer to set the dead time

Register 2: Overcurrent:

- OCQ, selects overcurrent qualifier mode
- OCT[3:0], 4-bit integer to set the overcurrent threshold
- TOC[3:0], 4-bit integer to set the overcurrent qualifier time

Register 2: VDS:

- VDQ, selects VDS qualifier mode
- VQT[5:0], 6-bit integer to set the VDS qualifier time

Register 3: VDS:

- VT[5:0], 6-bit integer to set the V_{DS} threshold

Register 4: BEMF detect:

- BXM[2:0], 3 bits to select output on BXM terminal
- BF[3:0], 4 bits to select BEMF Filter time

Register 5: Watchdog:

- WM[4:0], 5-bit integer to set the minimum watchdog time

Register 6: Watchdog:

- WC[3:0], 4-bit integer to set watchdog cycle count
- WW[4:0], 5-bit integer to set the watchdog window time

Register 7: Sense Amps:

- SAC, initiate sense amp calibration
- SAO[3:0], 4 bits to sense amp offset
- OSO, outputs the zero current offset on CSO
- SAG[2:0], 3 bits to set sense amp gain

Register 8: Gate drive:

- IR1[3:0], 4 bits to set turn-on current 1
- IR2[3:0], 4 bits to set turn-on current 2

Register 9: Gate drive:

- IF1[3:0], 4 bits to set turn-off current 1
- IF2[3:0], 4 bits to set turn-off current 2

Register 10: Gate drive:

- TRS[3:0], 4-bit integer to set turn-on time
- TFS[3:0], 4-bit integer to set turn-off time

Register 11: Regulators:

- VLS, VLR output during V_{BB} undervoltage event
- VRS, VREG output during V_{BB} undervoltage event

Register 21: Control:

- IGP, disable wake on LIN terminal
- CH, CL, MOSFET control for phase C
- BH, BL, MOSFET control for phase B
- AH, AL, MOSFET control for phase A

Register 22: Diagnostic Select:

- DG[1:0], select output on DIAG
- DSR, disable reset on serial transfer
- ESF, enable stop on fail
- CKS, output clock on SDO
- RBS[1:0], select contents for register 31 readback

Register 23: System Functions:

- GTS, initiates go-to-sleep function
- VLR, selects logic regulator voltage
- VRG, selects gate drive regulator voltage
- VIO, selects logic I/O regulator voltage
- BRS, bridge switch control
- OPM, selects the operating mode
- LBR, sets LIN speed
- LEN, controls LIN standby/active state
- VLRD, disables the VLR regulator

Register 24: NVM:

- SAV[1:0], controls and reports saving the register contents to the NVM

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Mask Registers

Two mask registers allow individual diagnostics to be disabled. If a bit is set to one in the mask registers, then the corresponding diagnostic will be completely disabled. No fault states for the disabled diagnostic will be generated, no action will be taken, and no fault flags or diagnostic bits will be set.

Register 26: Mask 0:

Individual bits for each gate drive output to disable V_{DS} diagnostic monitors, a bit to disable the overcurrent monitor, and a bit to disable the ENABLE input watchdog timeout.

Register 27: Mask 1:

Individual bits to disable the microcontroller window watchdog, temperature monitors, and the supply and bootstrap undervoltage monitors.

Verification Register

The verification register is used to manage the system verification features.

Register 28: Verification:

Individual bits holding the state of the system clock, motor direction, gate drives off monitor, and MOSFET active monitors.

Status and Diagnostic Registers

The chip and some external status is provided by a Status register and two Diagnostic registers. Normally any fault bits set in these registers will be cleared on a successful read. However, in some systems it is preferable to be able to read the Status or Diagnostic registers without causing a reset and allowing the AMT49105 to re-enable the outputs. The DSR (Disable Serial Reset) bit provides this functionality. When DSR is set to one, any valid read of any of the diagnostic registers will not result in that register being reset. When DSR = 0, any valid read of any of the diagnostic registers will reset the content of that register. This provides a way for the external controller to access the diagnostic information without automatically re-enabling any outputs, but retains a way to reset the faults under control of the controller.

Diagnostic Registers

In addition to the read-only status register, two read-only diagnostic registers provide detailed diagnostic management and reporting. When DSR = 0, any bits set in a diagnostic register are reset on completion of a successful read of that register. When DSR = 1, the register will not be reset. Reading one diagnostic register will not affect the fault bits in any other register. Reading the status register will not affect fault bits in any diagnostic register.

Register 29: Diagnostic 0 (read only):

Individual bits indicating faults detected in V_{DS} diagnostic monitors for each gate drive output.

Register 30: Diagnostic 1 (read only):

Individual bits indicating faults detected in voltage regulators and bootstrap undervoltage monitors for each high-side gate drive output.

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Status Register

There is one status register in addition to the addressable registers. When any register transfer takes place, the first six bits output on SDO are always the most significant six bits of the status register regardless of whether the addressed register is being read or written (see Serial Timing diagram). The content of the remaining ten bits will depend on the state of the WR bit input on SDI. Except for the read only registers, when WR is 1, the addressed register will be written and the remaining ten bits output on SDO will be the least significant nine bits of the status register followed by a parity bit. For the read only registers—that is, the two diagnostic registers and the data readback register—if WR is 1, the data bits will be ignored, no data will be written to the register, and the remaining ten bits output on SDO will be the least significant nine bits of the status register followed by a parity bit. For both read only and read/write registers, when WR is 0, the addressed register will be read and the remaining ten bits will be the contents of the addressed register followed by a parity bit.

The read only status register provides a summary of the chip status by indicating if any diagnostic monitors have detected a fault. The most significant four bits of the status register indicate critical system faults. Bits 11 through 1 provide indicators for specific individual monitors and the contents of the two diagnostic registers. The contents and mapping to the diagnostic registers is listed in Table 9.

Table 9: Status Register Mapping

Status Register Bit	Diagnostic	Related Diagnostic Register Bits
FF	Status Flag	None
POR	Power-On-Reset	None
SE	Serial Error	None
EE	EEPROM Error	None
OC	Overcurrent	None
IG	IG Input Status	None
OT	Overtemperature	None
TW	Temperature Warning	None
WD	MCU Watchdog	None
ETO	ENABLE Timeout	None
VSU	Supply Undervoltage	VBU, VRU
VLU	Logic Supply Undervoltage	VLRU, VIOU
BSU	Bootstrap UV	VA, VB, VC
DSO	VDS OV	AHO, ALO, BHO, BLO, CHO, CLO

UV = Undervoltage, OV = Overvoltage

The first most significant bit in the register is the diagnostic status flag, FF. This is high if any fault bits in the status register except IG is set. If there are no fault bits in the status register, then FF will be zero. IG is the only bit that has no effect on the state of the FF bit. When STRn goes low to start a serial write, SDO outputs the diagnostic status flag. This allows the main controller to poll the AMT49105 through the serial interface to determine if a fault has been detected. If no faults have been detected, then the serial transfer may be terminated without generating a serial read fault by ensuring that SCK remains high while STRn is low. When STRn goes high, the transfer will be terminated and SDO will go into its high-impedance state.

The second most significant bit is the POR bit. At power-up or after a power-on-reset, the FF bit and the POR bit are set, indicating to the external controller that a power-on-reset has taken place. All other diagnostic bits are reset and all other registers are returned to their default state. Note that a power-on-reset only occurs when the output of the internal logic regulator rises above its undervoltage threshold. Power-on-reset is not affected by the state of the VBB supply or VREG regulator output. In general the VBU, VRU, VLRU, and VIOU bits may also be set following a power-on-reset, as the regulators will not have reached their respective rising undervoltage thresholds until after the register reset is completed.

The third bit in the status register is the SE bit, which indicates that the previous serial transfer was not completed successfully.

The fourth bit in the Status register is the EE bit, which indicates that an EEPROM error was detected at device power-up. This bit can only be cleared by sequencing the power off then on again.

The sixth bit IG is a status indicator showing the state of the IG input. This bit has no effect on the FF bit or the general fault flag output on DIAG.

Of the remaining bits, the contents of OC, OT, TW, WD, and ETO are determined by individual diagnostics. These bits along with the POR and SE bits will be reset on the completion of a successful serial write transaction of the status register with DSR = 0. If DSR = 1, the fault bits will not be affected. Resetting only affects latched fault bits for faults that are no longer present. For any static faults that are still present, for example overtemperature, the fault flag will remain set after the reset.

The contents of the remaining bits in the status register, VSU, VLU, BSU, and DSO are all derived from the contents of the diagnostic registers. These bits are only cleared when the corresponding contents of the diagnostic registers are reset; they cannot be reset by reading the status register. A fault indicated on any

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of the related diagnostic register bits will set the corresponding status register bit to 1. The related diagnostic register must then be read to determine the exact fault and clear the fault state if the fault condition has cleared.

Readback Register

The read-only readback register, register 31, provides access to two additional measurements. The measurement to be output on SDO when register 31 is addressed is selected by the RBS[1:0] variable as shown in Table 10:

Table 10: Readback Output Select

RBS	Register 31 Output
0	Chip Temperature
1	Supply Voltage (V_{BRG})
2	VLR Output Voltage
3	Not Used

The first five bits of the readback register are always the most significant five bits of the Status register. The 10-bit readback value is the next ten bits followed by a parity bit.

The chip junction temperature measurement is determined by the voltage of the internal temperature measurement diodes. The chip junction temperature, T_J, is defined as:

$$T_J = 367.7 - (n \times 0.451) \quad (°C)$$

where n is a positive integer defined by DO[9:0].

The temperature measurement result range is –93°C to 367°C, but the useable measurement range is –50°C to 190°C.

The supply voltage measurement is a direct measurement of the VBRG voltage with a resolution of 53 mV and a range of 54 V. The supply voltage, V_S, is defined as:

$$V_S = n \times 0.0528 \text{ V}$$

where n is a positive integer defined by DO[9:0].

The supply voltage measurement is updated every 1 ms and the chip temperature measurement is updated every 0.5 ms.

The VLR voltage measurement is a direct measurement of the VLR output voltage with a resolution of 4 mV and a range of 4 V when VLR = 0, and a resolution of 6 mV and a range of 5.9 V when VLR = 1.

The VLR output voltage, V_{LR}, is defined as:

$$V_{LR} = n \times 0.004025 \text{ V} \quad (\text{VLR} = 0)$$

$$V_{LR} = n \times 0.005787 \text{ V} \quad (\text{VLR} = 1)$$

where n is a positive integer defined by DO[9:0].

The supply and VLR voltage measurements are updated every 1 ms and the chip temperature measurement is updated every 0.5 ms.

Nonvolatile memory

The values in the configuration and control registers are held in nonvolatile EEPROM (NVM), allowing the AMT49105 to be preprogrammed with different user-defined register values for each application, thus avoiding the need to program the register contents at each power-on.

The AMT49105 provides a simple method to write the contents of the registers into the NVM using the serial interface. When the SAV[1:0] bits in register 24 are changed from [01] to [10] in a single serial write, the present contents of registers 0 to 10, 21 to 23, except register 23 bit 9 (GTS), and registers 26 and 27, are saved (written to NVM) as a single operation. The save sequence takes typically 400 ms to complete. It is not possible to save single register values. Although the motor may be operating during the save sequence, it is recommended that the motor drive is disabled before starting a save sequence to avoid any corruption caused by the electrical noise or any faults from the motor.

Note that the GTS bit (register 23[9]) is not saved. This is to avoid a lockout condition where the AMT49105 is commanded to go to sleep as soon as the wakeup sequence is complete.

The register save sequence requires a programming voltage, V_{PP}, to be applied to the VBB terminal. V_{PP} must be present on the VBB terminal for a period of time, t_{PRS}, before the save sequence is started. V_{PP} must remain on VBB until the save sequence is completed.

During the save sequence, the SPI remains active for read only. Any attempt to write to the registers during the save sequence will cause the FF and SE bits to be set in the Status register.

During the save sequence, the AMT49105 will automatically complete all the necessary steps to ensure that the NVM is correctly programmed and will complete the sequence by verifying that the contents of the NVM have been securely programmed. On successful completion of a save sequence, the SAV[1:0] bits will be set to 01. Register 24 should be read to determine if the save has completed successfully. If SAV[1:0] is reset to 00, then the save sequence has been terminated and has not completed successfully.

If V_{PP} drops below the programming undervoltage level, V_{PPUV},

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during the save sequence, then the sequence will be terminated immediately and SAV[1:0] will be reset to 00.

To externally verify the data saved in the NVM, the V_{BB} supply must be cycled off then on to cause a power-on-reset. Following a power-on-reset, the contents of the NVM are copied to the serial registers when can then be read through the serial interface and verified.

For guaranteed data retention reliability, the NVM in the AMT49105 should be written no more than 1000 times.

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Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0: Bridge	0	0	0	0	0	WR	DBM			DT5	DT4	DT3	DT2	DT1	DT0	P
							0	0	0	1	1	1	1	1	1	
1: Overcurrent	0	0	0	0	1	WR	OCQ	OCT3	OCT2	OCT1	OCT0	TOC3	TOC2	TOC1	TOC0	P
							0	0	0	1	0	1	1	1	1	

*Power-on reset value shown below each input register bit.

Register 0: Bridge Configuration

DBM Disable Bootstrap manager

DBM	Bootstrap Manager	Default
0	Active	D
1	Disabled	

DT[5:0] Dead time.

$t_{DEAD} = n \times 50$ ns

where where n is a positive integer defined by DT[5:0]. For example, for the power-on reset condition, DT[5:0] = [11 1111], t_{DEAD} = 3.15 µs.

The range of t_{DEAD} is 100 ns to 3.15 µs. Selecting a value of 1 or 2 will set the dead time to 100 ns. Setting DT[5:0]=0 disables the dead time.
If DT = 0 and DBM = 0, a fixed value of dead time of 3.15 µs is applied on bootstrap management cycles.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Register 1: Overcurrent Configuration

OCQ Overcurrent time qualifier mode

OCQ	Qualifier	Default
0	Debounce	D
1	Blanking	

OCT[3:0] Overcurrent threshold.

$V_{OCT} = (n + 1) \times 200$ mV

where n is a positive integer defined by OCT[3:0], e.g. for the power-on-reset condition.
OCT[3:0] = [0010] then V_{OCT} = 0.6 V.
The range of V_{OCT} is 0.2 to 3.2 V.

TOC[3:0] Overcurrent qualify time.

$t_{OCQ} = n \times 500$ ns

where n is a positive integer defined by TOC[3:0], e.g. for the power-on-reset condition.
TOC[3:0] = [1111] then t_{OCQ} = 7.5 µs.
The range of t_{OCQ} is 0 to 7.5 µs.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

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Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2: VDS monitor	0	0	0	1	0	WR		VDQ		VQT5	VQT4	VQT3	VQT2	VQT1	VQT0	P
							0	0	0	0	1	0	0	0	0	
3: VDS monitor	0	0	0	1	1	WR				VT5	VT4	VT3	VT2	VT1	VT0	P
							0	0	0	0	1	1	0	0	0	

*Power-on reset value shown below each input register bit.

Register 2: VDS Monitor Configuration

VDQ VDS Fault qualifier mode.

VDQ	VDS Fault Qualifier	Default
0	Debounce	D
1	Blank	

VQT[5:0] VDS qualification time.

$t_{VDQ} = n \times 100$ ns

where n is a positive integer defined by VQT[5:0].
e.g. for the power-on-reset condition.
VQT[5:0] = [01 0000] then t_{VDQ} = 1.6 µs.
The usable range of t_{VDQ} is 600 ns to 6.3 µs.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Register 3: VDS Monitor Configuration

VT[5:0] VDS overvoltage threshold.

$V_{DST} = n \times 50$ mV

where n is a positive integer defined by VT[5:0],
e.g. for the power-on-reset condition.
VT[5:0] = [01 1000] then V_{DST} = 1.2 V.
The range of V_{DST} is 0 to 3.15 V.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

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Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4: BEMF detect	0	0	1	0	0	WR	0	0	BXM2	BXM1	BXM0	BF3	BF2	BF1	BF0	P
									0	0	0	0	0	0	1	

*Power-on reset value shown below each input register bit.

Register 4: BEMF detect

BXM [2:0] Selects output on BXM.

BXM2	BXM1	BXM0	BXM Output	Default
0	0	0	FG	D
0	0	1	Phase A	
0	1	0	Phase B	
0	1	1	Phase C	
1	X	X	LO	

BF[3:0] Windmill BEMF Filter Time.
t_{BF} defined by:

BF3	BF2	BF1	BF0	Filter time	Default
0	0	0	0	0	
0	0	0	1	200 µs	D
0	0	1	0	400 µs	
0	0	1	1	600 µs	
0	1	0	0	800 µs	
0	1	0	1	1 ms	
0	1	1	0	2 ms	
0	1	1	1	4 ms	
1	0	0	0	5 ms	
1	0	0	1	6 ms	
1	0	1	0	10 ms	
1	0	1	1	12 ms	
1	1	0	0	14 ms	
1	1	0	1	16 ms	
1	1	1	0	18 ms	
1	1	1	1	20 ms	

P Parity bit. Ensures an odd number of 1s in any serial transfer.

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Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
5: Watchdog	0	0	1	0	1	WR					WM4	WM3	WM2	WM1	WM0	P
							0	0	0	0	0	0	0	0	0	
6: Watchdog	0	0	1	1	0	WR	WC3	WC2	WC1	WC0	WW4	WW3	WW2	WW1	WW0	P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Register 5: Watchdog Configuration

WM[4:0] Watchdog minimum time.

$t_{WM} = 1 + (n \times 2)$ ms

where n is a positive integer defined by WM[4:0], e.g. when WM[4:0] = [0 1010] then t_{WM} = 21 ms. The range of t_{WM} is 1 ms to 63 ms.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Register 6: Watchdog configuration

WC[3:0] Watchdog fail cycle count before sleep.

$C_{WC} = n \quad | n > 0$

where n is a positive integer defined by WC[3:0], e.g. when WC[3:0] = [1010] then C_{WC} = 10. The range of C_{WC} is 1 to 15. Setting WC[3:0] to [0000] disables the watchdog cycle counter.

WW[4:0] Watchdog window time.

$t_{WW} = 10 + (n \times 10)$ ms

where n is a positive integer defined by WW[4:0], e.g. when WW[4:0] = [0 1010] then t_{WW} = 110 ms. The range of t_{WW} is 10 ms to 320 ms.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

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Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7: Sense Amp	0	0	1	1	1	WR	SAC	SAO3	SAO2	SAO1	SAO0	OSO	SAG2	SAG1	SAG0	P
							0	1	1	0	0	0	0	1	0	

*Power-on reset value shown below each input register bit.

Register 7: Sense Amp Configuration

SAC Calibrate Sense Amp.

SAC	Offset	Default
0	No change in state	D
1	No change in state	
1 → 0	No change in state	
0 → 1	Initiate Calibration (when OSO = 0)	

SAO[3:0] Sense amp offset.

SAO	Offset	Default
0	0	
1	0	
2	100 mV	
3	100 mV	
4	200 mV	
5	300 mV	
6	400 mV	
7	500 mV	
8	750 mV	
9	1 V	
10	1.25 V	
11	1.5 V	
12	1.65 V	D
13	2 V	
14	2.25 V	
15	2.5 V	

where SAO is a positive integer defined by SAO[3:0].

P Parity bit. Ensures an odd number of 1s in any serial transfer.

OSO Output Offset.

OSO	Gain	Default
0	Normal sense amp output	D
1	Sense amp outputs offset voltage	

SAG[2:0] Sense amp gain.

SAG	Gain	Default
0	10	
1	15	
2	20	D
3	25	
4	30	
5	35	
6	40	
7	50	

where SAG is a positive integer defined by SAG[2:0].

P Parity bit. Ensures an odd number of 1s in any serial transfer.

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Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
8: Gate drive	0	1	0	0	0	WR		IR13	IR12	IR11	IR10	IR23	IR22	IR21	IR20	P
							0	0	0	0	0	0	0	0	0	
9: Gate drive	0	1	0	0	1	WR		IF13	IF12	IF11	IF10	IF23	IF22	IF21	IF20	P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Register 8: Gate drive configuration

IR1[3:0] Turn-on current 1.

$I_{R1} = n \times -5.5$ mA

where n is a positive integer defined by IR1[3:0], e.g. when IR1[3:0] = [1000] then $I_{R1} = -44$ mA. The range of I_{R1} is –5.5 mA to –82.5 mA. Selecting a value of 0 will set the gate drive to switch mode to turn on the MOSFET as quickly as possible.

IR2[3:0] Turn-on current 2.

$I_{R2} = n \times -5.5$ mA

where n is a positive integer defined by IR2[3:0], e.g. when IR2[3:0] = [0010] then $I_{R2} = -11$ mA. The range of I_{R2} is –5.5 mA to –82.5 mA. Selecting a value of 0 will set the gate drive to switch mode to turn on the MOSFET as quickly as possible.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Register 9: Gate drive configuration

IF1[3:0] Turn-off current 1.

$I_{F1} = n \times 5.3$ mA

where n is a positive integer defined by IF1[3:0], e.g. when IF1[3:0] = [1100] then $I_{F1} = 63.6$ mA. The range of I_{F1} is 5.3 mA to 79.5 mA. Selecting a value of 0 will set the gate drive to switch mode to turn off the MOSFET as quickly as possible.

IF2[3:0] Turn-off current 2.

$I_{F2} = n \times 5.3$ mA

where n is a positive integer defined by IF2[3:0], e.g. when IF2[3:0] = [0011] then $I_{F2} = 15.9$ mA. The range of I_{F2} is 5.3 mA to 79.5 mA. Selecting a value of 0 will set the gate drive to switch mode to turn off the MOSFET as quickly as possible.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

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Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
10: Gate drive	0	1	0	1	0	WR		TRS3	TRS2	TRS1	TRS0	TFS3	TFS2	TFS1	TFS0	P
							0	0	0	0	0	0	0	0	0	
11: Regulators	0	1	0	1	1	WR								VRS	VLS	P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Register 10: Gate drive configuration

TRS[3:0] Slew control turn-on time.

$t_{RS} = n \times 50$ ns

where n is a positive integer defined by TRS[3:0], e.g. when TRS[3:0] = [0110] then t_{RS} = 300 ns. The range of t_{RS} is 0 ns to 750 ns.

TFS[3:0] Slew control turn-off time.

$t_{FS} = n \times 50$ ns

where n is a positive integer defined by TFS[3:0], e.g. when TFS[3:0] = [1100] then t_{FS} = 600 ns. The range of t_{FS} is 0 ns to 750 ns.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Register 11: Regulators configuration

VRS VREG output during V_{BB} undervoltage.

VRS	VREG regulator	Default
0	Disabled	D
1	Enabled	

VLS VLR output during V_{BB} undervoltage.

VLS	VLR regulator	Default
0	Disabled	D
1	Enabled	

P Parity bit. Ensures an odd number of 1s in any serial transfer.

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Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
21: Control	1	0	1	0	1	WR	IGP			CH	CL	BH	BL	AH	AL	P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Register 21: Gate drive control

IGP Disable wake on LIN terminal.

IGP	Wake on LIN terminal	Default
0	Active	D
1	Disabled	

CH Phase C, High-side gate drive

CL Phase C, Low-side gate drive

BH Phase B, High-side gate drive

BL Phase B, Low-side gate drive

AH Phase A, High-side gate drive

AL Phase A, Low-side gate drive

See Table 2 and Table 3 for control logic operation.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

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Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
22: Diagnostic Select	1	0	1	1	0	WR	DG1	DG0	DSR	ESF		CKS		RBS1	RBS0	P
							0	0	0	1	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Register 22: Diagnostic Select

DG[1:0] Selects output DIAG terminal.

DG1	DG0	DIAG Output	Default
0	0	Fault– low true	D
0	1	Pulse Fault	
1	0	Fault– low true	
1	1	Clock	

DSR Serial reset of fault state and fault bit.

DSR	Reset on serial read	Default
0	Enabled	D
1	Disabled	

ESF Enable stop on fail select.

ESF	Stop on fail	Default
0	No stop on fail	
1	Stop on fail	D

CKS Selects output on SDO when STRn = 1.

CKS	SDO Output (STRn = 1)	Default
0	High impedance	D
1	Divided system clock	

RBS[1:0] Selects data output on register 31.

RBS1	RBS0	Register 31 contents	Default
0	0	Chip temperature	D
0	1	Supply voltage (VBRG)	
1	0	VLR output voltage	
1	1	Reserved	

P Parity bit. Ensures an odd number of 1s in any serial transfer.

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Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
23: System	1	0	1	1	1	WR	GTS	VLR	VRG	VIO	BRS	OPM	LBR	LEN	VLRD	P
							0	0	1	0	1	0	0	0	0	

*Power-on reset value shown below each input register bit.

Register 23: System configuration

GTS Go to sleep command.

GTS	Sleep transition	Default
0	No change in state	D
1	No change in state	
1 → 0	No change in state	
0 → 1	Enter sleep state if enabled	

VLR Logic regulator voltage.

VLR	Logic regulator voltage	Default
0	3.3 V	D
1	5 V	

VRG Gate drive regulator voltage.

VRG	Gate drive regulator voltage	Default
0	8 V	
1	11 V	D

VIO Logic I/O regulator voltage.

VIO	Logic I/O regulator voltage	Default
0	3.3 V	D
1	5 V	

BRS Bridge switch control.

BRS	Bridge Switch Activity	Default
0	Off	
1	Active	D

OPM Operating mode select.

OPM	Operating Mode	Default
0	LIN	D
1	PWM	

LBR LIN Baud Rate.

LBR	Baud rate	Default
0	10 kHz	D
1	20 kHz	

LEN LIN Enable.

LEN	LIN State	Default
0	Standby	D
1	Active	

VLRD Disables VLR regulator.

VLRD	VLR regulator	Default
0	Enabled	D
1	Disabled	

P Parity bit. Ensures an odd number of 1s in any serial transfer.

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Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
24: NVM Write	1	1	0	0	0	WR	SAV1	SAV0								P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Register 24: Write NVM control

SAV[1:0] Save parameters to Nonvolatile Memory (NVM).

When SAV[1:0] is changed from 01 to 10, the present contents of registers 0 to 10, 21 to 23, except register 23 bit 9, and registers 26 and 27 will be written to NVM.
When the NVM save has completed successfully, SAV[1:0] will be set to 01 and can be read to verify completion of the write. If SAV[1:0] is reset to 00, the save has not completed successfully.

P Parity bit. Ensures an odd number of 1s in any serial transfer.

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	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
26: Mask 0	1	1	0	1	0	WR	ETO	OC		CHO	CLO	BHO	BLO	AHO	ALO	P
						0	1	0	0	0	0	0	0	0	0	
27: Mask 1	1	1	0	1	1	WR		VBU	VRU	VLRU	VIOU	WD	OT	TW	BSU	P
						0	0	0	0	0	0	1	0	0	0	

*Power-on reset value shown below each input register bit.

Register 26: Mask 0 Register

ETO ENABLE timeout

OC Overcurrent

CHO Phase C high-side VDS overvoltage

CLO Phase C low-side VDS overvoltage

BHO Phase B high-side VDS overvoltage

BLO Phase B low-side VDS overvoltage

AHO Phase A high-side VDS overvoltage

ALO Phase A low-side VDS overvoltage

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Register 27: Mask 1 Register

VBU VBB undervoltage

VRU VREG undervoltage

VLRU VLR undervoltage

VIOU VIO undervoltage

WD Microcontroller Watchdog

OT Overtemperature

TW Temperature warning

BSU Bootstrap undervoltage

P Parity bit. Ensures an odd number of 1s in any serial transfer.

xx	Fault mask
0	Fault detection permitted
1	Fault detection disabled

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Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
28: Verification	1	1	1	0	0	0				SC	DIRO	GDO	SCM	SBM	SAM	P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Register 28: Verification Register (read only)

SC System Clock

SC	System Clock	Default
0	Clock running	D
1	Clock stopped	

DIRO Motor Direction

DIRO	Motor Direction	Default
0	Reverse	D
1	Forward	

GDO All gate drives off

GDO	Gate Drives	Default
0	Gate drives not off	D
1	Gate drives off	

SCM Phase C Monitor

SBM Phase B Monitor

SAM Phase A Monitor

SxM	MOSFET Active Monitor	Default
0	Phase x low-side active	D
1	Phase x high-side active	

P Parity bit. Ensures an odd number of 1s in any serial transfer.

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Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
29: Diagnostic 0	1	1	1	0	1	0				CHO	CLO	BHO	BLO	AHO	ALO	P
							0	0	0	0	0	0	0	0	0	
30: Diagnostic 1	1	1	1	1	0	0		VBU	VRU	VLRU	VIOU		VC	VB	VA	P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Register 29: Diagnostic 0 Register (read only)

CHO Phase C high-side VDS overvoltage

CLO Phase C low-side VDS overvoltage

BHO Phase B high-side VDS overvoltage

BLO Phase B low-side VDS overvoltage

AHO Phase A high-side VDS overvoltage

ALO Phase A low-side VDS overvoltage

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Register 30: Diagnostic 1 Register (read only)

VBU VBB undervoltage

VRU VREG undervoltage

VLRU VLR undervoltage

VIOU VIO undervoltage

VC Phase C bootstrap undervoltage

VB Phase B bootstrap undervoltage

VA Phase A bootstrap undervoltage

P Parity bit. Ensures an odd number of 1s in any serial transfer.

xxx	Status
0	No fault detected
1	Fault detected

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Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
31: Data Acquisition (Input)	1	1	1	1	1	0	X	X	X	X	X	X	X	X	X	P
SDO Output	FF	POR	SE	EE	OC	DO9	DO8	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0	P
	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Register 31: Data Acquisition Register (read only)

Input to SDI:

Bits[9:1] Don't care

P Parity bit. Ensures an odd number of 1s in any serial transfer.

Output to SDO:

Bits[15:11] From Status Register

The contents of DO[9:0] are selected by the RBS[2:0] variable as follows:

DO[9:0] (RBS=0) Chip Temperature.

$T_J = 367.7 – (n \times 0.451)$ (°C)
where n is a positive integer defined by DO[9:0].
The result range is –93°C to 367°C, but the useable measurement range is –50°C to 190°C.

DO[9:0] (RBS=1) Supply voltage (VBRG).

$V_S = n \times 0.0528$ V
where n is a positive integer defined by DO[9:0].
The measurement range is 0 to 50.4 V.

DO[9:0] (RBS=2) VLR output voltage.

$V_{LR} = n \times 0.004025$ V (VLR = 0)
$V_{LR} = n \times 0.005787$ V (VLR = 1)
where n is a positive integer defined by DO[9:0].

P Parity bit. Ensures an odd number of 1s in any serial transfer.

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Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Status	FF	POR	SE	EE	OC	IG	OT	TW	–	WD	ETO	VSU	VLU	BSU	DSO	P
	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

Status Register

FF Status register flag (not including IG)

POR Power-on-reset

SE Serial transfer error

EE EEPROM error

OC Overcurrent

IG Ignition Input State*

OT Over temperature

TW Temperature warning

WD Microcontroller watchdog

ETO ENABLE watchdog timeout

VSU Supply (V_{BB} or V_{REG}) undervoltage

VLU Logic supply (V_{LR} or V_{IO}) undervoltage

BSU Bootstrap undervoltage

DSO V_{DS} fault

P Parity bit. Ensures an odd number of 1s in any serial transfer.

*The state of the IG bit does not affect the FF bit.

xxx	Status
0	No fault detected
1	Fault detected

Status Register Bit Mapping

Status Register Bit	Related Diagnostic Register Bits
FF	None
POR	None
SE	None
EE	None
OC	None
IG	None
OT	None
TW	None
WD	None
ETO	None
VSU	VBU, VRU
VLU	VLRU, VIOU
BSU	VA, VB, VC
DSO	AHO, ALO, BHO, BLO, CHO, CLO

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INPUT/OUTPUT STRUCTURES

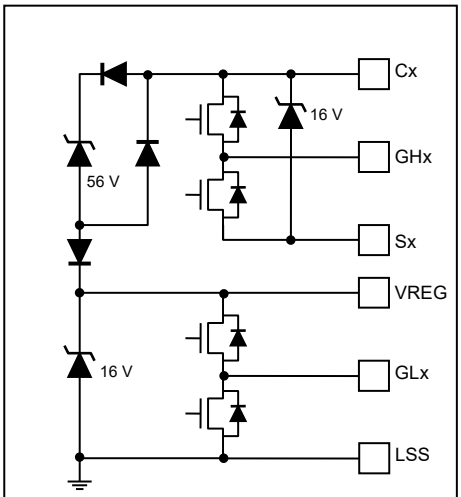

Figure 17a: Gate Drive Outputs

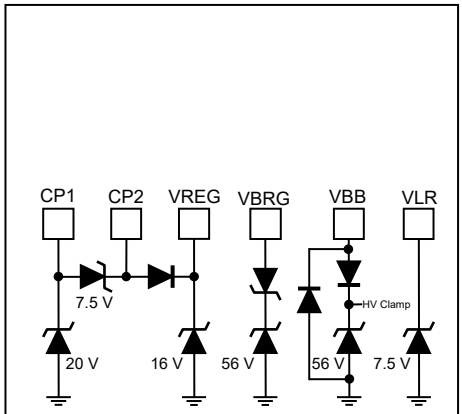

Figure 17b: Supplies

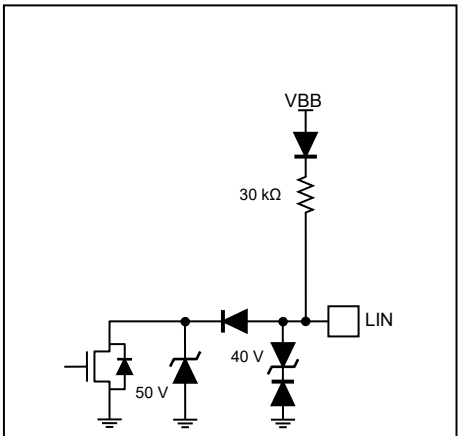

Figure 17c: LIN Bus I/O

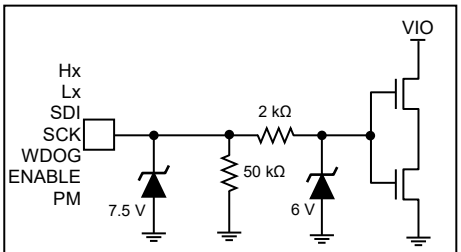

Figure 17d: Logic Inputs with Pull-Down

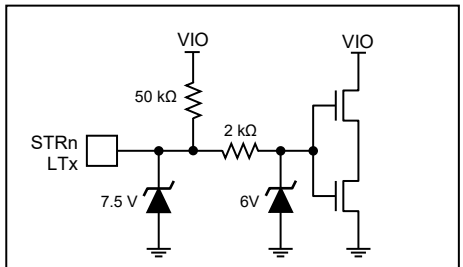

Figure 17e: Logic Inputs with Pull-Up

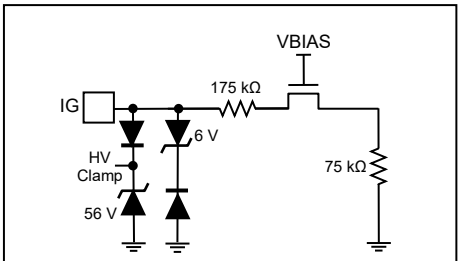

Figure 17f: HV-Compliant IG Inputs

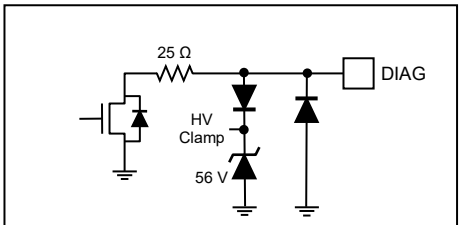

Figure 17g: HV- Compliant DIAG Output

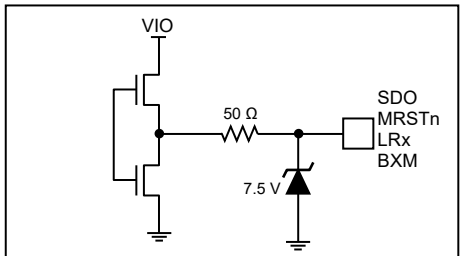

Figure 17h: Logic Outputs

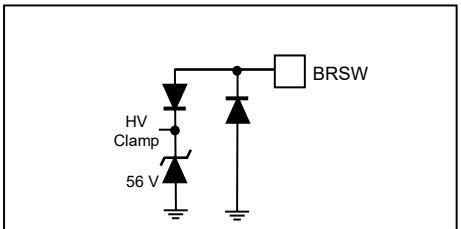

Figure 17i: HV-Compliant BRSW Output

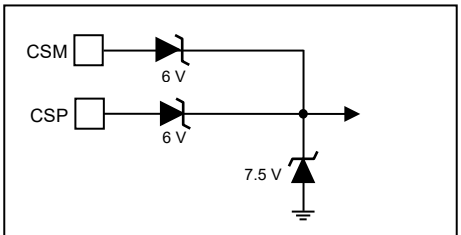

Figure 17j: Current Sense Amp Inputs

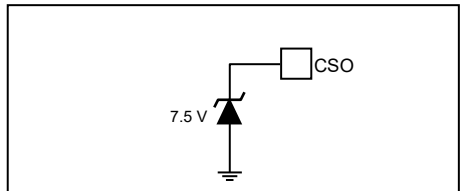

Figure 17k: Current Sense Amp Output

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LAYOUT RECOMMENDATIONS

Careful consideration must be given to PCB layout when designing high-frequency, fast-switching, high-current circuits:

• The three AMT49105 ground terminals, all designated GND, are internally connected but must also be connected together on the PCB close to the device for correct operation. This common point should return separately to the negative side of the motor supply filtering capacitor. This will minimize the effect of switching noise on the device logic and analog reference.

• The exposed thermal pad should be connected to the common point of the three GND terminals.

• Minimize stray inductance by using short, wide copper traces at the drain and source terminals of all power MOSFETs. This includes motor lead connections, the input power bus, and the common source of the low-side power MOSFETs. This will minimize voltages induced by fast switching of large load currents.

• Consider the addition of small (100 nF) ceramic decoupling capacitors across the source and drain of the power MOSFETs to limit fast transient voltage spikes caused by PCB trace inductance.

• Keep the gate discharge return connections Sx and LSSx as short as possible. Any inductance on these traces will cause negative transitions on the corresponding AMT49105 terminals, which may exceed the absolute maximum ratings. If this is likely, consider the use of clamping diodes to limit the negative excursion on these terminals with respect to the GND terminals.

• Supply decoupling, typically a 100 nF ceramic capacitor, should be connected between VBB and GND as close to the AMT49105 terminals as possible.

• Supply decoupling should be connected between VREG and GND as close to the AMT49105 terminals as possible.

• Supply decoupling should be connected between VLR and GND as close to the AMT49105 terminals as possible.

• Check the peak voltage excursion of the transients on the LSSx terminals with reference to the GND terminals using a close-grounded (‘tip and barrel’) probe. If the voltage at any LSSx terminal exceeds the absolute maximum in the datasheet, add additional clamping and/or capacitance between the LSSx terminal and the GND terminals.

• Gate charge drive paths and gate discharge return paths may carry a large transient current pulse. Therefore the traces from GHx, GLx, Sx, and LSSx (x = A, B, or C) should be as short as possible to reduce trace inductance.

• Provide an independent connection from each LSSx terminal to the source of the corresponding low-side MOSFET in the power bridge. Connection of the LSSx terminals directly to the GND terminals is not recommended as this may inject noise into sensitive functions such as the various voltage monitors.

• The inputs to the sense amplifier, CSP and CSM, should take the form of independent tracks and for best results should be matched in length and route.

• A low-cost diode can be placed in the connection to VBB to provide reverse-battery protection. In reverse-battery conditions, it is possible to use the body diodes of the power MOSFETs to clamp the reverse voltage to approximately 4 V. In this case, the additional diode in the VBB connection will prevent damage to the AMT49105 and the VBRG input will survive the reverse voltage.

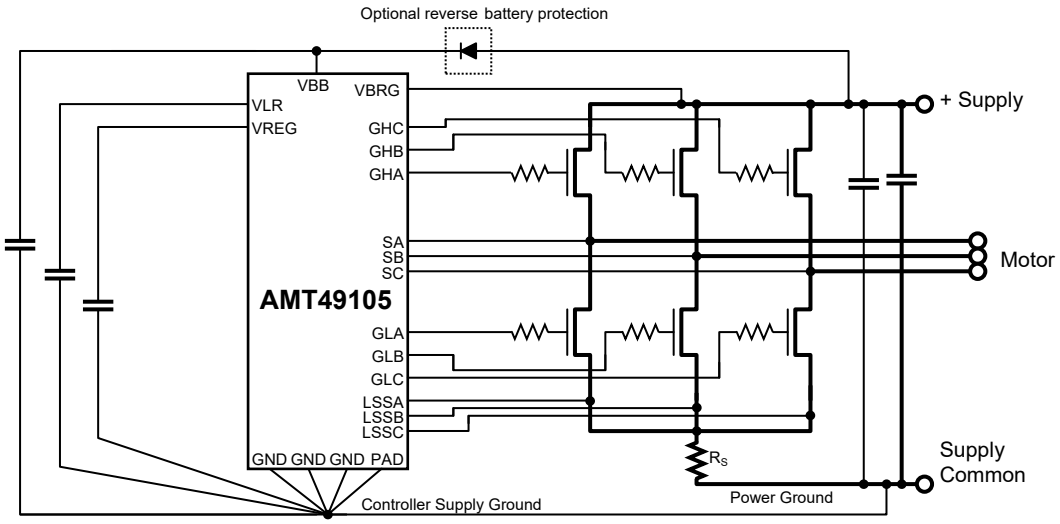

Figure 18: Supply Routing Suggestions

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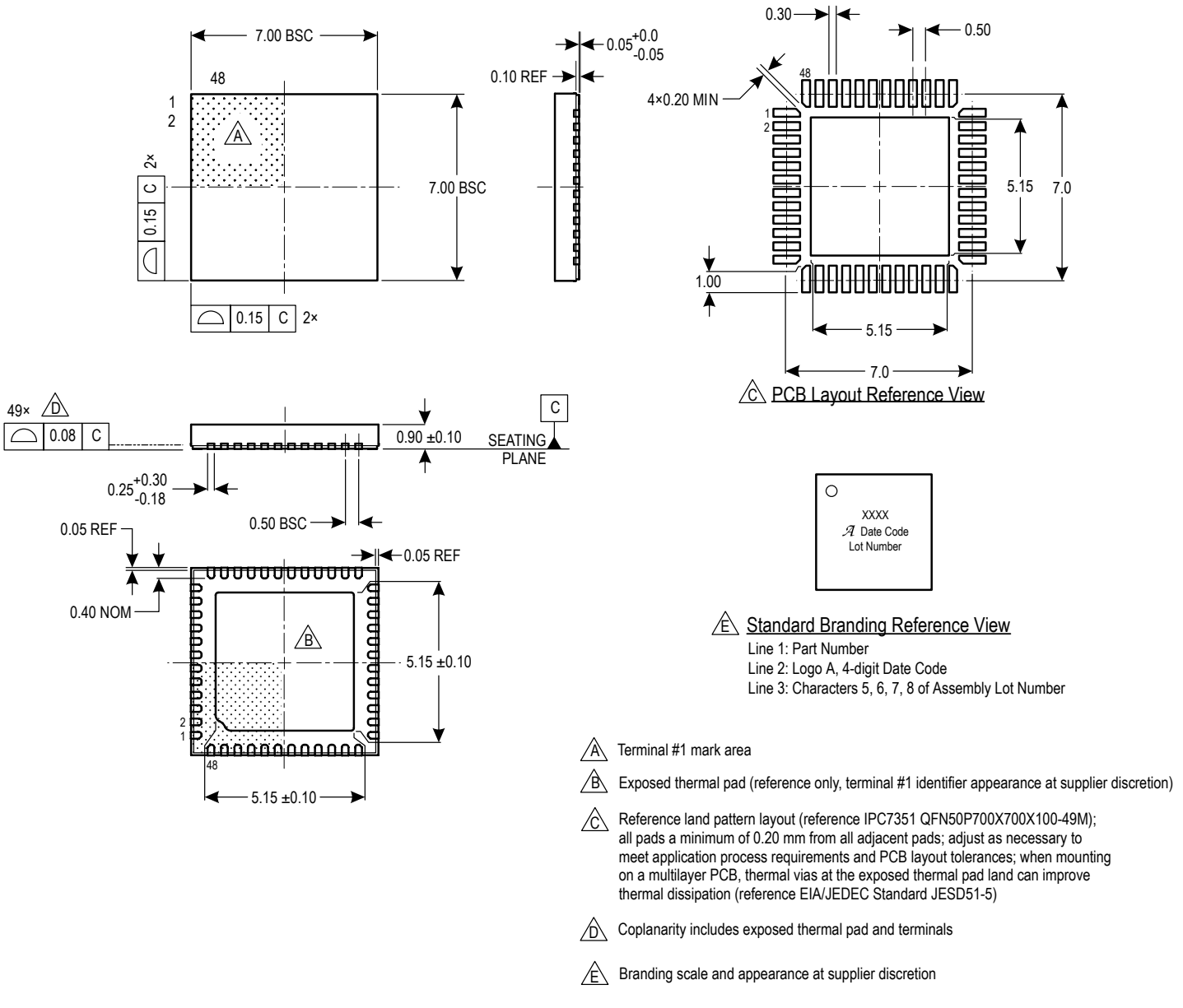
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference DWG-0000378, Rev. 3)
Dimensions in millimeters
NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P700X700X100-49M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Branding scale and appearance at supplier discretion

Figure 19: EV Package, 48-Pin QFN with Exposed Thermal Pad and Wettable Flank

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Revision History

Number	Date	Description
–	November 2, 2018	Initial release
1	December 12, 2018	Added ASIL logo; updated Features and Benefits
2	September 18, 2019	Corrected reel quantity in Selection Guide (page 2)
3	September 26, 2022	Updated package drawing (page 72)
4	October 7, 2025	Updated ASIL logo and text (page 1)

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