ARG81402

ISO 26262 ASIL Compliant

Multi-Output Regulator with Buck Pre-Regulator, 5× LDO Outputs, Watchdog, and SPI

FEATURES AND BENEFITS

- ASIL Compliant: ASIL D safety element out-of-context (SEooC) developed in accordance with ISO 26262, when used as specified in the safety manual
- Automotive AEC-Q100 qualified
- Control and diagnostic reporting through a serial peripheral interface (SPI)
- Wide input voltage range (6 to 36 V_{IN} operating range, 40 V_{IN} maximum)
- 2.2 MHz synchronous buck 5.35 V pre-regulator (VREG) for integration and efficiency
  - □ Frequency dithering and controlled slew rate helps reduce EMI/EMC
- Five internal linear regulators with foldback short-circuit protection
  - □ 3.3 V and 4× 5 V outputs (one with short- to-supply protection for remote sensors)
- Power-on reset signal indicating a fault on the 1.3 V monitor, 3V3, or V5A regulator outputs (NPOR)
- OV and UV protection for all output rails provides ability to monitor health of outputs
- Three configurable watchdogs with fail-safe features: pulse period, window, Q&A watchdog

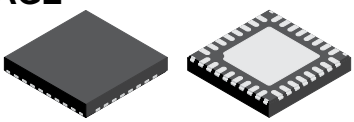
Continued on next page...

APPLICATIONS

Provides system power (for microcontroller/DSP, CAN, sensors, etc.) in:

- Industrial applications
- Electronic power steering (EPS)
- Advanced braking systems (ABS)
- Transmission control units (TCU)
- Emissions control modules
- Other automotive applications

PACKAGE



32-Pin QFN (suffix ET)

Not to scale

DESCRIPTION

The ARG81402 is designed to provide power to loads such as microprocessors, sensors, and communication transceivers, and is ideal for both automotive and industrial applications. It integrates a synchronous buck pre-regulator, five LDOs, a configurable Watchdog, and SPI communications interface.

The output of the pre-regulator supplies a 5 V/ 100 mA protected linear regulator, a 3.3 V / 300 mA linear regulator, a 5 V / 100 mA linear regulator, a 5 V / 55 mA linear regulator, and a 5 V / 30 mA linear regulator.

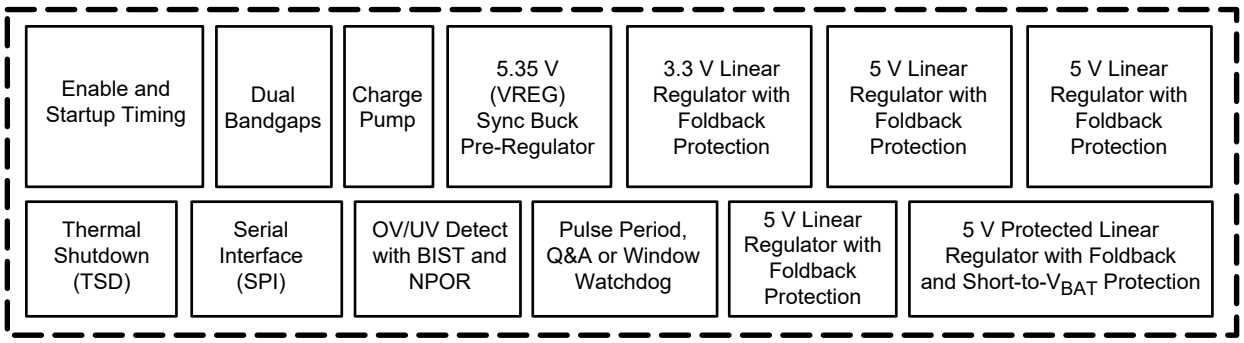
Enable inputs to the ARG81402 include a logic level (ENB) and a high voltage (ENBAT). The ARG81402 also provides flexibility with disable function of the individual 5 V rails through a serial peripheral interface (SPI).

Diagnostic outputs from the ARG81402 include a power-on-reset output (NPOR), an ENBAT status output, and a fault flag output to alert the microprocessor that a fault has occurred. The microprocessor can read fault status through SPI. Dual bandgaps—one for regulation and one for fault checking—improve safety coverage and fault detection of the ARG81402.

The ARG81402 contains three types of Watchdog functions: Pulse Period, Window, and Q&A watchdog timer. The Window and Q&A Watchdog is enabled through SPI, and the Pulse Period Watchdog timer is activated once it receives valid 2 ms pulses from the processor. It can be put into flash mode or reset via secure SPI commands.

Protection features include undervoltage and overvoltage on all output rails. All linear regulators feature foldback overcurrent protection. In addition, the V5P output is protected from a short-to-supply event. The switching regulator includes pulse-by-pulse current limit, hiccup mode short-circuit protection, LX short-circuit protection, and thermal shutdown.

The ARG81402 is supplied in a low-profile 32-lead, 5 mm × 5 mm, 0.5 mm pitch QFN package (suffix “ET”) with exposed thermal pad and wettable flank to allow solder joint inspection.



ARG81402 Simplified Block Diagram

FEATURES AND BENEFITS (continued)

- Power-on reset signal (NPOR) indicating a fault on the 3.3 V output, the optional 1.3 V input monitor (for self-powered core voltage), and a watchdog failure
- Safety signal (POE) can disable a separate function (e.g., Motor Driver) due to a Watchdog Failure
- Thermal shutdown protection
- –40°C to 150°C junction temperature range
- Pin-to-pin and pin-to-ground tolerant at every pin
- 5 mm × 5 mm eQFN wettable flank package for small solution size, good thermals, and guaranteed solder fillet

SELECTION GUIDE

Part Number	Temperature Range	Package	Packing [1]	Lead Frame
ARG81402KETATR	–40 to 150°C	32-pin QFN w/ thermal pad and wettable flank	1500 pieces per 7-inch reel	100% matte tin

[1] Contact Allegro for additional packing options.

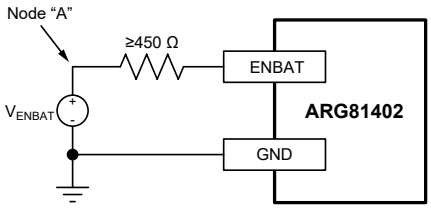
SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS [2]

Characteristic	Symbol	Notes	Rating	Unit
VIN	V_{VIN}		−0.3 to 40	V
ENBAT	V_{ENBAT}	With current limiting resistor [3]	−13 to 40	V
			−0.3 to 8	V
	I_{ENBAT}		±75	mA
LX	V_{LX}		−0.3 to V_{VIN} + 0.3	V
		t < 250 ns	−1.5	V
		t < 50 ns	V_{VIN} + 3	V
BOOT	V_{BOOT}		V_{VIN} + 7	V
VCP, CP1, CP2, VREG, LDOIN	V_{VCP}, V_{CP1}, V_{CP2}, V_{VREG}, V_{LDOIN}		−0.3 to 20	V
V5P	V_{V5P}	Independent of V_{VIN}	−1 to 20	V
All other pins			−0.3 to 7	V
Junction Temperature	T_J		−40 to 165	°C
Storage Temperature Range	T_{stg}		−40 to 150	°C

[2] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[3] The higher ENBAT ratings (–13 V and 40 V) are measured at node “A” in the following circuit configuration:



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THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions [4]	Value	Unit
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	QFN-32 (ET) package, 4-layer PCB based on JEDEC standard footprint	30	°C/W

[4] Additional thermal information available on the Allegro website.

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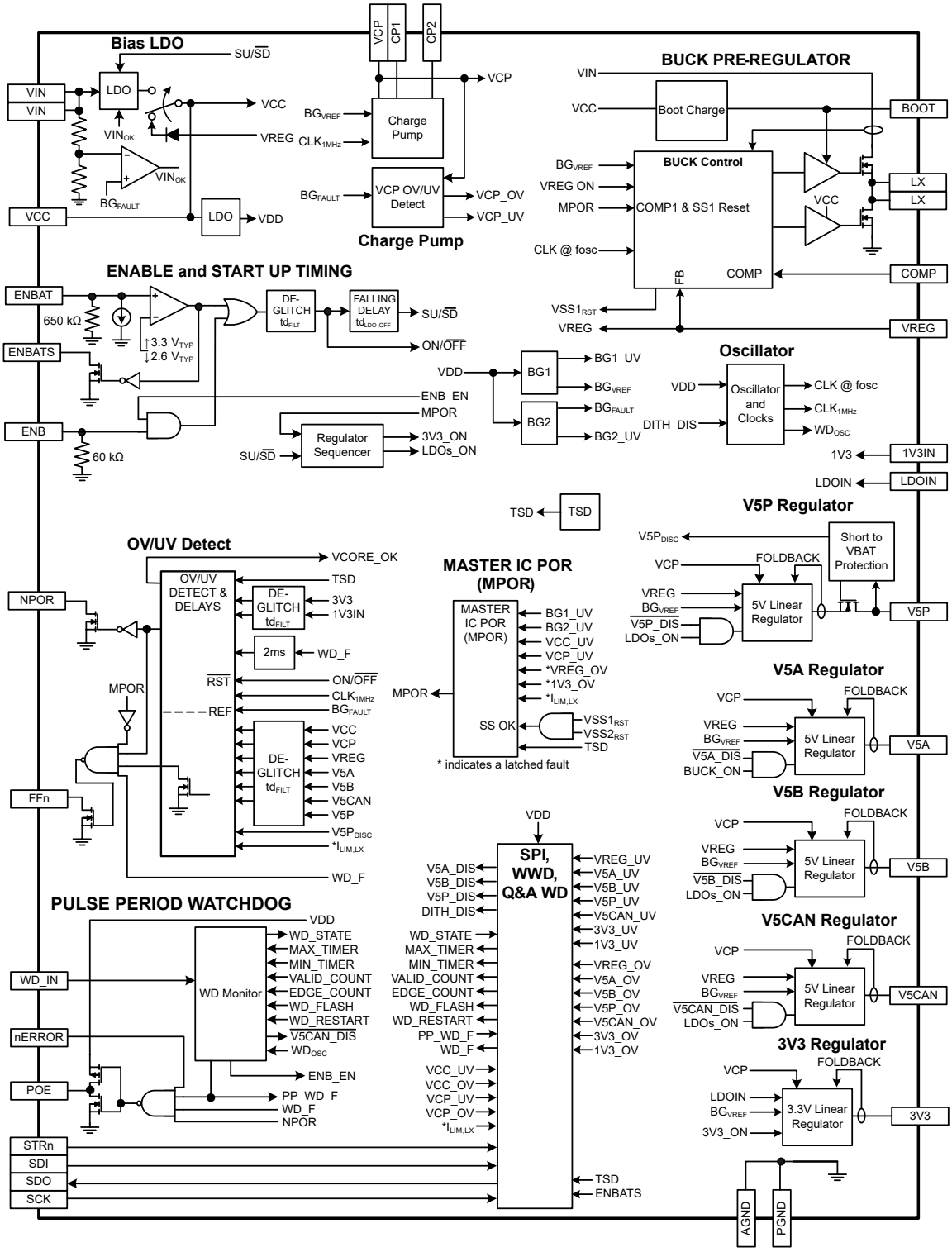
FUNCTIONAL BLOCK DIAGRAM



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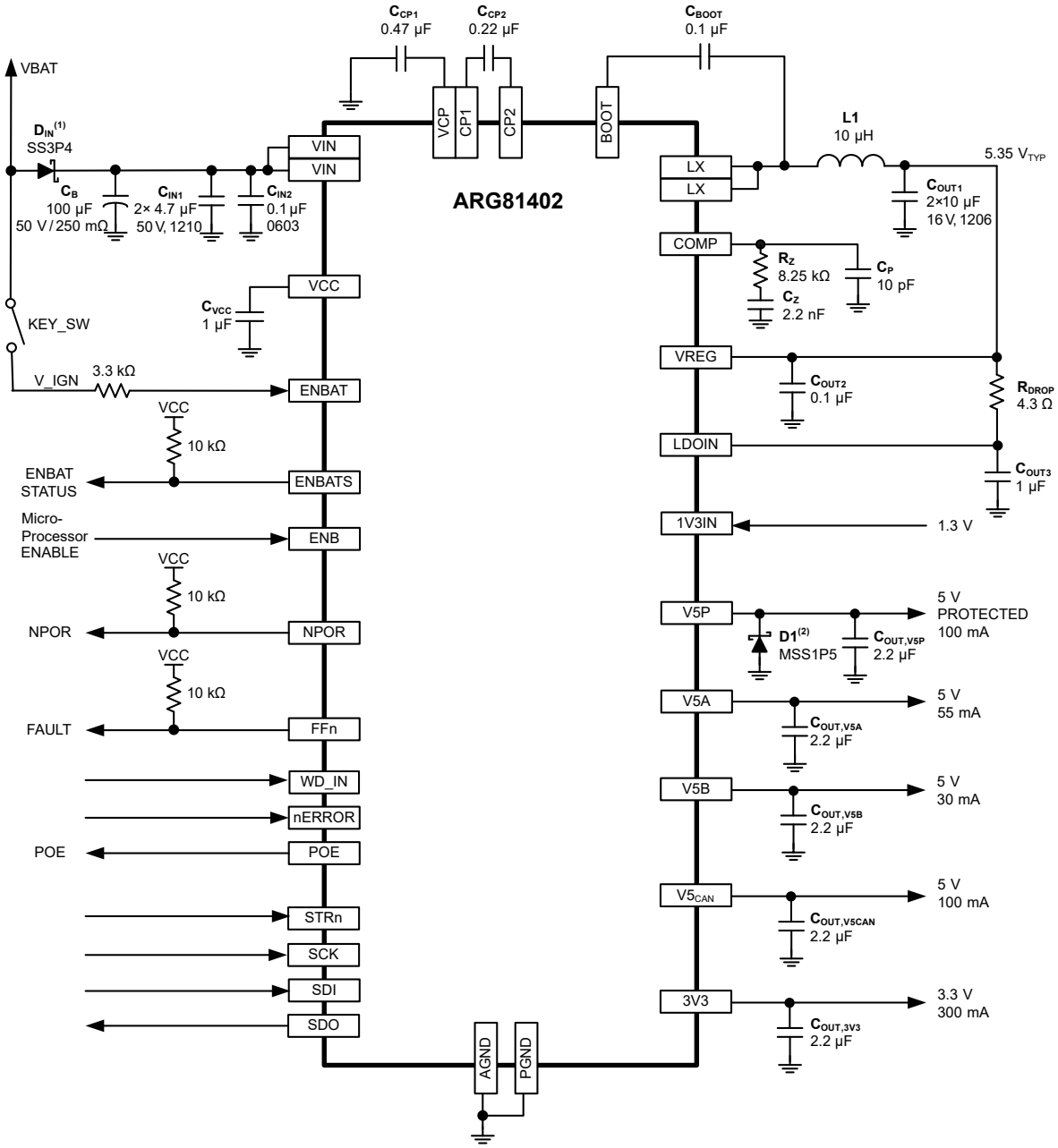
TYPICAL SCHEMATIC



Notes:

1. Using a series diode for reverse-battery protection (DIN).
2. Protection diodes D1 are required when the V5P pin is driving a wiring harness (or excessively long PCB trace) where parasitic inductance will cause negative spikes on the V5P pin if a short occurs. It is recommended to use a small diode to clamp this negative spike. A MSSP5 is recommended.

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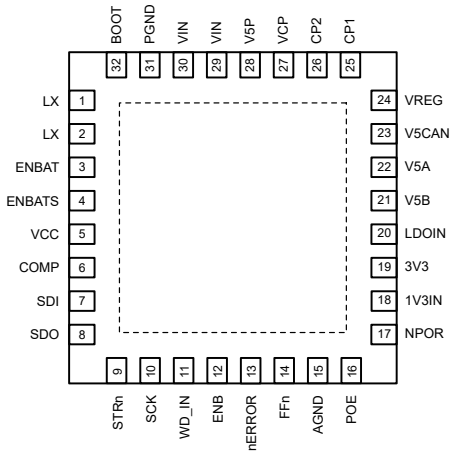
PINOUT DIAGRAM AND TERMINAL LIST



Package ET, 32-Pin QFN
Pinout Diagram

Terminal List Table

Number	Name	Function
1, 2	LX	Switching node for the buck pre-regulator.
3	ENBAT	Ignition enable input from the key/switch via a series resistor.
4	ENBATS	Open drain ignition status output of ENBAT.
5	VCC	Internal voltage regulator bypass capacitor pin, place a 1 µF capacitor to PGND pin.
6	COMP	Compensation pin for synchronous buck pre-regulator. Connect compensation network from this pin to ground to ensure stable operation of the pre-regulator.
7	SDI	SPI data input from the microcontroller.
8	SDO	SPI data output to the microcontroller.
9	STRn	Chip select input from the microcontroller.
10	SCK	Clock input from the microcontroller.
11	WD_IN	Watchdog pulse train input from a microcontroller or DSP.
12	ENB	Logic enable input from a micro-controller or DSP.
13	nERROR	System fault input. This fault is ANDed with the watchdog fault to create the POE signal. Allows for external fault to pull POE low.
14	FFn	Open-drain active-low fault flag or interrupt signal to alert the microprocessor of a fault within the regulator. The microprocessor can then read the fault condition through SPI.
15	AGND	Signal ground pin
16	POE	Safe state signal. Goes low if a watchdog fault is detected or nERROR is low. This is a push-pull output and does not require any external pull-up or pull-down. 2.85 V_{MIN} when high.
17	NPOR	Active-low, open-drain regulator fault detection output.
18	1V3IN	Input to 1.3 V monitoring circuits. Reports OV and UV through NPOR and SPI.
19	3V3	3.3 V regulator output. Capable of delivering 300 mA DC.
20	LDOIN	Input to 3.3V LDO. Connect to VREG through a resistor. Helps remove power dissipation from IC.
21	V5B	5 V regulator output. Capable of delivering 30 mA DC.
22	V5A	5 V regulator output. Capable of delivering 55 mA DC.
23	V5CAN	5 V regulator output for communications. Capable of delivering 100mA DC.
24	VREG	Output of the pre-regulator and input to the linear regulators.
25	CP1	Charge pump capacitor connection. Connect a 220 nF capacitor from this pin to the CP2 pin.
26	CP2	Charge pump capacitor connection. Connect a 220 nF capacitor from this pin to the CP1 pin.
27	VCP	Charge pump reservoir capacitor. Connect a 0.47 µF cap from this pin to the PGND pin.
28	V5P	5 V protected regulator output with short-to-battery protection. Capable of delivering 100 mA DC.
29,30	VIN	Input voltage pins. Place high frequency decoupling capacitor from this pin to the PGND.
31	PGND	Power ground for the synchronous pre-regulator; see VIN pin description.
32	BOOT	Boot capacitor connection for buck pre-regulator high-side driver. Connect a 0.1 µF capacitor from this pin to the LX pin.

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ELECTRICAL CHARACTERISTICS – GENERAL SPECIFICATIONS [1]: Valid at 6 V ≤ V_{VIN} ≤ 36 V, –40°C ≤ T_J ≤ 150°C, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL SPECIFICATIONS						
Operating Input Voltage	V_{VIN}	V_{ENB} > 2 V or V_{ENBAT} > 3.5 V	6.0	13.5	36	V
VIN UVLO START Voltage	$V_{VIN(START)}$	V_{VIN} rising	5.40	5.7	5.95	V
VIN UVLO STOP Voltage	$V_{VIN(STOP)}$	V_{VIN} falling, V_{ENBAT} ≥ 3.8 V or V_{ENB} ≥ 2 V, V_{VREG} = 5.2 V	4.0	4.25	4.5	V
VIN UVLO Hysteresis	$V_{VIN(HYS)}$	$V_{VIN(START)}$ – $V_{VIN(STOP)}$	–	1.3	–	V
Supply Quiescent Current [1]	I_Q	V_{VIN} = 13.5 V, V_{ENBAT} ≥ 3.8 V or V_{ENB} ≥ 2.0 V, V_{VREG} = 5.6 V (no PWM)	–	20	–	mA
	$I_{Q(SLEEP)}$	V_{VIN} = 13.5 V, V_{ENBAT} ≤ 2.2 V and V_{ENB} ≤ 0.8 V, −40°C ≤ T_J ≤ 85°C [3]	–	–	10	µA
PWM SWITCHING FREQUENCY AND DITHERING						
Switching Frequency	f_{OSC}	Dithering disabled	2.0	2.2	2.4	MHz
Frequency Dithering	Δf_{OSC}	As a percent of f_{OSC}	–	±10	–	%
Dither/Slew START Threshold	$V_{VIN(DS,ON)}$	V_{VIN} rising	8.5	9.0	9.5	V
		V_{VIN} falling	–	17	–	V
Dither/Slew STOP Threshold	$V_{VIN(DS,OFF)}$	V_{VIN} falling	7.8	8.3	8.8	V
		V_{VIN} rising	–	18	–	V
VIN Dithering/Slew Hysteresis	$V_{VIN(DS,HYS)}$	V_{VIN} < 9 V	–	0.7	–	V
		V_{VIN} > 16 V	–	1.4	–	V
CHARGE PUMP (VCP)						
Output Voltage	V_{VCP}	V_{VIN} ≥ 6.0 V	7.9	9.0	11.0	V
Switching Frequency	$f_{SW(VCP)}$		–	62.5	–	kHz
VCC PIN VOLTAGE						
Output Voltage	V_{VCC}	V_{VREG} = 5.35 V	–	4.65	–	V
THERMAL PROTECTION						
Thermal Shutdown Threshold [2]	T_{TSD}	T_J rising	165	–	–	°C
Thermal Shutdown Hysteresis [2]	T_{HYS}		–	15	–	°C

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[2] Specifications at 25°C or 85°C are guaranteed by design and characterization, not production tested.

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ELECTRICAL CHARACTERISTICS – BUCK PRE-REGULATOR SPECIFICATIONS [1]: Valid at 6 V ≤ V_{VIN} ≤ 36 V, –40°C ≤ T_J ≤ 150°C, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
OUTPUT VOLTAGE SPECIFICATIONS						
Buck Output Voltage Regulation [2]	V_{VREG}	8 V ≤ V_{VIN} ≤ 20 V, 0.1 A ≤ I_{VREG} ≤ 0.6 A, f_{SW} = 2.2 MHz, ENB = 1	5.25	5.35	5.45	V
PULSE-WIDTH MODULATION (PWM)						
PWM Ramp Offset	$V_{PWM(OFFS)}$	V_{COMP} for 0% duty cycle	–	400	–	mV
LX Rising Slew Rate Control [2]	$SR_{LX(RISE)}$	V_{VIN} = 13.5 V, 10% to 90%, I_{VREG} = 0.6 A	–	1.4	–	V/ns
LX Falling Slew Rate [2]	$SR_{LX(FALL)}$	V_{VIN} = 13.5 V, 90% to 10%, I_{VREG} = 0.6 A	–	1.5	–	V/ns
Minimum On-Time	$t_{ON(MIN)}$		–	90	120	ns
Minimum Off-Time	$t_{OFF(MIN)}$		–	90	120	ns
INTERNAL MOSFET						
High-Side MOSFET On-Resistance	$R_{ds(on)HS}$	V_{VIN} = 13.5 V, T_J = –40°C [2], I_{DS} = 0.6 A	–	82	102	mΩ
		V_{VIN} = 13.5 V, T_J = 25°C [3], I_{DS} = 0.6 A	–	112	130	mΩ
		V_{VIN} = 13.5 V, T_J = 150°C, I_{DS} = 0.1 A	–	162	205	mΩ
Low-Side MOSFET On-Resistance	$R_{ds(on)LS}$	V_{VIN} = 13.5 V, T_J = –40°C [2], I_{DS} = 0.6 A	–	123	155	mΩ
		V_{VIN} = 13.5 V, T_J = 25°C [3], I_{DS} = 0.6 A	–	172	198	mΩ
		V_{VIN} = 13.5 V, T_J = 150°C, I_{DS} = 0.1 A	–	252	300	mΩ

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ELECTRICAL CHARACTERISTICS – BUCK PRE-REGULATOR SPECIFICATIONS (continued) [1]:
Valid at 6 V ≤ V_{VIN} ≤ 36 V, –40°C ≤ T_J ≤ 150°C, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SOFT-START						
SS Ramp Time	t_{SS}		–	0.9	–	ms
SS PWM Frequency Foldback	$f_{SW(SS)}$	0 V ≤ V_{VREG} < 1.34 V typical and V_{COMP} < $V_{O(EA,MAX)}$	–	f_{OSC} / 4	–	–
		1.34 V ≤ V_{VREG} < 2.68 V typical and V_{COMP} < $V_{O(EA,MAX)}$	–	f_{OSC} / 2	–	–
		V_{VREG} ≥ 2.68 V typical and V_{COMP} < $V_{O(EA,MAX)}$	–	f_{OSC}	–	–
HICCUP MODE						
Hiccup OCP PWM Counts	$t_{HIC(OCP)}$	V_{VREG} < 1.95 V_{TYP}, V_{COMP} = $V_{O(EA,MAX)}$	–	64	–	PWM cycles
		V_{VREG} > 1.95 V_{TYP}, V_{COMP} = $V_{O(EA,MAX)}$	–	120	–	PWM cycles
CURRENT PROTECTIONS						
Pulse-by-Pulse Current Limit	$I_{LIM(ton,min)}$		1.4	1.55	1.7	A
LX Short-Circuit Current Limit	$I_{LIM(LX)}$	Latched fault after 3rd detection	2.3	3.0	3.7	A

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ELECTRICAL CHARACTERISTICS – LINEAR REGULATOR SPECIFICATIONS [1]:

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
V5CAN, V5A, V5B, AND V5P LINEAR REGULATORS						
V5CAN Accuracy and Load Regulation	V_{V5CAN}	10 mA < I_{V5CAN} < 100 mA, V_{VREG} = 5.25 V	4.9	5.0	5.1	V
V5CAN Output Capacitance Range [2]	$C_{OUT(V5CAN)}$		1.0	–	15	µF
V5A Accuracy and Load Regulation	V_{V5A}	5 mA < I_{V5A} < 55 mA, V_{VREG} = 5.25 V	4.9	5.0	5.1	V
V5A Output Capacitance Range [2]	$C_{OUT(V5A)}$		1.0	–	15	µF
V5B Accuracy and Load Regulation	V_{V5B}	5 mA < I_{V5B} < 30 mA, V_{VREG} = 5.25 V	4.9	5.0	5.1	V
V5B Output Capacitance Range [2]	$C_{OUT(V5B)}$		1.0	–	15	µF
V5P Accuracy and Load Regulation	V_{V5P}	5 mA < I_{V5P} < 100 mA, V_{VREG} = 5.25 V	4.9	5.0	5.1	V
V5P Output Capacitance Range [2]	$C_{OUT(V5P)}$		1.0	–	15	µF
V5CAN OVERCURRENT PROTECTION						
V5CAN Current Limit [1]	$I_{LIM(V5CAN)}$	V_{V5CAN} = $V_{V5(UV,L)}$, when FFn goes low	−120	−155	−220	mA
V5CAN Foldback Current [1]	$I_{FBK(V5CAN)}$	V_{V5CAN} = 0 V	−30	−40	−90	mA
V5A OVERCURRENT PROTECTION						
V5A Current Limit [1]	$I_{LIM(V5A)}$	V_{V5A} = $V_{V5(UV,L)}$, when FFn goes low	−60	−100	−140	mA
V5A Foldback Current [1]	$I_{FBK(V5A)}$	V_{V5A} = 0 V	−15	−30	−55	mA
V5B OVERCURRENT PROTECTION						
V5B Current Limit [1]	$I_{LIM(V5B)}$	V_{V5B} = $V_{V5(UV,L)}$, when FFn goes low	−50	−90	−145	mA
V5B Foldback Current [1]	$I_{FBK(V5B)}$	V_{V5B} = 0 V	−15	−20	−55	mA
V5P OVERCURRENT PROTECTION						
V5P Current Limit [1]	$I_{LIM(V5P)}$	V_{V5P} = $V_{V5(UV,L)}$, when FFn goes low	−110	−155	−220	mA
V5P Foldback Current [1]	$I_{FBK(V5P)}$	V_{V5P} = 0 V	−10	−40	−70	mA
V5CAN, V5A, V5B, AND V5P STARTUP TIMING						
V5CAN Startup Time [2]	$t_{V5CAN(START)}$	C_{V5CAN} ≤ 2.9 µF, Load = 200 Ω ±5% (25 mA)	–	0.4	1.0	ms
V5A Startup Time [2]	$t_{V5A(START)}$	C_{V5A} ≤ 2.9 µF, Load = 200 Ω ±5% (25 mA)	–	0.6	1.0	ms
V5B Startup Time [2]	$t_{V5B(START)}$	C_{V5B} ≤ 2.9 µF, Load = 333 Ω ±5% (15 mA)	–	0.8	1.0	ms
V5P Startup Time [2]	$t_{V5C(START)}$	C_{V5P} ≤ 2.9 µF, Load = 100 Ω ±5% (50 mA)	–	0.5	1.0	ms
3V3 LINEAR REGULATOR						
3V3 Accuracy and Load Regulation	V_{3V3}	5 mA < I_{3V3} < 300 mA, V_{VREG} = 5.25 V	3.23	3.30	3.37	V
3V3 Output Capacitance Range [2]	$C_{OUT(3V3)}$		1.0	–	15	µF
3V3 OVERCURRENT PROTECTION						
3V3 Current Limit [1]	$I_{LIM(3V3)}$	V_{3V3} = $V_{3V3(UV,L)}$, when FFn goes low	−360	−500	−640	mA
3V3 Foldback Current [1]	$I_{FBK(3V3)}$	V_{3V3} = 0 V	−60	−160	−250	mA
3V3 STARTUP TIMING						
3V3 Startup Time [2]	$t_{3V3(START)}$	C_{3V3} ≤ 2.9 µF, Load = 18 Ω ±5% (180 mA)	–	0.5	0.8	ms

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ELECTRICAL CHARACTERISTICS – CONTROL INPUTS [1]: Valid at 6 V ≤ V_{VIN} ≤ 36 V, –40°C ≤ T_J ≤ 150°C, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
IGNITION ENABLE (ENBAT) INPUT						
ENBAT Thresholds	$V_{ENBAT(H)}$	V_{ENBAT} rising	2.8	3.1	3.5	V
	$V_{ENBAT(L)}$	V_{ENBAT} falling	2.2	2.6	2.8	V
ENBAT Hysteresis	$V_{ENBAT(HYS)}$	$V_{ENBAT(H)} – V_{ENBAT(L)}$	–	500	–	mV
ENBAT Bias Current [1]	$I_{ENBAT(BIAS)}$	V_{ENBAT} = 5.5 V via a 1 kΩ series resistor	–	50	100	µA
		V_{ENBAT} = 0.8 V via a 1 kΩ series resistor	0.5	–	5	µA
ENBAT Pull-Down Resistance	R_{ENBAT}	V_{ENBAT} < 1.2 V	–	600	–	kΩ
LOGIC ENABLE (ENB) INPUT						
ENB Thresholds	$V_{ENB(H)}$	V_{ENB} rising	–	–	2.0	V
	$V_{ENB(L)}$	V_{ENB} falling	0.8	–	–	V
ENB Bias Current [1]	$I_{ENB(IN)}$	V_{ENB} = 3.3 V	–	–	175	µA
ENB Resistance	R_{ENB}		–	60	–	kΩ
ENB/ENBAT FILTER/DEGLITCH						
Enable Filter/Deglitch Time	$t_{dFILT(EN)}$		10	15	20	µs
nERROR INPUT						
nERROR Thresholds	$V_{nERROR(H)}$	V_{nERROR} rising	–	–	2	V
	$V_{nERROR(L)}$	V_{nERROR} falling	0.8	–	–	V

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ELECTRICAL CHARACTERISTICS – DIAGNOSTIC OUTPUTS [1]: Valid at 6 V ≤ V_{VIN} ≤ 36 V, –40°C ≤ T_J ≤ 150°C, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
3V3 AND 1V3IN OV/UV PROTECTION THRESHOLDS						
3V3 OV Thresholds	$V_{3V3(OV,H)}$	V_{3V3} rising	3.41	3.51	3.60	V
	$V_{3V3(OV,L)}$	V_{3V3} falling	–	3.49	–	V
3V3 OV Hysteresis	$V_{3V3(OV,HYS)}$	$V_{3V3(OV,H)} – V_{3V3(OV,L)}$	10	20	40	mV
3V3 UV Thresholds	$V_{3V3(UV,H)}$	V_{3V3} rising	–	3.12	–	V
	$V_{3V3(UV,L)}$	V_{3V3} falling	3.00	3.1	3.19	V
3V3 UV Hysteresis	$V_{3V3(UV,HYS)}$	$V_{3V3(UV,H)} – V_{3V3(UV,L)}$	10	20	40	mV
1V3IN OV Thresholds	$V_{1V3IN(OV,H)}$	V_{1V3IN} rising	1.35	1.41	1.45	V
1V3IN UV Thresholds	$V_{1V3IN(UV,H)}$	V_{1V3IN} rising	1.13	1.17	1.21	V
	$V_{1V3IN(UV,L)}$	V_{1V3IN} falling	1.12	1.14	1.15	V
V5CAN, V5A, V5B, AND V5P OV/UV PROTECTION THRESHOLDS						
V5CAN, V5A, V5B, and V5P OV Thresholds	$V_{V5(OV,H)}$	V_{V5} rising	5.15	5.33	5.50	V
	$V_{V5(OV,L)}$	V_{V5} falling	–	5.30	–	V
V5CAN, V5A, V5B, and V5P OV Hysteresis	$V_{V5(OV,HYS)}$	$V_{V5(OV,H)} – V_{V5(OV,L)}$	–	30	–	mV
V5CAN, V5A, V5B, and V5P UV Thresholds	$V_{V5(UV,H)}$	V_{V5} rising	–	4.71	–	V
	$V_{V5(UV,L)}$	V_{V5} falling	4.50	4.68	4.85	V
V5CAN, V5A, V5B, and V5P UV Hysteresis	$V_{V5(UV,HYS)}$	$V_{V5(UV,H)} – V_{V5(UV,L)}$	–	30	–	mV
V5P Output Disconnect Threshold	$V_{V5P(DISC)}$	V_{V5P} rising	–	7.2	–	V
VREG, VCP, AND BG THRESHOLDS						
VREG Non-Latching OV Threshold	$V_{VREG(OV1,H)}$	V_{VREG} rising, LX1 PWM disabled, as a percent of V_{VREG}	102	104	107	%
	$V_{VREG(OV1,L)}$	V_{VREG} falling, LX1 PWM enabled, as a percent of V_{VREG}	–	103	–	%
VREG Non-Latching OV Hysteresis	$V_{VREG(OV1,HYS)}$	As a percent of V_{VREG}	–	1	–	%
VREG Latching OV Threshold	$V_{VREG(OV2,H)}$	V_{VREG} rising, all regulators latched off	–	6.55	–	V
VREG UV Thresholds	$V_{VREG(UV,H)}$	V_{VREG} rising, triggers rise of 3V3 linear regulator	4.14	4.38	4.62	V
	$V_{VREG(UV,L)}$	V_{VREG} falling	–	4.28	–	V
VREG UV Hysteresis	$V_{VREG(UV,HYS)}$	$V_{VREG(UV,H)} – V_{VREG(UV,L)}$	–	100	–	mV
VCP OV Thresholds	$V_{VCP(OV,H)}$	V_{VCP} rising	12.2	–	12.8	V
	$V_{VCP(OV,L)}$	V_{VCP} falling	–	11.55	–	V
VCP OV Hysteresis	$V_{VCP(OV,HYS)}$	$V_{VCP(OV,H)} – V_{VCP(OV,L)}$	–	950	–	mV
VCP UV Thresholds	$V_{VCP(UV,H)}$	V_{VCP} rising	6.0	–	6.6	V
	$V_{VCP(UV,L)}$	V_{VCP} falling	5.6	–	6.2	V
VCP UV Hysteresis	$V_{VCP(UV,HYS)}$	$V_{VCP(UV,H)} – V_{VCP(UV,L)}$	–	400	–	mV

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ELECTRICAL CHARACTERISTICS – DIAGNOSTIC OUTPUTS (continued) [1]:

Valid at 6 V ≤ V_{VIN} ≤ 36 V, –40°C ≤ T_J ≤ 150°C, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
NPOR TURN-ON AND TURN-OFF DELAYS						
NPOR Turn-On Delay	$t_{dNPOR(ON)}$	Time from when 3V3 and 1V3IN are in regulation to NPOR being asserted high	15	20	25	ms
NPOR OUTPUT VOLTAGES						
NPOR Output Low Voltage	$V_{NPOR(L)}$	ENB or ENBAT high, V_{VIN} ≥ 2.5 V, I_{NPOR} = 2 mA	–	150	400	mV
NPOR Leakage Current [1]	$I_{NPOR(LKG)}$	V_{NPOR} = 3.3 V	–	–	2	µA
FAULT FLAG OUTPUT VOLTAGES (FFn)						
FFn Output Voltage	$V_{FF(L)}$	ENB = 1 or ENBAT = 1 and FFn is tripped, V_{VIN} ≥ 2.5 V, I_{FF} = 2 mA	–	150	400	mV
FFn Leakage Current	$I_{FF(LKG)}$	V_{FF}= 3.3 V	–	–	2	µA
IGNITION STATUS (ENBATS)						
ENBATS Output Voltage	$V_{ENBATS(LO)}$	I_{ENBATS} = 2 mA, V_{ENBAT} < $V_{ENBAT(L)}$	–	–	400	mV
ENBATS Leakage Current [1]	I_{ENBATS}	V_{ENBATS} = 3.3 V	–	–	2	µA
OV FILTERING/DEGLITCH TIME						
Overvoltage Detection Delay	$t_{dFILT(OV)}$	Overvoltage detection delay time	10	15	20	µs
UV FILTERING/DEGLITCH TIME						
UV Filter/Deglitch Times	$t_{dFILT(UV)}$	Undervoltage detection delay time	10	15	20	µs

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ELECTRICAL CHARACTERISTICS – WINDOW WATCHDOG TIMER (WWDT) [1]:

Valid at 6 V ≤ V_{VIN} ≤ 36 V, –40°C ≤ T_J ≤ 150°C, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
WD_IN VOLTAGE THRESHOLDS AND CURRENT						
WD_IN Input Voltage Thresholds	$V_{WD\_IN(LO)}$	V_{WD_IN} falling	0.8	–	–	V
	$V_{WD\_IN(HI)}$	V_{WD_IN} rising	–	–	2.0	V
WD_IN Pull-Down Resistance [2]	R_{WD_IN}		–	50	–	kΩ
WD_IN TIMING SPECIFICATIONS						
Pulse Period WD_IN Frequency	f_{WD_IN}		–	500	–	Hz
WD Clock Tolerance	$f_{SYS(TOL)}$		–4	–	4	%
Window WD_IN “SLOW” Nominal Frequency Range	$f_{WD\_IN(SLOW)}$		10	–	250	Hz
Window WD_IN “FAST” Nominal Frequency Range	$f_{WD\_IN(FAST)}$		80	–	2000	Hz
WD_IN Pulse High Time	$t_{WD\_IN(HI)}$		50	–	–	µs
WD_IN Pulse Low Time	$t_{WD\_IN(LO)}$		50	–	–	µs
WATCHDOG ONE-SHOT TIME						
WD Pulse Time After Window or Q&A Watchdog Fault	$t_{WD(FAULT)}$		1.9	2	2.1	ms
GATE DRIVE ENABLE (POE)						
POE Output Voltage	$V_{POE(L)}$	I_{POE} = 4 mA	–	150	400	mV
POE Output Voltage	$V_{POE(H)}$	I_{POE} = –3.5 mA	2.85	–	–	V
Power Supply Disable Delay	$t_{PS(DISABLE)}$	Time from POE going low due to watchdog fault to V5CAN starts to decay	–	250	–	ms
Anti-Latchup Timeout	$t_{ANTI\_LATCHUP}$	Time from POE going low due to watchdog fault to when enable control is removed from the ENB pin	–	10	–	s

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ELECTRICAL CHARACTERISTICS – COMMUNICATIONS INTERFACE [1]:

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SERIAL INTERFACE (STRn, SDI, SDO, SCK)						
Input Low Voltage	V_{IL}		–	–	0.8	V
Input High Voltage	V_{IH}	All logic inputs	2.0	–	–	V
Input Hysteresis	V_{Ihys}	All logic inputs	250	550	–	mV
Input Pull-Down SDI, SCK	R_{PDS}	0 V < V_{VIN} < 5 V	–	50	–	kΩ
Input Pull-Up To VCC	I_{PU}	STRn	–	50	–	kΩ
Output Low Voltage	V_{OL}	I_{OL} = 1 mA [1]	–	0.2	0.4	V
Output High Voltage	V_{OH}	I_{OL} = –1 mA [1]	2.8	V_{DD} – 0.2	–	V
Output Leakage [1]	$I_{SDO(LKG)}$	0 V < V_{SDO} < 5.5 V, STRn = 1	–1	–	1	µA
Clock High Time	t_{SCKH}	A in figure 4	50	–	–	ns
Clock Low Time	t_{SCKL}	B in figure 4	50	–	–	ns
Strobe Lead Time	t_{STLD}	C in figure 4	30	–	–	ns
Strobe Lag Time	t_{STLG}	D in figure 4	30	–	–	ns
Strobe High Time	t_{STRH}	E in figure 4	300	–	–	ns
Data Out Enable Time [2]	t_{SDOE}	F in figure 4	–	–	40	ns
Data Out Disable Time [2]	t_{SDOD}	G in figure 4	–	–	30	ns
Data Out Valid Time From Clock Falling [2]	t_{SDOV}	H in figure 4	–	–	40	ns
Data Out Hold Time From Clock Falling [2]	t_{SDOH}	J in figure 4	5	–	–	ns
Data In Setup Time To Clock Rising	t_{SDIS}	K in figure 4	15	–	–	ns
Data In Hold Time From Clock Rising	t_{SDIH}	L in figure 4	10	–	–	ns
Wake Up From Sleep	t_{EN}		–	–	2	ms

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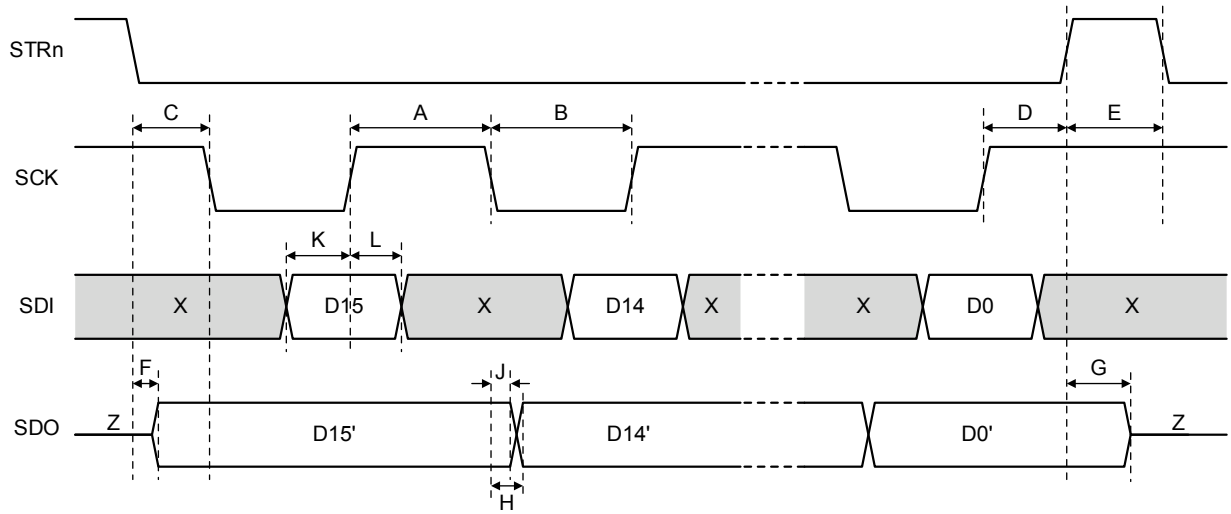

Figure 1: Serial Interface Timing
X = don't care; Z = high-impedance (tri-state)

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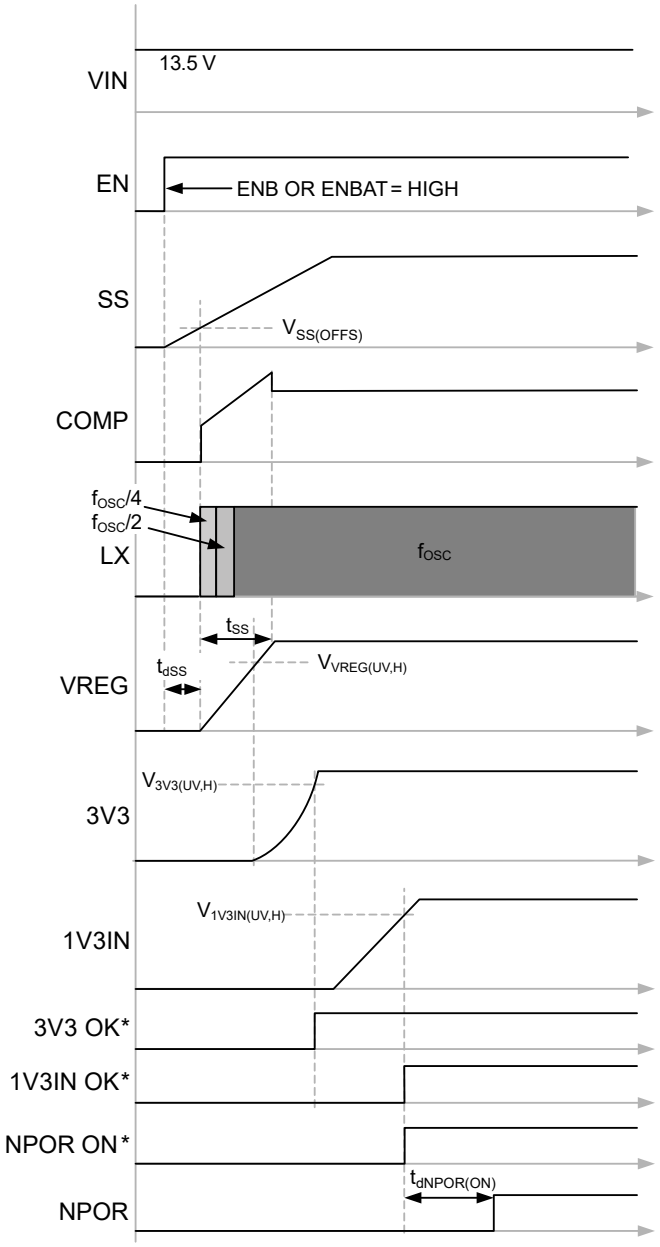

Figure 2: Startup Timing Diagram

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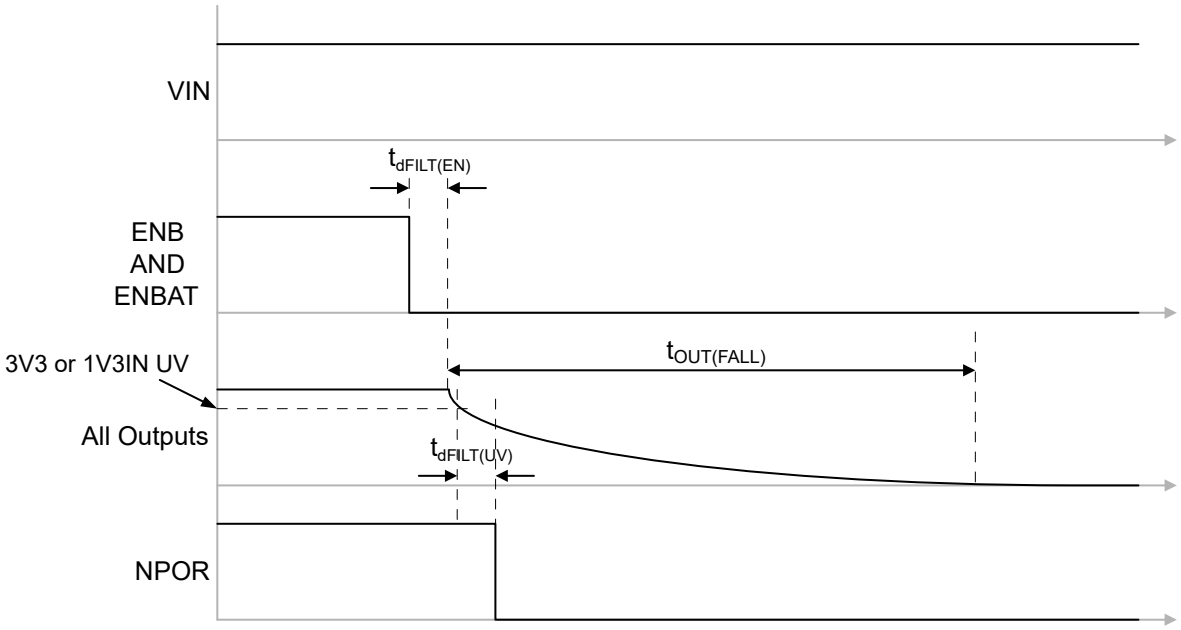

All outputs start to decay $t_{dFILT(EN)}$ seconds after ENB and ENBAT are low.
Time for outputs to drop to zero, $t_{OUT(FALL)}$, various for each output and depends on load current and capacitance.
NPOR falls when 3V3 or 1V3IN reaches its UV point.

Figure 3: Shutdown Timing Diagram

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Table 1: Summary of Fault Mode Operation

FAULT TYPE and CONDITION	ARG81402 RESPONSE TO FAULT	LATCHED FAULT?	VCC	VCP	VREG	3V3	V5CAN	V5A	V5B	V5P	NPOR	FFn	POE	SPI	WD	RESET METHOD
LATCHING FAULTS																
VREG overvoltage $V_{VREG} > V_{REGOV2(H)}$	Results in an MPOR after 1 detection, so all regulators are shut off	Yes	No effect	No effect	Off	Off	Off	Off	Off	Off	Low	Low	Low	On	On	Check the short/ Cycle EN or VIN / replace ARG81402
1V3IN overvoltage	If OV condition persists for more than t_{dOV}, then set NPOR low and shut off all regulators	Yes	No effect	No effect	Off	Off	Off	Off	Off	Off	Low	Low	Low	On	On	Check for short circuits then cycle EN or VIN
LX shorted to ground	Results in an MPOR after the high side MOSFET current exceeds $I_{LIM(LX)}$ so all regulators are shut off	Yes	No effect	No effect	Off	Off	Off	Off	Off	Off	Low if V_{3V3} or V_{1V3IN} are too low	Low	Low	On	On	Remove the short then cycle EN or VIN
NON-LATCHING FAULTS																
VIN UVLO	ARG81402 is in reset state	No	Ramping	VIN	Off	Off	Off	Off	Off	Off	Low if V_{3V3} or V_{1V3IN} are too low	Low	Low	Off	Off	None
VCC UVLO	ARG81402 is in reset state	No	On	VIN	Off	Off	Off	Off	Off	Off	Low if V_{3V3} or V_{1V3IN} are too low	Low	Low	Off	Off	None
VCC short limit	ARG81402 is in reset state	No	UVLO	VIN	Off	Off	Off	Off	Off	Off	Low if V_{3V3} or V_{1V3IN} are too low	Low	Low	Off	Off	None
CP UVLO	If UV condition persists for more than t_{dUV} then set FFn Low	No	On	Ramping	Off	Off	Off	Off	Off	Off	Low if V_{3V3} or V_{1V3IN} are too low	Low	Low	On	On	None
CP OV	If OV condition persists for more than t_{dOV} then set FFn Low	No	No effect	< 2 × V_{VREG}	On	On	On	On	On	On	High	Low	High	On	On	None
VREG overvoltage $V_{VREG} > V_{VREGOV1(H)}$	Stop PWM switching of LX	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	Low if V_{3V3} or V_{1V3IN} are too low	Low if V5 or V5P are too Low	High	On	On	None
VREG pin open circuit	V_{VREG} will decay to 0 V, LX will switch at maximum duty cycle so the voltage on the output capacitors will be very close to V_{BAT}	No	No effect	No effect	Off	Off	Off	Off	Off	Off	Low if V_{3V3} or V_{1V3IN} are too low	Low	Low	On	On	Connect the VREG pin
VREG shorted to ground, $V_{VREG} <$ 1.95 V, $V_{COMP} \neq V_{O(EA,MAX)}$	Continue to PWM but turn off LX when the high side MOSFET current exceeds I_{LIM}	No	No effect	No effect	Shorted	Off if $V_{VREG} < V_{UVLO}$	Off if $V_{VREG} < V_{UVLO}$	Off if $V_{VREG} < V_{UVLO}$	Off if $V_{VREG} < V_{UVLO}$	Off if $V_{VREG} < V_{UVLO}$	Low if V_{3V3} or V_{1V3IN} are too low	Low	Low	On	On	Remove the short circuit
VREG overcurrent, $V_{VREG} <$ 1.95 V, $V_{COMP} = V_{O(EA,MAX)}$	Enters hiccup mode after 30 OCP faults	No	No effect	No effect	Shorted	Off if $V_{VREG} < V_{UVLO}$	Off if $V_{VREG} < V_{UVLO}$	Off if $V_{VREG} < V_{UVLO}$	Off if $V_{VREG} < V_{UVLO}$	Off if $V_{VREG} < V_{UVLO}$	Low if V_{3V3} or V_{1V3IN} are too low	Low	Low	On	On	Decrease the load
VREG overcurrent, $V_{VREG} >$ 1.95 V, $V_{COMP} = V_{O(EA,MAX)}$	Enters hiccup mode after 120 OCP faults	No	No effect	No effect	Shorted	Off if $V_{VREG} < V_{UVLO}$	Off if $V_{VREG} < V_{UVLO}$	Off if $V_{VREG} < V_{UVLO}$	Off if $V_{VREG} < V_{UVLO}$	Off if $V_{VREG} < V_{UVLO}$	Low if V_{3V3} or V_{1V3IN} are too low	Low	Low if $V_{3V3} < V_{3V3(UV,L)}$	On	On	Decrease the load

Continued on next page...

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Table 1: Summary of Fault Mode Operation (continued)

FAULT TYPE and CONDITION	ARG81402 RESPONSE TO FAULT	LATCHED FAULT?	VCC	VCP	VREG	3V3	V5CAN	V5A	V5B	V5P	NPOR	FFn	POE	SPI	WD	RESET METHOD
3V3 undervoltage	Closed loop control will try to raise the voltage but may be constrained by the foldback or pulse-by-pulse current limit	No	No effect	No effect	No effect	Low	No effect	No effect	No effect	No effect	Low	Low	Low	On	On	Decrease the load
3V3 overvoltage	If OV condition persists for more than t_{dOV} then set NPOR low	No	No effect	No effect	No effect	> $V_{3V3(OV,H)}$	No effect	No effect	No effect	No effect	Low	Low	Low	On	On	Check for short circuits
3V3 overcurrent	Foldback current limit will reduce the output voltage	No	No effect	No effect	No effect	Falling	No effect	No effect	No effect	No effect	Low if V_{3V3} < $V_{3V3(UV,L)}$	Low if V_{3V3} < $V_{3V3(UV,L)}$	Low if V_{3V3} < $V_{3V3(UV,L)}$	On	On	Decrease the load
V5P undervoltage	Closed loop control will try to raise the voltage but may be constrained by the foldback current limit	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	UVLO	No effect	Low	No effect	On	On	Decrease the load
V5P overvoltage or shorted to V_{BAT}	If OV condition persists for more than t_{dOV} then set FF Low	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	> $V_{V5P(OV,H)}$	No effect	Low	No effect	On	On	Check for short circuits on V5P
V5P overcurrent	Foldback current limit will reduce the output voltage	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	Falling	No effect	Low if V5P are too Low	No effect	On	On	Decrease the load
V5A undervoltage	Closed loop control will try to raise the voltage but may be constrained by the foldback current limit	No	No effect	No effect	No effect	No effect	No effect	Low	No effect	No effect	No effect	Low	No effect	On	On	Decrease the load
V5A overvoltage	If OV condition persists for more than t_{dOV} then set FF Low	No	No effect	No effect	No effect	No effect	No effect	> $V_{V5A(OV,H)}$	No effect	No effect	No effect	Low	No effect	On	On	Check for short circuits on V5A
V5A overcurrent	Foldback current limit will reduce the output voltage	No	No effect	No effect	No effect	No effect	No effect	Falling	No effect	No effect	No effect	Low if V_{V5A} < $V_{V5A3(UV,L)}$	No effect	On	On	Decrease the load
V5CAN overvoltage	If OV condition persists for more than t_{dOV} then set FF Low	No	No effect	No effect	No effect	No effect	> $V_{V5CAN(OV,H)}$	No effect	No effect	No effect	No effect	Low	No effect	On	On	Check for short circuits on V5CAN
V5CAN undervoltage	Closed loop control will try to raise the voltage but may be constrained by the foldback current limit	No	No effect	No effect	No effect	No effect	Low	No effect	No effect	No effect	No effect	Low	No effect	On	On	Decrease the load
V5CAN overcurrent	Foldback current limit will reduce the output voltage	No	No effect	No effect	No effect	No effect	Falling	No effect	No effect	No effect	No effect	Low if V5CAN is too Low	No effect	On	On	Decrease the load
V5B overvoltage	If OV condition persists for more than t_{dOV} then set FF Low	No	No effect	No effect	No effect	No effect	> $V_{V5CAN(OV,H)}$	No effect	No effect	No effect	No effect	Low	No effect	On	On	Check for short circuits on V5CAN
V5B undervoltage	Closed loop control will try to raise the voltage but may be constrained by the foldback current limit	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	Low	No effect	On	On	Decrease the load
V5B overcurrent	Foldback current limit will reduce the output voltage	No	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	No effect	Low if V5B is too Low	No effect	On	On	Decrease the load
Thermal shutdown	Results in an MPOR, so all regulators are shut off	No	No effect	No effect	No effect	off	off	off	off	off	off	Low	Low	On	On	Let the ARG81402 cool

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TIMING DIAGRAMS (not to scale)
* is for “and”, + is for “or”

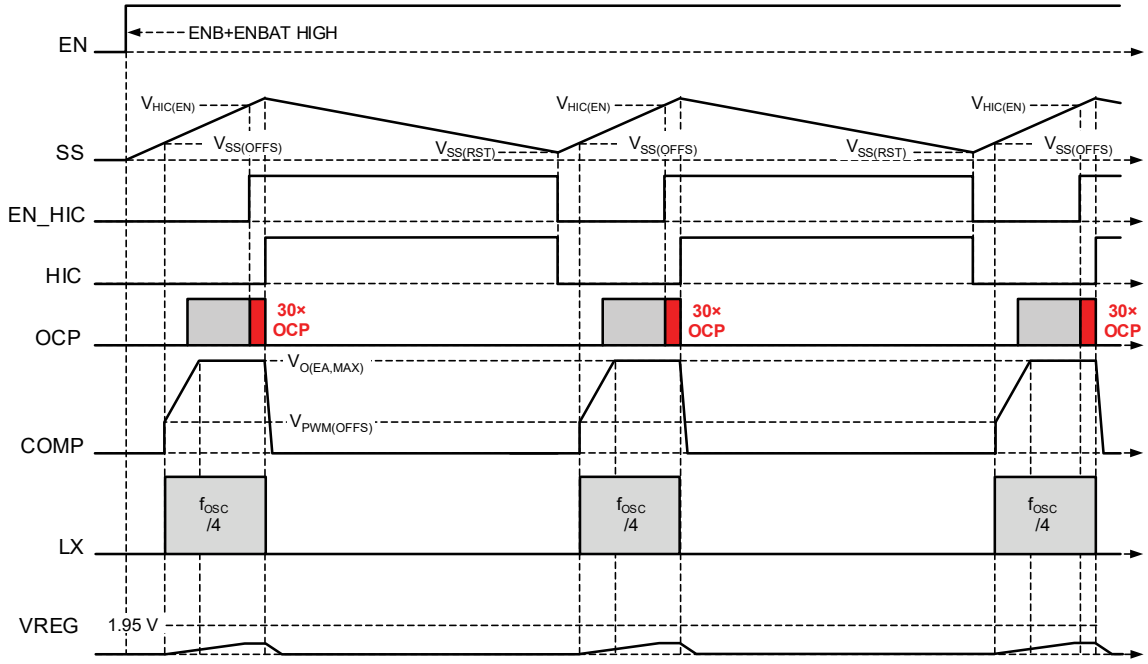

Figure 4: Hiccup Mode Operation with VREG or Synchronous Buck Shorted to GND (R_{LOAD} < 50 mΩ)

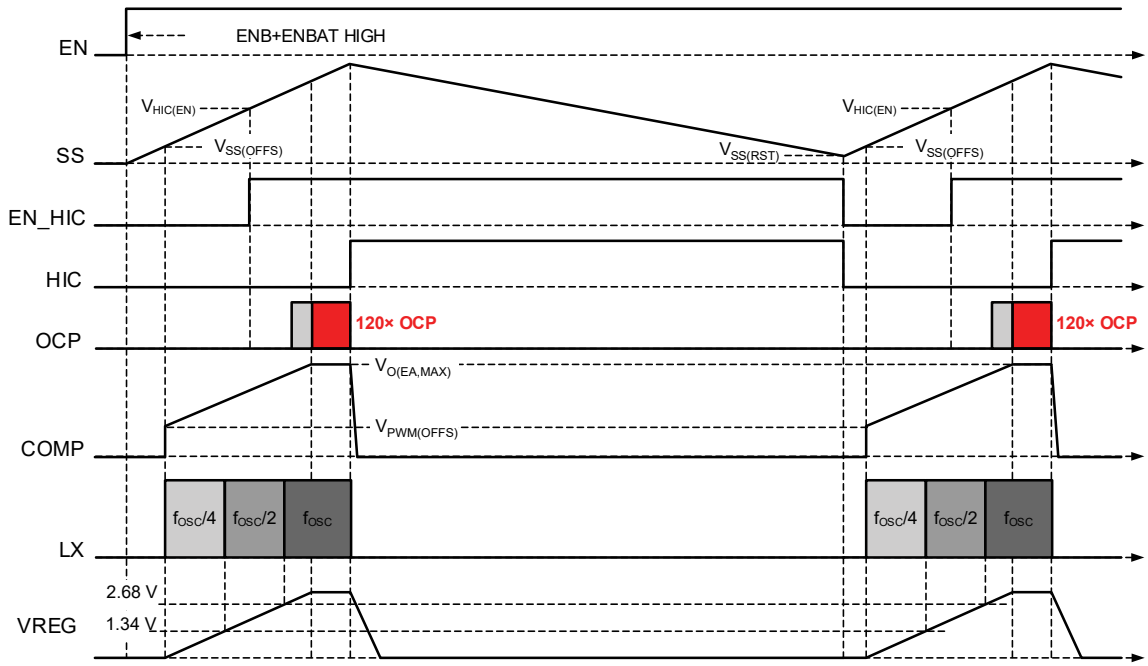

Figure 5: Hiccup Mode Operation with VREG or Synchronous Buck Overloaded (R_{LOAD} ≈ 0.5 Ω)

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FUNCTIONAL DESCRIPTION

Overview

The ARG81402 pre-regulator is a synchronous buck converter. This pre-regulator generates a fixed 5.35 V and can deliver up to 600 mA to power the internal post regulators. These post regulators generate the various voltage levels for the end system.

The ARG81402 includes five internal post-regulators.

Pre-Regulator

The pre-regulator incorporates internal high-side and low-side switches for buck configuration. An LC filter is required to complete the buck converter.

The pre-regulator provides many protection and diagnostic functions:

1. Pulse-by-pulse and hiccup mode current limit
2. Undervoltage and overvoltage detection and reporting
3. Shorted switch node to ground
4. High voltage rating for load dump

PWM Switching Frequency

The switching frequency of the ARG81402 is fixed at 2.2 MHz nominal. The ARG81402 includes a frequency foldback scheme to improve regulation and efficiency at higher and lower supply voltages. Between 18 and 36 V, the switching frequency will foldback linearly from 2.2 to 1 MHz typical. At lower V_{VIN}, the switching frequency will foldback to 550 kHz typical when the regulator reaches maximum duty cycle, which happens at around 7 V.

Bias Supply

The bias supply (V_{CC}) is generated by an internal linear regulator. This supply is the first rail to start up. Most of the internal control circuitry is powered by this supply. The bias supply includes some unique features to ensure safe operation of the ARG81402. These features include:

1. Input voltage undervoltage lockout
2. Output undervoltage and overvoltage detection and reporting
3. Overcurrent and short-circuit limit
4. Dual input, VIN and VREG, for low battery voltage operation
5. Short protection of the series pass device. If the internal linear regulator shorts to VIN, this protection will ensure that the ARG81402 enters a safe mode

Charge Pump

A charge pump doubler provides the voltage necessary to drive the linear regulators. Two external capacitors are required for charge pump operation.

The charge pump incorporates some safety features:

1. Undervoltage detection and reporting
2. Overcurrent safe mode protection

Bandgap

Dual bandgaps are implemented within the ARG81402. One bandgap is dedicated to the voltage regulation loops within each of the regulators, VCC, VCP, VREG, and the six post regulators. The second is dedicated to the monitoring function of all the regulators undervoltage and overvoltage. This improves safety coverage and fault reporting from the ARG81402.

Should the regulation bandgap fail, then the outputs will be out of specification and the monitoring bandgap will report the fault.

If the monitoring bandgap fails, the outputs will remain in regulation but the monitoring circuits will report the outputs as out of specification and trip the fault flag.

The bandgap circuits include two other bandgaps that are used to monitor the undervoltage state of the main bandgaps.

Enable

Two enable pins are available on the ARG81402. A high signal on either of these pins enables the regulated outputs of the ARG81402. One enable (ENB) is logic level compatible. The second enable (ENBAT) is battery level rated and can be connected to the ignition switch through a resistor.

A logic level battery enable status (ENBATS) pin provides the user with a low level signal of ENBAT input status.

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Linear Regulators

The ARG81402 has five linear regulators, one 3.3 V, three 5 V and one protected 5 V.

All linear regulators provide the following protection features:

1. Current limit with foldback
2. Undervoltage and overvoltage detection and reporting

The protected 5 V regulator includes protection against connection to the battery voltage. This makes this output most suitable for powering remote sensors or circuitry where short-to-battery is possible.

The pre-regulator powers these linear regulators which reduces power dissipation and temperature.

Fault Detection and Reporting

There is extensive fault detection within the ARG81402, as discussed previously. There are two fault reporting mechanisms used by the ARG81402: through hardwired pins and through a serial communications interface (SPI).

Two hardwired pins on the ARG81402 are used for fault reporting. The first pin, NPOR, reports on the status of the 3V3 and 1V3IN levels. This signal goes low if either of these are out of regulation. The NPOR signal may also toggle low for 2 ms if the window or Q&A watchdogs detect a watchdog fault. This NPOR function is selectable through SPI. The second pin, FFn (active-low fault flag), reports on all other faults. FFn goes low if a fault within the ARG81402 exists. The FFn pin can be used by the processor as an alert to check the status of the ARG81402 via SPI and see where the fault occurred.

Startup Self-Test

The ARG81402 includes self-test which is performed during the startup sequence. This self-test verifies the operation of the undervoltage and overvoltage detect circuits for the main outputs.

In the event the self-test fails, the ARG81402 will report the failure through SPI.

Undervoltage Detect Self-Test

The undervoltage (UV) detectors are verified during startup of the ARG81402. A voltage that is higher than the undervoltage threshold is applied to each UV comparator; this should cause the relative undervoltage fault bit in the diagnostic registers to change state. If the diagnostic UV register bits change state, the corresponding verify register bits will latch high. When the test of all UV detectors is complete, the verify register bits will remain high if the test passed. If any UV bits in the verify registers after test are not set high, then the verification has failed. The following UV detectors are tested: VREG, 3V3, V5A, V5B, V5P, V5CAN, and 1V3IN.

Overvoltage Detect Self-Test

The overvoltage (OV) detectors are verified during startup of the ARG81402. A voltage is applied to each OV comparator that is higher than the overvoltage threshold; this should cause the relative overvoltage fault bit in the diagnostic registers to change state. If the diagnostic OV register bits change state, the corresponding verify register bits will latch high. When the test of all OV detectors is complete, the verify register bits will remain high if the test passed. If any OV bits in the verify registers after test are not set high, then the verification has failed. The following OV detectors are tested: VREG, 3V3, V5A, V5B, V5P, V5CAN, and IV3IN.

Overtemperature Shutdown Self-Test

The overtemperature shutdown (TSD) detector is verified on startup of the ARG81402. A voltage is applied to the comparator that is lower than the overtemperature threshold, and should cause the general fault flag to be active and an overtemperature fault bit, TSD, to be latched in the Verify Result register 0. When the test is complete, the general fault flag will be cleared and the overtemperature fault will remain in the Verify Result register 0 until reset. If the TSD bit is not set, then the verification has failed.

Power-On Enable Self-Test

The ARG81402 also incorporates continuous self-testing of the power-on enable (POE) output. It compares the status of the POE pin with the internal demanded status. If they differ for any reason, an FFn is set and the POE_OK in SPI diagnostic register goes low.

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Watchdog

The ARG81402 contains three types of watchdog. This section will describe each one in detail. The selection and programming parameters for each watchdog is done through SPI. Once the watchdog is selected and running it cannot be modified without going through a secure SPI procedure. All registers containing configuration information are ignored once the watchdog is running.

The three possible watchdogs are:

1. Pulse period watchdog (default)
2. Window watchdog
3. Q&A watchdog

The Pulse Period Watchdog is the default watchdog. This watchdog starts once NPOR goes high. The user has 250 ms to reconfigure the watchdog, after which the selected watchdog will operate.

Pulse Period Watchdog (PPWD)

The period watchdog circuit within the ARG81402 will monitor a 500 Hz temporal signal from a processor for its period between pulses. If the signal does not meet the requirements, the ARG81402 Pulse Period Watchdog will put the system into a safe state. It does this by setting the power-on enable (POE) pin immediately low; after 250 ms, the V5CAN output is disabled, and after 10 seconds, the enabling function of ENB pin for the ARG81402 is removed. See Figure 7 for a simplified block diagram of the Pulse Period Watchdog circuit.

The Pulse Period Watchdog function (see Figure 6) uses two timers and two counters to validate the incoming temporal signal. The user has some programmability of the counters and timer windows through SPI.

The first counter counts the rising edges of the temporal signal. If the correct count is completed after the minimum timer expires and before the maximum timer expires, then the second (valid) counter is incremented. Once the valid counter has incremented, the programmed number of counts the Pulse Period Watchdog issues a Pulse Period Watchdog OK (WD_IN_OK) signal. This signal, along with NPOR, 3V3 enable, and nERROR enables the POE.

If the edge count reaches its final value before the minimum timer or after the maximum timer expires, the valid counter decrements. Once the valid counter reaches zero, the Pulse Period Watchdog fault signal issues that a fault has occurred. The POE is driven low; after a time out period, the V5CAN output is disabled, and after a further timeout, enabling of the ARG81402 via the ENB pin is no longer possible.

If insufficient edges are received before the maximum timer expires, the valid counter decrements and the minimum and maximum counters are reset and start to count again. If an edge is subsequently received, the timers reset once again to synchronize on the incoming pulses. The valid counter is not decremented in this instance; see Figure 6.

The number of edge counts (k_{EDGE}), valid counts, and timer windows can be programmed through SPI. The min and max timer nominal values in milliseconds are calculated by the following equations:

$$t_{WD(MIN)} = k_{EDGE} \times (2 + WD\_MIN)$$

$$t_{WD(MAX)} = k_{EDGE} \times (2 + WD\_MAX)$$

where k_{EDGE} is the edge count number programmed through SPI, programmable counts are 4, 6, 8 or 10, default is 4,

WD_MIN is the min timer adjust value in milliseconds programmed in SPI, value can be programmed from –0.8 to –0.15 ms in steps of –0.01 ms, default is –0.12 ms, and

WD_MAX is the min timer adjust value in milliseconds programmed in SPI (default is 0.12 ms).

Tolerance on $t_{WD(MIN)}$ and $t_{WD(MAX)}$ is related to the system clock tolerance, $f_{SYS(TOL)}$ in %, by the following equations:

$$\frac{100}{100 - f_{SYS(TOL)}} - 1$$

$$\frac{100}{100 + f_{SYS(TOL)}} - 1$$

The Pulse Period Watchdog also has a provision to be placed in “flash mode”. While in flash mode, the Pulse Period Watchdog keeps the POE signal low but does not disable the V5CAN or the ENB function. This is required should the processor need to be re-flashed. Flash mode is accessed through secure SPI commands. To exit flash mode, the Pulse Period Watchdog must be restarted via separate secure SPI commands. If the ARG81402 has not lost power during flash mode, then the Pulse Period Watchdog will restart with the previous configuration. If power was lost during flash mode, then the Pulse Period Watchdog configuration will be reset to default.

On startup, the Pulse Period Watchdog (WD_IN) must receive a series of valid and qualified pulse trains, per the programmed EDGE_COUNT and VALID_COUNT registers, followed by a series of invalid qualified pulses. Once a second series of valid and qualified pulse are received before the power supply disable time ($t_{PS(DISABLE)}$) expires, then the Pulse Period Watchdog enters the active state and the WD_F signal on SPI becomes active, see

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Figure 6. During the test state, WD_F is not active and FFn does not alert a Pulse Period Watchdog fault. When the Pulse Period Watchdog is waiting for the second series of pulse on WD_IN, it sets the valid counter to one half its programmed value. This aids in speeding up startup of a system using the ARG81402. Once the WD_IN pulses have met all criteria and POE is released, then the valid counter reverts to its correct programed value. If the second series of pulses is not received before the $t_{PS(DISABLE)}$ time, then the Pulse Period Watchdog will enter Pulse Period Watchdog fault mode. It will set the POE signal low, disable the V5CAN after $t_{PS(DISABLE)}$, and remove enable control via ENB after $t_{PS(DISABLE)}$.

If the Pulse Period Watchdog has indicated invalid WD_IN pulses, it latches the POE signal low. Once the power supply disable time ($t_{PS(DISABLE)}$) expires, then the Pulse Period Watchdog will disable the V5CAN. After the anti-latchup timeout, $t_{ANTI\_LATCHUP}$, the Pulse Period Watchdog will remove enable control via the ENB pin. The only way to prevent this would be to restart the Pulse Period Watchdog either through SPI or shutting down and restarting the ARG81402.

The processor can restart the Pulse Period Watchdog by using a secure SPI command.

The processor can restart the watchdog by using a secure SPI command.

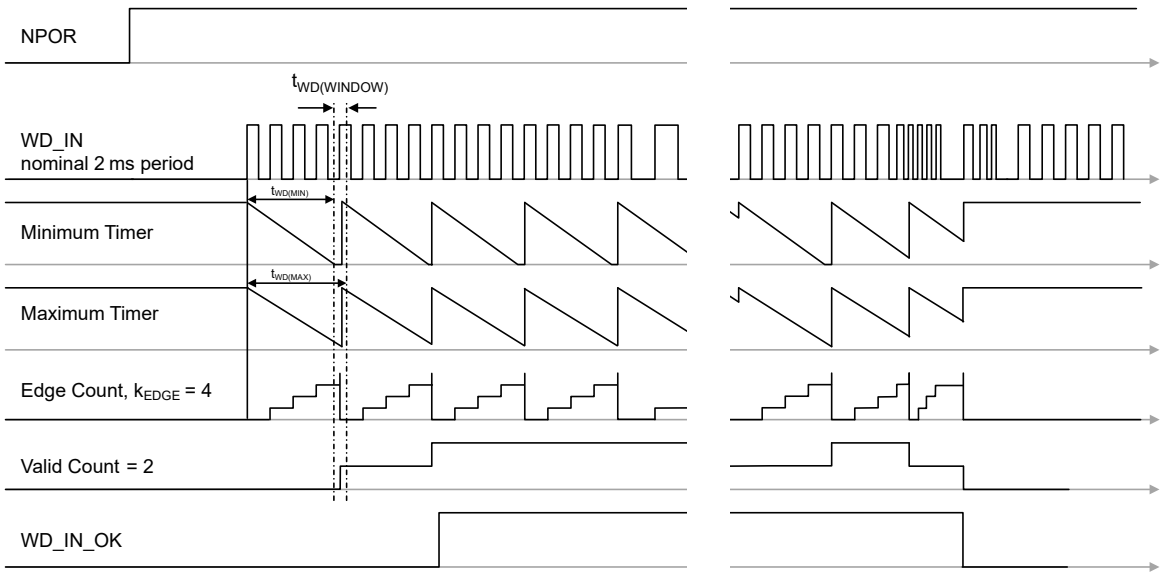

Figure 6: Pulse Period Watchdog Valid Signal Timing Diagram

$t_{WD(MIN)}$ = 7.52 ms, $t_{WD(MAX)}$ = 8.48 ms, $t_{WD(WINDOW)}$ = 0.96 ms

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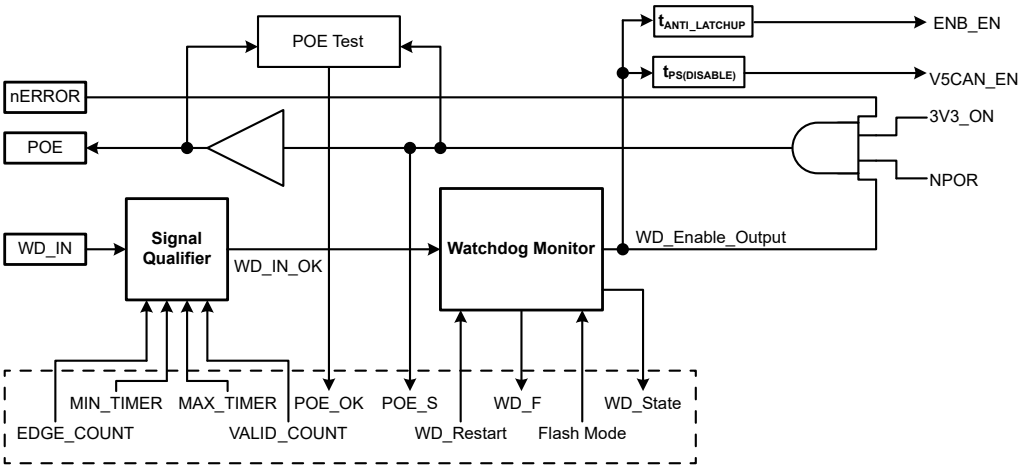

Figure 7: Pulse Period Watchdog Block Diagram

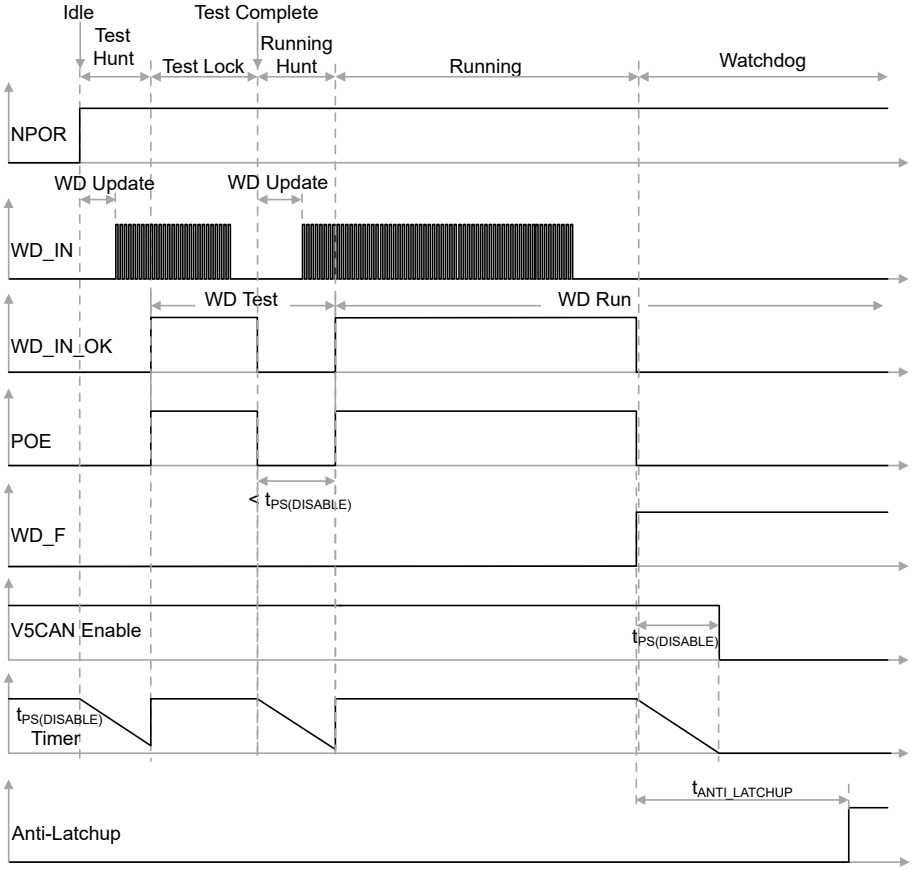

Figure 8: Pulse Period Watchdog Timing at Startup

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Window Watchdog (WWD)

The window watchdog can be selected at startup by setting the configuration register 0x08. This watchdog circuit in the ARG81402 monitors an external clock applied to the WD_IN pin. This clock should be generated by the microcontroller or DSP. The time between rising edges of the clock must fall within an acceptable "window" or a watchdog fault is generated.

The timing, $t_{WD(FAST)}$ and $t_{WD(SLOW)}$, for the WWD can be programmed through register 0x09. The processor can also select how NPOR behaves when there is a watchdog fault. Usually watchdog does not impact NPOR. If the user wants the watchdog to attempt to reset the processor, the NPOR_RST_EN bit in register 0x0A should be set to 1. Once NPOR goes high, the processor has $t_{PS(DIS)}$ to program the WWD registers and initiate WD pulses on the WD_IN pin of the ARG81402. Once this is complete, the processor can then select the WWD through register 0x08.

Once the window watchdog is selected, it starts to monitor the pulses on the WD_IN pin of the ARG81402. A watchdog fault will set POE low. If NPOR_RST_EN is 1, then a watchdog fault will set NPOR low for $t_{WD(FAULT)}$. The watchdog remains in this state until a "restart" command through secure SPI is received.

On receiving a restart command, the watchdog will continue in the previous configuration state unless power was lost to the ARG81402. If this was the case, then the processor must reconfigure the watchdog. Note it is recommended that the processor initiate valid pulses on WD_IN prior to issuing a restart command.

A watchdog fault will occur if the time between rising edges is either too short (a FAST fault) or too long (a SLOW fault).

The watchdog's time window is programmable via SPI configuration register 0x09.

Typical watchdog operation and FAST and SLOW fault conditions are shown in Figures 9 and 10.

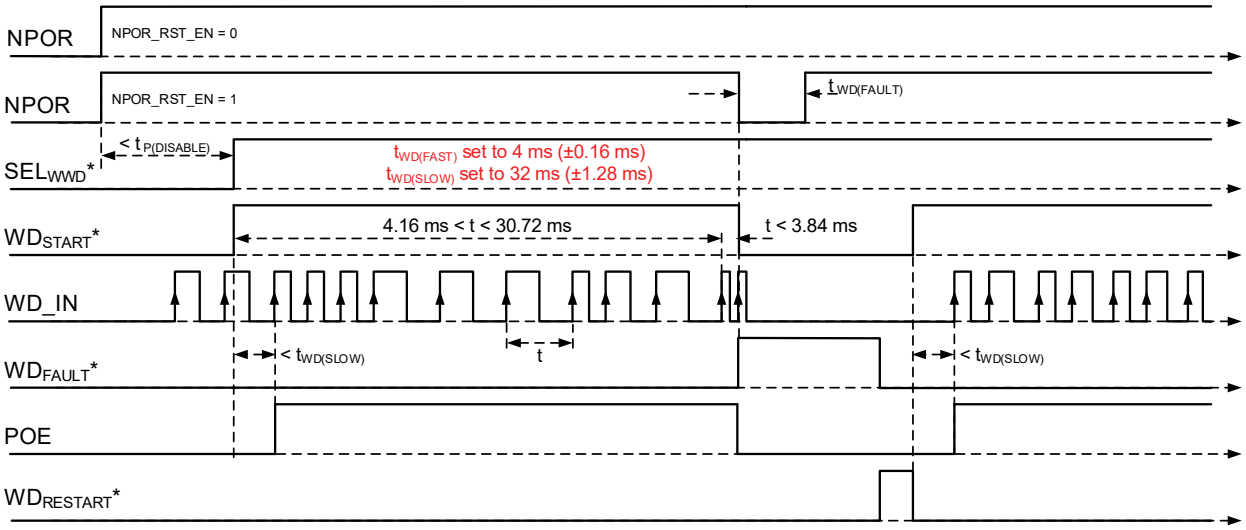

Figure 9: Window Watchdog Timer FAST Fault, t = WD_IN period, Shows NPOR signal when NPOR_RST_EN is 1 and 0.

*** Signal is internal to ARG81402**

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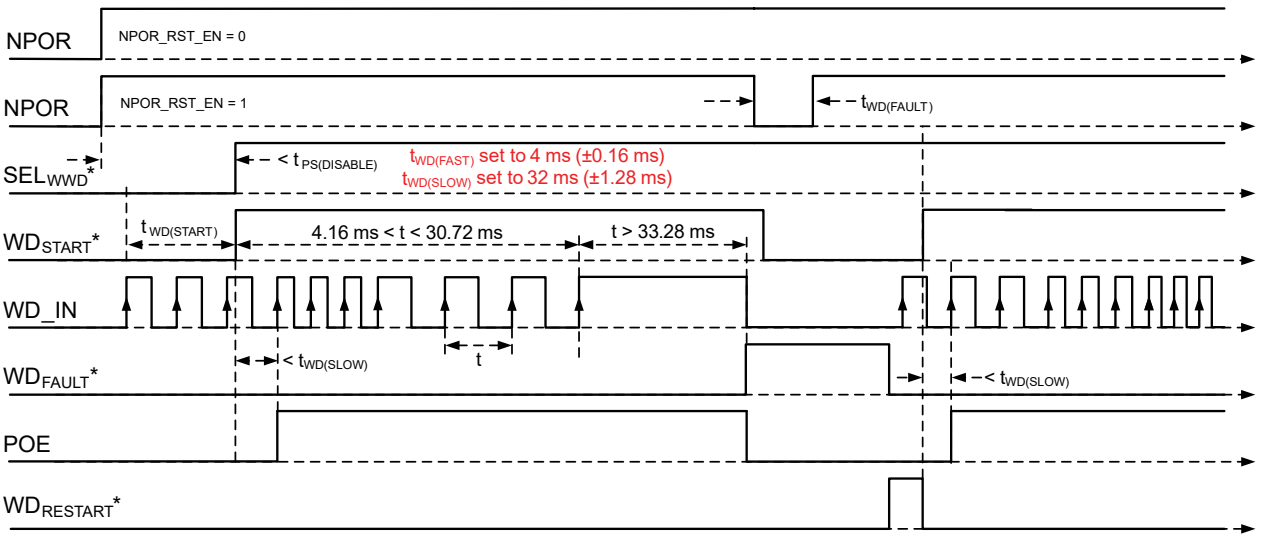

Figure 10: Window Watchdog Timer SLOW Fault, t = WD_IN period. Shows NPOR signal when NPOR_RST_EN is 1 and 0.

*** Signal is internal to ARG81402**

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Q&A Watchdog

The Q&A watchdog can be selected through SPI configuration register 0x08. This watchdog monitors an answer code from a microprocessor or DSP. The ARG81402 generates a random word which the microprocessor or DSP must read. The microprocessor or DSP then performs an inversion of each bit and writes the code back to the ARG81402. This action must be completed within a programmed time limit. These time limits are programmed in register 0x0A using a 4-bit word [D3:D0]. The microprocessor or DSP is allowed to fail the Q&A watchdog a defined number of times before a watchdog error is giving. The number of allowed failures is programmed using a 2-bit word [D5:D4] in register 0x0A. The behavior of the NPOR signal due to a watchdog fault can be programmed in register 0x0A. All programming of the watchdog should be done before setting watchdog select bits in register 0x08. Also, programming of the watchdog must be completed before $t_{PS(DISABLE)}$. Once a watchdog error is given, the POE signal goes low. If NPOR reset is selected, the NPOR signal goes low for $t_{WD(FAULT)}$, and then returns high. The watchdog remains in this state until a "restart" command through secure SPI is received. The number of incorrect attempts by the microprocessor or DSP can be programmed in configuration register 0x0A. This register also programs the time the microprocessor or DSP has to respond to the question.

1. NPOR goes high. POE remains low.
2. Microprocessor selects Q&A watchdog using SPI register 0x08.
3. ARG81402 starts Q&A minimum and maximum timers and creates random word in register 0x0B.
4. Microprocessor reads 0x0B after minimum timer expires but before maximum timer expires.
5. Microprocessor inverts each bit of the word read and writes the result back to register 0x0B. This must be completed after minimum timer expires but before maximum timer expires.
6. If microprocessor fails, then the retry counter is decremented. If the retry counter reaches zero, a watchdog fail signal is generated. NPOR goes low for $t_{WD(FAULT)}$. POE goes low and stays low until a "restart" command through secure SPI is received and the microprocessor successfully completes a Q&A session. If the retry counter is greater than zero, ARG81402 restarts both timers and generates a new random word in register 0x0B. POE and NPOR do not change states.
7. If the microprocessor passes, then POE goes high (first correct Q&A result) or remains high. ARG81402 restarts both timers and generates a new random word in register 0x0B
8. Repeat #4 to #7.

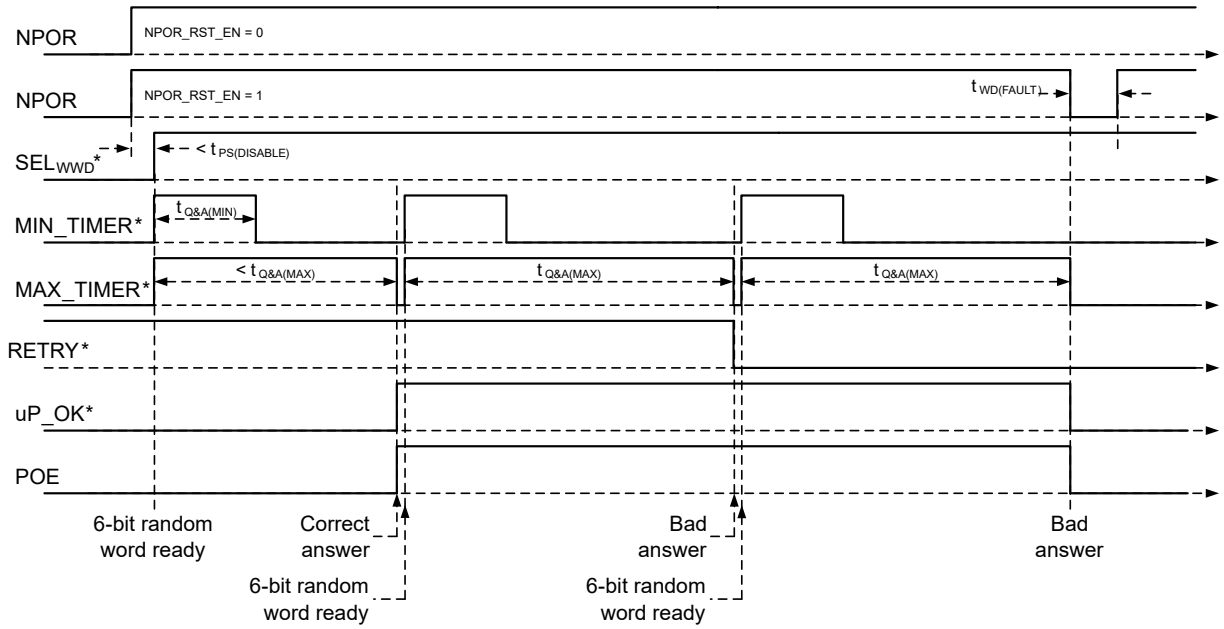

Figure 11: Q&A Startup Timing and Fault Example. Shows NPOR Signal when NPOR_RST_EN is 1 and 0.

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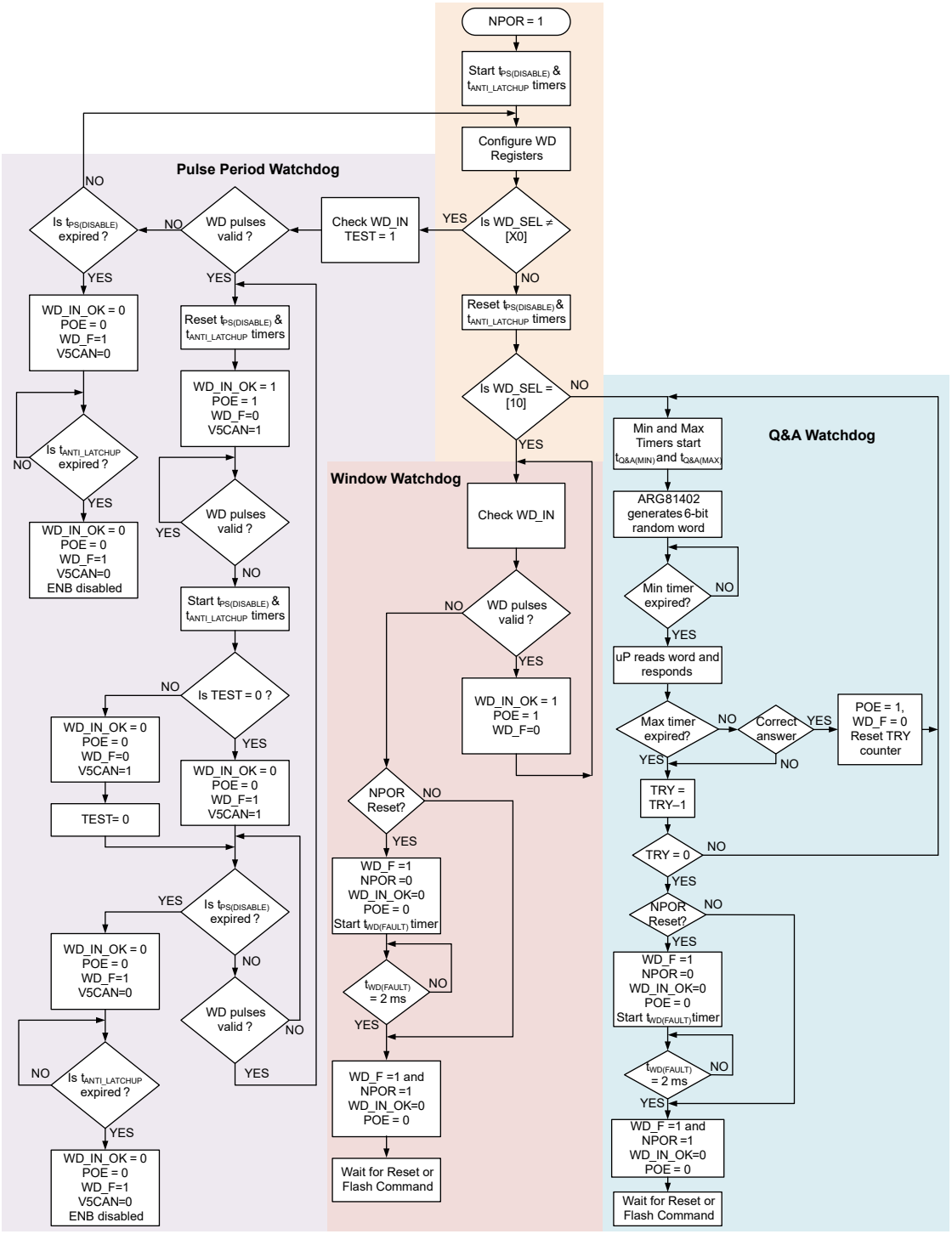

Figure 12: Three Watchdog Flowchart

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SERIAL COMMUNICATION INTERFACE

The ARG81402 provides the user with a three-wire synchronous serial interface that is compatible with SPI (Serial Peripheral Interface). A fourth wire can be used to provide diagnostic feedback and readback of the register content.

The serial interface timing requirements are specified in the electrical characteristics table and illustrated in the Serial Interface Timing diagram (Figure 1). Data is received on the SDI terminal and clocked through a shift register on the rising edge of the clock signal input on the SCK terminal. STRn is normally held high, and is only brought low to initiate a serial transfer. No data is clocked through the shift register when STRn is high, allowing multiple SDI slave units to use common SDI, SCK and SDO connections. Each slave then requires an independent STRn connection.

When 16 data bits have been clocked into the shift register, STRn must be taken high to latch the data into the selected register. When this occurs, the internal control circuits act on the new data and the Diagnostic register is reset.

If there are more than 16 rising edges on SCK or if STRn goes high and there are fewer than 16 rising edges on SCK, the write will be cancelled without writing data to the registers. In addition, the Diagnostic register will not be reset and the SE (serial error) bit will be set to indicate a data transfer error.

Diagnostic information or the contents of the configuration and control registers are output on the SDO terminal MSB first, while STRn is low, and changes to the next bit on each falling edge of SCK. The first bit, which is always the FFn (active low fault flag) bit from the Diagnostic register, is output as soon as STRn goes low.

Each of the programmable (configuration and control) registers has a write bit, WR (bit 10), as the first bit after the register address. This bit must be set to 1 to write the subsequent bits into the selected register. If WR is set to 0, then the remaining data bits (bits 9 to 0) are ignored. The state of the WR bit also determines the data output on SDO. If WR is set to 1 then the Diagnostic register is output. If WR is set to 0, then the contents of the register selected by the first five bits is output. In all cases, the first bit output on SDO will always be the FFn bit from the Diagnostic Register.

The ARG81402 has 13 register banks. Bit <15:11> represents the register address for read and write. Bit <10> detects the read and write operation: for write operation, Bit <10> = 1, and for read operation, bit value is logic low. Bit <9> is an unused bit. Maximum data size is eight bits so Bit<8:1> represents the data word. The last bit in a serial transfer, Bit<0>, is a parity bit that is set to ensure odd parity in the complete 16-bit word. Odd parity means that the total number of 1s in any transmission should always be

Pattern at SDI Pin

MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A4	A3	A2	A1	A0	W/R	NU	D7	D6	D5	D4	D3	D2	D1	D0	P
5-Bit Address							8-Bit Data								

Pattern at SDO Pin after SDI Write

MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FFn	SE	ENBATS	WD_F	TSD_OK	VREG_OK	1V3IN_OK	VCC_OK	VCP_OK	V5P_OK	V5B_OK	V5A_OK	V5CAN_OK	3V3_OK	0	P
Diagnostics															

Pattern at SDO Pin after SDI Read

MSB															LSB
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FFn	SE	ENBATS	WD_F	TSD_OK	VREG_OK	1V3IN_OK	D7	D6	D5	D4	D3	D2	D1	D0	P
Diagnostics							8-Bit Data								

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an odd number. This ensures that there is always at least one bit set to 1 and one bit set to 0, and allows detection of stuck-at faults on the serial input and output data connections. The parity bit is not stored but generated on each transfer.

Register data is output on the SDO terminal MSB first, while STRn is low, and changes to the next bit on each falling edge of the SCK. The first bit which is always the FFn bit from the status register, is output as soon as STRn goes low.

If there are more than 16 rising edges on SCL, or if STRn goes high and there are fewer than 16 rising edges on SCK, then the write will be cancelled without writing data to the registers. In addition, the diagnostic register will not be reset; the SE bit will be set to indicate a data transfer error.

SDI: Serial data logic input with pull-down. 16-bit serial word, input MSB first.

SCK: Serial clock logic input with pull-down. Data is latched in from SDI on the rising edge of SCL. There must be 16 rising edges per write and SCK must be held high when STRn changes.

STRn: Serial data strobe and serial access enable logic input with pull-up. When STRn is high, any activity on SCK or SDI is ignored and SDO is high impedance, allowing multiple SDI slaves to have common SDI, SCK, and SDO connections.

SDO: Serial data output. High impedance when STRn is high. Output bit 15 of the status register, the fault flag (FFn), as soon as STRn goes low.

Register Mapping

STATUS REGISTERS

The ARG81402 provides 3 status registers. These registers are read-only. They provide real-time status of various functions within the ARG81402.

These registers report on the status of all six system rails. They also report on internal rail status, including the charge pump, VREG, VCC, and VDD rails. The general fault flag and watchdog fault state are found in these status registers.

The logic that creates the power-on enable and power reset status are reported through these registers.

CONFIGURATION REGISTERS

Four configuration registers in the ARG81402 are used to configure the watchdog parameters.

The watchdog configuration registers can be written to at any time. The watchdog will only update during either hunt states when it receives the first pulse on WD_IN, as shown in Figure 8 WD update. If the user wants to change the watchdog configuration after the hunt states, then a WD_RESTART is required via the “watchdog_mode_key” register 0x07.

The type of watchdog can be selected via register 0x08. Default watchdog is the pulse period watchdog.

The timers, valid count, and edge count for the pulse period watchdog are programmed in registers 0x08 and 0x09.

The window watchdog fast and slow times are programmed in register 0x08.

The Q&A watchdog timers and allowed number of incorrect responses are programmed in register 0x0A.

Configuration register 0x09 also allows the user to disable the dither feature of the ARG81402.

DISABLE REGISTER

The disable register provides the user control of the 5 V outputs. Two bits must be set high to disable an output. If only one bit is high, then the 5 V outputs remain on. Only V5A, V5B, and V5P can be disabled. If an output is disabled, the UV alarm will be set. However the fault flag will not register a fault as this condition is expected. This allows the user to disable one of the 5 V rails and still maintain fault flag interrupt. If a rail is disabled and the output remains above the UV threshold, an OV fault will be registered on this rail.

V5x_DIS1	V5x_DIS0	5Vx_OK	V5x_UV	V5x_OV	FF
0	X	1	0	0	0
x	0	1	0	0	0
1	1	0	0	1	1
1	1	1	1	0	0

WATCHDOG MODE KEY REGISTER

At times it may be necessary to re-flash or restart the processor. To do this, the user must put the watchdog into “Flash Mode” or “restart”. This is done writing a sequence of key words to the “watchdog_mode_key” register. If the correct word sequence is not received, then the sequence must restart.

Once flash is complete, the processor must send the restart sequence of key words for the watchdog to exit “Flash Mode”. If VCC has not been removed from the ARG81402, the watchdog will restart with the current configuration.

While in flash mode, the watchdog keeps the POE signal low but

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does not disable the V5CAN or the ENB function (pulse period watchdog).

VERIFY RESULT REGISTERS

On every startup, the ARG81402 performs a self-test of the UV and OV detect circuits. This test should cause the diagnostic registers to toggle state. If the diagnostic register successfully changes state, the verify result register will latch high. Upon completion of startup, the system's microprocessor can check the verify result registers to see if the self-test passed.

Table 2: Register Map

Hex. Address	Register Name	Decimal Address	Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	status_0	0	RO	FF	POE_OK	VCC_OK	VDD_OK	V5P_OK	V5B_OK	V5A_OK	V5CAN_OK
0x01	status_1	1	RO	LX_OK	NPOR_OK	WD_F	TSD	VCP_OK	VREG_OK	3V3_OK	1V3IN_OK
0x02	status_2	2	RO		DBE	NPOR_S	POE_S	ENBATS	WD_STATE		
0x03	diag_0	3	RW1C	V5A_OV	V5A_UV	V5CAN_OV	V5CAN_UV	V5P_OV	V5P_UV	V5B_OV	V5B_UV
0x04	diag_1	4	RW1C	VDD_OV	VDD_UV	VREG_OV	VREG_UV	3V3_OV	3V3_UV	1V3IN_OV	1V3IN_UV
0x05	diag_2	5	RW1C					VCC_OV	VCC_UV	VCP_OV	VCP_UV
0x06	output_disable	6	RW	V5P_DIS1	V5A_DIS1	V5B_DIS1		V5P_DIS0	V5A_DIS0	V5B_DIS0	
0x07	watchdog_mode_key	7	WO	Keycode Entry (Write Only)							
			RO	0	0	0	0	0	0	0	Unlocked
0x08	config_0	8	RW	WD_SEL1	WD_SEL0	MAX_TIMER			MIN_TIMER		
0x09	config_1	9	RW	WIN_Timer2	WIN_Timer1	WIN_Timer0	DITH_DIS	VALID_COUNT		EDGE_COUNT	
0x0A	config_2	10	RW		NPOR_RST_EN	TRY1	TRY0	TIMER3	TIMER2	TIMER1	TIMER0
0x0B	config_3	11	RW			RND5	RND4	RND3	RND2	RND1	RND0
0x0C	Reserved	12	–								
0x0D	verify_result_0	13	RW1C	V5A_OV_OK	V5A_UV_OK	V5CAN_OV_OK	V5CAN_UV_OK	V5P_OV_OK	V5P_UV_OK	V5B_OV_OK	V5B_UV_OK
0x0E	verify_result_1	14	RW1C	BIST_PASS	TSD_OK	VREG_OV_OK	VREG_UV_OK	3V3_OV_OK	3V3_UV_OK	1V3IN_OV_OK	1V3IN_UV_OK

Register Types:
RO = Read-Only
RW = Read or Write
RW1C = Read or Write 1 to clear
WO = Write-Only

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0X00. STATUS REGISTER 0:

D7	D6	D5	D4	D3	D2	D1	D0
FF	POE_OK	VCC_OK	VDD_OK	V5P_OK	V5B_OK	V5A_OK	V5CAN_OK
0	0	0	0	0	0	0	0

Address 00000

Read-only register

Data

FF [D7]: Fault flag. 0 = no fault, 1 = fault

POE_OK [D6]: Power-on enable signal matches what ARG81402 is demanding, 0 = fault, 1 = no fault

VCC_OK [D5]: Internal VCC rail is OK, 0 = fault, 1 = no fault

VDD_OK [D4]: Internal VDD rail is OK, 0 = fault, 1 = no fault

V5P_OK [D3]: Protected 5 V rail is OK, 0 = fault, 1 = no fault

V5B_OK [D2]: 5 V rail B is OK, 0 = fault, 1 = no fault

V5A_OK [D1]: 5 V rail A is OK, 0 = fault, 1 = no fault

V5CAN_OK [D0]: CAN bus 5 V rail is OK, 0 = fault, 1 = no fault

0X01. STATUS REGISTER 1:

D7	D6	D5	D4	D3	D2	D1	D0
LX_OK	NPOR_OK	WD_F	TSD	VCP_OK	VREG_OK	3V3_OK	1V3IN_OK
0	0	0	0	0	0	0	0

Address 00001

Read-only register

Data

LX_OK [D7]: Pre-regulator switch node is OK, 0 = fault on LX, 1 = LX is working correctly

NPOR_OK [D6]: NPOR signal matches what ARG81402 is demanding, 0 = fault, 1 = no fault

WD_F [D5]: Watchdog is active, 0 = watchdog off or no fault, 1 = watchdog fault

TSD [D4]: Thermal shutdown status, 0 = temperature OK, 1 = overtemperature event

VCP_OK [D3]: Charge pump rail is OK, 0 = fault, 1 = no fault

VREG_OK [D2]: Pre-regulator voltage is OK, 0 = fault, 1 = no fault

3V3_OK [D1]: 3.3 V rail is OK, 0 = fault, 1 = no fault

1V3IN_OK [D0]: Synchronous buck adjustable rail is OK, 0 = fault, 1 = no fault

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0X02. STATUS REGISTER 2:

D7	D6	D5	D4	D3	D2	D1	D0
	DBE	NPOR_S	POE_S	ENBATS	WD_state_2	WD_state_1	WD_state_0
0	0	0	0	0	0	0	0

Address 00010

Read-only register

Data

DBE [D6]: indicates if there is a double bit error, 0 = double bit error, 1 = no double bit error

NPOR_S [D5]: Power on reset internal logic status, 0 = NPOR is Low, 1 = NPOR is high

POE_S [D4]: Power on enable internal logic status, 0 = POE is Low, 1 = POE is high

ENBATS [D3]: Battery enable status, reports the status of the high voltage enable pin ENBAT on the ARG81402, 0 = ENBAT is Low, 1 = ENBAT is high

WD_state_x [D2:D0]: Shows the state that the pulse period watchdog is currently in, see table for the different states.

WD_state_2	WD_state_1	WD_state_0	Pulse Period Watchdog State
0	0	0	Idle
0	0	1	Test Hunt
0	1	0	Test Lock
0	1	1	Test Complete
1	0	0	Running Hunt
1	0	1	Running
1	1	0	Watchdog/Safe State
1	1	1	Flash

0X03. DIAGNOSTIC REGISTER 0:

D7	D6	D5	D4	D3	D2	D1	D0
V5A_OV	V5A_UV	V5CAN_OV	V5CAN_UV	V5P_OV	V5P_UV	V5B_OV	V5B_UV
0	0	0	0	0	0	0	0

Address 00011

Read register, write 1 to clear

Data

V5A_OV [D7]: 5 V rail A overvoltage occurred, 0 = rail OK, 1 = overvoltage occurred

V5A_UV [D6]: 5 V rail A undervoltage occurred, 0 = rail OK, 1 = undervoltage occurred

V5CAN_OV [D5]: 5 V CAN bus rail overvoltage occurred, 0 = rail OK, 1 = overvoltage occurred

V5CAN_UV [D4]: 5 V CAN bus rail undervoltage occurred, 0 = rail OK, 1 = undervoltage occurred

V5P_OV [D3]: Protected 5 V rail overvoltage occurred, 0 = rail OK, 1 = overvoltage occurred

V5P_UV [D2]: Protected 5 V rail undervoltage occurred, 0 = rail OK, 1 = undervoltage occurred

V5B_OV [D1]: 5 V rail B overvoltage occurred, 0 = rail OK, 1 = overvoltage occurred

V5B_UV [D0]: 5 V rail B undervoltage occurred, 0 = rail OK, 1 = undervoltage occurred

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0X04. DIAGNOSTIC REGISTER 1:

D7	D6	D5	D4	D3	D2	D1	D0
VDD_OV	VDD_UV	VREG_OV	VREG_UV	3V3_OV	3V3_UV	1V3IN_OV	1V3IN_UV
0	0	0	0	0	0	0	0

Address 00100

Read register, write 1 to clear

Data

VDD_OV [D7]: Internal VDD rail overvoltage occurred, 0 = rail OK, 1 = overvoltage occurred

VDD_UV [D6]: Internal VDD rail undervoltage occurred, 0 = rail OK, 1 = undervoltage occurred

VREG_OV [D5]: Pre-regulator voltage rail overvoltage occurred, 0 = rail OK, 1 = overvoltage occurred

VREG_UV [D4]: Pre-regulator voltage rail undervoltage occurred, 0 = rail OK, 1 = undervoltage occurred

3V3_OV [D3]: 3.3 V rail overvoltage occurred, 0 = rail OK, 1 = overvoltage occurred

3V3_UV [D2]: 3.3 V rail undervoltage occurred, 0 = rail OK, 1 = undervoltage occurred

1V3IN_OV [D1]: Voltage on pin 1V3IN is above specification, 0 = rail OK, 1 = overvoltage occurred

1V3IN_UV [D0]: Voltage on pin 1V3IN is below specification, 0 = rail OK, 1 = undervoltage occurred

0X05. DIAGNOSTIC REGISTER 2:

D7	D6	D5	D4	D3	D2	D1	D0
				VCC_OV	VCC_UV	VCP_OV	VCP_UV
0	0	0	0	0	0	0	0

Address 00101

Read register, write 1 to clear

Data

VCC_OV [D3]: Internal VCC rail overvoltage occurred, 0 = rail OK, 1 = overvoltage occurred

VCC_UV [D2]: Internal VCC rail undervoltage occurred, 0 = rail OK, 1 = undervoltage occurred

VCP_OV [D0]: Charge pump voltage rail overvoltage occurred, 0 = rail OK, 1 = overvoltage occurred

VCP_UV [D0]: Charge pump voltage rail undervoltage occurred, 0 = rail OK, 1 = undervoltage occurred

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0X06. OUTPUT DISABLE REGISTER:

D7	D6	D5	D4	D3	D2	D1	D0
V5P_DIS1	V5A_DIS1	V5B_DIS1		V5P_DIS0	V5A_DIS0	V5B_DIS0	
0	0	0	0	0	0	0	0

Address 00110

Read or write register

Data

V5P_DIS [D7:D3]: Disable protected 5 V output, 11 = disabled, x0 = enabled, 0x = enabled

V5A_DIS [D6:D2]: Disable 5 V rail A output, 11 = disabled, x0 = enabled, 0x = enabled

V5B_DIS [D5:D1]: Disable 5 V rail B output, 11 = disabled, x0 = enabled, 0x = enabled

0X07. WATCHDOG MODE KEY REGISTER:

D7	D6	D5	D4	D3	D2	D1	D0
KEY_7	KEY_6	KEY_5	KEY_4	KEY_3	KEY_2	KEY_1	KEY_0
0	0	0	0	0	0	0	0

Address 00111

Write register

Data

KEY [D7:D0]: Three 8-bit words must be sent in the correct order to enable flash mode or restart the watchdog. If an incorrect word is received, then the register resets and the first word has to be resent.

	Flash Mode	Restart
WORD1	0xD3	0xD3
WORD2	0x33	0x33
WORD3	0xCC	0xCD

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0X08. CONFIGURATION REGISTER 0:

D7	D6	D5	D4	D3	D2	D1	D0
WD_SEL1	WD_SEL2	WD_MAX_2	WD_MAX_1	WD_MAX_0	WD_MIN_2	WD_MIN_1	WD_MIN_0
0	0	1	0	0	1	0	0

Address 01000

Read or write register

Data

WD_MAX [D7:D6]: 2-bit word to select one of the possible three watchdogs.

D7	D6	Watchdog
WD_SEL1	WD_SEL0	
0	**X**	Pulse period watchdog
1	0	Window watchdog
1	1	Q&A watchdog

WD_MAX [D5:D3]: 3-bit word to adjust the watchdog maximum timer set point

WD_MAX_2	WD_MAX_1	WD_MAX_0	Maximum Timer	WD Typical Maximum Pulse
0	0	0	+0.08 ms	2.08 ms
0	0	1	+0.09 ms	2.09 ms
0	1	0	+0.10 ms	2.10 ms
0	1	1	+0.11 ms	2.11 ms
1	**0**	**0**	**+0.12 ms**	**2.12 ms**
1	0	1	+0.13 ms	2.13 ms
1	1	0	+0.14 ms	2.14 ms
1	1	1	+0.15 ms	2.15 ms

WD_MIN [D2:D0]: 3-bit word to adjust the watchdog minimum timer set point

WD_MIN_2	WD_MIN_1	WD_MIN_0	Minimum Timer	WD Typical Minimum Pulse
0	0	0	–0.08 ms	1.92 ms
0	0	1	–0.09 ms	1.91 ms
0	1	0	–0.10 ms	1.90 ms
0	1	1	–0.11 ms	1.89 ms
1	**0**	**0**	**–0.12 ms**	**1.88 ms**
1	0	1	–0.13 ms	1.87 ms
1	1	0	–0.14 ms	1.86 ms
1	1	1	–0.15 ms	1.85 ms

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0X09. CONFIGURATION REGISTER 1:

D7	D6	D5	D4	D3	D2	D1	D0
WIN_Timer2	WIN_Timer1	WIN_Timer0	DITH_DIS	VALID_1	VALID_0	EDGE_1	EDGE_0
0	0	0	0	0	0	0	0

Address 01001

Read or write register

Data

WIN_Timer [D7:D5]: 3-bit word to set the window watchdog fast and slow timeout periods.

D7	D6	D5	$t_{WD(FAST)}$	$t_{WD(SLOW)}$
WIN_Timer2	WIN_Timer1	WIN_Timer0		
0	0	0	0.5 ms	4 ms
0	0	1	1 ms	8 ms
0	1	0	2 ms	16 ms
0	1	1	4 ms	32 ms
1	0	0	6 ms	42 ms
1	0	1	8 ms	64 ms
1	1	0	10 ms	80 ms
1	1	1	12.5 ms	100 ms

DITH_DIS [D4]: This bit allows the user to disable the dither function for the switching converters, 0 = dither enabled, 1= dither disabled.

VALID [D3:D2]: 2-bit counter to set the number of counts before a valid watchdog signal is set or reset.

VALID_1	VALID_0	Valid Counts
0	0	2
0	1	4
1	0	6
1	1	8

EDGE [D1:D0]: 2-bit counter to set the number of edges to count before incrementing the VALID counter. The EDGE value also sets the minimum and maximum nominal timers. The minimum and maximum timers will be based on the number of edge counts times 2 ms plus the delta stored in WD_MIN and WD_MAX.

EDGE_1	EDGE_0	Edge Counts	Nominal Timer
0	0	4	8 ms
0	1	6	12 ms
1	0	8	16 ms
1	1	10	20 ms

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0X0A. CONFIGURATION REGISTER 2:

D7	D6	D5	D4	D3	D2	D1	D0
	NPOR_RST_EN	TRY1	TRY0	TIMER3	TIMER2	TIMER1	TIMER0
0	0	0	0	0	0	0	0

Address 01010

Read or write register

Data

NPOR_RST_EN [D6]: NPOR toggle select for window watchdog and Q&A watch dog. 0 = NPOR is unaffected by watchdog fault, 1 = NPOR is toggled low for 2 ms if there is a watchdog fault. NPORRST = 1 is default state.

TRY [D5:D4]: 2-bit word to select the number of incorrect responses form the microprocessor/DSP when using the Q&A watchdog.

D5	D4	Acceptable number of incorrect responses
TRY1	TRY0	
0	0	0 times
0	1	2 times
1	0	4 times
1	1	8 times

TIMER [D3:D0]: 4-bit timer to set the set open window period to accept a Q&A watchdog response from the microprocessor/DSP.

D3	D2	D1	D0	min timeout, $t_{Q\&A(MIN)}$	max timeout, $t_{Q\&A(MAX)}$
Timer3	Timer2	Timer1	Timer0		
0	0	0	0	0.5 ms	1 ms
0	0	0	1	1 ms	2 ms
0	0	1	0	2 ms	4 ms
0	0	1	1	4 ms	8 ms
0	1	0	0	8 ms	16 ms
0	1	0	1	12 ms	24 ms
0	1	1	0	16 ms	32 ms
0	1	1	1	24 ms	48 ms
1	0	0	0	32 ms	64 ms
1	0	0	1	40 ms	80 ms
1	0	1	0	64 ms	128 ms
1	0	1	1	72 ms	144 ms
1	1	0	0	80 ms	160 ms
1	1	0	1	96 ms	192 ms
1	1	1	0	128 ms	256 ms
1	1	1	1	144 ms	288 ms

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0X0B. VERIFY RESULT REGISTER 3:

D7	D6	D5	D4	D3	D2	D1	D0
		RND5	RND4	RND3	RND2	RND1	RND0
0	0	0	0	0	0	0	0

Address 01011

Read or Write register

Data

RND [D5:D0]: Randomly generated 6-bit word for Q&A watchdog

0X0D. VERIFY RESULT REGISTER 0:

D7	D6	D5	D4	D3	D2	D1	D0
V5A_OV_OK	V5A_UV_OK	V5CAN_OV_OK	V5CAN_UV_OK	3V3_OV_OK	3V3_UV_OK	1V3IN_OV_OK	1V3IN_UV_OK
0	0	0	0	0	0	0	0

Address 01101

Read register, write 1 to clear

Data

V5A_OV_OK [D7]: 5 V rail A overvoltage self-test passed, 0 = test failed, 1 = test passed

V5A_UV_OK [D6]: 5 V rail A undervoltage self-test passed, 0 = test failed, 1 = test passed

V5CAN_OV_OK [D5]: 5 V CAN bus rail overvoltage self-test passed, 0 = test failed, 1 = test passed

V5CAN_UV_OK [D4]: 5 V CAN bus rail undervoltage self-test passed, 0 = test failed, 1 = test passed

3V3_OV_OK [D3]: 3.3 V rail overvoltage self-test passed, 0 = test failed, 1 = test passed

3V3_UV_OK [D2]: 3.3 V rail undervoltage self-test passed, 0 = test failed, 1 = test passed

1V3IN_OV_OK [D1]: 1V3IN monitor overvoltage self-test passed, 0 = test failed, 1 = test passed

1V3IN_UV_OK [D0]: 1V3IN monitor adjustable voltage rail undervoltage self-test passed, 0 = test failed, 1 = test passed

0X0E. VERIFY RESULT REGISTER 1:

D7	D6	D5	D4	D3	D2	D1	D0
BIST_PASS	TSD_OK	VREG_OV_OK	VREG_UV_OK	V5P_OV_OK	V5P_UV_OK	V5B_OV_OK	V5B_UV_OK
0	0	0	0	0	0	0	0

Address 01110

Read register, write 1 to clear

Data

BIST_PASS [D7]: Self-test status, 0 = self-test failed, 1 = self-test passed

TSD_OK [D6]: Thermal shutdown circuit passed self-test, 0 = test failed, 1 = test passed

VREG_OV_OK [D5]: Pre-regulator voltage rail overvoltage self-test passed, 0 = test failed, 1 = test passed

VREG_UV_OK [D4]: Pre-regulator voltage rail undervoltage self-test passed, 0 = test failed, 1 = test passed

V5P_OV_OK [D3]: Protected 5 V rail overvoltage self-test passed, 0 = test failed, 1 = test passed

V5P_UV_OK [D2]: Protected 5 V rail undervoltage self-test passed, 0 = test failed, 1 = test passed

V5B_OV_OK [D1]: 5 V rail B overvoltage self-test passed, 0 = test failed, 1 = test passed

V5B_UV_OK [D0]: 5 V rail B undervoltage self-test passed, 0 = test failed, 1 = test passed

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APPLICATION INFORMATION

The following section describes the component selection for the ARG81402. It should be cross-referenced with the typical schematics on page 5.

Table 3: Recommended Values for Critical External Components

Component Name	Value	Description
Charge pump capacitors (C_{CP1}, C_{CP2})	C_{CP1} = 0.47 µF C_{CP2} = 0.22 µF	Use 50 V, X5R/X7R ceramic capacitors.
Pre-regulator output inductor (L1)	10 µH	Select the inductor current rating for the maximum switch current of the pre-regulator or higher (>1.7 A).
Pre-regulator ceramic output capacitor (C_{OUT})	>10 µF	2 × 10 µF (16 V, X5R/X7R, 1206) should be sufficient. It is also recommended to add smaller size capacitors close to the VREG pin and LDOIN pin.
Ceramic input capacitor (C_{IN})	>5 µF	2 × 4.7 µF (50 V, X5R/X7R, 1210) should be sufficient for most applications. Add smaller size capacitors (10 pF to 0.1 µF, 0402/0603) close to the VIN pin for local decoupling. Add bulk capacitor (33 to 100 µF) closer to the power supply if can undergo heavy transient.
Compensation network (R_Z, C_Z, C_P)	R_Z = 8.25 kΩ C_Z = 2.2 nF C_P = 100 pF	Provides good loop stability for most applications (see below for Bode Plot measurement).
Bootstrap capacitor (C_{BOOT})	0.1 µF	Use 50 V, X5R/X7R ceramic capacitor
3.3 V regulator external resistor (R_{DROP})	0 to 4.3 Ω	Prevents the internal 3V3 regulator from dissipating too much power. Make sure the power rating can support $I_{3V3(MAX)}^2 \times R^{DROP}$.
Linear regulator output capacitors ($C_{OUT(V5A)}$, $C_{OUT(V5B)}$, $C_{OUT(V5CAN)}$, $C_{OUT(V5P)}$, $C_{OUT(3V3)}$)	1 to 15 µF	2.2 µF ceramic capacitor per regulator should be sufficient.
VCC capacitor (C_{VCC})	1 µF	Use 16 V, X5R/X7R ceramic capacitor.

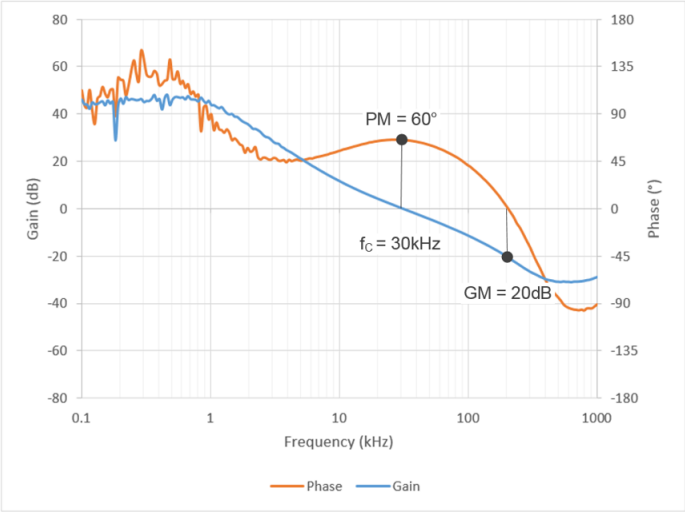

Figure 13: Bode plot measurement of the complete system
R_Z = 8.25 kΩ, C_Z = 2.2 nF, C_P = 100 pF,
L_1 = 10 µH, C_{OUT} = 2 × 10 µF Ceramic

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PCB Layout Guidelines

1. Place the ceramic input capacitors as close as possible to the VIN pins and ground the capacitors at the PGND pin. In general, the smaller capacitors (0402, 0603) must be placed very close to the VIN pin. The larger ceramic capacitors should be placed within 0.5 inches of the VIN pin. There must not be any vias between the input capacitors and the VIN pins.
2. Place the pre-regulator output inductor (L1) as close as possible to the LX pin. The inductor and the IC must be on the same layer. Connect the LX pin to the inductor with a relatively wide trace or polygon. For EMI/EMC reasons, it's best to minimize the area of this trace/polygon. Also, keep low-level analog signals (like COMP) away from LX.
3. Place the bootstrap capacitor near the BOOT pin and keep the routing from this capacitor to the LX node as short as possible.
4. Place the pre-regulator output ceramic capacitors (C_{OUT}) relatively close to the output inductor and the IC. Ideally, the output capacitors, output inductor, and the IC should be on the same layer. The output capacitors must use a ground place to make a very low-inductance connection back to the PGND pin. There must be 1 or 2 smaller ceramic capacitors as close as possible to the VREG pin.
5. The two charge pump capacitors must be placed as close as possible to VCP and CP1/CP2.
6. The ceramic capacitors for the LDOs (3V3, V5A, V5B, V5P, and V5CAN) must be placed near their output pins. The V5P output must have a 1 A/40 V Schottky diode located very close to its pin to limit negative voltages.
7. The VCC bypass capacitor must be placed very close to the VCC pin.
8. Place the COMP network (CZ, RZ, CP) as close as possible to the COMP pin. Place vias to the GND plane as close as possible to these components.
9. The thermal pad under the ARG81402 must connect to the ground plane(s) with multiple vias. More vias will ensure the lowest junction temperature and highest efficiency.

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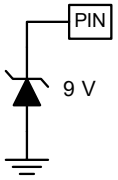
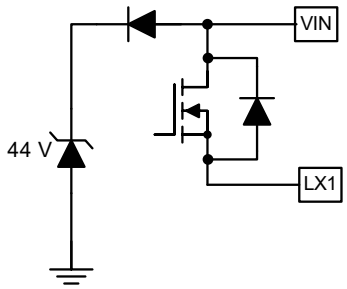
INPUT/OUTPUT STRUCTURES

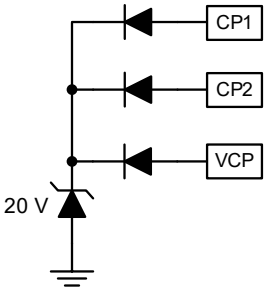
FFn, NPOR, 3V3, V5A, V5B, V5CAN, VREG, ENB, ENBAT, ENBATS, COMP, WD_IN, nERROR, VCC, POE



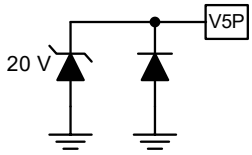
LX1



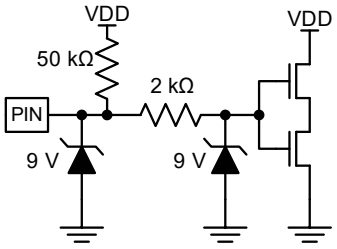
VCP, CP1, CP2



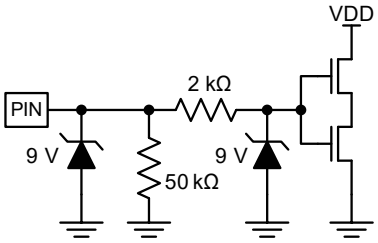
V5P



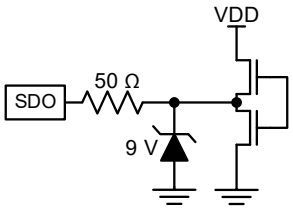
STRn Input



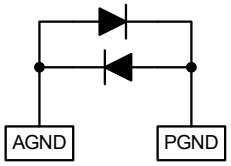
SDI, SCK



SDO



AGND, PGND



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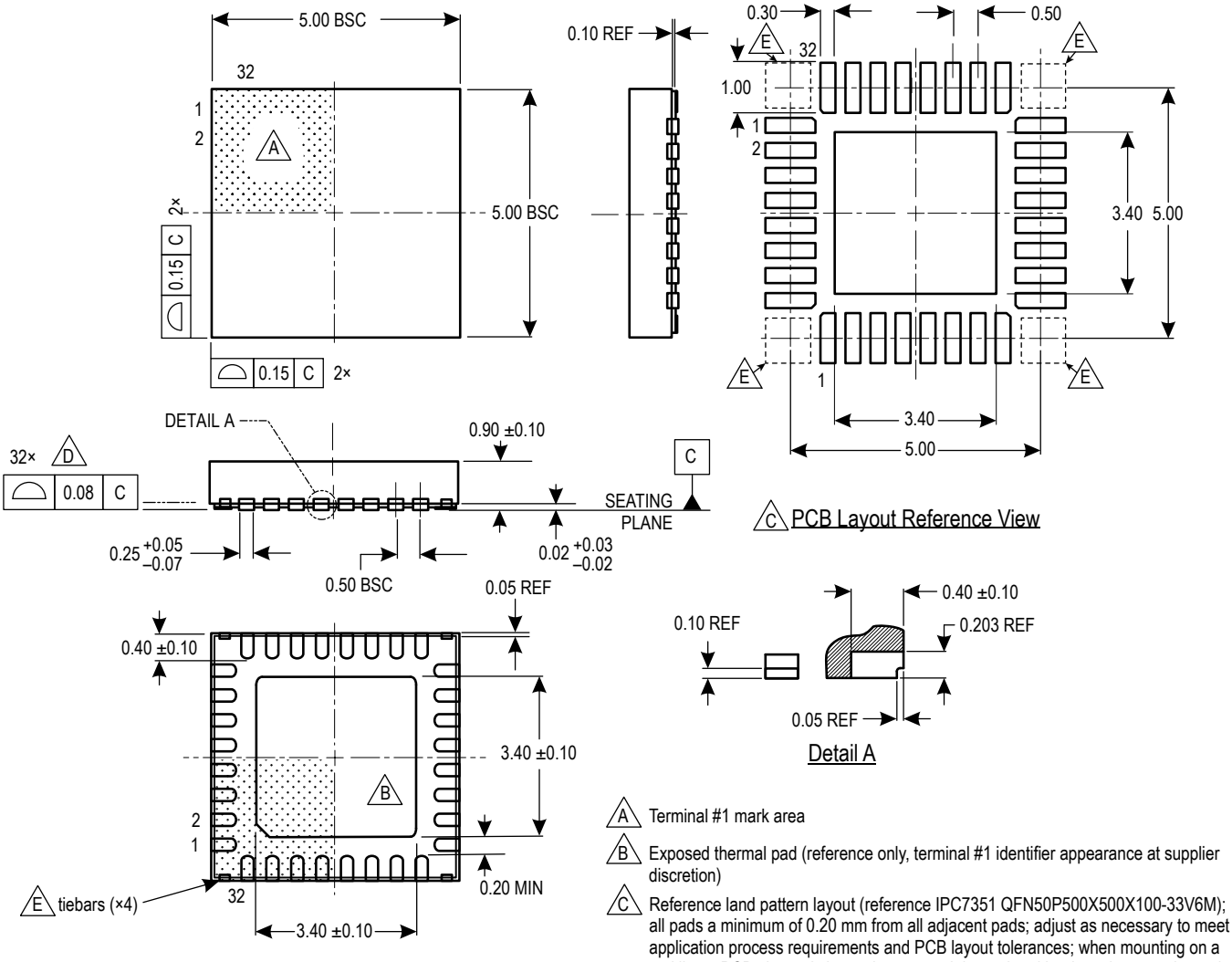
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000378, Rev. 3 and JEDEC MO-220VHHD-5)
Dimensions in millimeters – NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P500X500X100-33V6M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Tiebars (×4) are electrically connected to thermal pad. Avoid active traces in this area to avoid shorts. Ground plane in this area is acceptable when appropriate.

Figure 30: Package ET, 32-Pin QFN

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Revision History

Number	Date	Description
–	November 26, 2018	Initial release
1	April 12, 2019	Removed min/max values from V5CAN, V5A, V5B, and V5P OV and UV Hysteresis, updated VREG Non-Latching OV Threshold max value (page 12)
2	May 14, 2019	Added footnote to Data Out Enable Time, Data Out Disable Time, Data Out Valid Time From Clock Falling, and Data Out Hold Time From Clock Falling (page 15)
3	June 10, 2020	Updated Product Title, Features and Benefits, Description, and Applications (page 1) and Overview section (page 21)
4	March 31, 2021	Removed 1V3IN UV Hysteresis; updated 1V3IN UV Threshold falling minimum and maximum values (page 12)
5	October 5, 2021	Updated Serial Communication Interface section (pages 30-31)
6	September 30, 2022	Updated package drawing (page 44)
7	October 6, 2025	Updated ASIL logo and text (page 1)
8	January 14, 2026	Updated ASIL from A to D (page 1); updated LX Short-Circuit Current Limit test condition (page 9)

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